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Initial Stages of Time-Dependent Dielectric Breakdown: Atomic Scale Defects Generated by High-Field Gate Stressing in Si/SiO_2 Transistors

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Introduction

- The breakdown of SiO_2 gate dielectrics is preceded by the formation of traps in the oxide [1–4], as well as at the Si/SiO_2 interface [5,6]
- This trap generation causes time-dependent dielectric breakdown (TDDB), an important reliability issue
- Oxide traps contribute to the formation of a percolation path that greatly reduces the oxide resistance, leading to a spike in leakage current, and results in the breakdown of the device [7]

Introduction (cont.)

- Several physical mechanisms have been proposed for the generation of these traps [8–11]; however, only very limited and somewhat tentative experimental evidence about the identities of the traps currently exists [12–15]
- Understanding the nature of these stress-induced defects is key to understanding TDDB and stress-induced leakage currents (SILC)
- Electrically detected magnetic resonance (EDMR) and near-zero-field magnetoresistance (NZFMR) can provide chemical and physical information about these stress-induced traps

Background- Electron Paramagnetic Resonance

- The parent technique of EDMR is electron paramagnetic resonance (EPR)

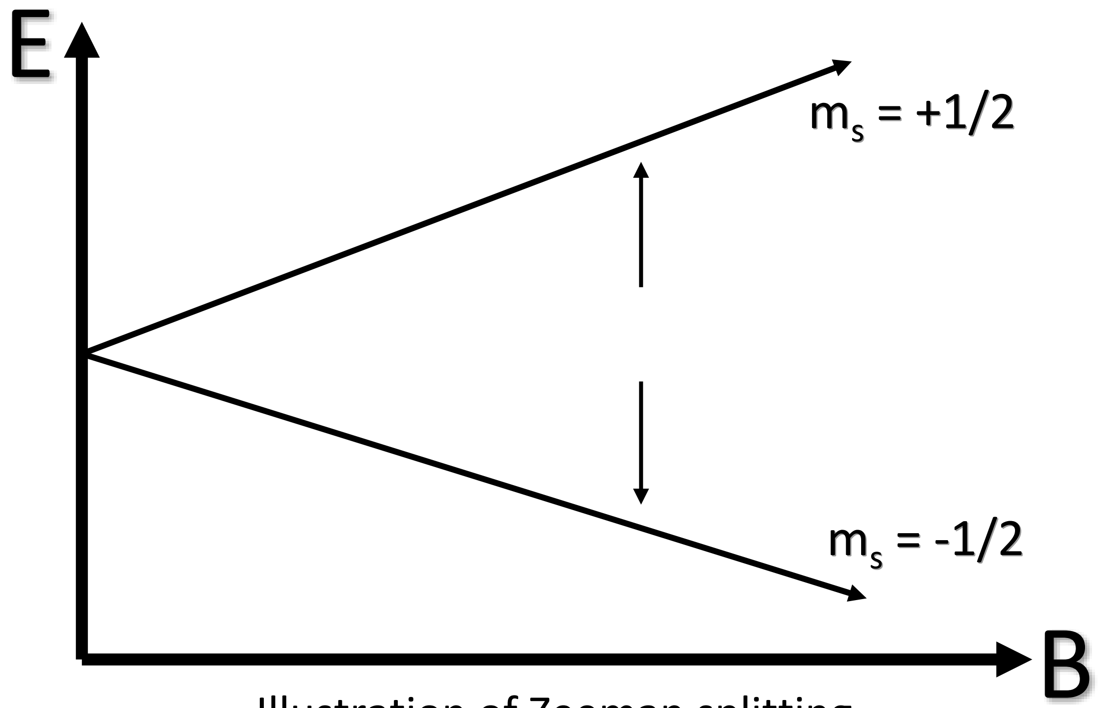
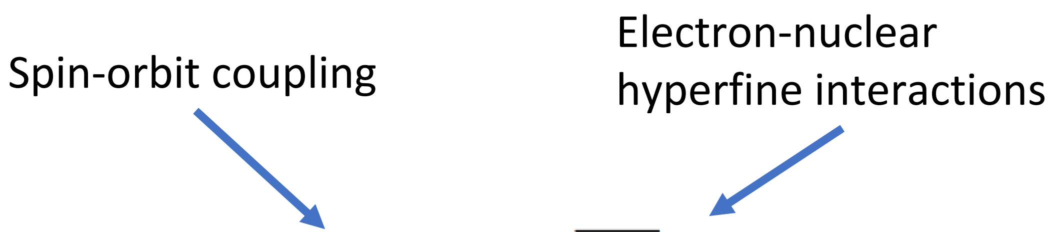
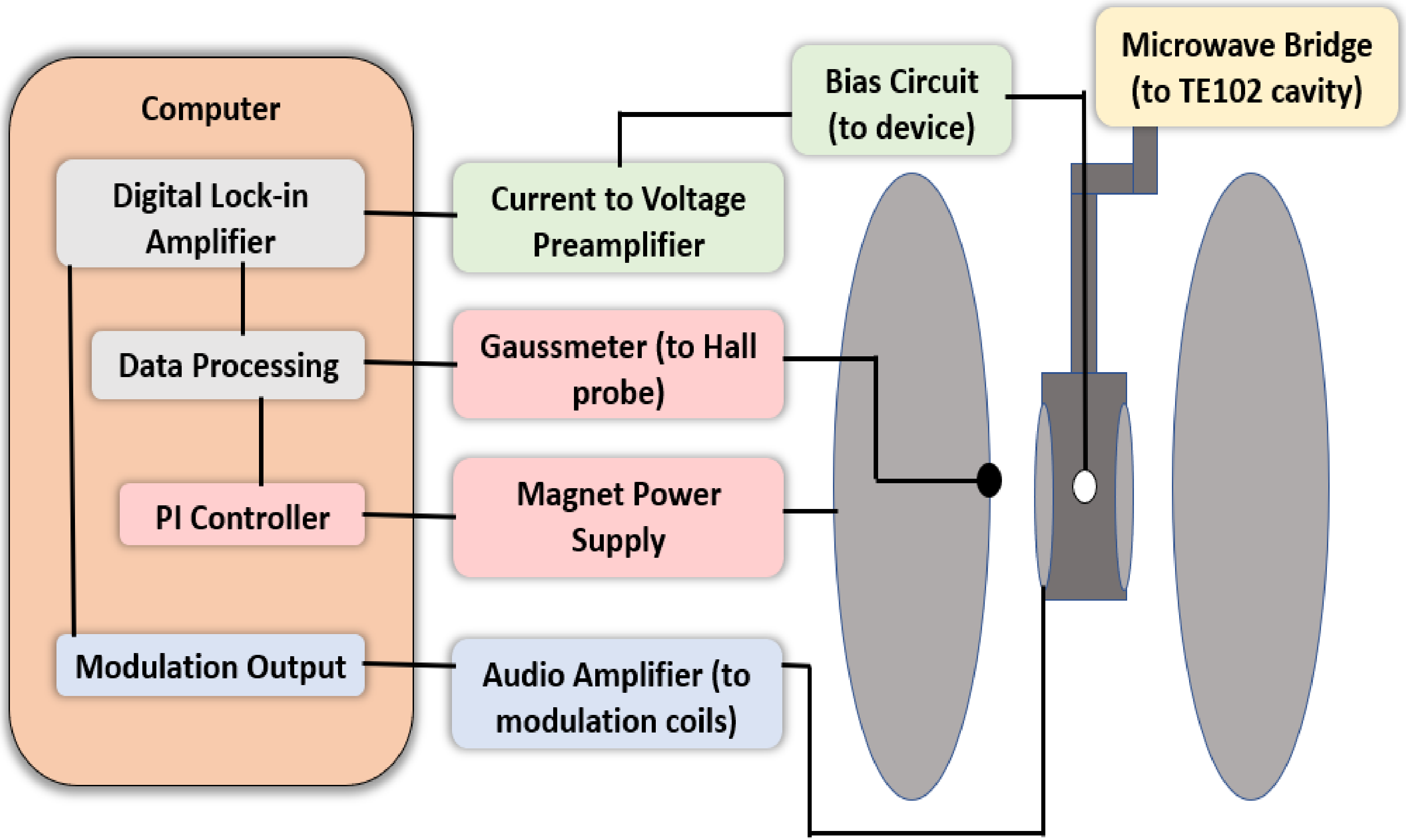


Illustration of Zeeman splitting



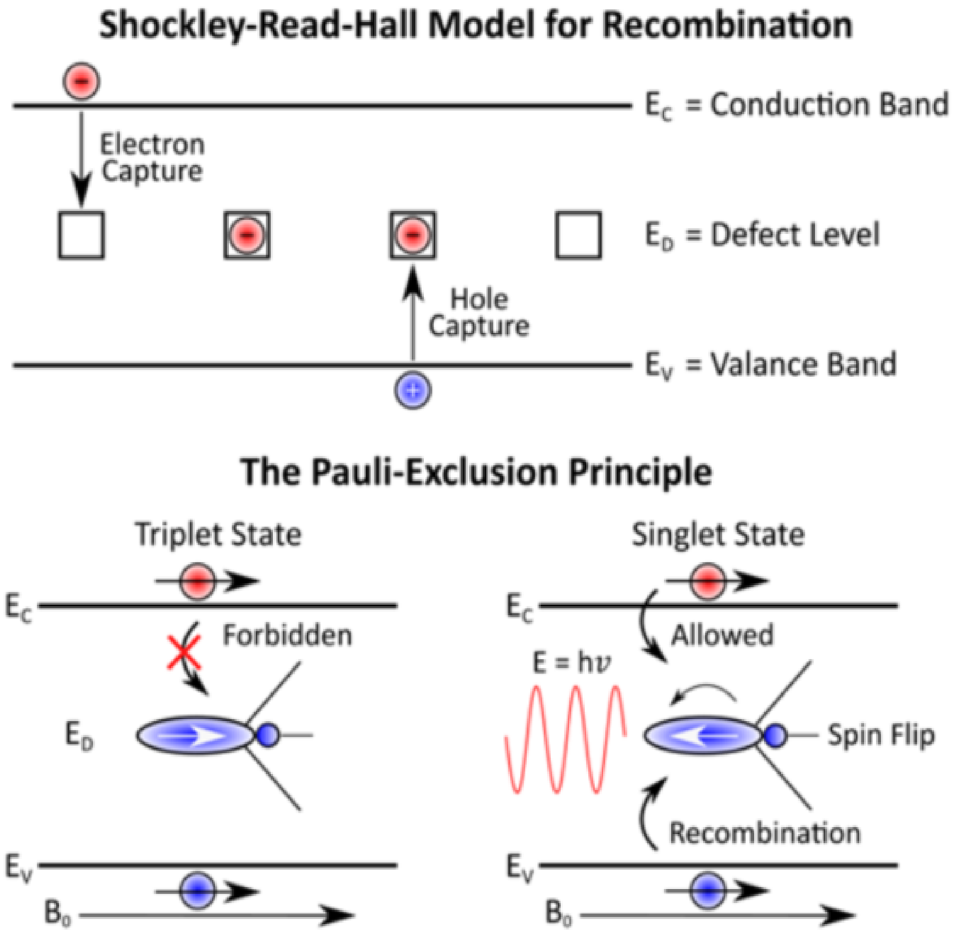
$$h\upsilon = g\mu_B B + \sum_i A_i I_i$$

EDMR Experiment



- The device sits in a high-Q microwave cavity
- A large electromagnet sweeps field across resonance condition
- Spin-dependent change in current contains chemical and physical information about paramagnetic defects
- Lock-in detection and signal averaging are used to improve sensitivity

Spin-Dependent Currents



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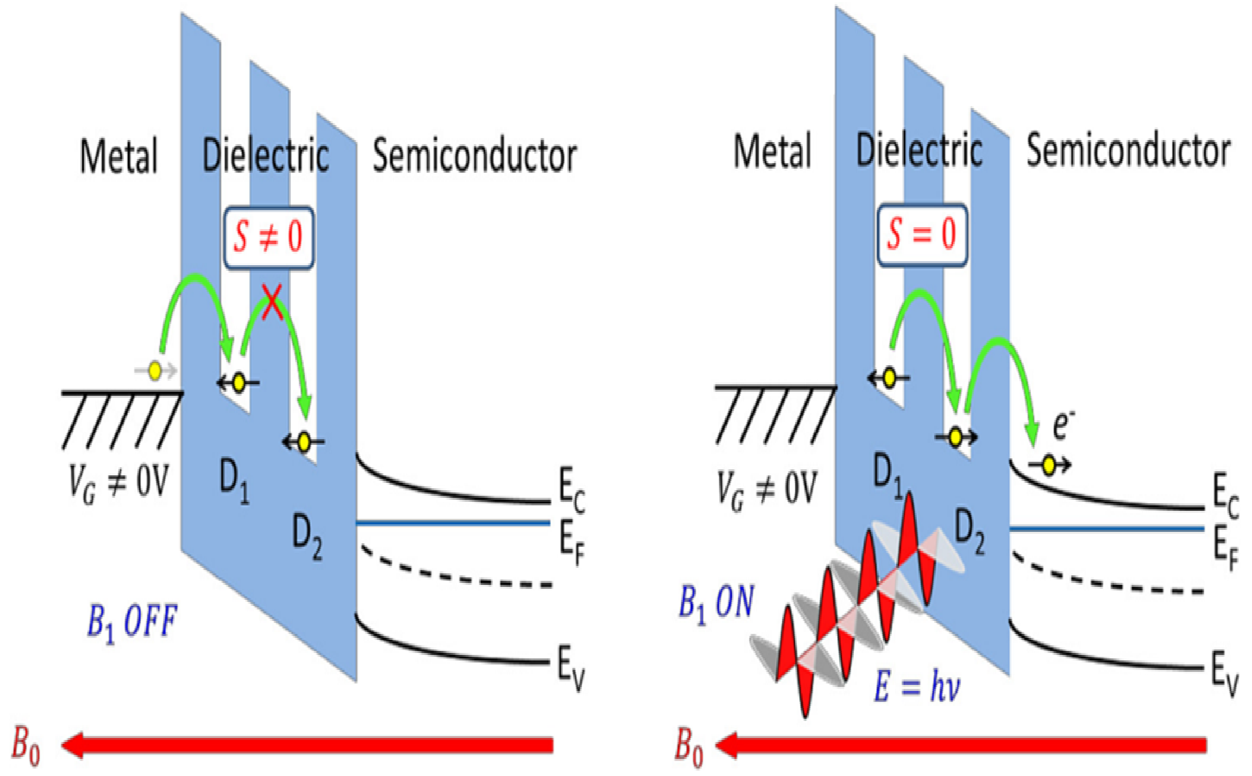


[17]

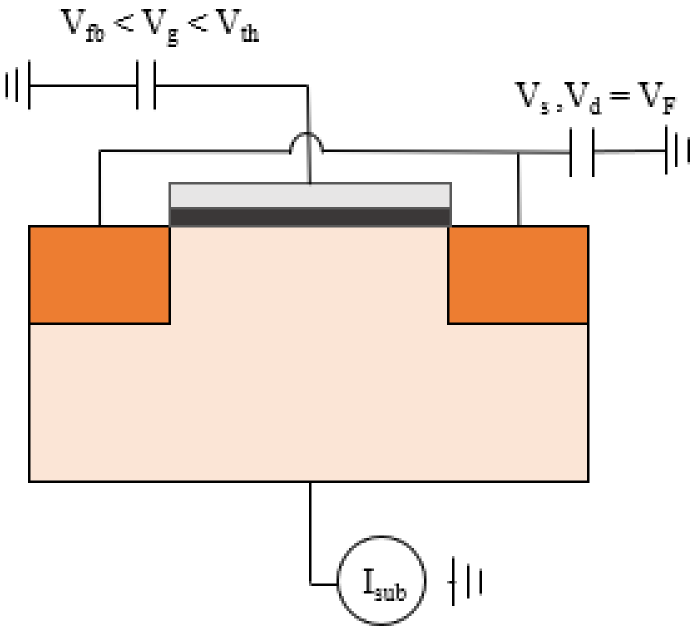
Spin-dependent recombination (SDR)

Spin-dependent trap-assisted tunneling (SDTAT)

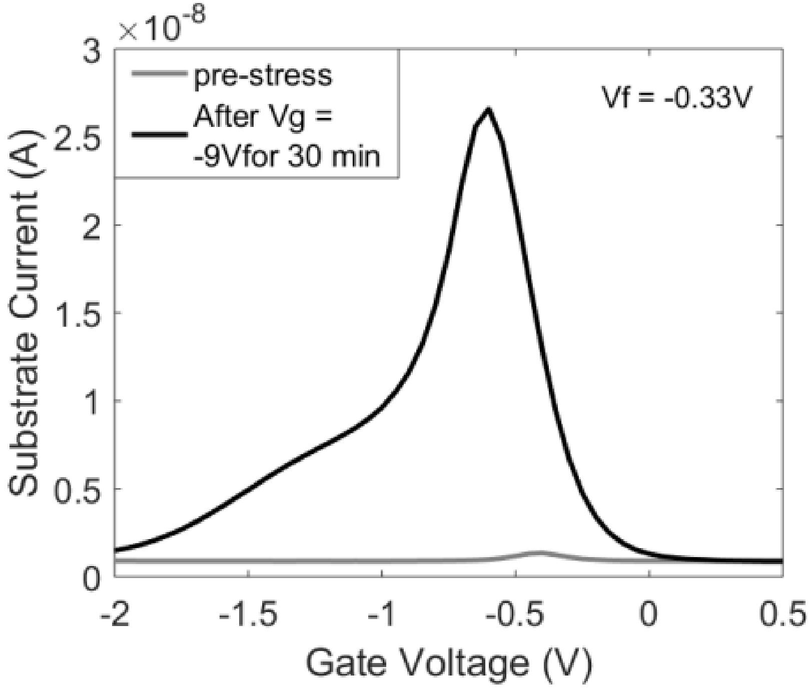
Other Experimental Details

- We report measurements of SDR and SDTAT currents on arrays of 126 Si/SiO_2 n-channel MOSFETs with 7.5nm gate thickness
- Devices were subjected to constant gate voltage or constant gate current stress, with interruptions for EDMR/NZFMR measurements
- We utilize the dc I-V biasing scheme to create recombination current at MOSFET interfaces, measuring the recombination current from the substrate [18]
- Tunneling currents through the gate dielectric were used to create SDTAT current

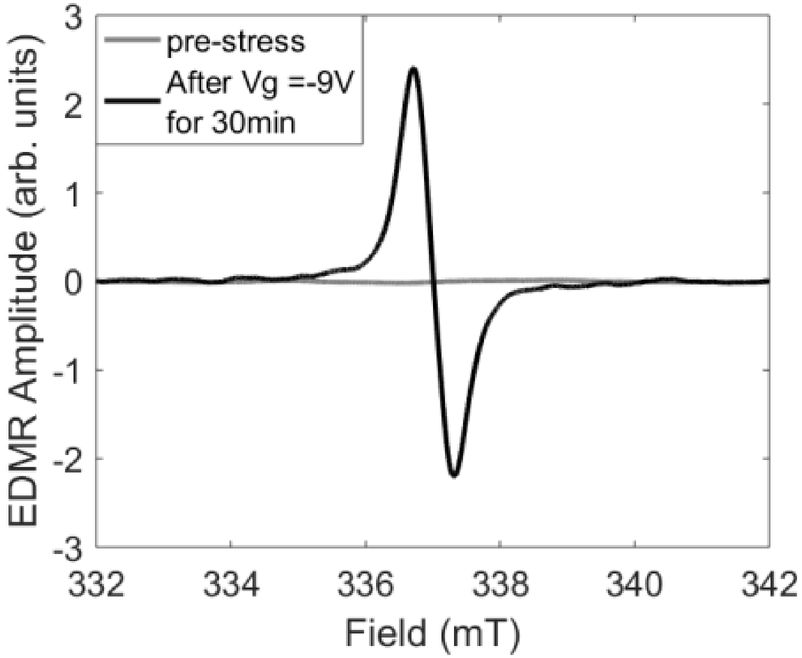
SDR Current and dc I-V Biasing



dc-IV biasing creates SRH recombination at the MOSFET interface



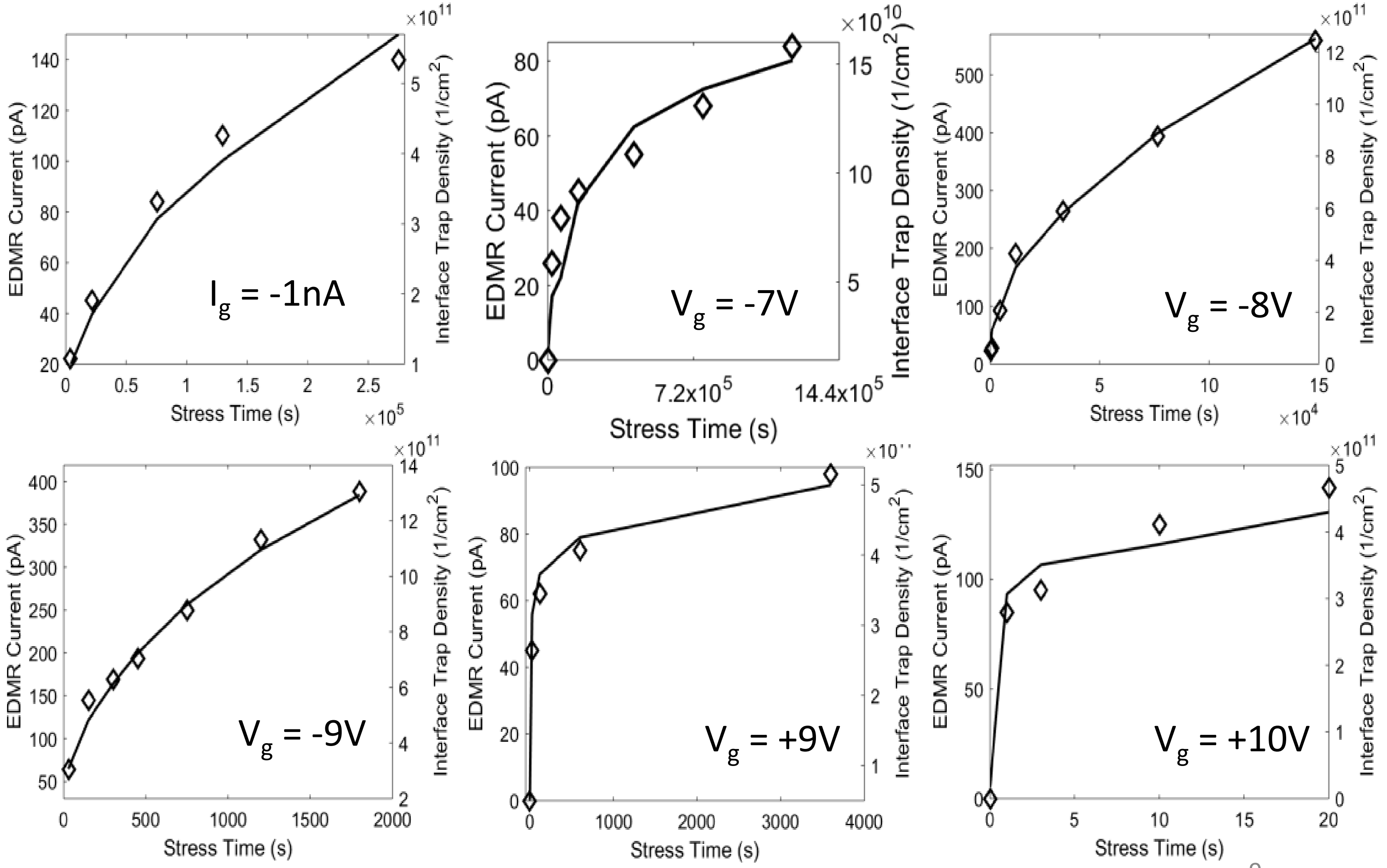
dc-IV peak in substrate current is used to calculate interface trap density [18]. Very few traps are observed pre-stress. A large increase occurs after stressing



EDMR is conducted with the device biased at the peak in dc-IV current. The field is swept and the resonance response is observed after stressing

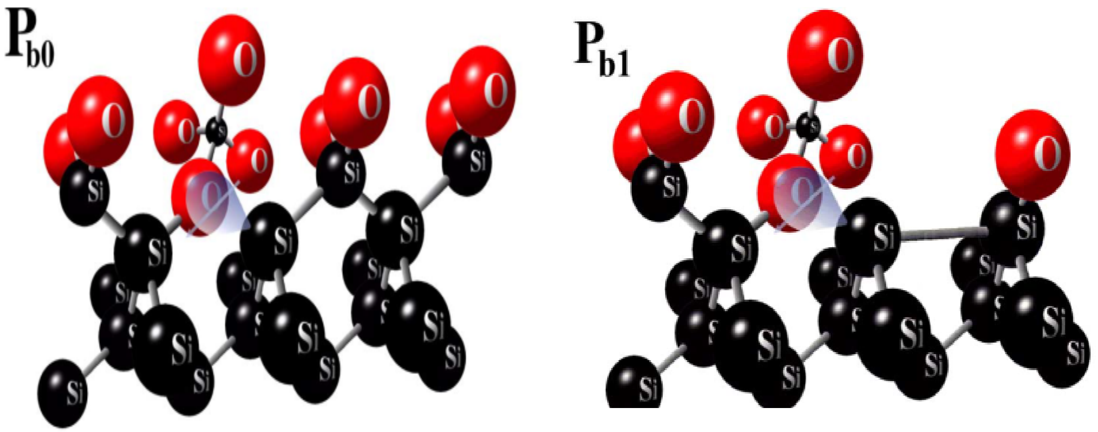
Interface Defect Density, SDR, and TDDB

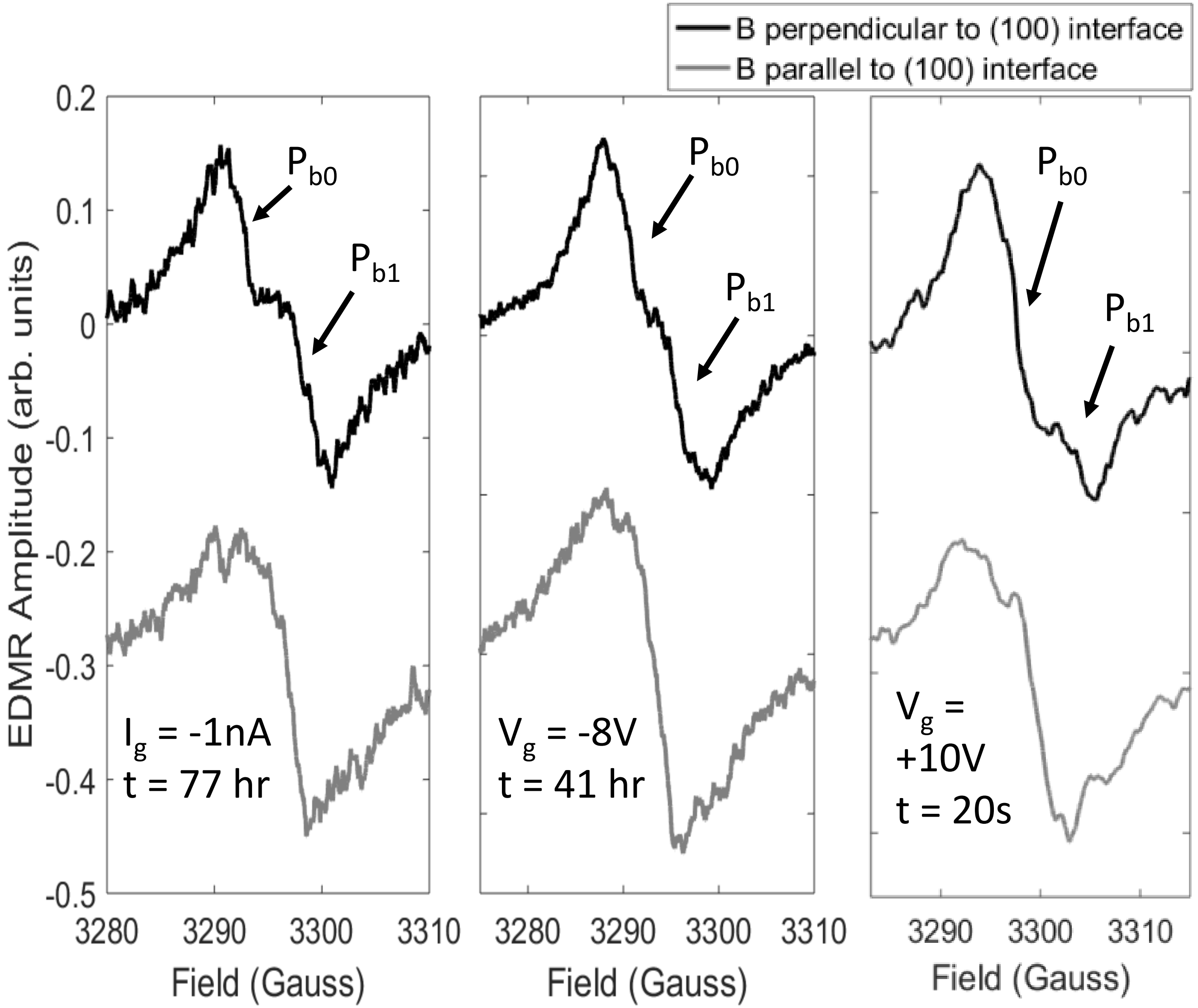
- SDR current tracks well with interface trap density as a function of stress time
- This remains true for a wide variety of gate stressing conditions
- Traps build up quickly near the start of stress, then more slowly as the stress continues



SDR EDMR Interface Trap Identification

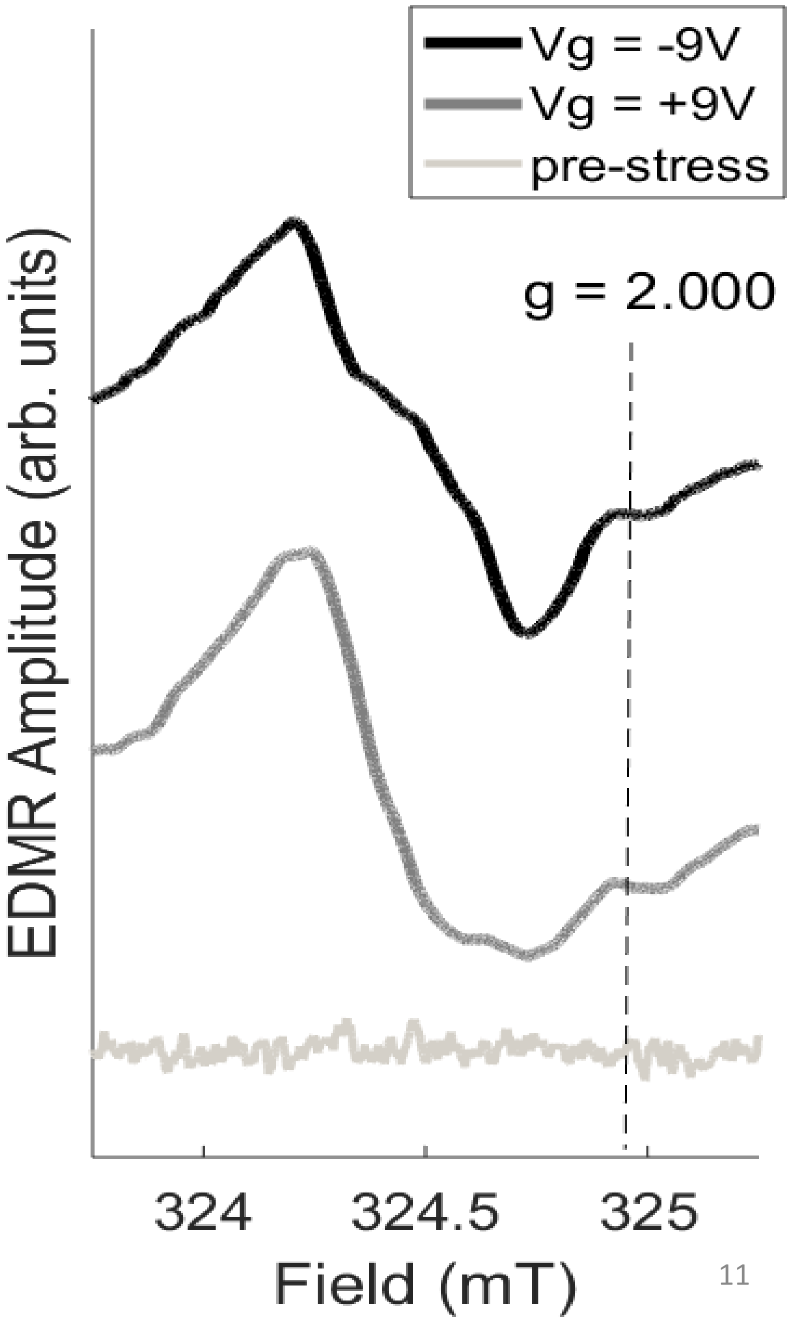
- Interface traps are a combination of P_{b0} and P_{b1} Si dangling bonds [19,20]
- Less P_{b1} contribution at (+) gate stress





SDR EDMR after High-Field Stress at Low Temperature

- In low temperature (T = 200K) SDR EDMR measurements of high-field stressed MOSFETs, spectra are still dominated by P_{b0} and P_{b1} defects
- Small, additional response appears at higher field, almost certainly due to near-interface E' centers. The E' center is a silicon dangling bond in the SiO_2, often described as a hole trapped at an oxygen vacancy [21]
- Low temperature measurements increase sensitivity to E' centers

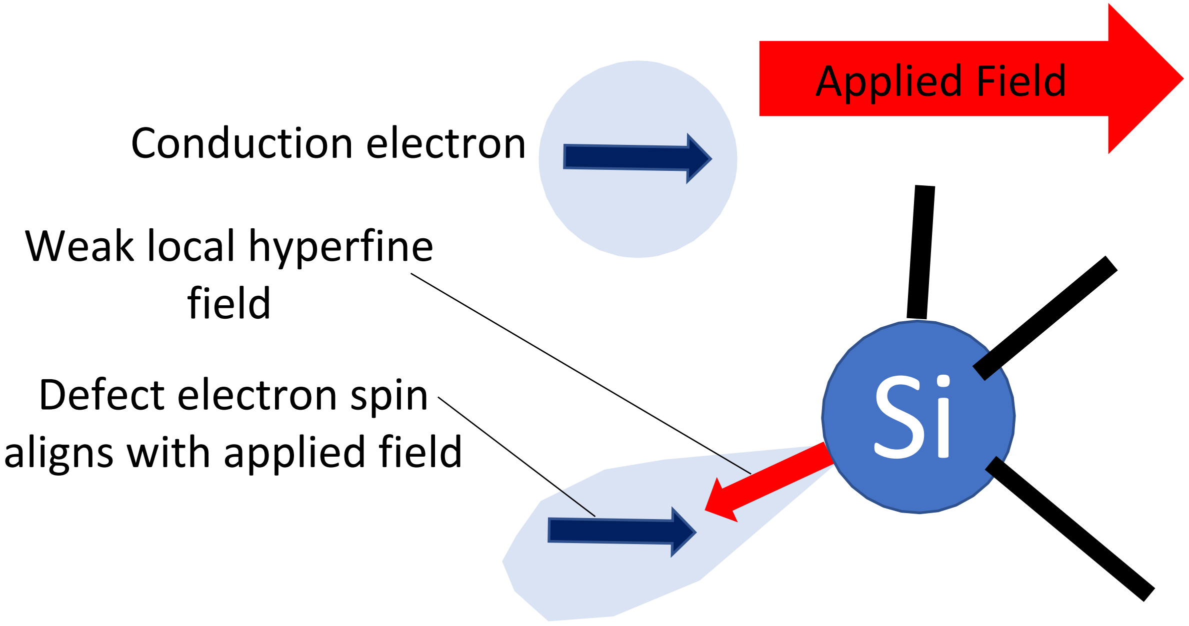


Near-Zero-Field Magnetoresistance (NZFMR)

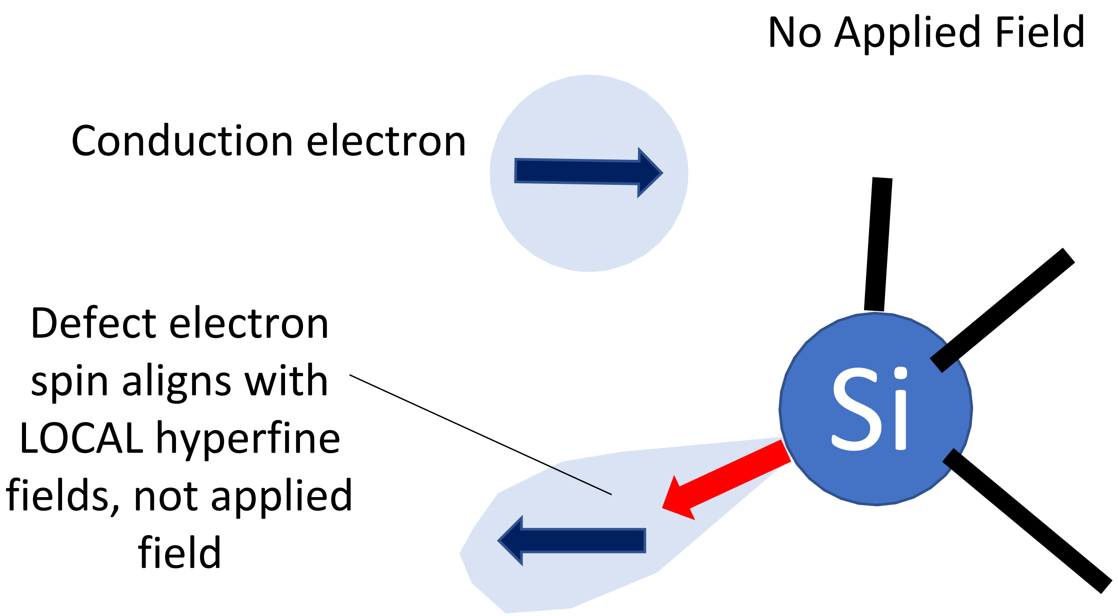
- Similar measurement to EDMR, but does not require microwave photons [22]
- Spin-dependent change in current is observed when sweeping through zero applied field
- Same spin pairs involved in SDR or SDTAT
- Mixing of singlet/triplet states occurs due to local hyperfine fields [23]
- NZFMR response is dependent on hyperfine coupling at the defect, and recombination/tunneling rates [23]

NZFMR (cont.)

Triplet Pair: $\Delta E \ \alpha \ \mu * B = 0$ for all B

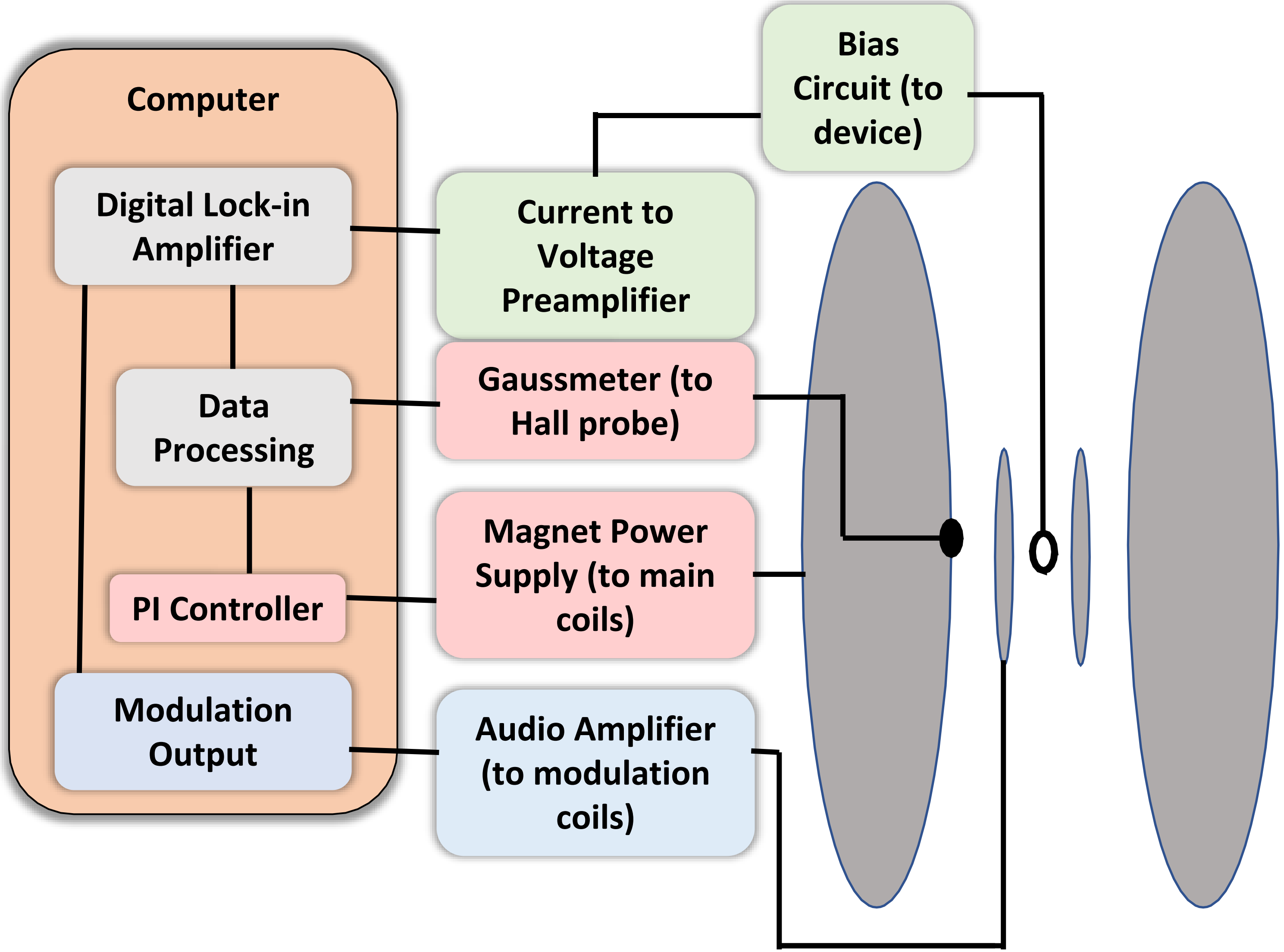


Singlet Pair: $\Delta E \ \alpha \ \mu * B = 0$ Only at B = 0



- So, at B = 0, singlet and triplet energy are both =0, and the **spins states can "mix"**
- This affects recombination probability (and thus recombination current)

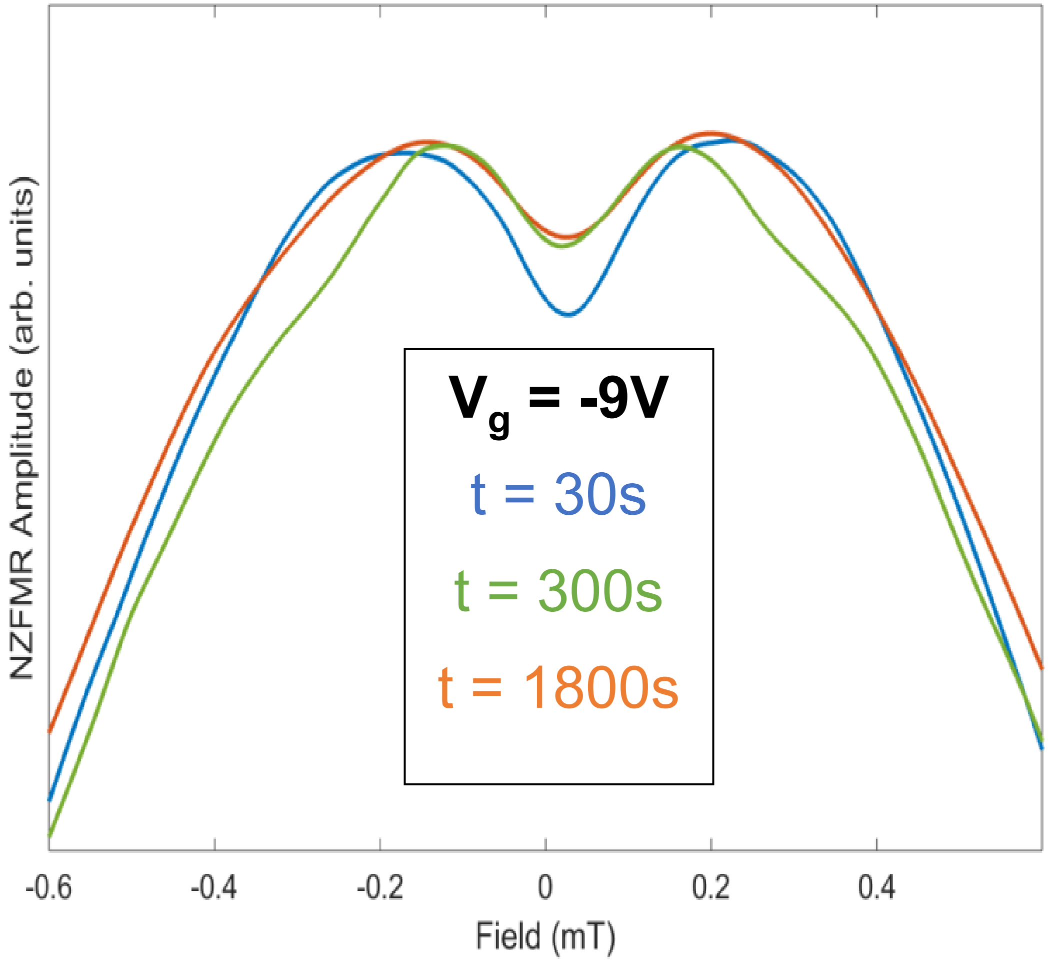
NZFMR (cont.)



- Similar to EDMR, but without the need for microwave source and cavity
- Field is swept across 0 rather than resonance condition
- SDR NZFMR measurements were conducted after different levels of device stress

SDR NZFMR and Device Lifetime

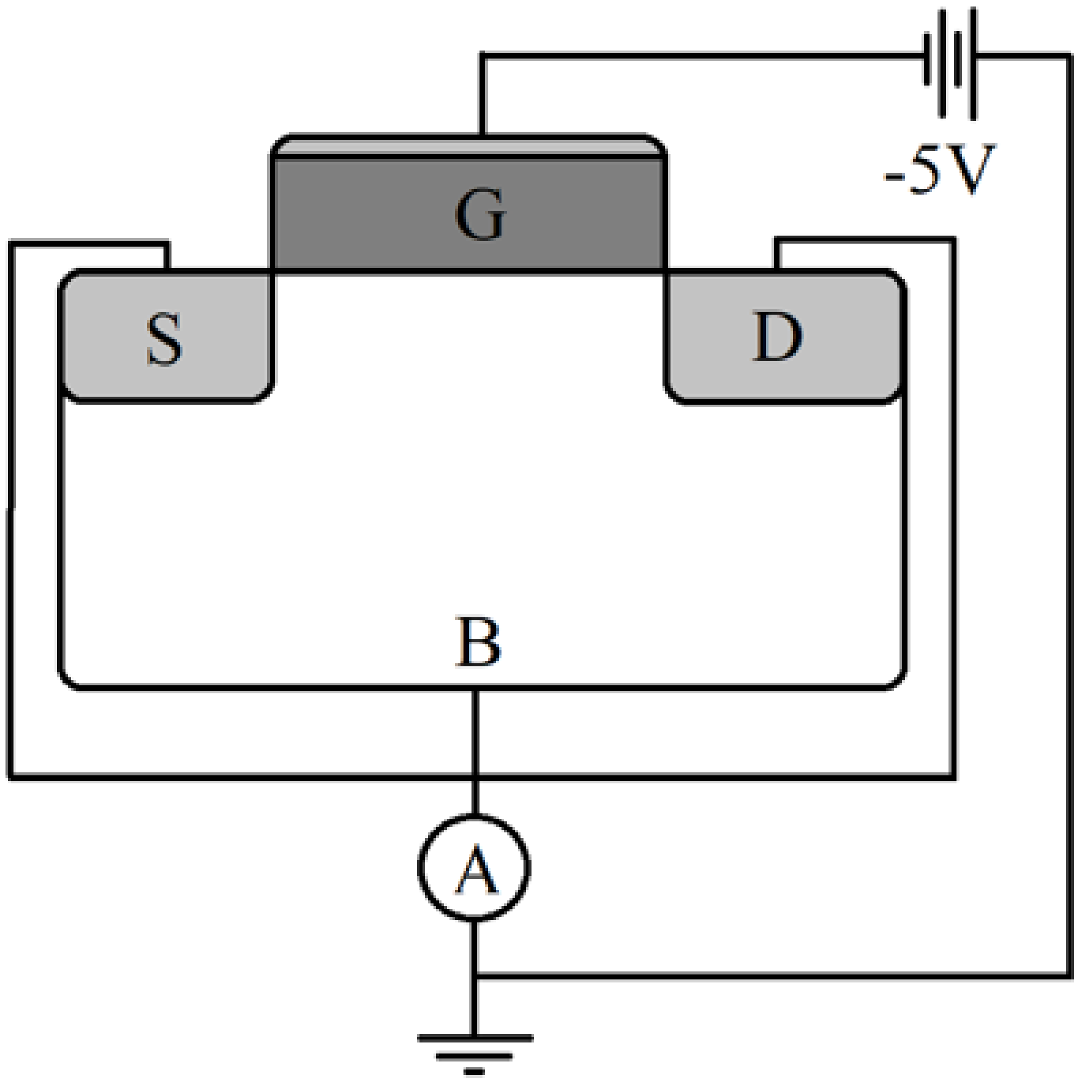
- Here, the integrated (and normalized) NZFMR spectra are compared at different points in device lifetime
- Subtle, but repeatable lineshape differences are seen between the NZFMR spectra
- These changes are due to changes in the local hyperfine environment of the defects
- The only mobile magnetic nuclei in the system is **hydrogen,** indicating that H is redistributed near the interface during TDDB



Note: pre-stress response cannot be resolved for adequate comparison

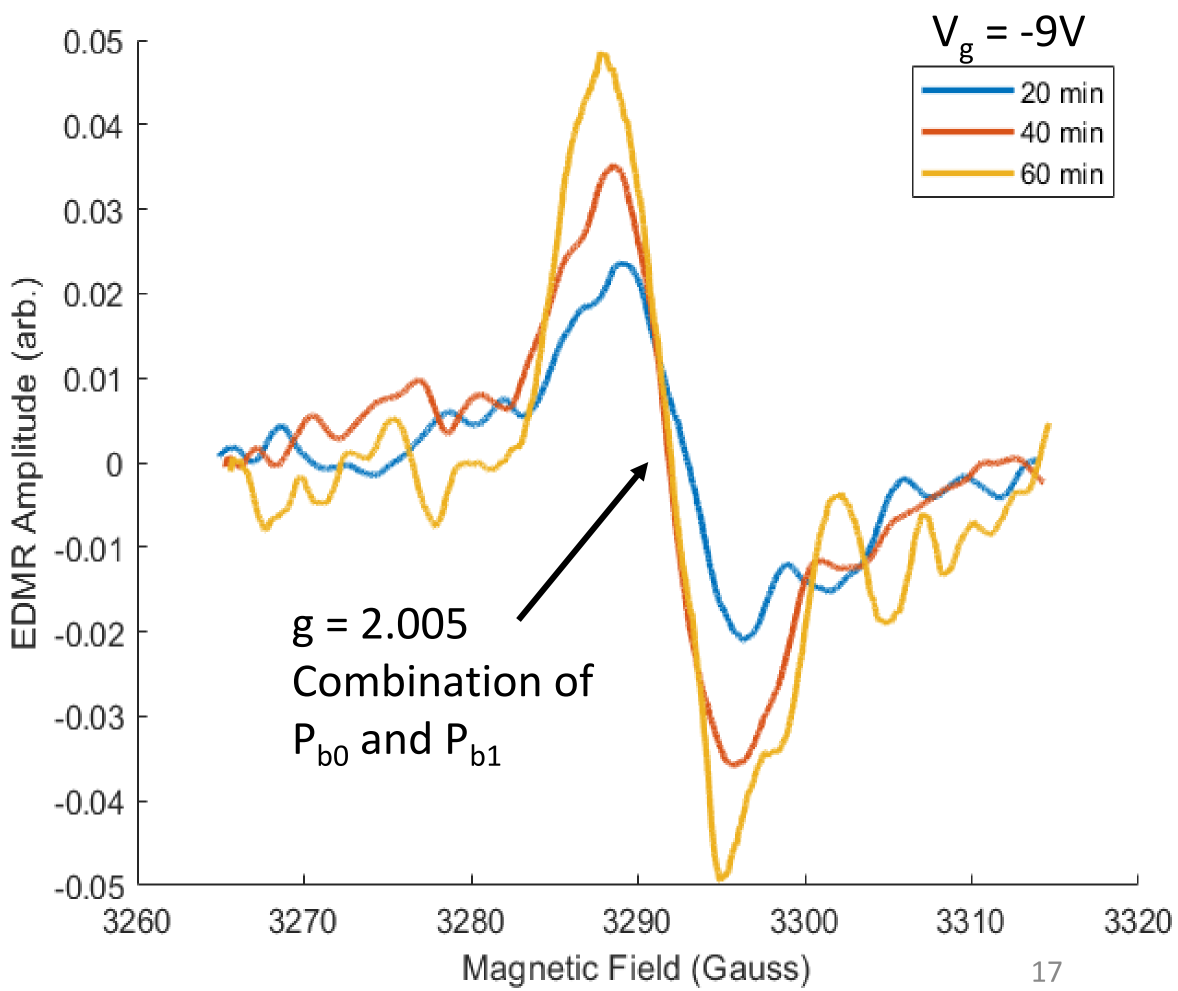
SDTAT Setup

- SDTAT EDMR measurements were made with on gate leakage current after various lengths of gate stress
- No pre-stress SDTAT response is visible
- These leakage currents are very small (1×10^{-10} A), which affects EDMR sensitivity



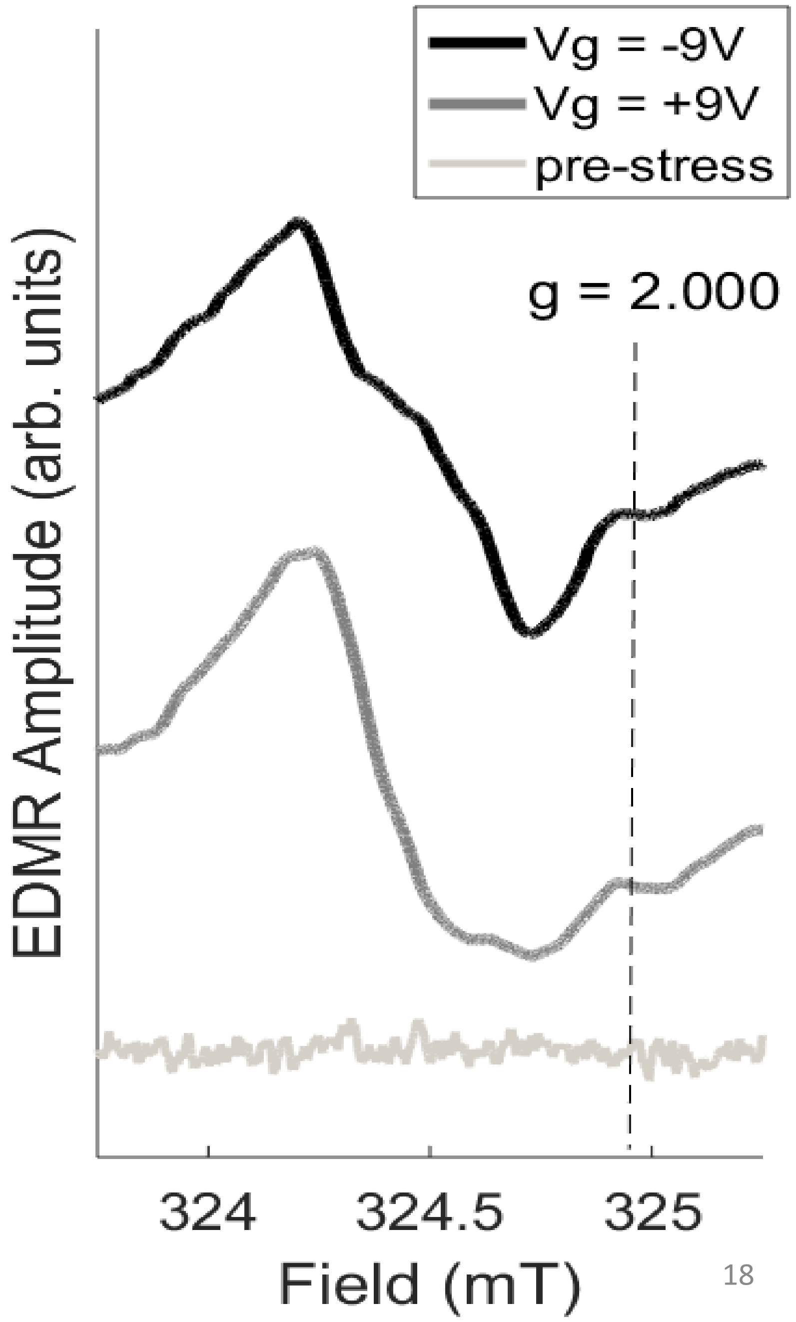
Spin-Dependent Trap Assisted Tunneling EDMR

- A weaker EDMR response is detected via SDTAT through the MOSFET gate
- The response is also dominated by P_{b0} and P_{b1} interface dangling bonds, and the response increases with stress time
- The lack of E' oxide trap response is surprising considering the 7.5nm thickness of the gate dielectrics



But… Where are the Oxide Defects?

- In low temperature (T = 200K) SDR EDMR measurements of high-field stressed MOSFETs, a small E’ center signal is seen
  - **We know E’ centers are present**, and likely involved in TDDB [24]
- Given the oxide thickness of 7.5nm, we would expect oxide trap – oxide trap tunneling events to dominate
- The **rate limiting tunneling event** must be the oxide trap – interface trap step



Summary of Atomic Scale Processes in TDDB

- We have extended the physical understanding of TDDB in MOS oxides using new methods (EDMR/NZFMR)
- EDMR and NZFMR results point to the following conclusions:

1. Interface dangling bond generation throughout device lifetime
2. At least some oxide E’ trap generation near the interface
3. Hydrogen redistribution near the interface
4. An important rate-limiting trap-assisted tunneling step between oxide and interface traps

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