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U.S. NAVAL RESEARCH LABORATORY

Vertical GaN Devices for Medium-Voltage Power Electronics

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arpa·e CHANGING WHAT'S POSSIBLE

OPEN

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Special Session on Medium- and High-Voltage Gallium Nitride Power Devices

October 11, 2021

U.S. DEPARTMENT OF ENERGY

NNSA National Nuclear Security Administration

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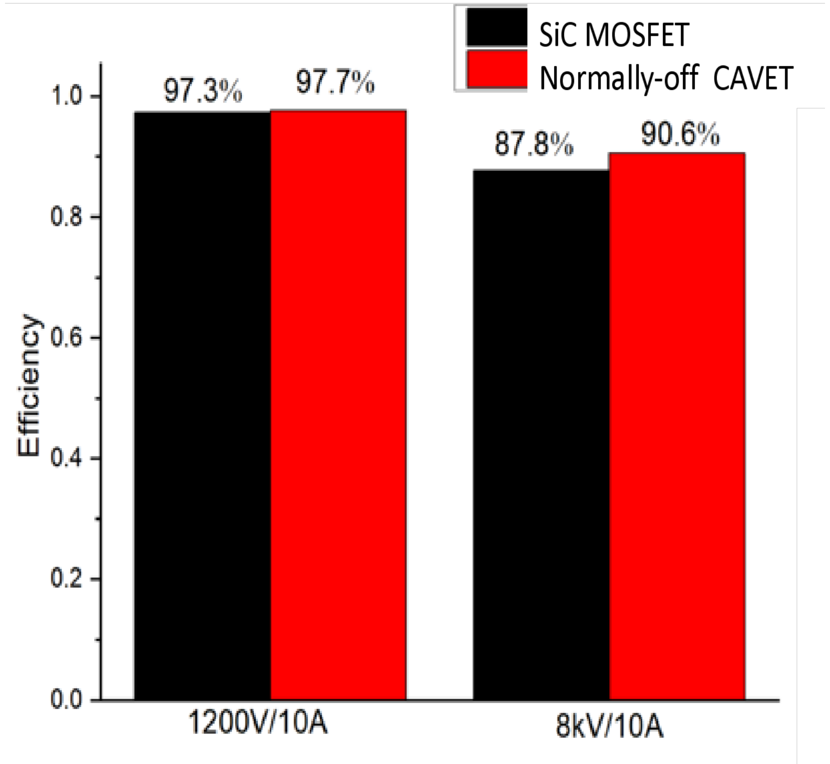
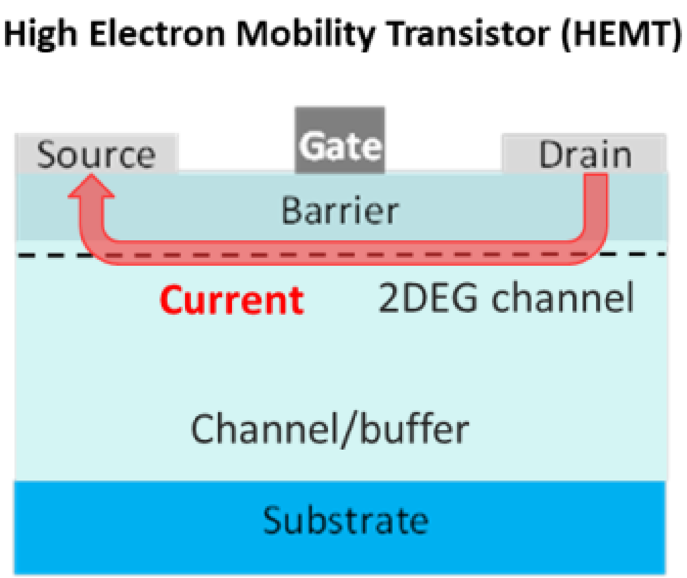
GaN may be Advantageous when Scaled to Medium Voltage

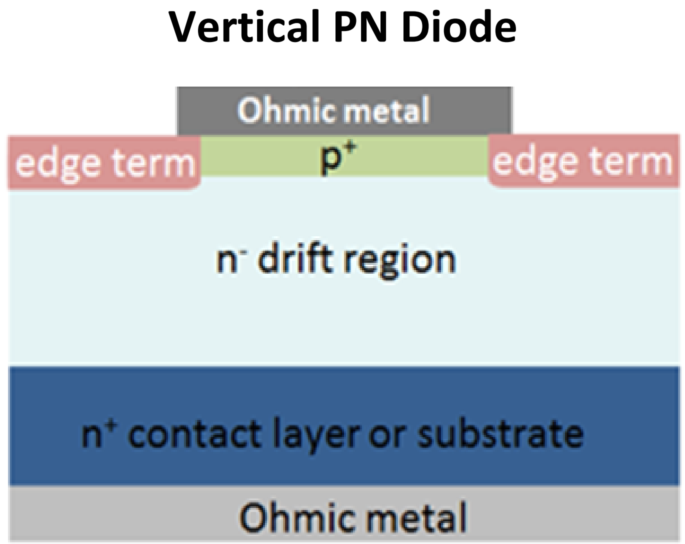
- Critical field of GaN ~2.8 MV/cm at $N_D = 1\times10^{16}$ cm^{-3} and room temperature based on most recent impaction ionization measurements [1]
- Slightly higher than E_C of SiC at the same temperature and doping [2]
- But higher mobility of GaN ~1200 cm^2/Vs [3] compared to ~950 cm^2/Vs for SiC [2] at the same doping and temperature lead to improvements in power converter efficiency [4]
- But devices are not widely available – a vertical GaN foundry is needed that monitors yield, reliability, etc.



[1] D. Ji, B. Ercan, and S. Chowdhury, "Experimental Determination of Impact Ionization Coefficients of Electrons and Holes in Gallium Nitride Using Homojunction Structures," *Appl. Phys. Lett.* **115**, 073503 (2019).
[2] J. A. Cooper and D. Morisette, "Performance Limits of Vertical Unipolar Power Devices in GaN and 4H-SiC," *Elec. Dev. Lett.* **41**, 892 (2020).
[3] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical Power PN Diodes Based on Bulk GaN," IEEE Trans. Elec. Dev. 62(2), 414 (2015).
[4] D. Ji and S. Chowdhury, "On the Progress Made in GaN Vertical Device Technology – Special Issue on Wide Band Gap Semiconductor Electronics and Devices," *Int. J. High-Speed Elec. Sys.* **28(01n02)**, 1940010 (2019).

Lateral vs. Vertical GaN Power Devices





Lateral Device

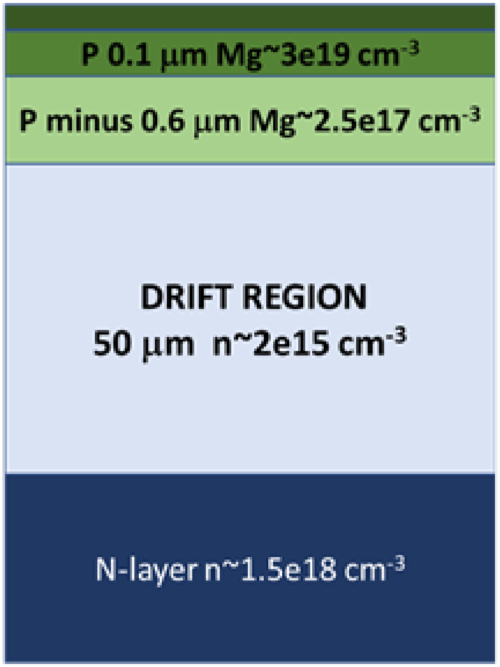
- **Current flow and voltage drop parallel to surface**
- **Availability of heterostructures is an advantage**
- **Electric field management is challenging – voltage scaling is lateral (consumes more chip area)**
- **Commercial GaN power devices available from many manufacturers, but generally <650 V**

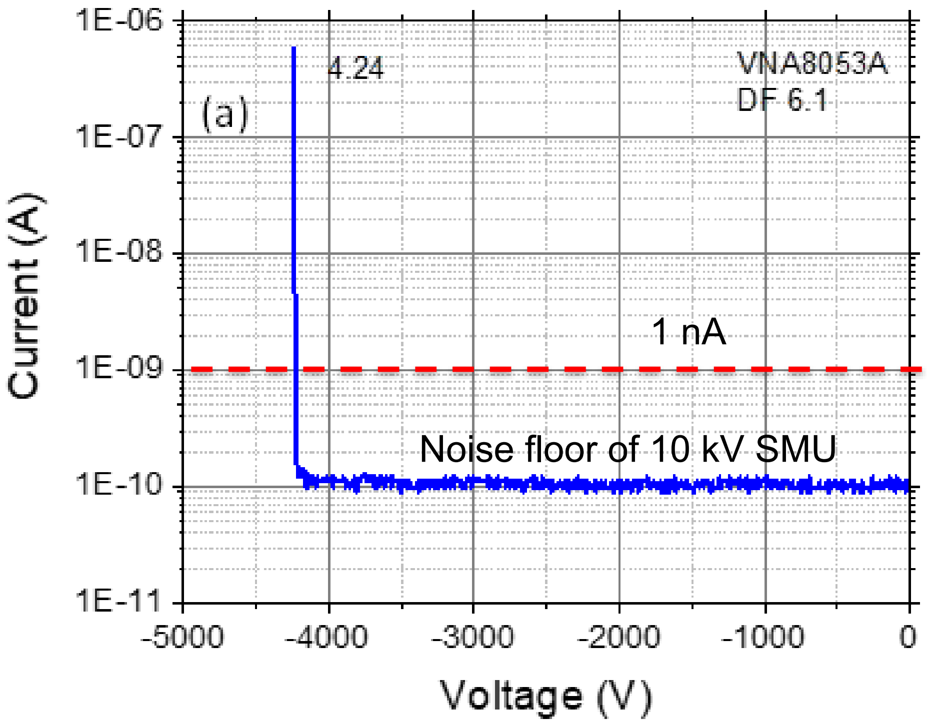
Vertical Device

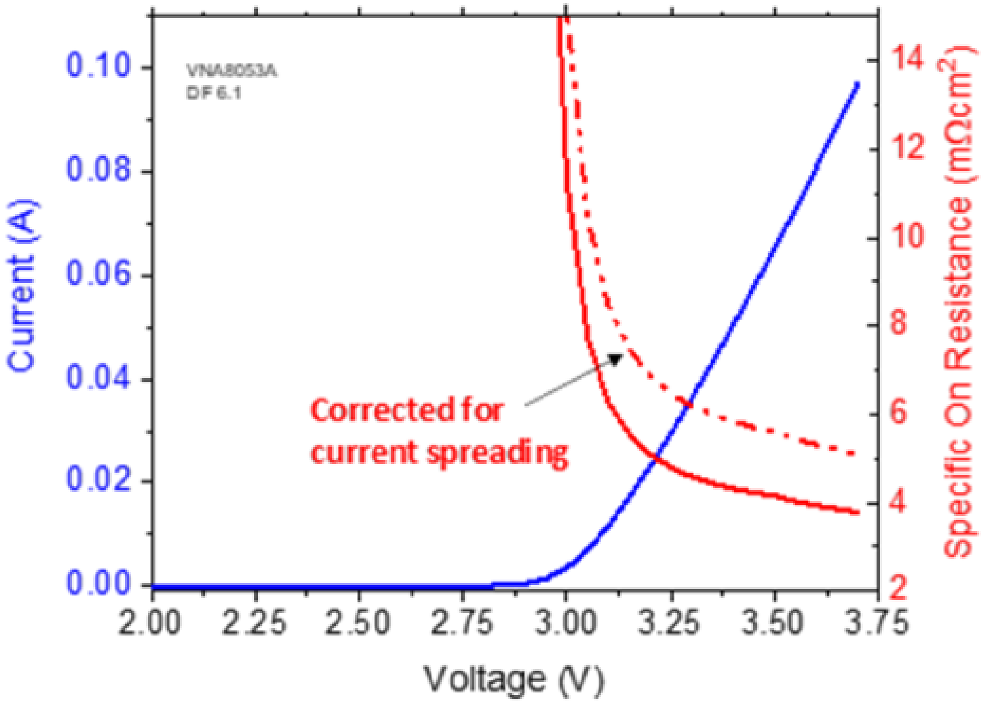
- **Current flow and voltage drop perpendicular to surface**
- **Architecture is better-suited to high voltage devices – voltage scaling accomplished by thickening drift region (does not consume more chip area)**
- **But requires native substrates and low doping**

IV Curves for Representative MV Vertical GaN PN Diode

- **MOCVD growth, step-etched JTE (30 μm step width for device below)**
- **Device shown has 0.063 mm2 area; 1 mm^2 devices also fabricated and tested**







- **V_b ~4.2 kV with very low leakage current until breakdown; not clear if limited by drift region or JTE**
- **Current spreading assumes 45-degree angle ➔ $R_{sp,on}$ = 5.1 mΩ cm^2**

A. Allerman, M. Crawford, J. Dickerson, J. Steinfeldt, L. Yates, M. Smith

Commercialization Potential: Vertical GaN Foundry

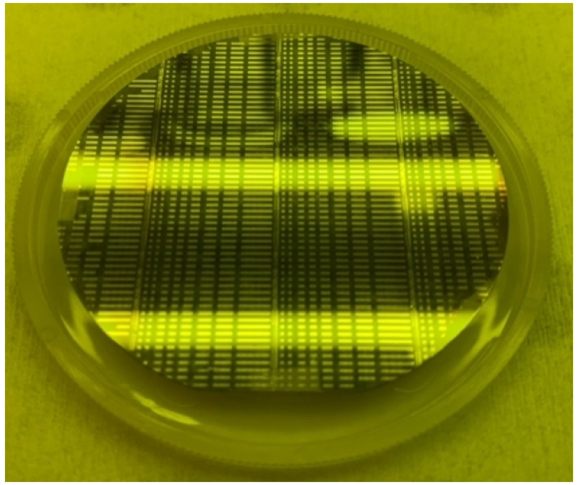
Lot	# of wafers	Experiments
1	2	Edge termination
2	4	Vary Anode thickness Alignment to dot-core
3	4	Type I (uniform) substrates
4	4	Vary drift layer thickness
5	6	Vary anode doping and other process variations
6	4	Baseline Process w/ improved epi and high yield wafers
7	3	Baseline Process w/ improved epi and new mask
8	4	New mask, varying implant profiles
9	4	Large-area mask, Back side process demo

- **Epitaxial growth done at Sandia by MOCVD and wafers delivered to NRL for characterization and processing**
- **35 wafers delivered to date, 23 processed through metals/isolation**
- **>26,000 devices processed to date**

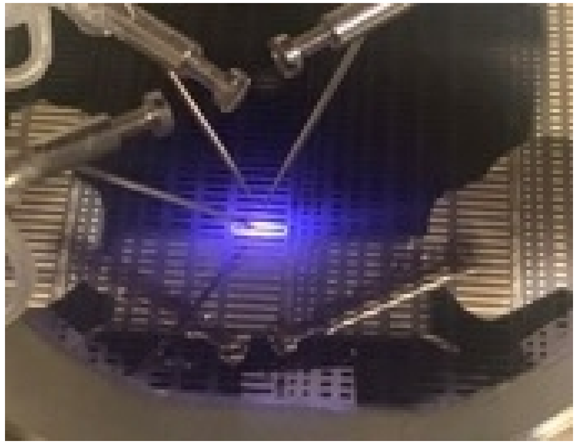
T. Anderson, J. Gallagher, A. G. Jacobs, K. Hobart, B. Gunning

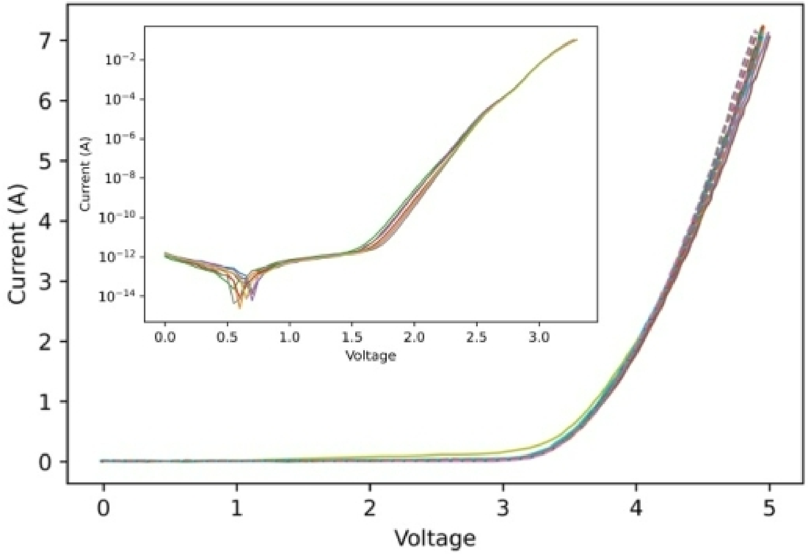
Foundry Electrical Testing and Results

Typical foundry wafer



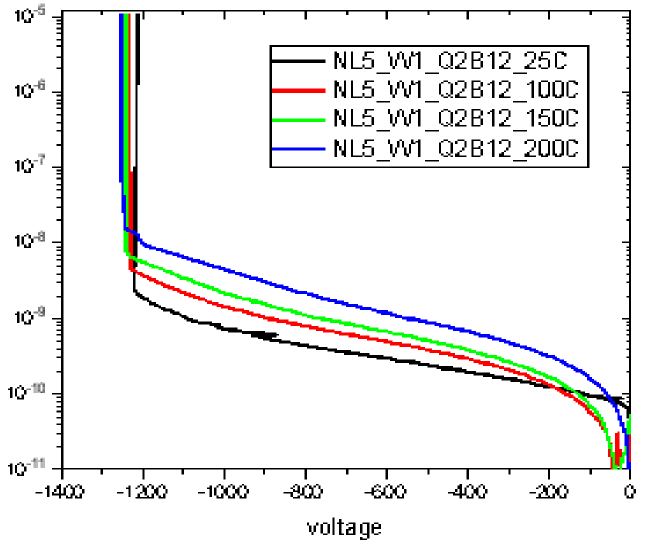
Wafer under test





Forward IV:

- **Several amps of current demonstrated for 1 mm^2 devices**



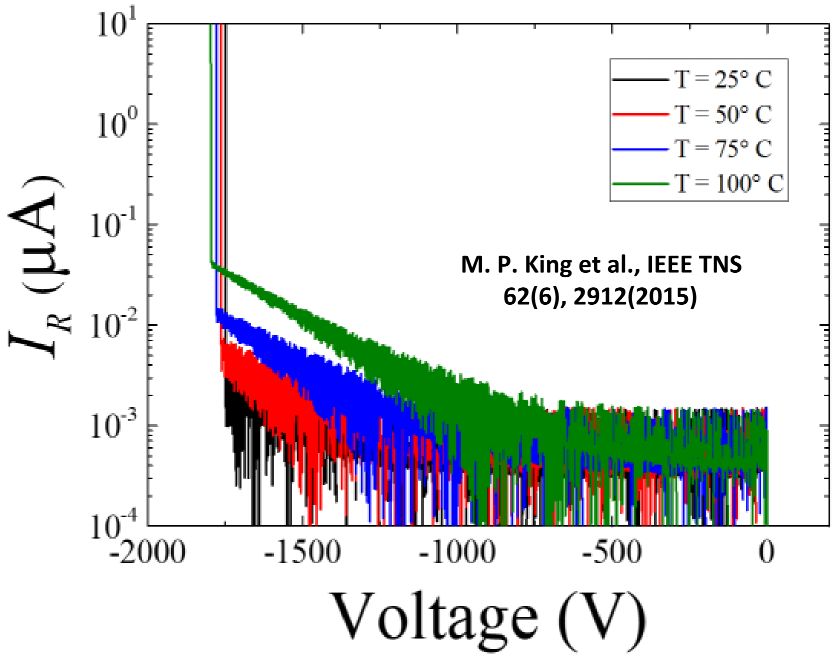
Reverse IV:

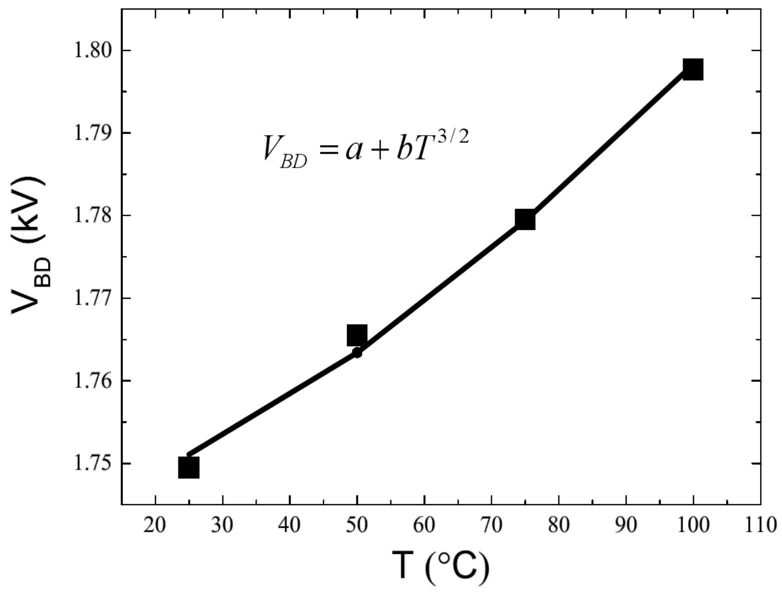
- **>1.3 kV breakdown demonstrated**
- **Positive temperature coefficient of breakdown consistent with avalanche**

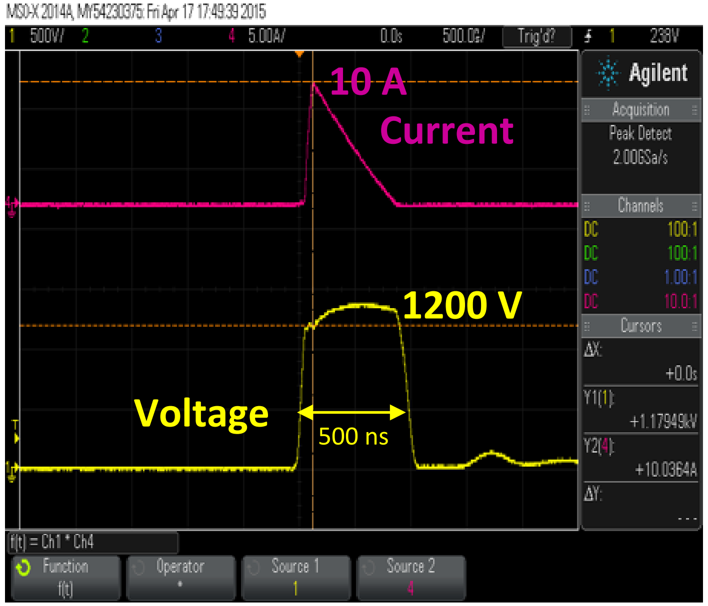
T. Anderson. M. Ebrish

Avalanche Ruggedness of Vertical GaN

- **Avalanche breakdown mechanism demonstrated via temperature dependence**
- **Avalanche ruggedness demonstrated in real power switching circuits**
- **Very different from the situation for GaN-on-Si power devices, where avalanche breakdown does not occur**

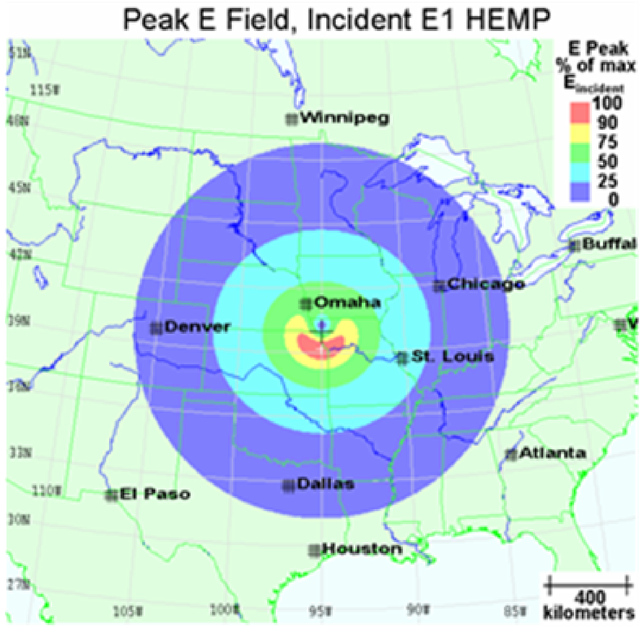






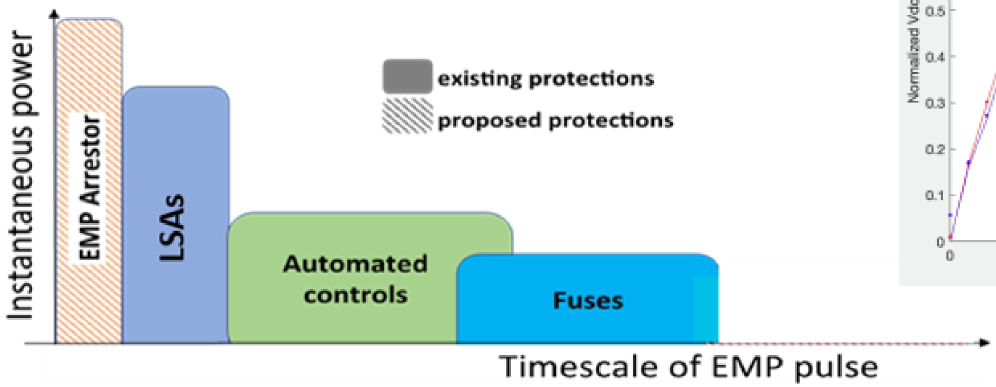
O. Aktas and I. C. Kizilyalli, IEEE EDL 36(9), 890 (2015)

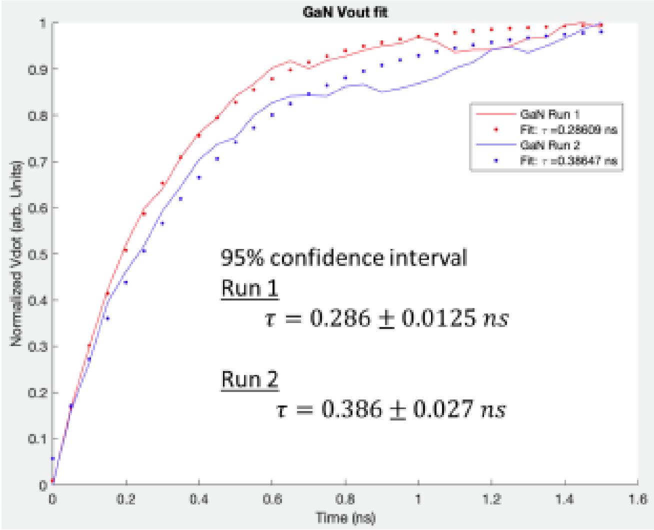
Special Application: Protection for the Electric Grid



➢ Electromagnetic pulses are a threat to the grid
- Very fast E1 component (< 1 ms)
- Unaddressed by current SOA technology (LSAs)

Use fast avalanche to clamp voltage and shunt current to protect grid equipment





➢ Transient protection is needed for MV grid-connected systems

GaN time to breakdown <1 ns

J. S. Foster Jr. et al., "Report of the Commission to Assess the Threat to the United States from Electromagnetic Pulse (EMP) Attack: Critical National Infrastructures," *Defense Technical Information Center* (2008).

J. Flicker

Questions?

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