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Vertical GaN PN Diodes for Grid Resiliency and Medium-Voltage Power Electronics

SOTAPOCS
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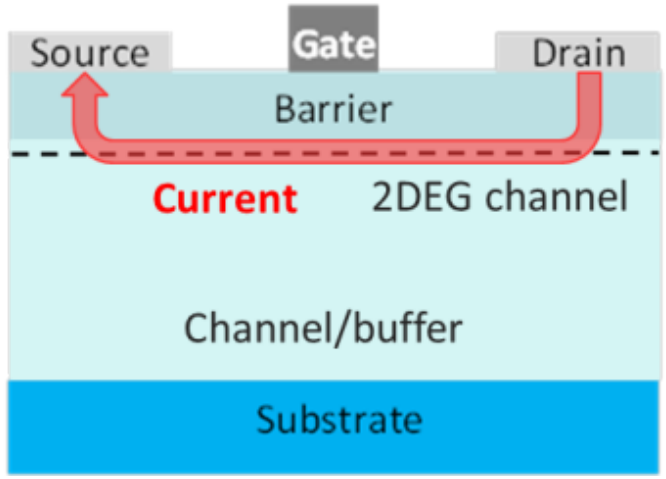
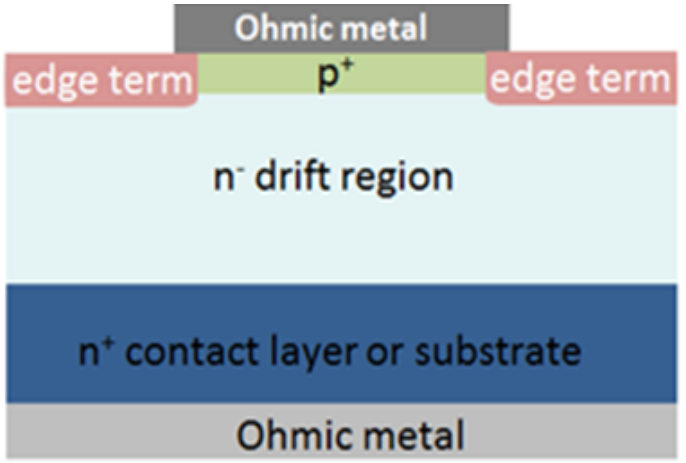
Introduction: Lateral vs. Vertical GaN Power Devices

High Electron Mobility Transistor (HEMT)



PN Diode



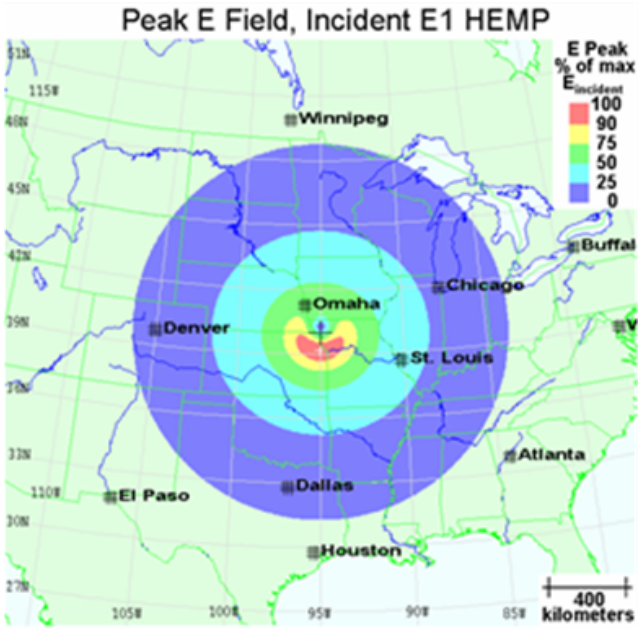
Lateral Device

- Current flow and voltage drop parallel to surface
- Availability of heterostructures is an advantage
- Electric field management is challenging – voltage scaling is lateral (consumes more chip area)
- Commercial GaN power devices available from many manufacturers, but generally <650 V

Vertical Device

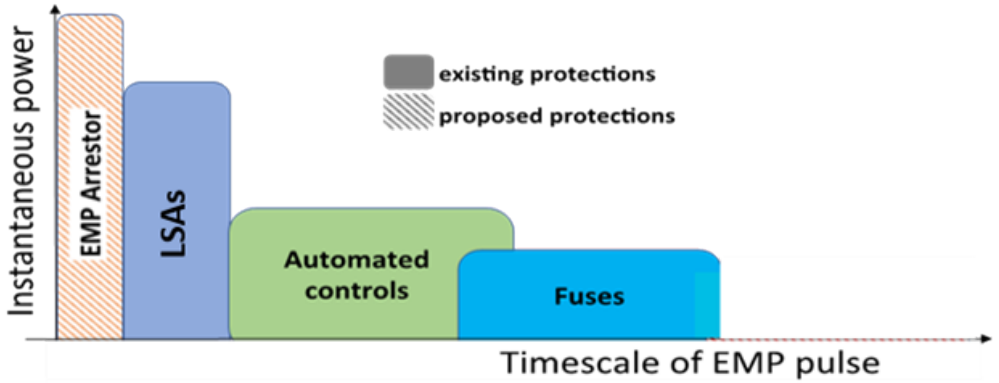
- Current flow and voltage drop perpendicular to surface
- Architecture is better-suited to high voltage devices – voltage scaling accomplished by thickening drift region (d0esmnto consume more chip area)
- But requires native substrates and low doping

Protection for the Electric Grid



- Electromagnetic pulses are a threat to the grid
  - Very fast E1 component (< 1 ms)
  - Unaddressed by current SOA technology (LSAs)

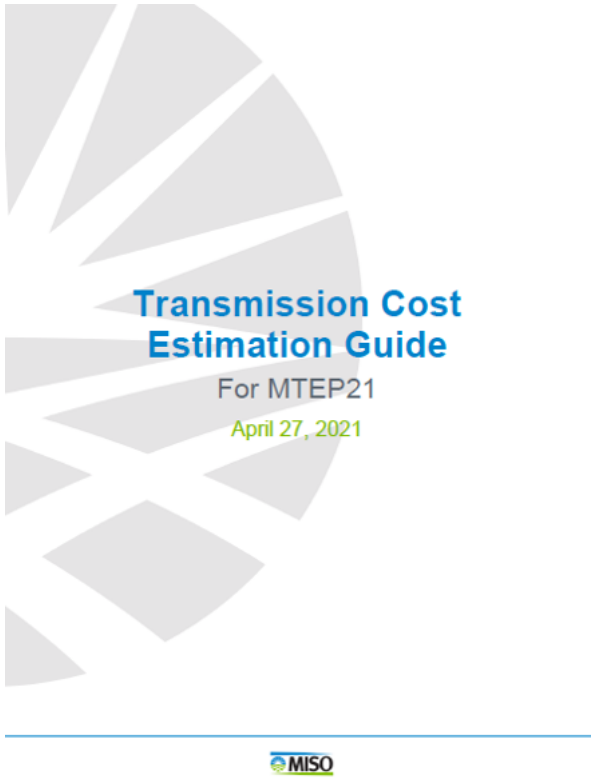
- Transient protection is needed for MV grid-connected systems



J. S. Foster Jr. et al., "Report of the Commission to Assess the Threat to the United States from Electromagnetic Pulse (EMP) Attack: Critical National Infrastructures," *Defense Technical Information Center* (2008).

A New Capability to Protect Grid Equipment

Cost estimates for grid equipment may be obtained from regional Independent System Operators (ISOs). For example, from the Midwest ISO:



New substation – 4 positions (ring / breaker-and-a-half / double-breaker bus)							
Scope of work	69kV	115kV	138kV	161kV	230kV	345kV	500kV
Land required (acre)	1.6 / 2.0 / 2.4	1.8 / 2.3 / 2.7	2.0 / 2.5 / 3.0	2.2 / 2.8 / 3.3	2.4 / 3.0 / 3.6	3.0 / 3.8 / 4.5	5.0 / 6.3 / 7.5
Access road (mile)	1 / 1 / 1	1 / 1 / 1	1 / 1 / 1	1 / 1 / 1	1 / 1 / 1	1 / 1 / 1	1 / 1 / 1
Circuit breakers (each)	4 / 6 / 8	4 / 6 / 8	4 / 6 / 8	4 / 6 / 8	4 / 6 / 8	4 / 6 / 8	4 / 6 / 8
Disconnect switches (each)	8 / 12 / 16	8 / 12 / 16	8 / 12 / 16	8 / 12 / 16	8 / 12 / 16	8 / 12 / 16	8 / 12 / 16

<u>Estimated costs for 115 kV substation:</u>

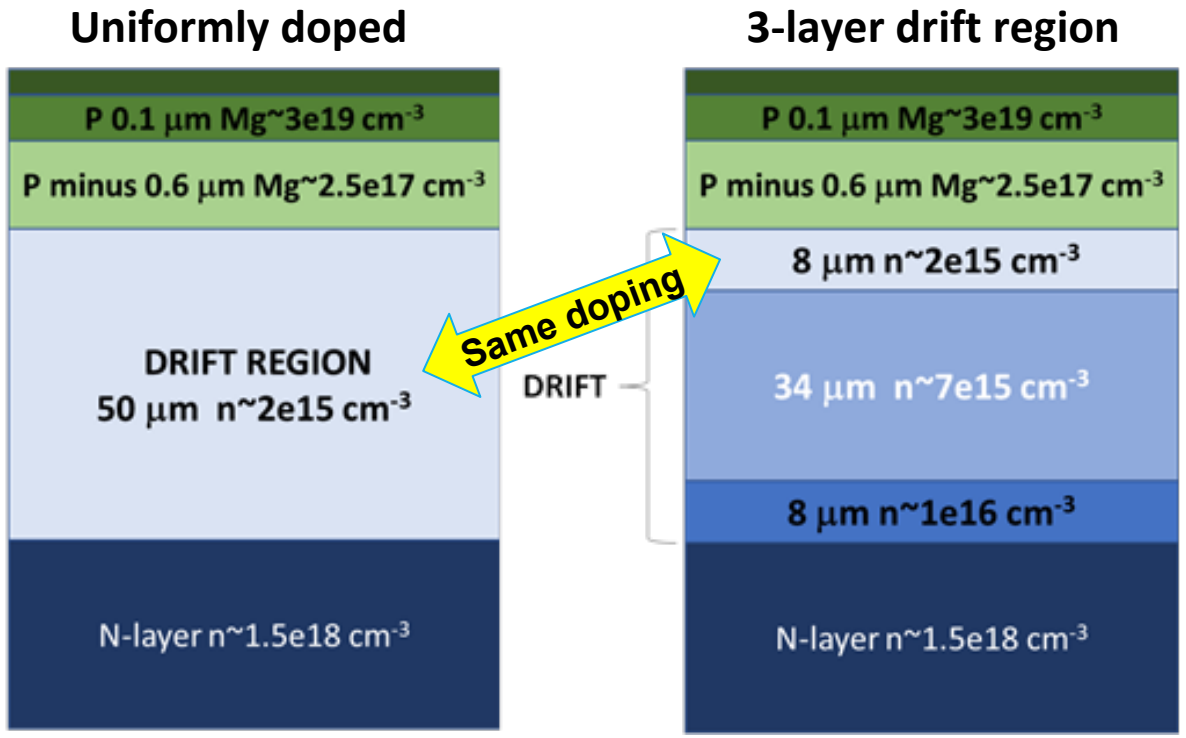
- **~$5K / 1000 ft on wires**
- **$84K on circuit breakers**
- **$49K on disconnect switches**
- **$80K on PTs (to measure voltage)**
- **$105K on CTs (to measure current)**
- **$5K / MVA on the transformer**

A fast arrestor is needed to protect expensive grid equipment that is currently vulnerable to E1

J. Flicker

https://cdn.misoenergy.org/Transmission%20Cost%20Estimation%20Guide%20for%20MTEP21337433.pdf

GaN PN Diode Epilayers for >5 kV Devices



Motivation for 3-layer drift region design:

- Do not expect higher breakdown voltage; potential for reduced R_{on}
- Growth benefits: Higher No allows for higher growth rate (more C thus compensation).
- Prior 5 kV results: Hosei Univ*

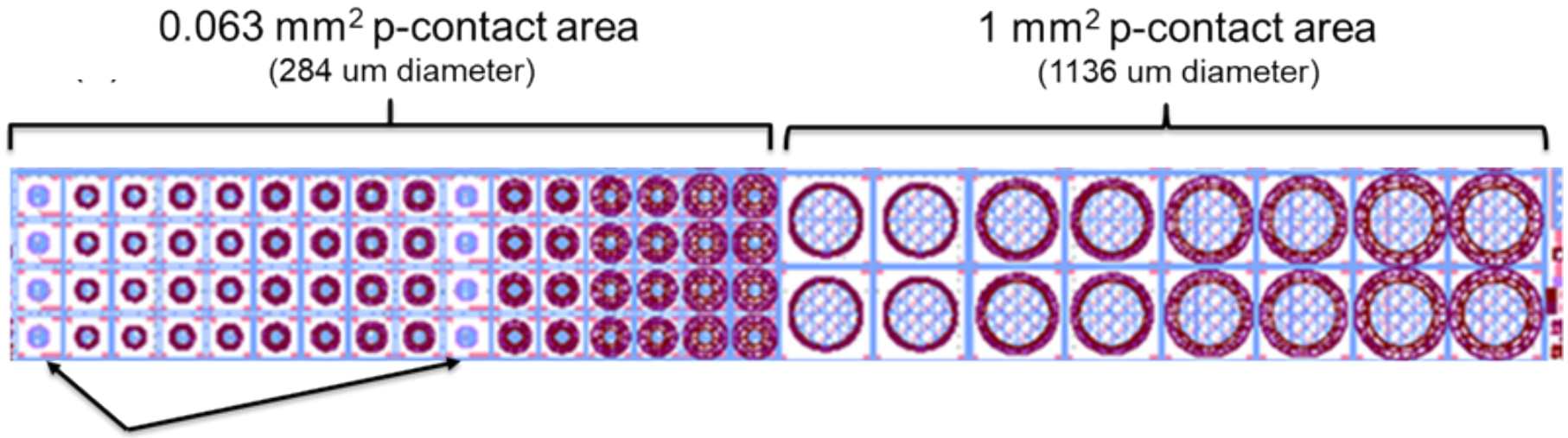
Key Attributes:

- 50 μm thick drift regions
- Two drift doping designs: Uniform and multi-layer doping levels
- Lowest p-minus doping to date (Mg ~ 2.5e17 cm^{-3})

* Similar to Ohta et al., Jpn. J Appl Phys 57, 04FG09 (2018)

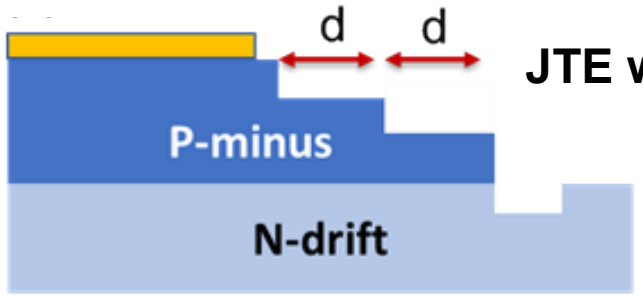
A. Allerman (growth), J. Dickerson (modeling)

Mask Layout for >5 kV Devices



Multi-step ICP Etched JTE

P-Area (mm^2)	Step Width d (μm)						
0.063	10	20	30	40	50	75	100
1		20			50	75	100



JTE width = 2d

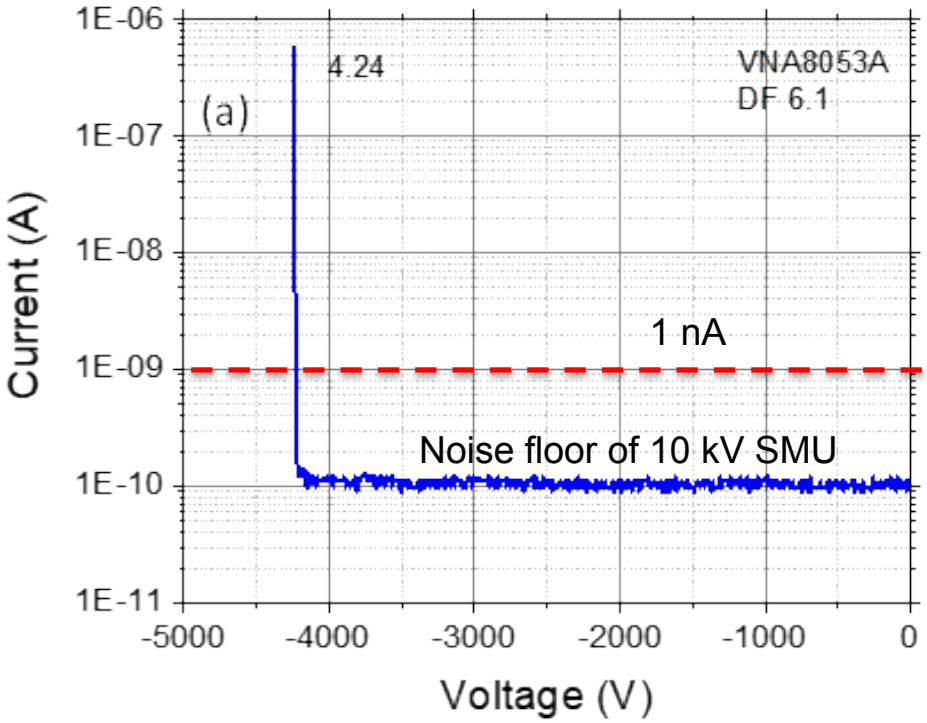
- **Devices do not yet have dielectric passivation or thick bond-pads**
- **Tested in Fluorinert**

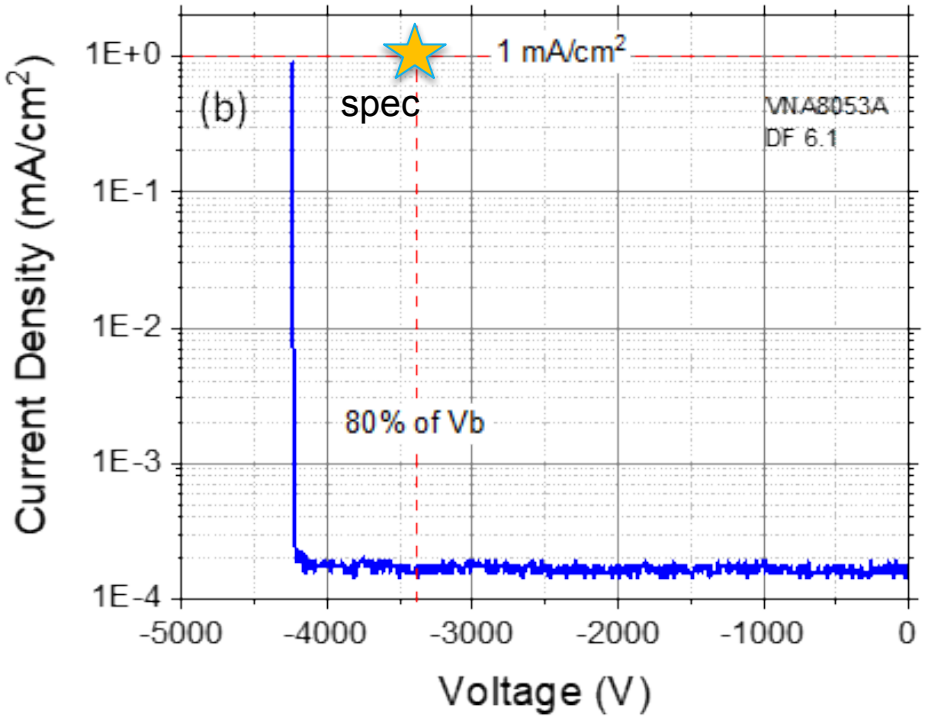
J. Steinfeldt, M. Crawford

Reverse IV for Uniformly Doped Drift Region Device

- **Uniformly-doped drift region, 30 µm step width**
- **Example of higher-performing device - reverse IV**

0.063 mm²



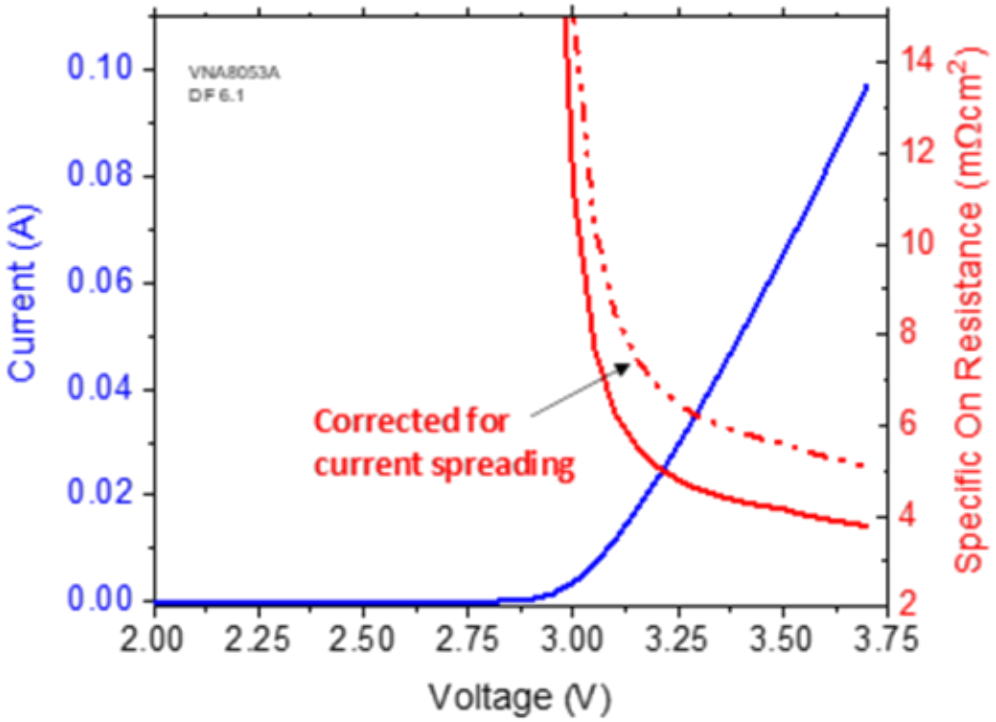


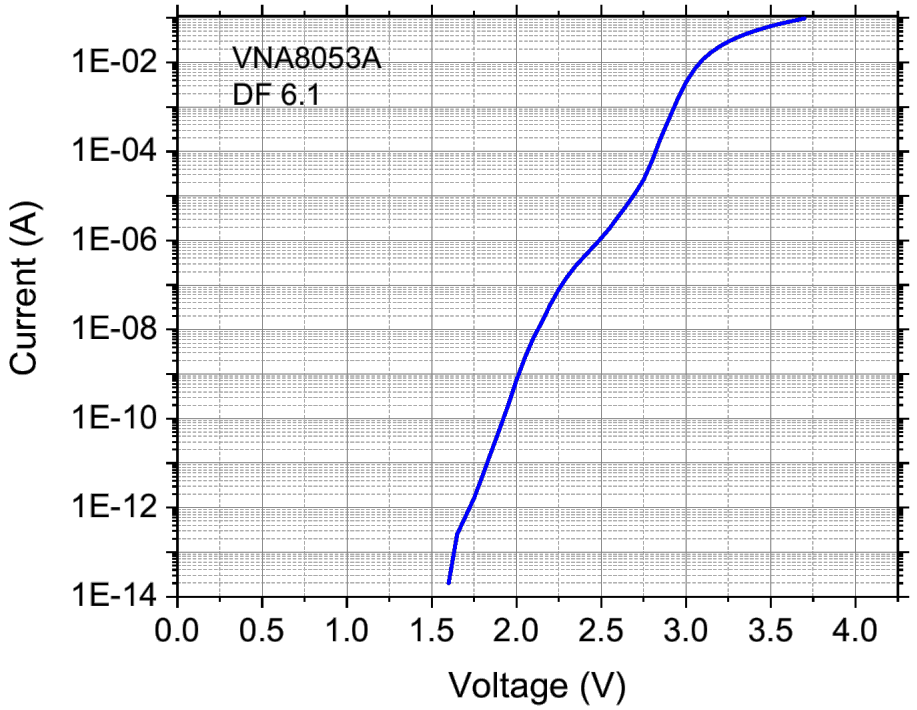
- **V_b ~4.2 kV; maintains very low current leakage until breakdown**
- **Difficult to say whether breakdown is limited by drift region or JTE**

Forward IV for Uniformly Doped Drift Region Device

- **Uniformly-doped drift region, 30 µm step width**
- **Same higher-performing device - forward IV**

0.063 mm²



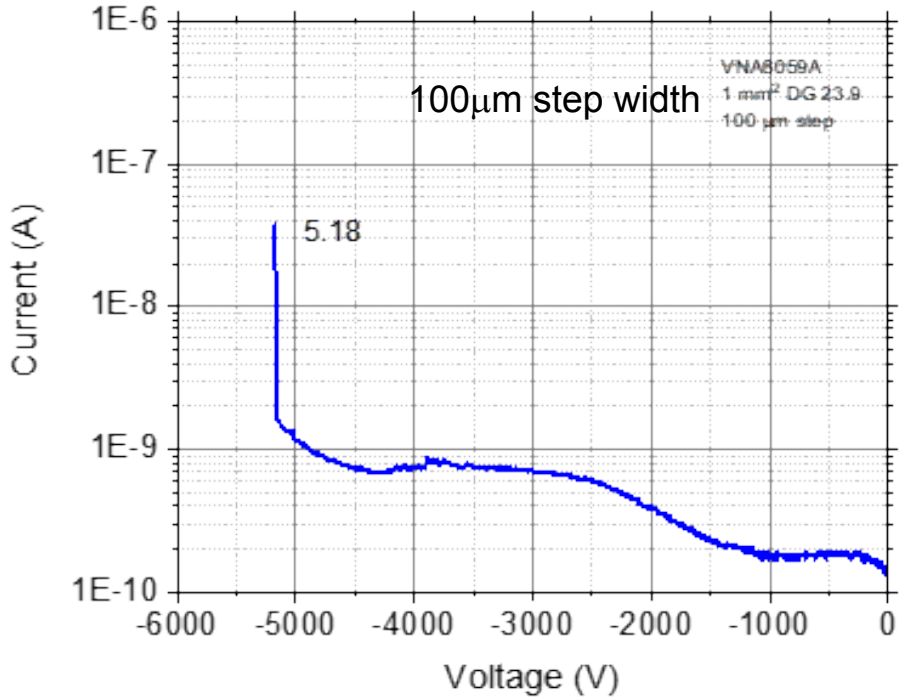


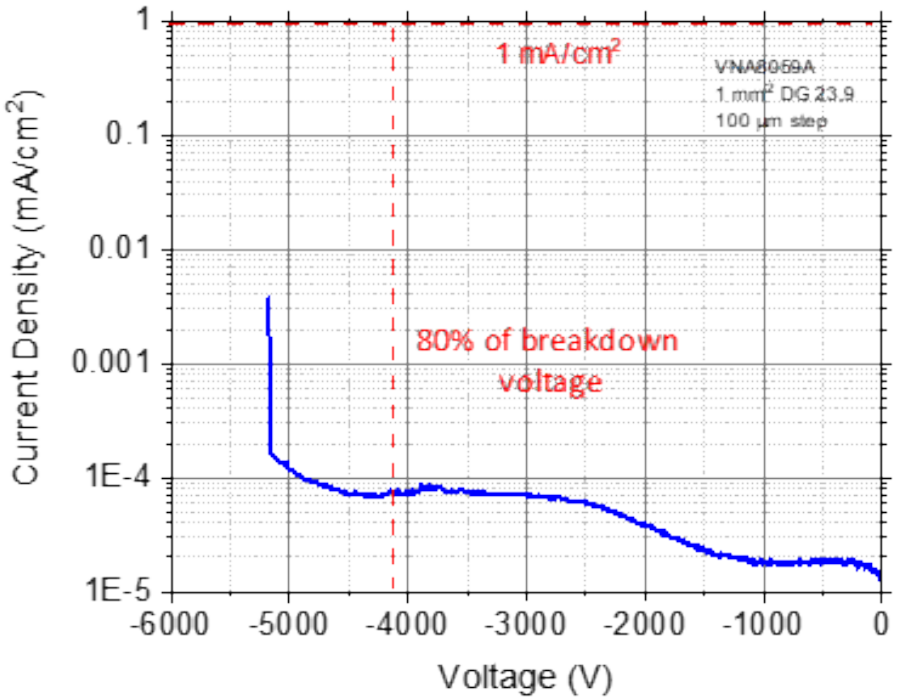
- **Current spreading assumes 45-degree angle ➔ $R_{sp,on}$ = 5.1 mΩ cm²**

Reverse IV for 3-Layer Drift Region Device

- 3-layer drift region, 100 mm step width
- Lower yield due to larger area
- Highest performing device shown

1 mm²



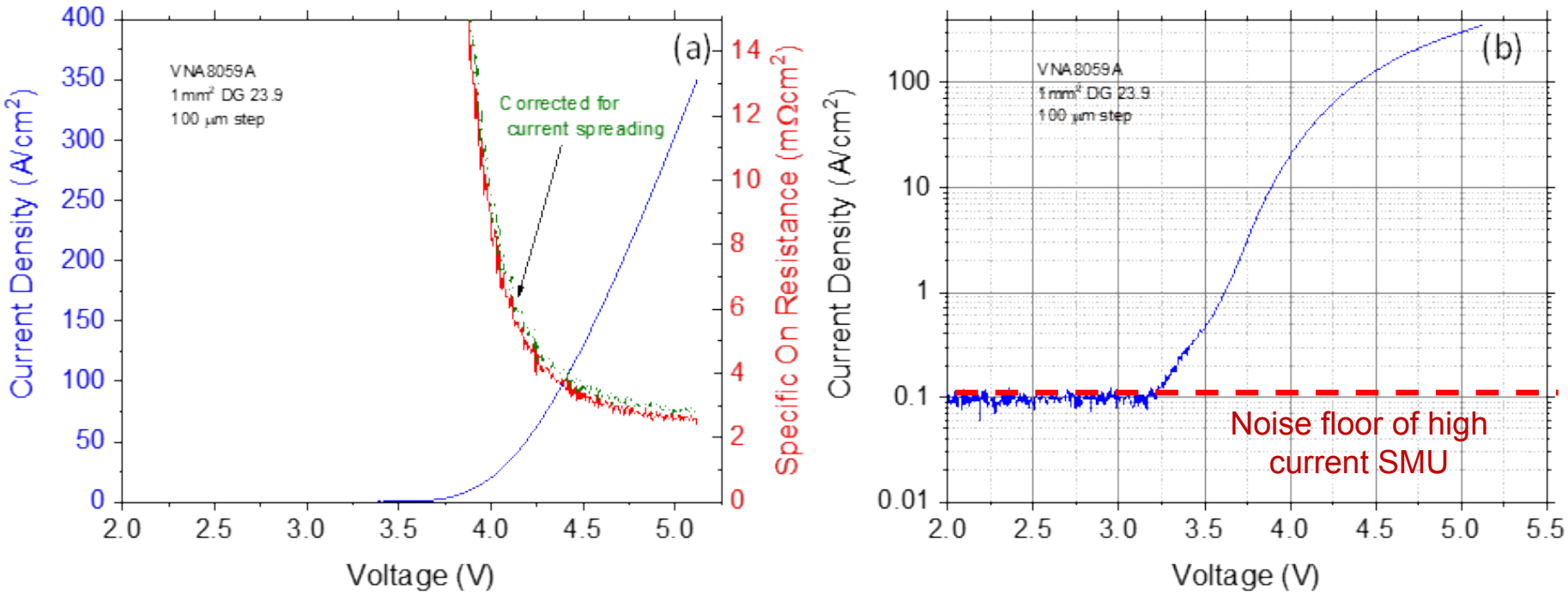


- Device not taken to as high compliance, did not suffer permanent degradation
- Also has good breakdown, difficult to say which drift region design is superior

Forward IV for 3-Layer Drift Region Device

- **Pulsed high current forward IV measurement**
- **Up to 3.5 A with 500 μsec sec pulses and 0.1% duty cycle**
- **Data are for same device**

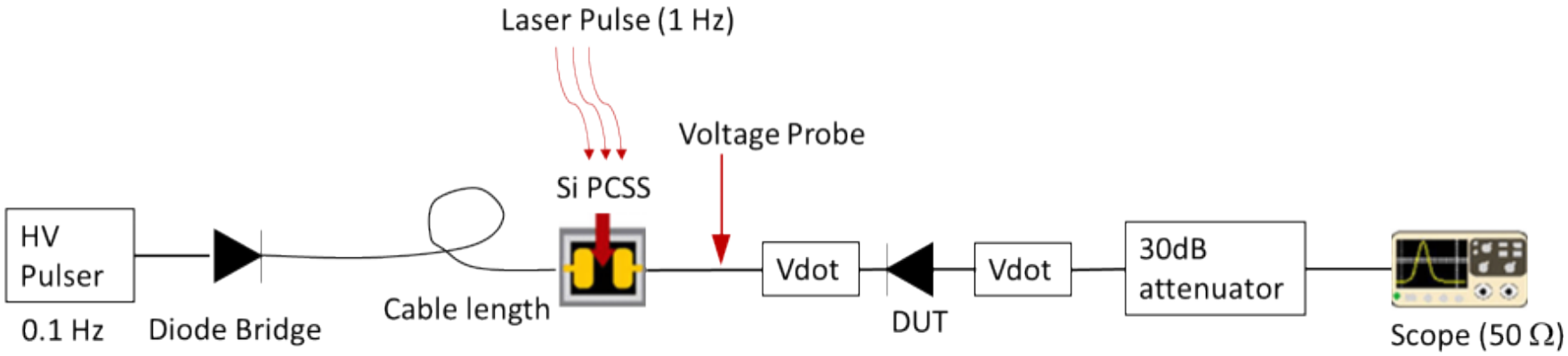
1 mm²



- **Specific on-resistance ~2.4 mΩ cm² including current spreading factor (45°)**
- **Taken up to 350 A/cm² – multiple scans, no degradation**

L. Yates, M. Smith

Time Response of Breakdown: GaN vs SiC

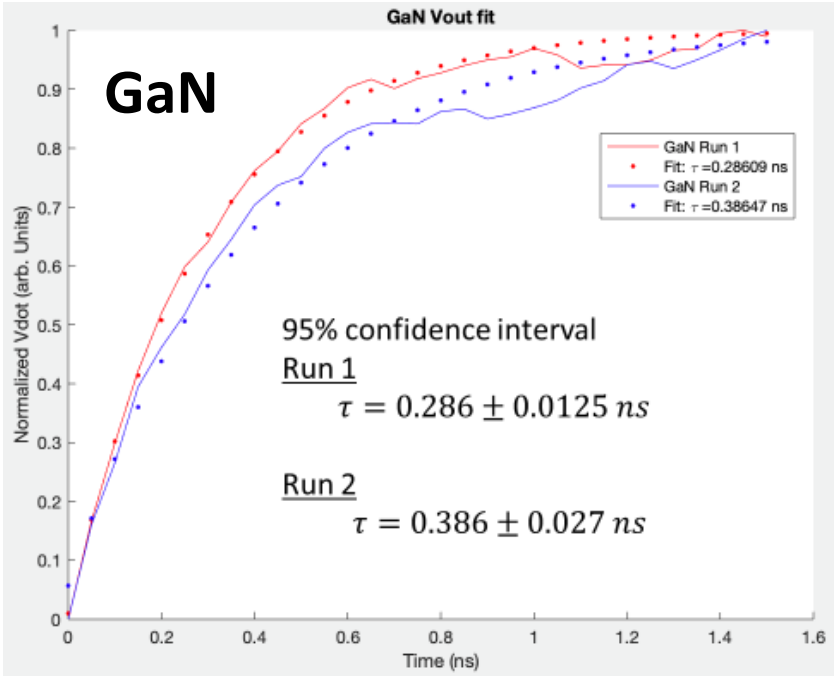


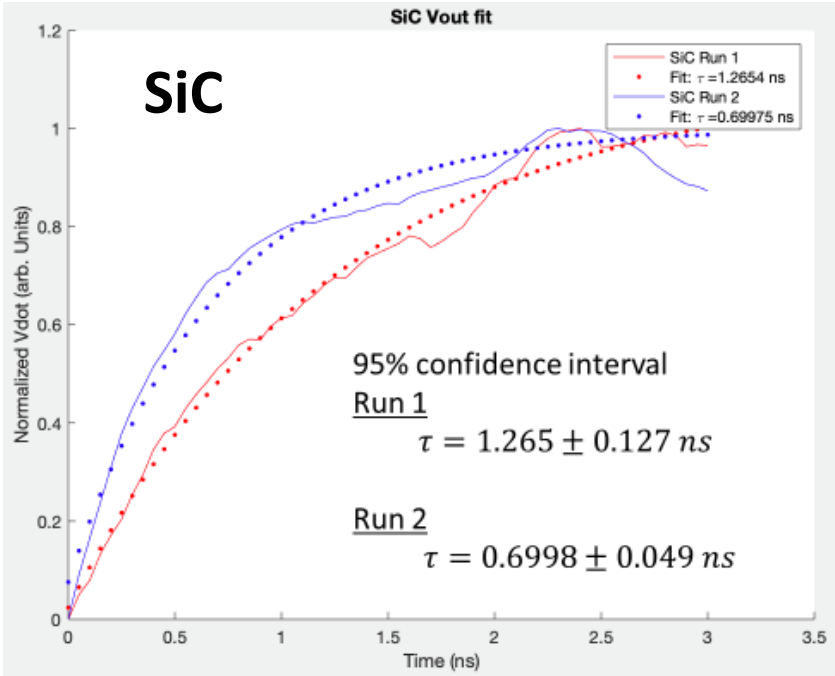
J. Flicker

Fit Data to: $-a \cdot e^{-\frac{t}{\tau}} + c$

$a \approx 1$

$c \approx 0$

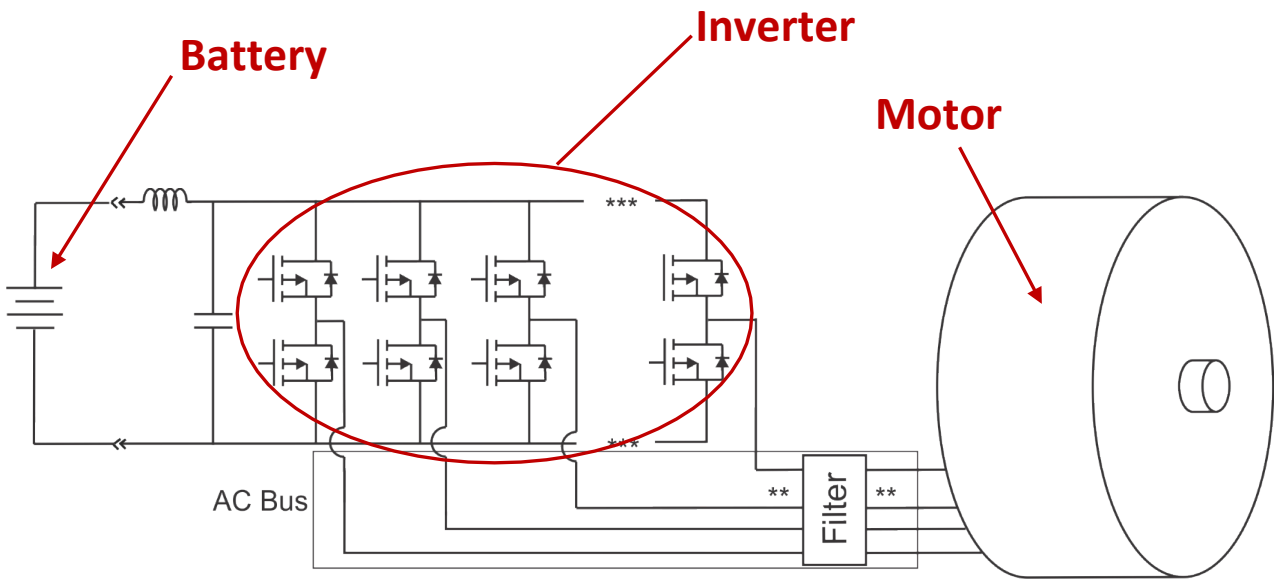


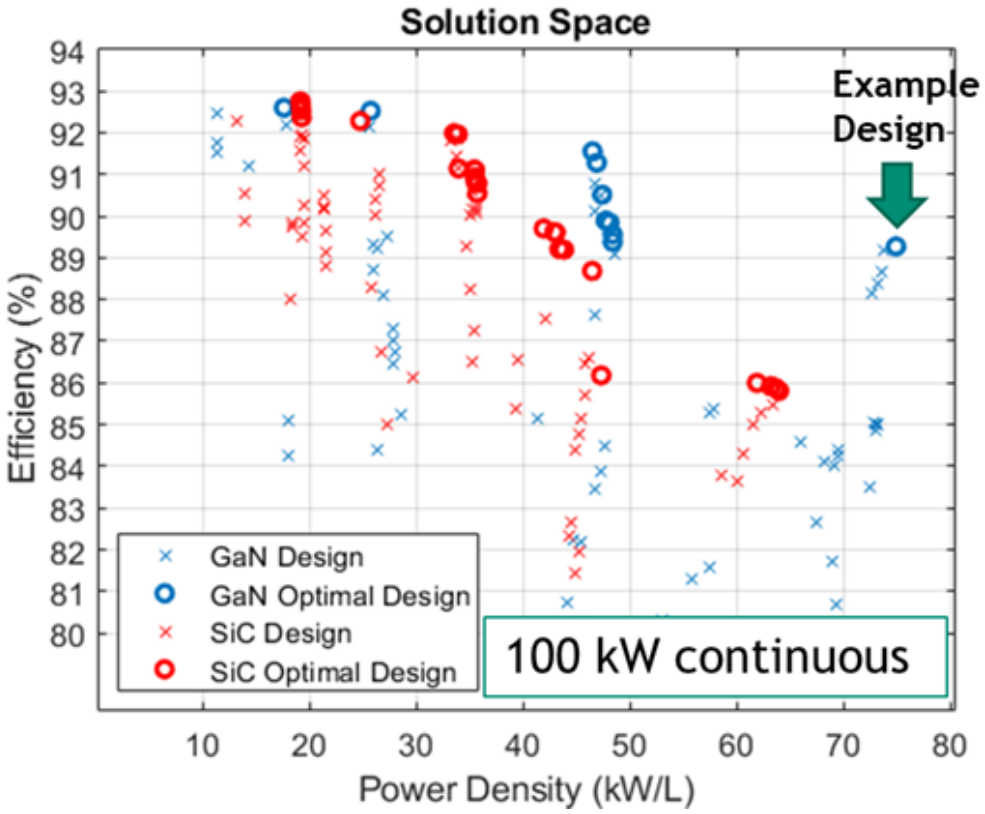


- **Within 95% confidence interval, GaN has a faster breakdown response than SiC**

Example: Advantages of Vertical GaN for Electric Vehicles

Electric Drivetrain Schematic





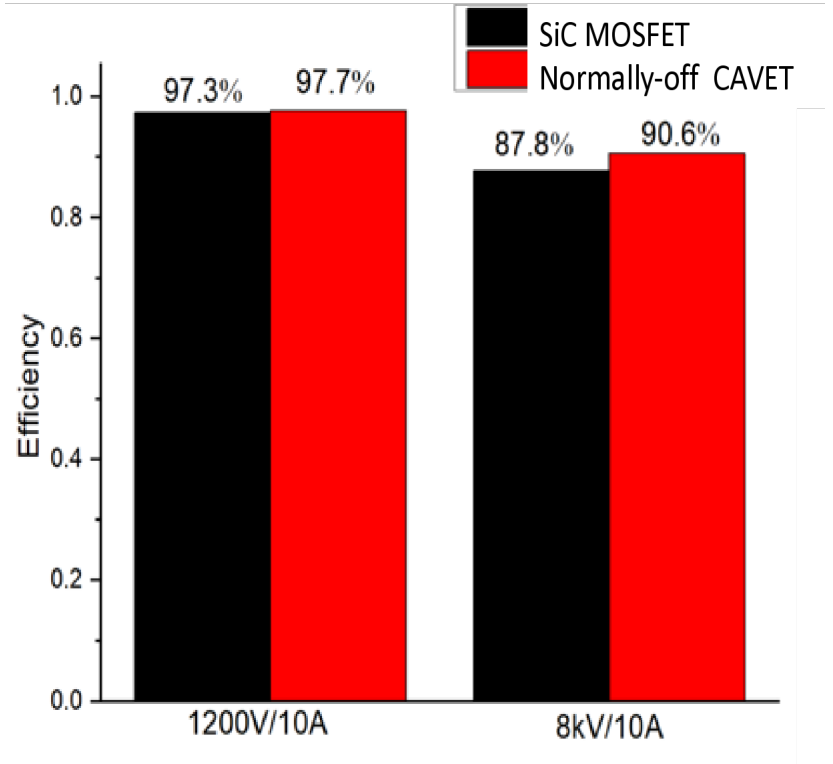
- Inverter and optional boost converter require switch-diode pairs (typical for switch-mode power conversion circuits)
- MOSFET and JBS diode are likely good choices (JBS diode combines best properties of Schottky and PN diodes)

- System-level genetic optimization indicates that vertical GaN diodes may out-perform SiC in terms of efficiency and power density

J. Neely, G. Pickrell, J. Flicker, L. Rashkin, and R. Kaplar, "The Case for Vertical Gallium Nitride Devices in Electric Vehicle Drives," *2020 IEEE Applied Power Electronics Conference* (APEC2020), Industry Session: Vehicle Electrification II (Virtual).

GaN may be Advantageous when Scaled to Medium Voltage

- Critical field of GaN ~2.8 MV/cm at $N_D = 1\times10^{16}$ cm^{-3} and room temperature based on most recent impaction ionization measurements [1]
- Slightly higher than E_C of SiC at the same temperature and doping [2]
- But higher mobility of GaN ~1200 cm^2/Vs [3] compared to ~950 cm^2/Vs for SiC [2] at the same doping and temperature lead to improvements in power converter efficiency [4]
- But devices are not widely available – a vertical GaN foundry is needed that monitors yield, reliability, etc.



[1] D. Ji, B. Ercan, and S. Chowdhury, "Experimental Determination of Impact Ionization Coefficients of Electrons and Holes in Gallium Nitride Using Homojunction Structures," *Appl. Phys. Lett.* **115**, 073503 (2019).
[2] J. A. Cooper and D. Morisette, "Performance Limits of Vertical Unipolar Power Devices in GaN and 4H-SiC," *Elec. Dev. Lett.* **41**, 892 (2020).
[3] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical Power PN Diodes Based on Bulk GaN," IEEE Trans. Elec. Dev. 62(2), 414 (2015).
[4] D. Ji and S. Chowdhury, "On the Progress Made in GaN Vertical Device Technology – Special Issue on Wide Band Gap Semiconductor Electronics and Devices," *Int. J. High-Speed Elec. Sys.* **28(01n02)**, 1940010 (2019).

Multiple Lots Processed to Date in NRL Foundry

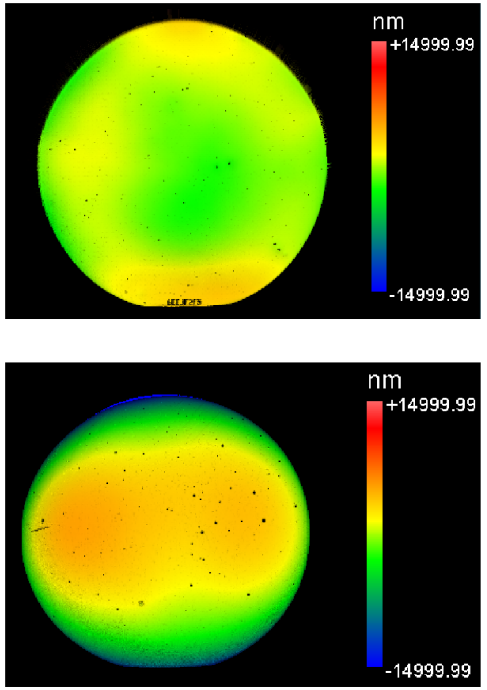
Lot	# of wafers	Experiments
1	2	Edge termination
2	4	Vary Anode thickness Alignment to dot-core
3	4	Type I (uniform) substrates
4	4	Vary drift layer thickness
5	6	Vary anode doping and other process variations
6	4	Baseline Process w/ improved epi and high yield wafers
7	3	Baseline Process w/ improved epi and new mask
8	4	New mask, varying implant profiles
9	4	Large-area mask, Back side process demo

- Epitaxial growth done at Sandia by MOCVD and wafers delivered to NRL for characterization and processing
- 35 wafers delivered to date, 23 processed through metals/isolation
- >26,000 devices processed to date

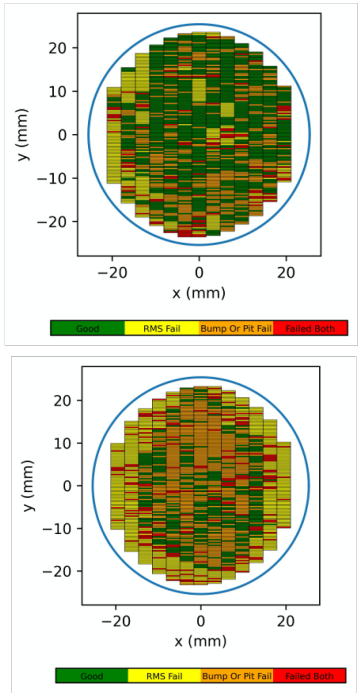
B. Gunning (growth)

Typical Incoming Wafer Metrology

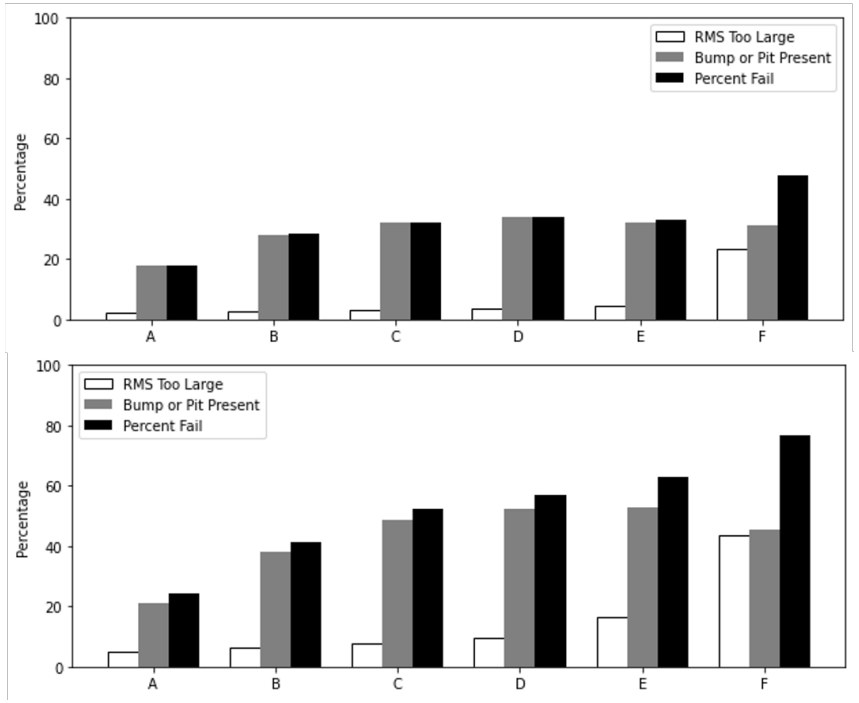
Raw Data



Device F Yield



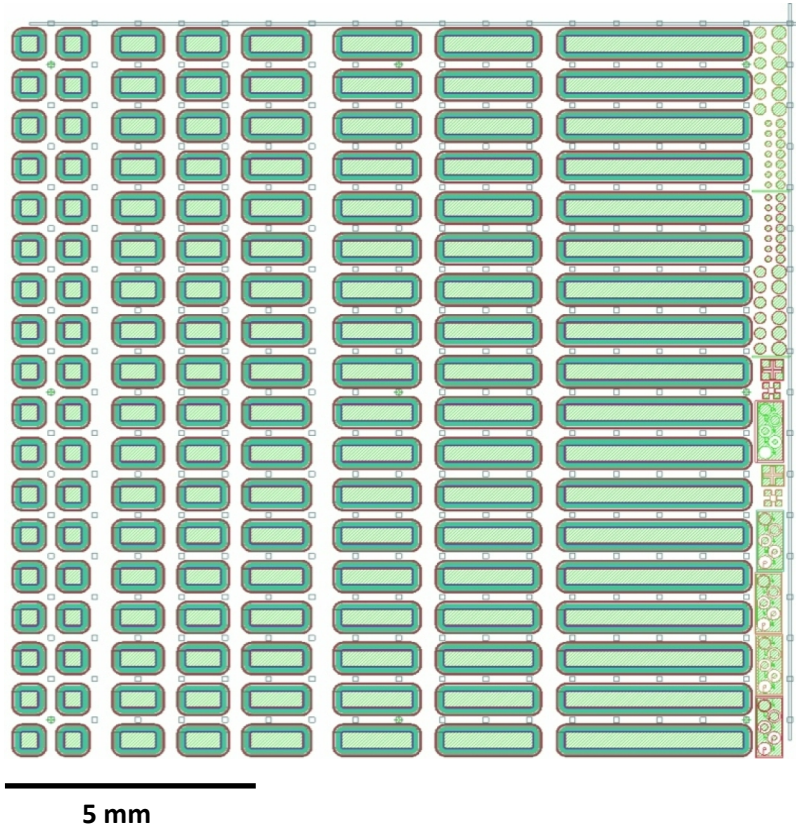
Failure Statistics



Geometry	Area (mm^2)	Devices (per 2" wafer)
A	0.105	280
B	0.215	280
C	0.325	150
D	0.430	150
E	0.535	150
F	1.05	140
Total		1150

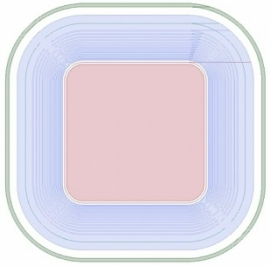
- Epitaxial growth done at Sandia, wafers delivered to NRL for characterization and processing
- Top wafer shows typical behavior – very few bumps/pits present
- Slightly more particles in bottom wafer, but still acceptable (first evaluation of different substrate)
- Images are representative of all wafers from a given epi growth campaign (typically several wafers)

Foundry Mask Layout



Base cell:
0.35 x 0.35 mm² anode

Larger devices scaled only in x-direction to avoid crossing dot-core (for now)



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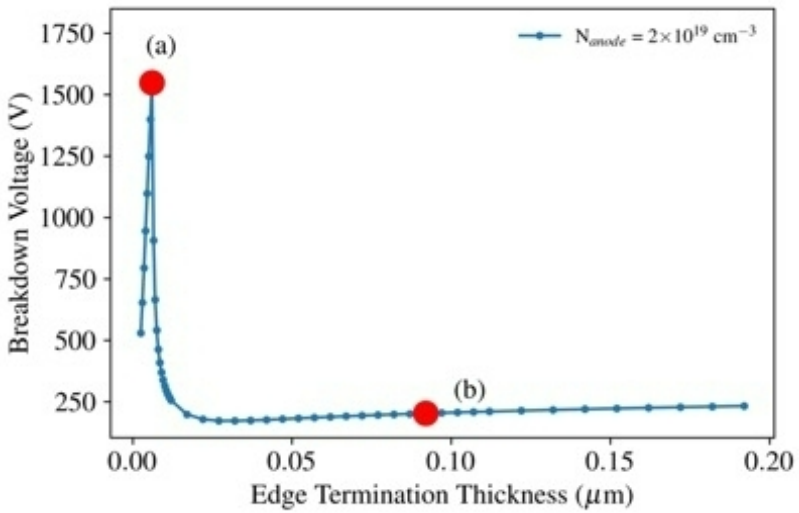
F	1.05	140
Total		1150

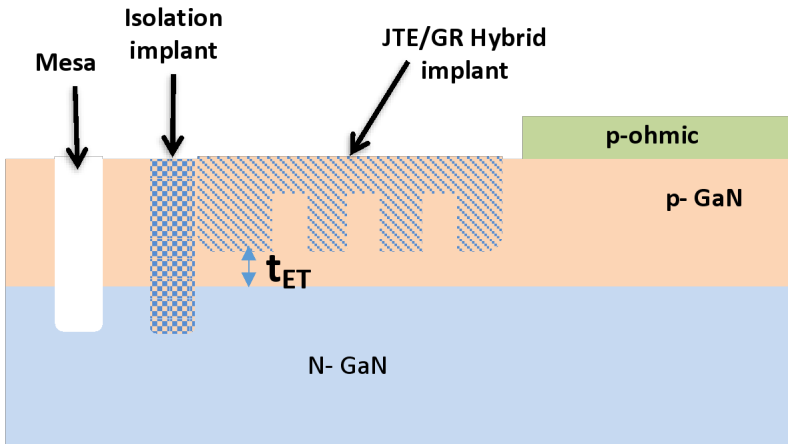
Features:

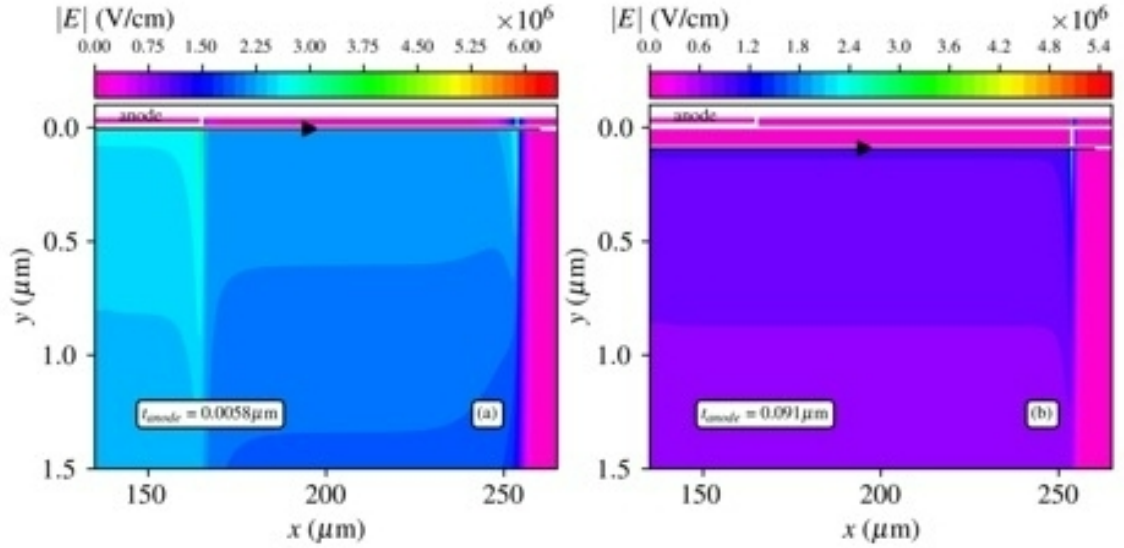
- Global alignment (Type IIa wafers)
- P-GaN ohmic CTLM
- P-GaN Hall
- Isolation test
- Termination test
- Small diameter circular diodes
- JTE and GR termination designs
- Passivation / Overlay for packaging

T. Anderson

Edge Terminations





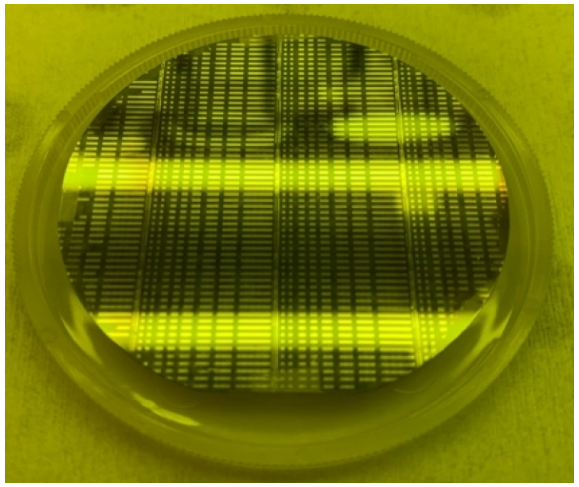


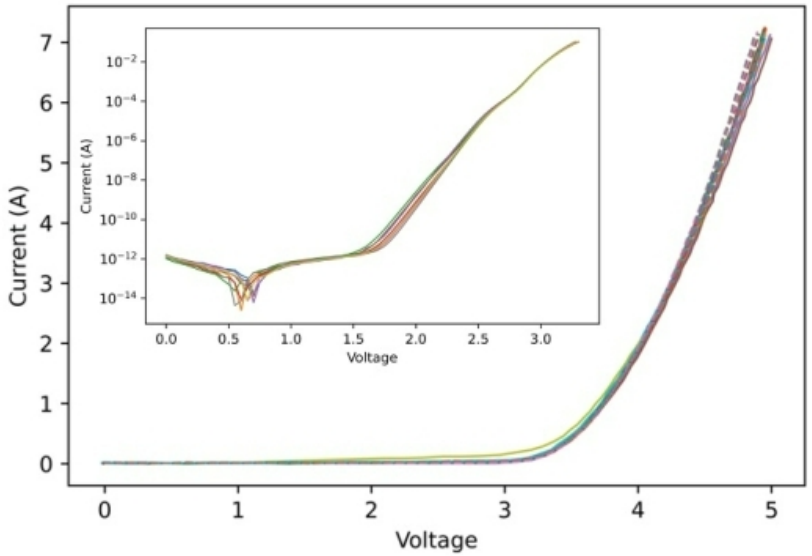
- **Using implanted (planar) structures**
- **Various permutations of isolation, guard rings, and JTEs**
- **Simulations guide epitaxial structures and device processing**

M. Porter

Foundry Electrical Testing and Results

Typical foundry wafer

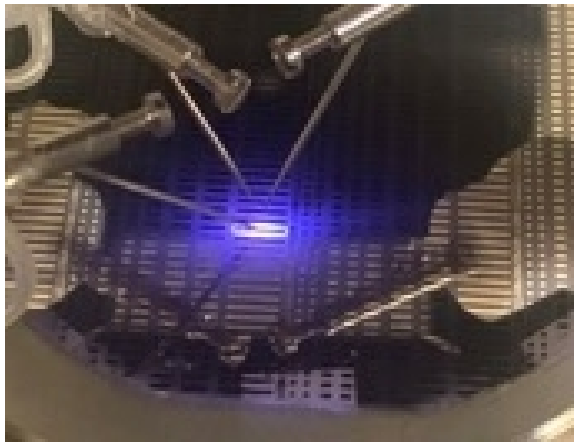


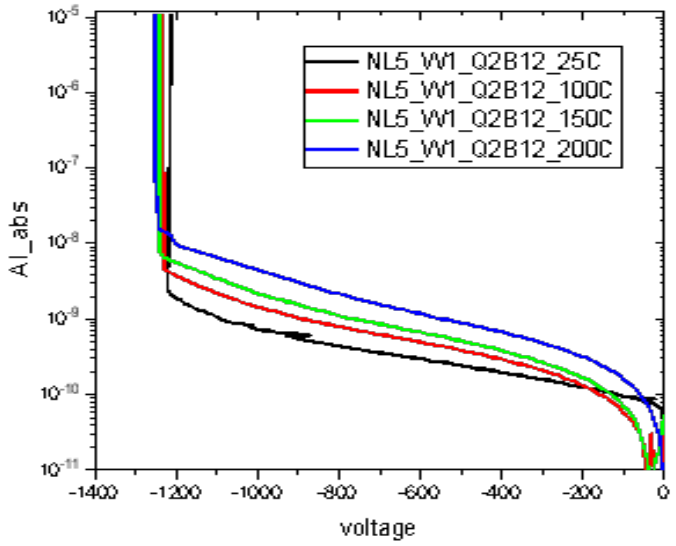


Forward IV:

- **Several amps of current demonstrated for 1 mm² devices**

Wafer under test





Reverse IV:

- **>1.3 kV breakdown demonstrated**
- **Positive temperature coefficient of breakdown consistent with avalanche**

T. Anderson. M. Ebrish

Correlations Between Measured Parameters

Q2

Breakdown (V)	I_c (A/cm^2)	R_{on} (Ω-cm^2)	N_d (cm^{-3})
820	7.10e-05	2.65	1.58e+16
823	7.21e-05	2.76	1.61e+16
822	7.75e-05	2.64	1.47e+16
822	7.67e-05	2.63	1.44e+16
840	2.20e-04	2.66	1.43e+16
	nan		3.06e+16
	nan		3.44e+16
837	7.87e-04	2.75	1.28e+16
830	5.81e-05	2.73	1.33e+16
838	7.37e-05	2.76	1.28e+16
830	9.14e-04	2.73	1.22e+16
610	6.51e-03	2.9	1.16e+16
839	1.08e-03	2.79	1.14e+16
852	7.88e-05	2.74	1.12e+16
863	8.17e-05	2.76	1.10e+16
855	8.39e-05	2.77	1.10e+16
876	4.79e-04	2.79	1.08e+16
867	8.49e-05	3.2	1.07e+16

Breakdown (V)	I_c (A/cm^2)	R_{on} (Ω-cm^2)	N_d (cm^{-3})
187	6.54e-03	2.71	2.60e+16
150	6.00e-03	2.53	2.55e+16
437	6.42e-03	2.43	2.54e+16
744	6.28e-05	2.37	2.54e+16
210	6.41e-03	2.36	2.12e+15
729	4.51e-03	2.31	2.58e+16
703	3.34e-05	2.29	2.56e+16
744	2.31e-03	2.21	2.47e+16
759	6.25e-04	2.13	2.57e+16
640	1.99e-05	2.19	2.56e+16
765	5.51e-05	2.18	2.46e+16
764	5.45e-05	2.2	2.43e+16
760	5.73e-05	2.29	2.51e+16
755	4.32e-05	2.27	2.44e+16
760	5.67e-05	2.41	2.42e+16
759	5.81e-05	2.55	2.34e+16
358	4.11e-03	2.63	2.81e+14
760	4.64e-05	2.99	Fail

Q3

870	3.10e-03	2.69	7.19e+15
814	5.26e-05	2.67	8.30e+15
885	8.61e-05	2.58	8.25e+15
903	9.03e-05	2.52	8.28e+15
895	4.60e-04	2.63	7.42e+15
700	5.77e-03	2.61	8.54e+15
748	1.42e-03	2.55	7.50e+15
697	1.39e-03	2.67	9.47e+15
	nan	2.72	Fail
773	1.89e-03	2.73	8.74e+15
730	2.25e-03	2.88	8.72e+15
669	2.21e-03	2.83	8.36e+15
734	2.24e-03	2.78	7.82e+15
856	3.38e-03	2.81	6.60e+15
	nan	2.73	Fail
760	3.28e-03	2.81	6.63e+15
630	2.43e-03	2.93	1.07e+16
567	1.89e-03	3.05	1.12e+16

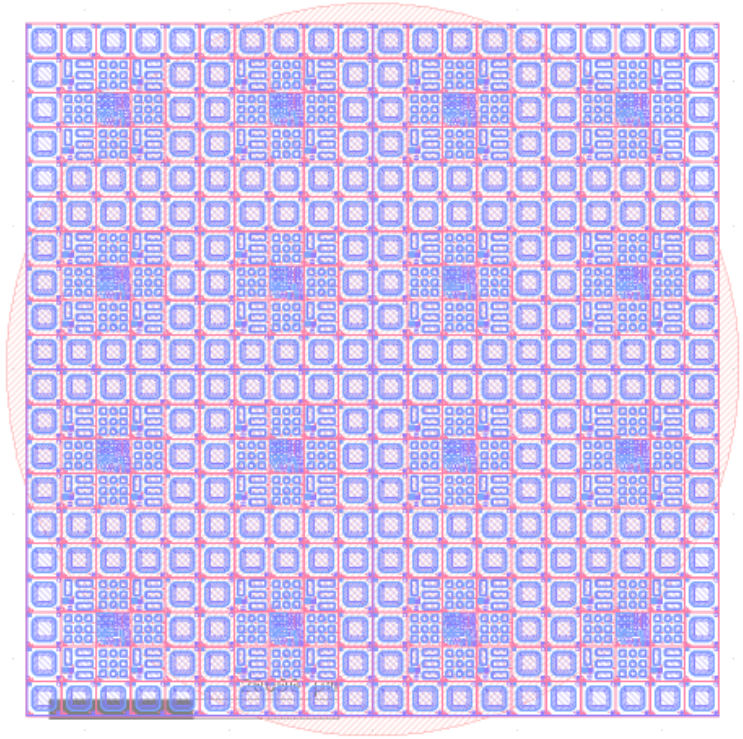
1155	1.75e-03	2.91	1.32e+16
1273	1.64e-03	3.1	1.28e+16
1270	2.16e-03	3.2	1.23e+16
1210	2.54e-03	3.07	1.29e+16
1100	2.04e-03	3.25	1.32e+16
1268	9.91e-04	3.16	1.18e+16
1292	2.30e-03	3.0	1.20e+16
1090	1.89e-03	3.01	1.18e+16
1291	8.12e-04	2.89	1.20e+16
118	1.04e-05	2.97	1.21e+16
1250	3.45e-03	2.96	1.23e+16
1260	1.18e-03	2.99	1.29e+16
1145	3.71e-03	2.95	1.26e+16
1258	3.02e-03	3.01	1.29e+16
960	4.06e-03	3.02	1.32e+16
390	1.23e-03	3.34	Fail
1230	1.10e-03	3.84	1.31e+16
850	4.92e-03	4.73	Fail

- **Data from "F" devices (1 mm^2)**
- **In general, higher N_D (from C-V) results in reduced V_{BR} and low R_{ON}**

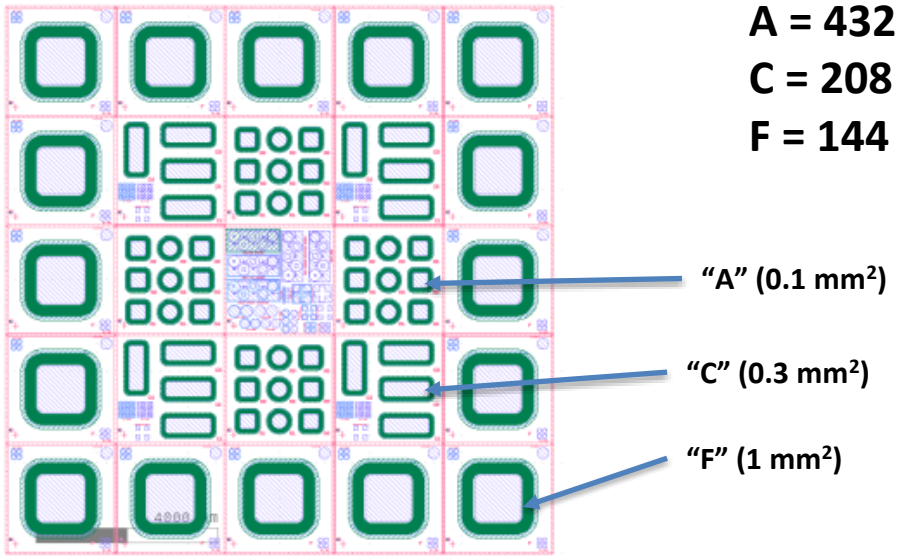
T. Anderson

Updated Foundry Mask Layout

2” Wafer



Unit Cell



Device Count
(per 2” wafer)

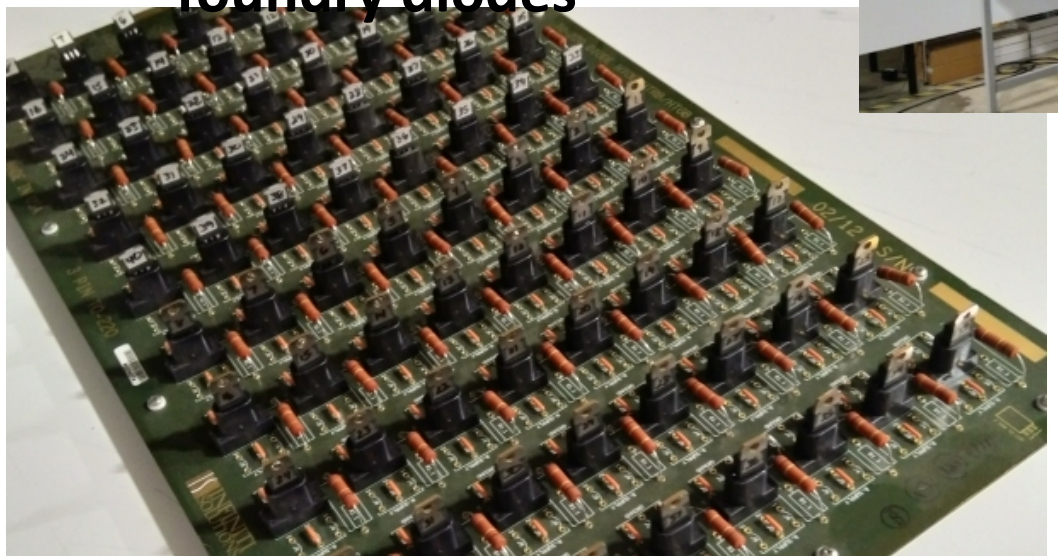
A = 432
C = 208
F = 144

- **Square devices, modular layout, and unique device IDs to facilitate dicing/packaging**
- **Device placement is symmetric across the wafer, which improves yield of “F” devices**

Reliability and Failure Analysis

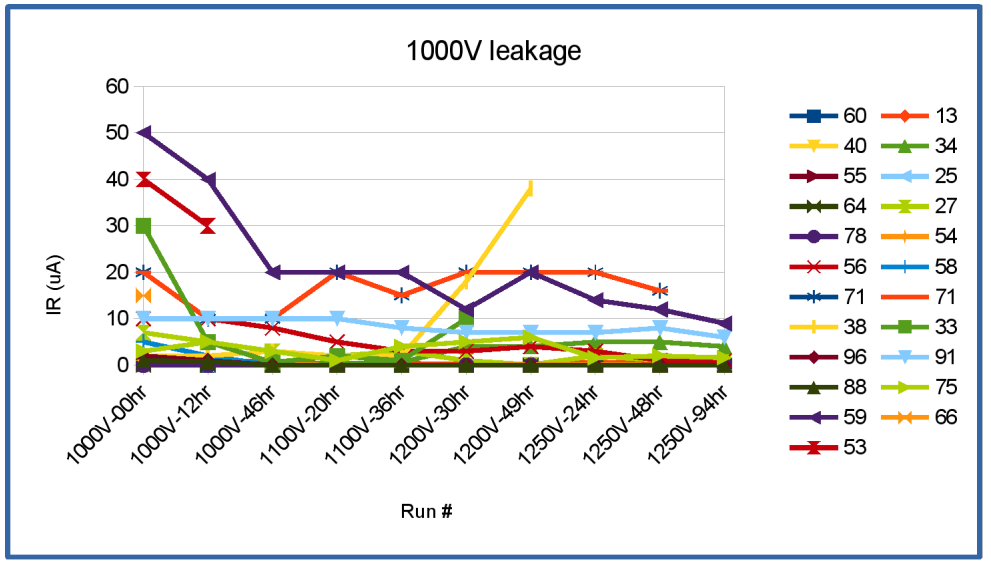
- Extensive reliability and FA effort ongoing
- Evaluating pre-existing diodes and foundry diodes

Reliability test ovens and power supplies



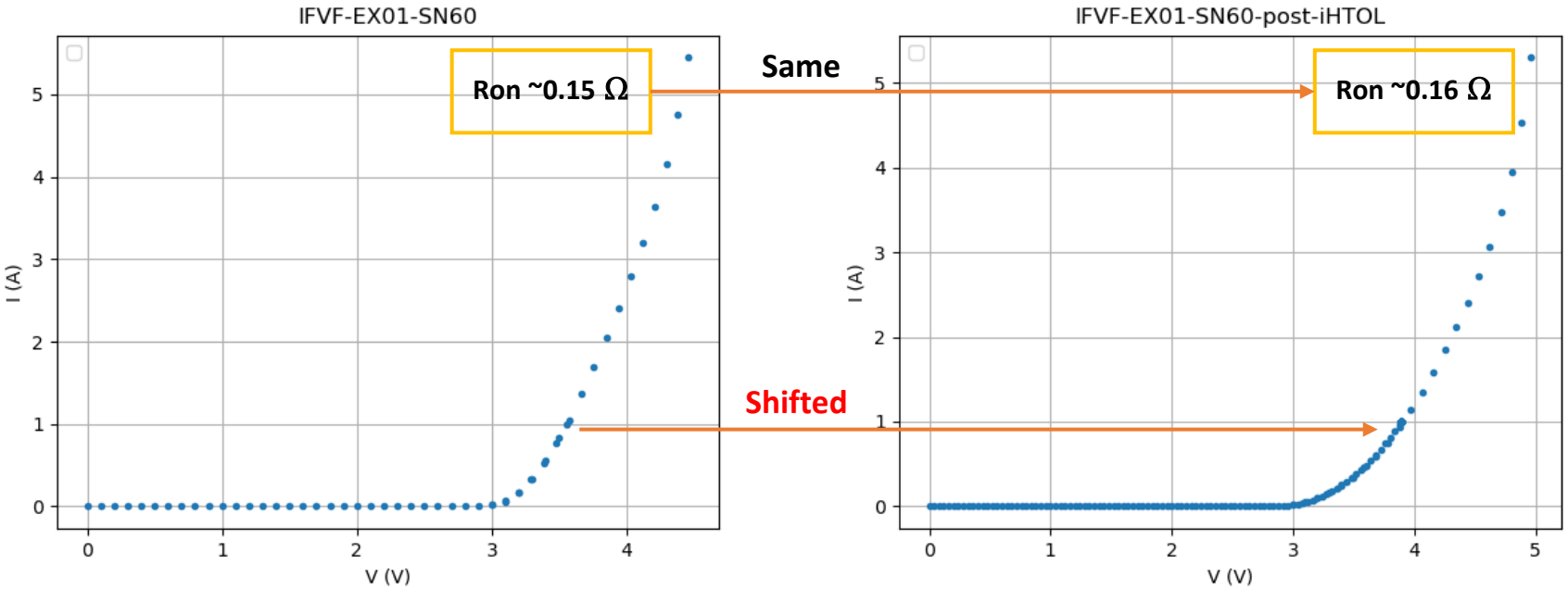
Test board

High Temperature Reverse Bias leakage current data

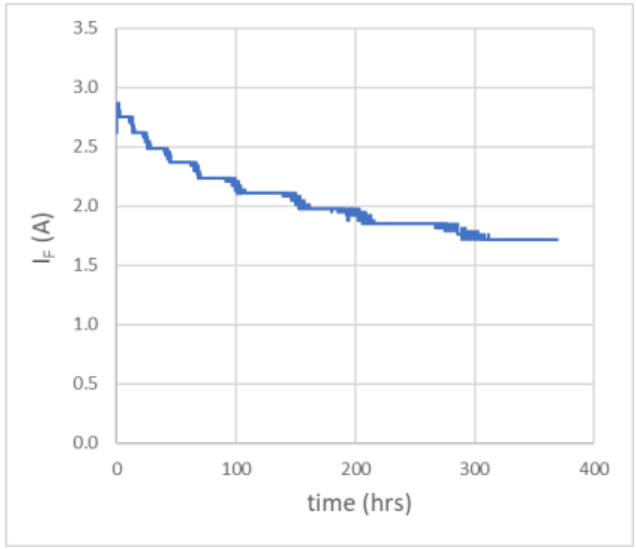


O. Aktas

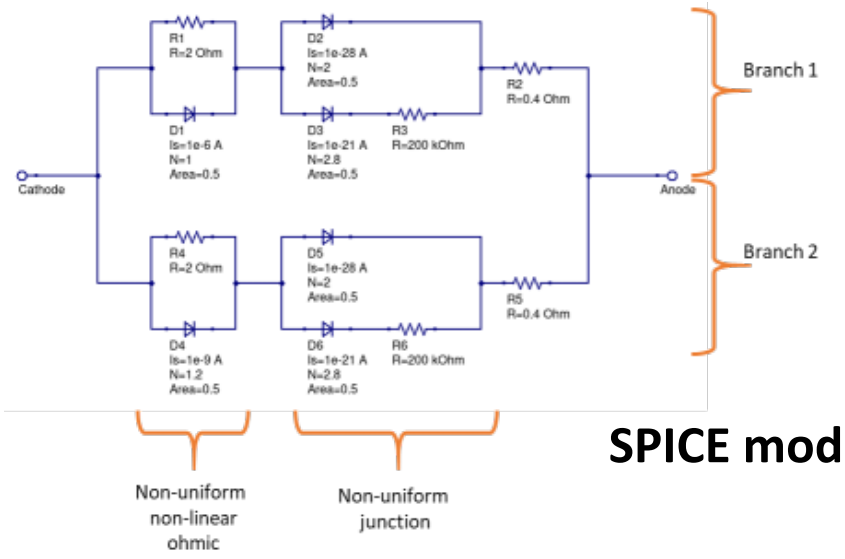
Reliability Testing – GaN Diode HTOL Results



HTOL I_F vs. time at 70˚C and 4 V



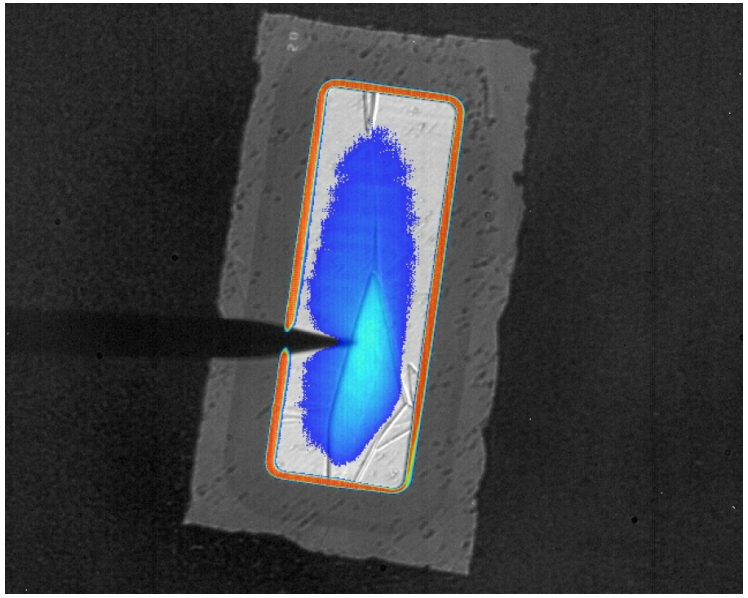
- **I-V curve walks out during HTOL stressing, resulting in decrease in I_F with time**
- **May be due to developing non-linearity of p-contact**



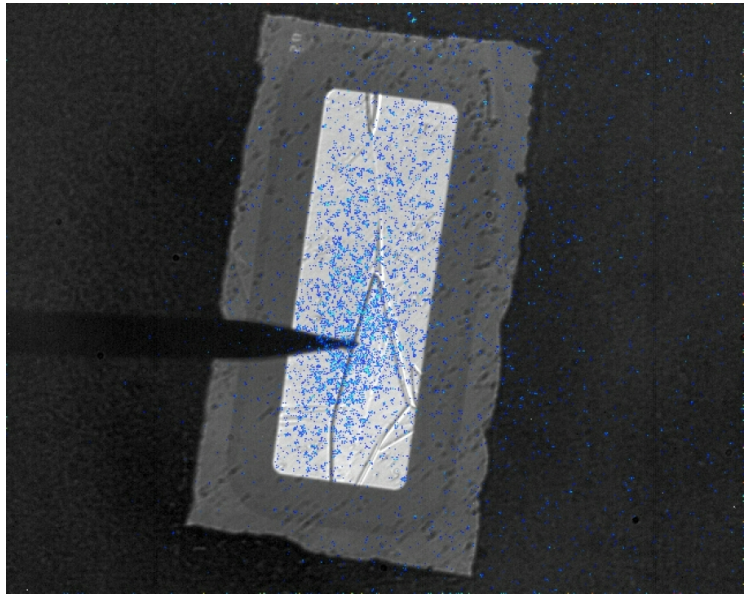
SPICE model

O. Aktas

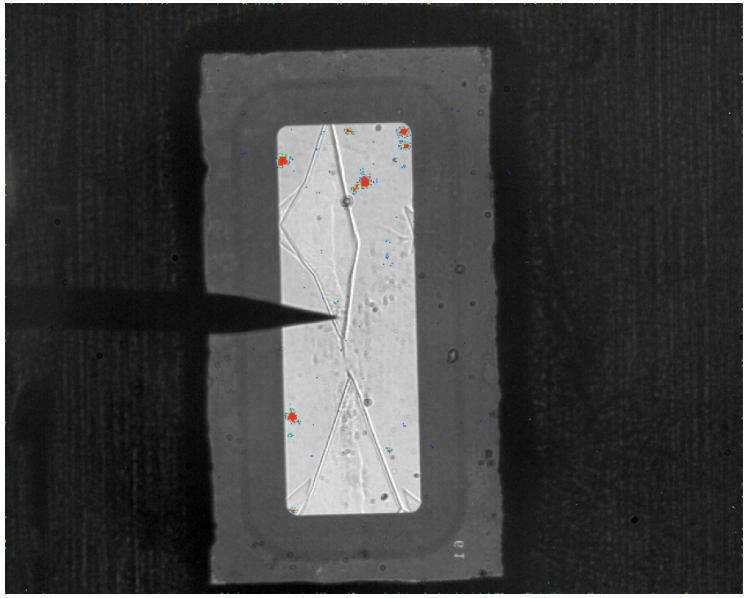
Emission Microscopy of HTOL-Failed Devices



Device 1:
V_F = 3V, I_F = 30 mA
Failed HTOL-I_F
Localized forward current



Device 1:
V_R = 325 V, I_R = 70 uA
Passed HTOL-I_R
Non-localized emission



Device 2:
V_R = 600 V, I_R = 1 uA
Failed HTOL-I_R
Localized emission

Questions?

Bob Kaplar: rjkapla@sandia.gov

arpa·e
CHANGING WHAT'S POSSIBLE

Sandia National Laboratories

U.S. NAVAL RESEARCH LABORATORY