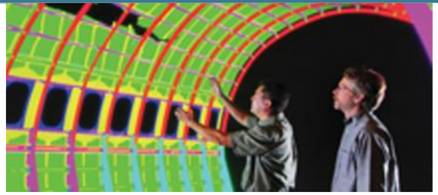
SAND2021-12308PE

GAA IBM Hot Carrier Study



Colin McKay

GAA IBM WLR Update

09/30/2021

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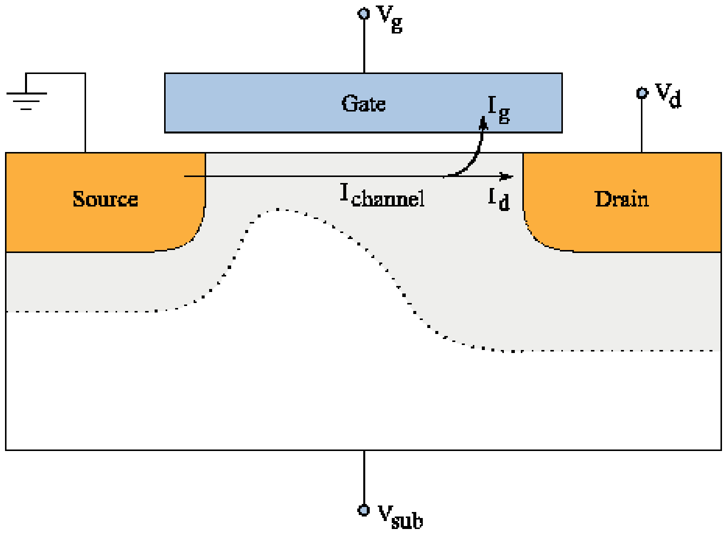
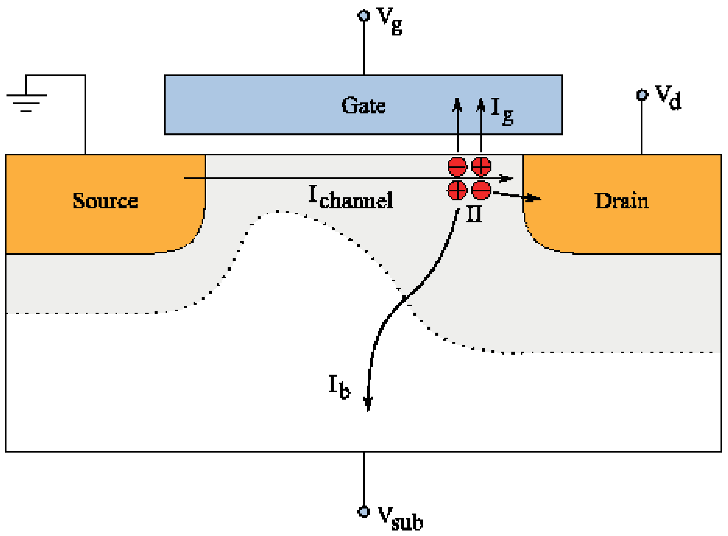
Hot Carrier Damage – Overview

- High energy ("hot") carriers travel across the transistor
- Hot electrons can tunnel into the oxide causing damage and creating performance limiting defects
- "Lucky" (hot enough) electrons can cause impact ionization events, creating electron-hole pairs near the drain causing gate and body current
- Both mechanisms lead to a reduction in drive current during normal operation
- Hot carrier testing stresses the device to age the part faster than normal operation
- Hot carrier degradation typically follows a power law, $y=At^B$

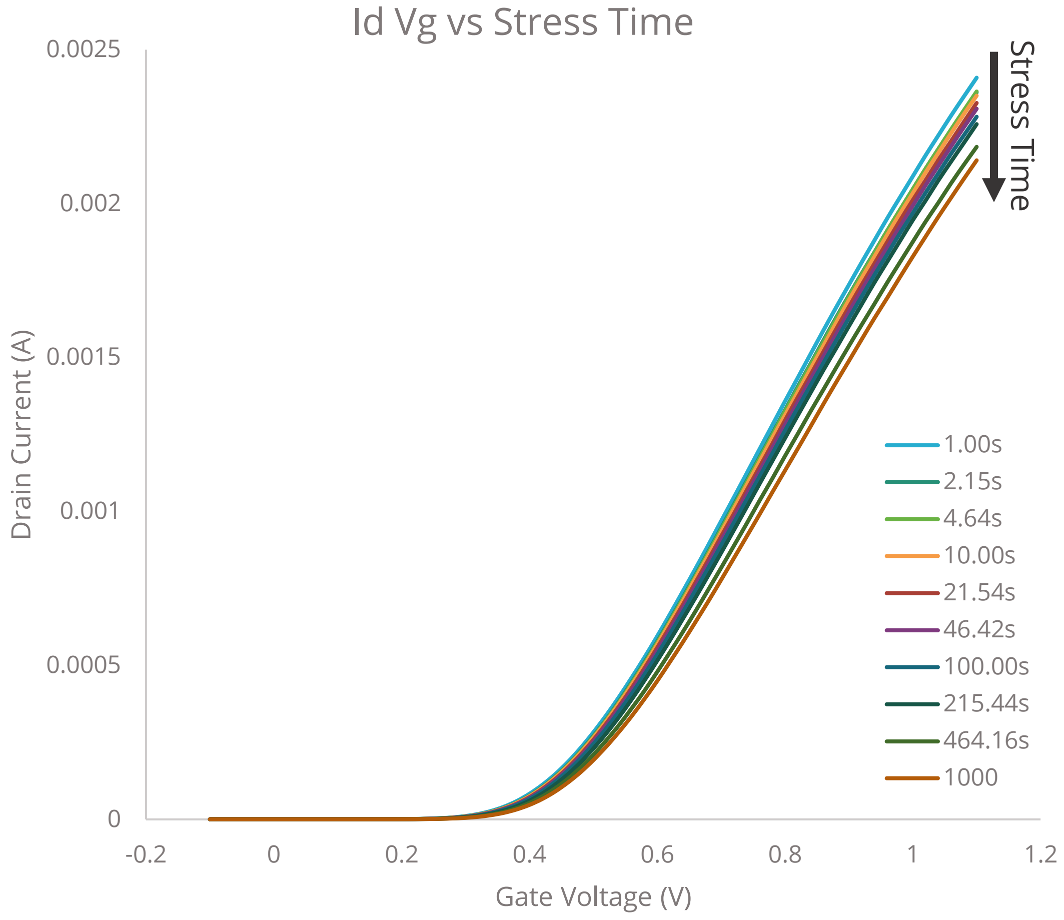


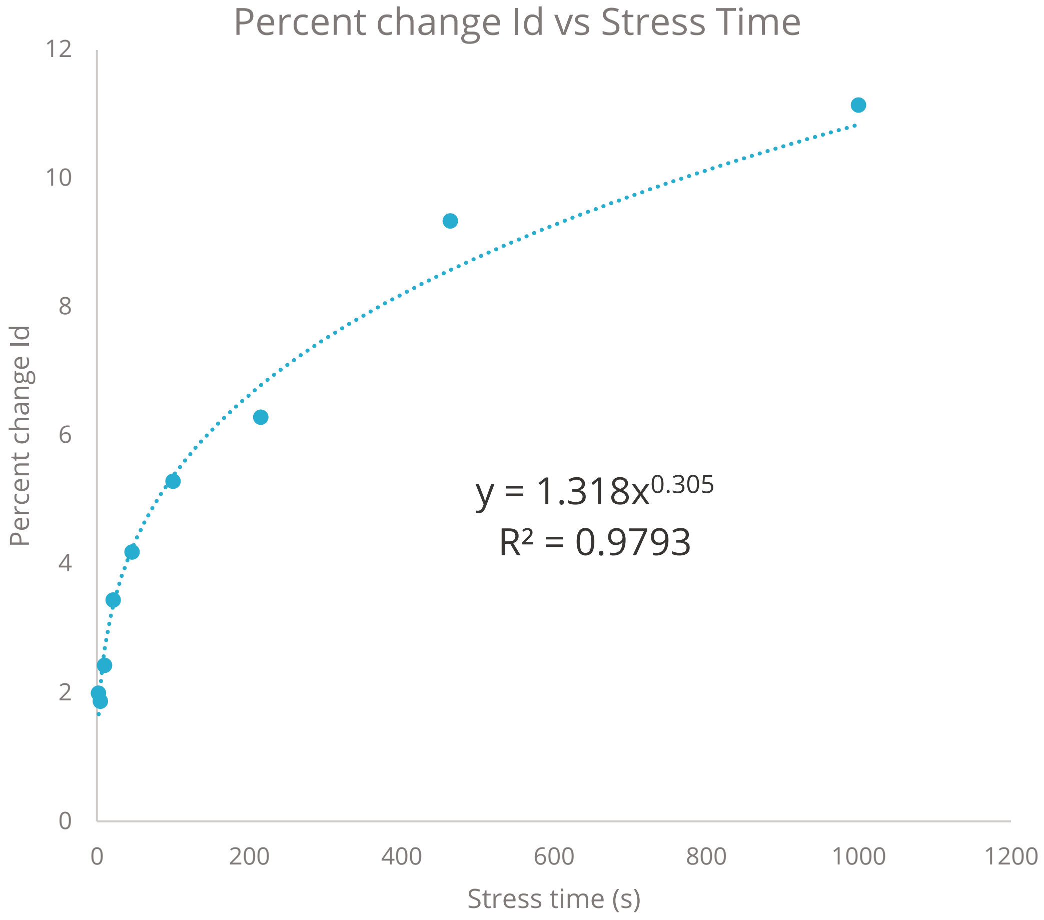


Hot Carrier Stress Test

- Measurements were taken using new software on the Cascade manual prober
  - 4 point prober to make contact with pads (contact was sometimes difficult to make)
  - B1500 SPA provided the necessary voltages and measured the currents
- Cycle between stress and characterization over time
- Stress conditions (picked to prioritize HCD over BTI)
  - Vg = 1.3V
  - Vd= 1.9V
- Characterization sweep
  - Vg swept from -0.1V to 1.1V
  - Vd = 0.7V
  - Tracked I_{Dmax} and V_{th} as a function of stress time
  - ~ 65 mV/decade subthreshold slope (theoretical is 60 mv/decade)
- 36 devices were tested across two sites of quadrant 4 (1,6 and 2,6)

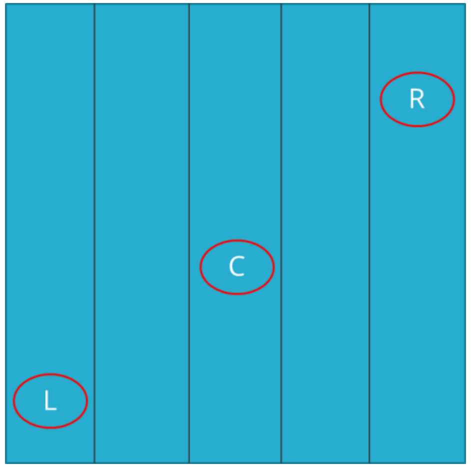
Hot Carrier Measurement Data Examples





Device Locations and Names

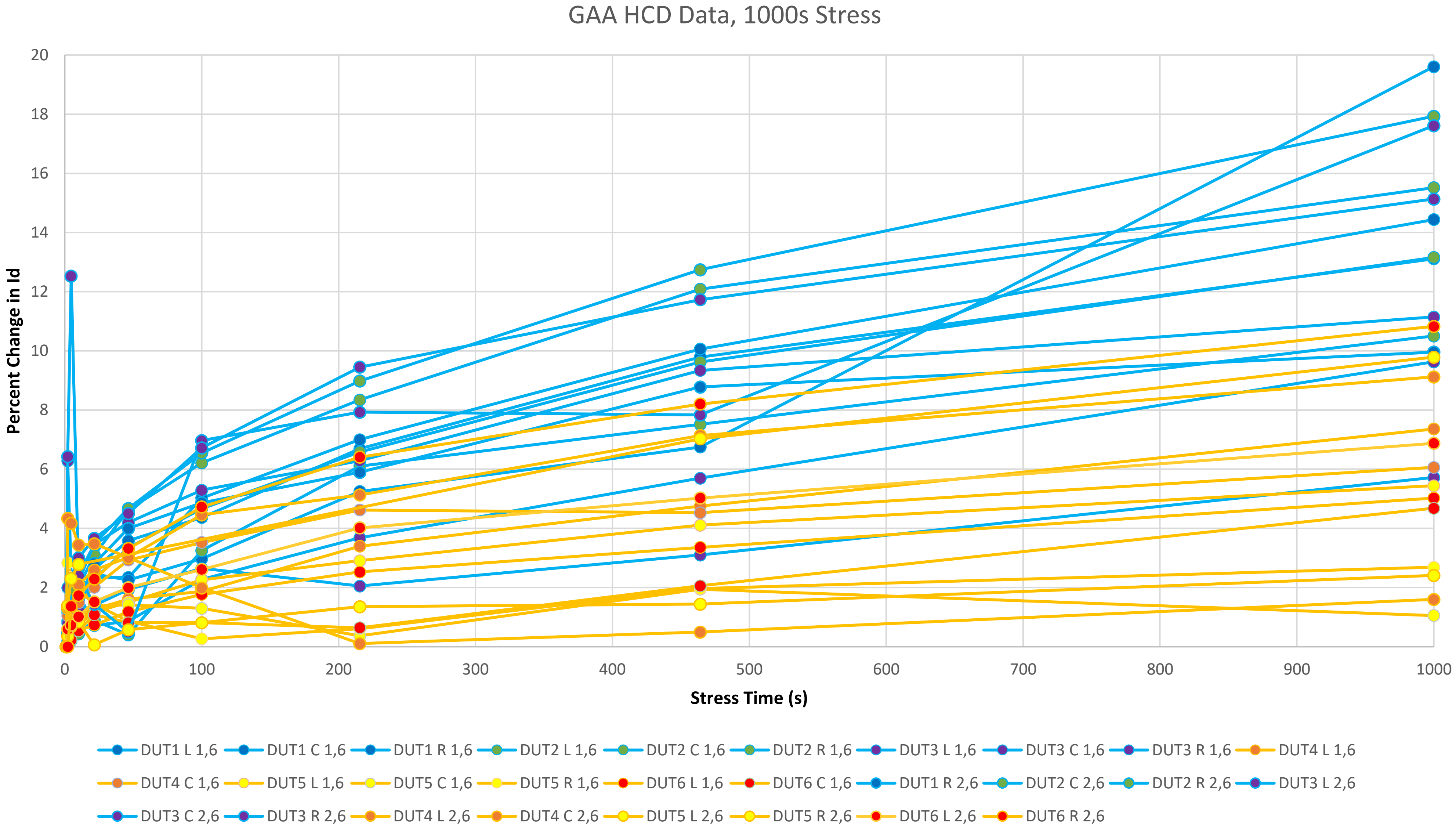
Row Name	Pad 1	Pad 2	Pad 3	Pad 4	Pad 5	Pad 6	Pad 7	<...>	Pad 18	Pad 19	Pad 20	Pad 21	Pad 22	Pad 23	Pad 24		Pad 25
DLWFET2_PS					DUT 3						DUT 6						
Unmarked	Pad 1	Pad 2	Pad 3	Pad 4	Pad 5 L=1x, W=3x	Pad 6	Pad 7	<...>	Pad 18	Pad 19	Pad 20 L=2x, W=3X	Pad 21	Pad 22	Pad 23	Pad 24		Single Test Pad
DLWFET2	Pad 1	Pad 2	Pad 3	Pad 4	Pad 5 L=1x, W=2x	Pad 6	Pad 7	<...>	Pad 18	Pad 19	Pad 20 L=2x, W=32	Pad 21	Pad 22	Pad 23	Pad 24		Single Test Pad
					DUT 2						DUT 5						
DLWFET1	Pad 1	Pad 2	Pad 3	Pad 4	Pad 5 L=1x, W=1x	Pad 6	Pad 7	<...>	Pad 18	Pad 19	Pad 20 L=2x, W=1x	Pad 21	Pad 22	Pad 23	Pad 24		Single Test Pad
					DUT 1						DUT 4						



Location of modules on the die

Quadrant #4, NMOS, IBM Lot # 305JE5						
Partial	Partial	Partial	Partial	Partial	Partial	Partial
1,6	2,6	3,6	4,6	5,6	6,6	Partial
Partial	2,5	3,5	4,5	5,5	6,5	Partial
Partial	2,4	3,4	4,4	5,4	6,4	Partial
Partial	Partial	3,3	4,3	5,3	6,3	Partial
	Partial	Partial	4,2	5,2	6,2	Partial
		Partial	Partial	Partial	6,1	Partial
					Partial	

Hot Carrier Raw Data



Blue line: L=1
Gold line: L=2

Blue spot,
Orange spot: W=1

Green spot,
Yellow spot: W=2

Purple spot,
Red spot: W=3

Results and Trends to note

- As expected, short channel devices suffer more than long channel devices
  - Shorter channel lengths mean less time for the carriers to scatter and lose energy
  - High energy (hot) carriers create defects near the drain of the device
- Width appears to play a role as well in shorter channel devices (not enough data to make a definite case for this)
  - Narrower devices appear to degrade more than the wider devices
  - This effect could be due to plasma damage during processing
  - Wider devices also suffer less from NBTI (*Wang et al., 2019 IEEE IRPS*)
- Only one stress condition was used due to time constraints, as such no field acceleration parameters can be extracted from the measurements
- Some measurements are noisier than others, attributed to unreliable contact to the device and vibrations due to nearby work

Potential Future Work?

- More time/measurements on these devices could lead to more interesting results
  - Multiple stress conditions will allow for voltage/field acceleration parameter extraction
  - Longer tests with lower stress values will provide more accurate data
- Other types of interesting measurements include time dependent dielectric breakdown (TDDB) and bias temperature instability (BTI) studies
- TDDB studies would likely need to include dicing and packaging as time to breakdown can be long and vary widely between devices
- BTI measurements include stress periods (like the HCD measurements) but the characterization measurement must be fast to prevent recovery from BTI damage
- More information about device architecture and band structure will allow for more details to be extracted from reliability measurements
- **Compare WLR measurements to FinFET and pre and post SRH exposure**