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Gallium Nitride Superjunction Transistor: Continued Funding Report

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Disclaimer

This work performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract DE-AC52-07NA27344.

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Abstract

The initial goal of this project is to develop the gallium vacancy assisted diffusion (GAID) method in GaN and apply it to demonstrate 2-terminal, 3-terminal, and large area Superjunction-enhanced modules. These devices will find use in high efficiency power conversion applications with the capability of operating at higher voltages, higher frequency, and less loss than comparable stat-of-the-art devices. The approach of this project has been to utilize simulation tools to drive diffusion experiments and inform semiconductor device fabrication processes. VASP has been relied upon to simulate first principles diffusion mechanisms while SILVACO TCAD has been utilized to understand tradeoffs of the the critical dimensions in GaN devices.

First principles simulations have been used to understand both the dynamics of magnesium diffusion into GaN along with the unintentional impurity incorporation that could be compensating hole formation. Results have shown a complex relationship between Mg_{Ga} and non-ideal impurity formation controlled primarily by the surface fermi-level at the diffusion interface. This work has served as the driving force for bias-assisted diffusion experiments. Recently, simulation of critical diffusion processes within a MgF_2 capping layer have been performed. Here it has been found that fermi-level engineering is required to balance the out diffusion of Mg with the incorporation of gallium from the GaN surface.

Driven by first principles simulations of atomic defect formation in GaN, we have selectively diffused Mg into GaN resulting in the first demonstration of selective area doping by diffusion at low temperatures. Confirmation was provided with the analysis of atomic composition measurements along with laterally mapped electrical characterization of prepared layers. Although magnesium has been observed in quantities consistent with highly doped GaN layers, hole concentrations necessary for demonstration of a high voltage PN diode have not been realized. Experiments designed to ‘trick’ the GaN lattice into Mg_{Ga} formation by varying the in-situ bias showed successful control of Mg incorporation, but PN diode formation was not realized.

In preparation for controllable diffusion of Mg in GaN, TCAD simulations have been performed to understand how an error function p-type profile in a Superjunction device affects the overall performance. Results show that tight control of the diffusion profile is necessary to achieve a device with both high breakdown voltage and low on-resistance capabilities but can ultimately lead to higher Baliga-Figure-of-Merit (BFOM) than an abrupt Superjunction device. Work has begun applying these results to the 3-terminal GaN SJ FinFET.

To achieve the breakdown and on-resistance enhancement predicted by the TCAD device modeling, microfabrication processes were designed to take advantage of the newly installed EBPG5200 e-beam direct write system. However, tool uptime has affected the consistent progress of process development needed to realize devices with sub-micron feature sizes. Recent service visits to the tool have alleviated these problems and it is expected that devices with sub-micron features will be realized by the end of FY2022.

To mitigate the risk of low hole concentration realized by the GAID process, external collaborators have agreed to grow GaN structures for lateral Superjunction formation. In this way we can decouple the LLNL-developed diffusion process and more rapidly develop the proposed devices. Here we plan to utilize TCAD and microfabrication capabilities established on this project to form

2- and 3-terminal lateral devices enhanced with changed balanced layers by MBE growth. Currently, TCAD simulations have focused on charge balanced layer formation and diode characteristics while MBE growth has focused on Fe-doping for electrical substrate isolation.

Background and Research Objectives

The power MOSFET switch is a necessary device in power conversion circuitry used to gate incoming electrical energy into passive elements (inductors and capacitors) such that the output voltage can be increased (boost converter) or decreased (buck converter) without power loss. For applications that require higher power conversion and lower loss, the fundamental material from which the switch is fabricated must be considered. Silicon as a power semiconductor has stayed relevant due to the ability to form a Superjunction structure, beating the breakdown vs. specific on-resistance 1-D unipolar material limit. This is accomplished by cleverly designing a charged balanced layer (CBL) into the voltage sustaining region so that the electric field is distributed throughout the volume and not concentrated at an interface. Power devices fabricated from so-called wide-bandgap semiconductors such as gallium nitride (GaN) have been shown to outperform state-of-the-art silicon-based power devices but because of the limited processing knowledge a GaN-based Superjunction has yet to be demonstrated. This project aims to develop the first GaN Superjunction transistor by harnessing technology developed at Lawrence Livermore National Laboratory.

Currently, GaN lacks a method to selectively dope regions of the material without introducing significant damage into the bulk of the semiconductor. Without this capability, a Superjunction structure cannot be realized. Previous work performed at LLNL has revealed a mechanism to enhance solid-state diffusion of magnesium in GaN at low temperatures. By patterning a thin layer of a Mg-containing film (MgF_2, MgO, Mg_3N_2 etc.) on the surface of the GaN followed by a gallide forming metal, we have shown that Mg can be incorporated into the bulk with temperatures as low as 700°C. Though Mg-incorporation has been successful, progress toward p-type GaN has been slow. To mitigate the risk of GaN SJ device realization, a lateral device architecture has been adopted to permit epitaxial growth of the charge balanced layers instead of selective area doping.

With this change, the goal of this project is to harness TCAD simulation tools to inform MBE growth along with continued development of microfabrication techniques to demonstrate progressively more complicated CBL-enhanced device structures. Initially, the stair step Superjunction and Schottky Superjunction devices will be fabricated to show the capability of these grown layers. Next, sidewall regrowth of cathode and anode contacts will be developed to allow for a true lateral SJ diode to be created. Finally, a gating mechanism will be established to demonstrate the first GaN SJ transistor. Once created the goal is to work with industrial/research partners to transfer into the market resulting in high efficiency power conversion modules for previously unreachable applications.

Scientific Approach and Accomplishments

Project main thrusts:

1. Charge Balancing by GAID Process
2. Charge Balancing by Epitaxial Growth

Charge Balancing by GAID Process

Summary of First Principles Simulation Work

With first principles simulations (VASP), models of atomic diffusivities, charge states, and activation energies can be used to understand the parameter-space of gallium vacancy enhanced diffusion experiments. Capitalizing on the success of previous work, simulations focused primarily on understanding MgF_2 as a diffusion source and possible compensation defects that may arise. Summary of findings are detailed below:

Fluorine interstitial diffusion and complexes in GaN

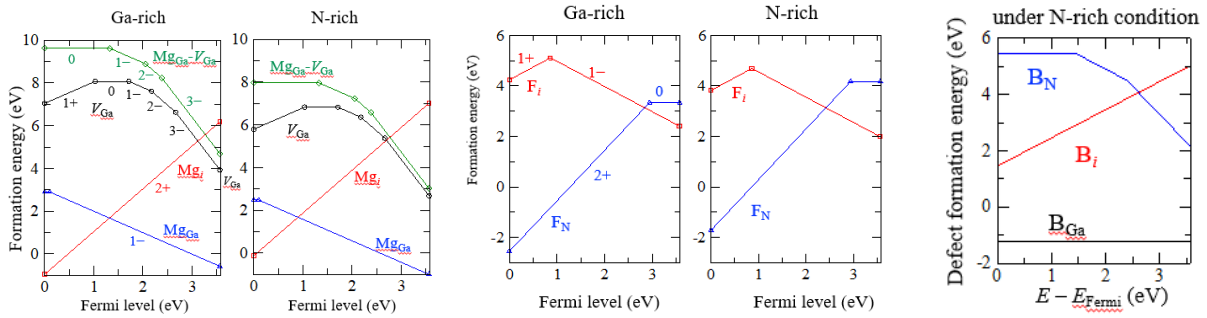
- Under both Ga- and N-rich conditions fluorine appears as an interstitial donor (F_i) when the fermi level is near the valence band and in the neutral nitrogen substitutional (F_N) when the fermi level is near the conduction band
- Fluorine interstitial diffusion is enhanced with presence of gallium vacancies

Formation and diffusion of H_i in GaN

- Hydrogen interstitials largely slowed down under n-type conditions (fermi level closer to conduction band)

Boron versus Mg Diffusion in GaN

- Boron diffuses more readily in the presence of gallium vacancies but with a higher activation energy than Mg
- Boron on gallium sites energetically favor a neutral configuration (no electrical compensation)



(A) (B) (C)

Figure 1. First principles simulations of the formation energy vs. fermi level position in GaN for (A) Mg/V_{Ga} (B) fluorine (C) and boron along with relevant complexes in GaN.

Carbon Complexes with Mg_{Ga}

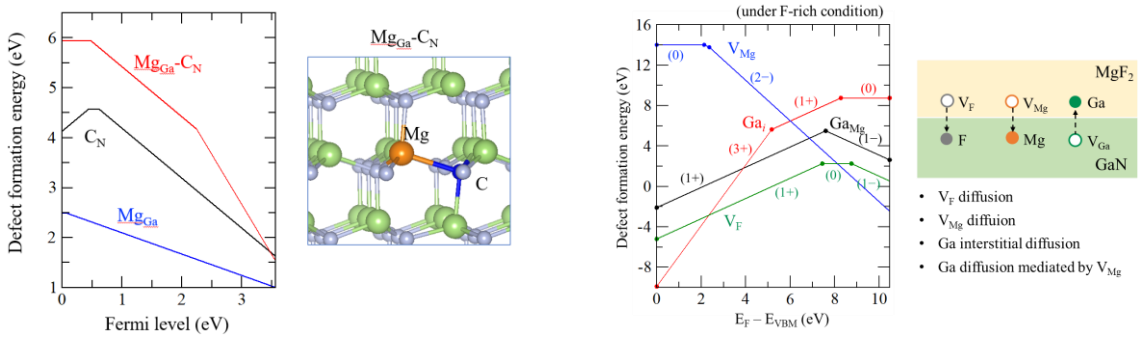
- Carbon on nitrogen and its complex with Mg_{Ga} are favorable under n-type conditions just as Mg_{Ga}
- Mg_{Ga} has a lower defect formation energy than CN or its complex and thus thought to be energetically favorable

Mg and F diffusion into GaN Sidewall

- Magnesium and fluorine diffusion into the m and a planes of GaN occurs largely within the basal plane
- The activation energy of magnesium along the basal plane (into sidewall) should be lower than the c-direction thus GaN:Mg sidewall diffusion should happen more readily than from the top surface
- The effect on fluorine is reversed, thus fluorine should diffuse more readily from the top surface of a GaN film

Critical Diffusion Processes within MgF_2

- Magnesium vacancy formation and Ga_i/Ga_{Mg} preferentially form under opposite fermi-level conditions
- Maintaining near midgap fermi level positioning is critical to GAID process



(A) (B)

Figure 2. First principles simulations of the formation energy vs. fermi level position in GaN for (A) carbon and carbon complexes in GaN vs Mg_{Ga} along with (B) formation energies for magnesium, gallium, and fluorine defects in MgF_2

Summary of Sample Fabrication and Diffusion

Due to the limited supply of available GaN to this project, three 4" wafers were purchased from IQE, each with a 3um thick active layer grown on a bulk GaN substrate. Specific free carrier concentrations were defined for each wafer and grown with special consideration given to lowering the background carbon concentration. This was done to ensure carrier compensation was minimized due to the introduction of impurities during the MOCVD growth process.

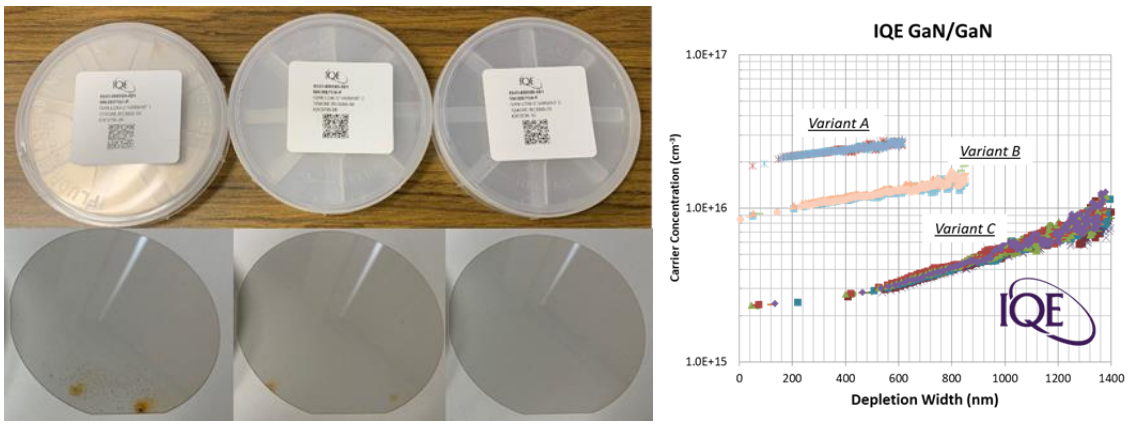


Figure 3. (Left) Image of three 4" MOCVD-grown GaN-on-GaN wafers purchased from IQE. Each wafer consists of a 3um thick low-doped layer targeted to have differing electron concentrations. (Right) Carrier concentrations extracted from C-V measurements on each

Test samples were fabricated by first dicing 5x5mm^2 coupons from the full wafers. Next, a Ti/Al/Ni/Au stack is evaporated on the backside of each sample as the ohmic contact followed by e-beam deposition of the test bilayer through a 2mm circular metal mask. Once completed, samples were annealed at temperatures between 600 and 1000 °C from 5 to 100 minutes in a controlled environment to understand the effect that temperature and time have on the diffusion of Mg into the GaN. Additionally, a two-probe vacuum feedthrough was developed to test the effect of in-situ bias. Here two stainless steel wires are fed through a two-hole ceramic isolator encased in a stainless-steel tube. Torr-seal was used to epoxy the atmosphere end of the assembly and the vacuum seal was made with an o-ring, like a quick connect coupling, between the tubing and the annealing chamber. Inside the chamber, the stainless-steel wires are cantilevered onto the sample and the conductive sample holder used to make backside contact. Sample fabrication and the bias-assisted probe setup are shown below in Figure 4. Once the diffusion process was complete, the bilayer and back ohmic contacts are removed in subsequent soaks of aquaregia, 44% KOH, and 49% HF revealing a clean GaN surface ready for SIMS or electrical measurements.

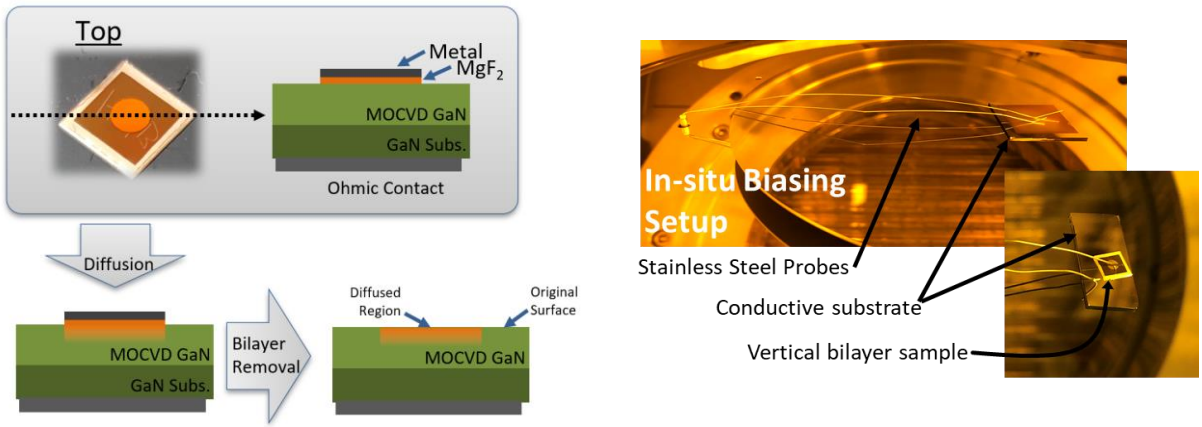


Figure 4. (A) Summary of basic fabrication process to test diffusion parameters and (B) two probe in-situ biasing setup created for this project.

Summary of SIMS Analysis

SIMS was performed on selected samples to investigate the diffusion of Mg in GaN under varying bilayer configuration, temperatures, times, and biasing conditions. Samples were sent to EAG Laboratories for tests. Each sample was scribed prior to bilayer removal to indicate the location of diffusion. A summary of SIMS data is below:

Yale GaN-on-GaN Bias Assisted Comparison

Two samples processed according to the images below on samples grown in collaboration with Yale University were sent to EAG Laboratories for magnesium and fluorine concentration profiling by SIMS. The results are shown below in Figure 5 reveal two distinct profiles. The magnesium concentration in the sample measured with no in-situ bias has a profile very similar to results from previous experiments (not shown) where the GaN layer was grown on sapphire. Applying a +4 V in-situ bias during the annealing process appears to increase the surface concentration while also extending the >1e18cm^{-3} crossing point from 10 to 35nm. Additionally, the +4 V in-situ bias suppresses the fluorine concentration when compared to the sample processed with no in-situ bias. These results are exciting and indicate that the core premise of surface fermi-level tailoring predicted by first principles simulations are correct.

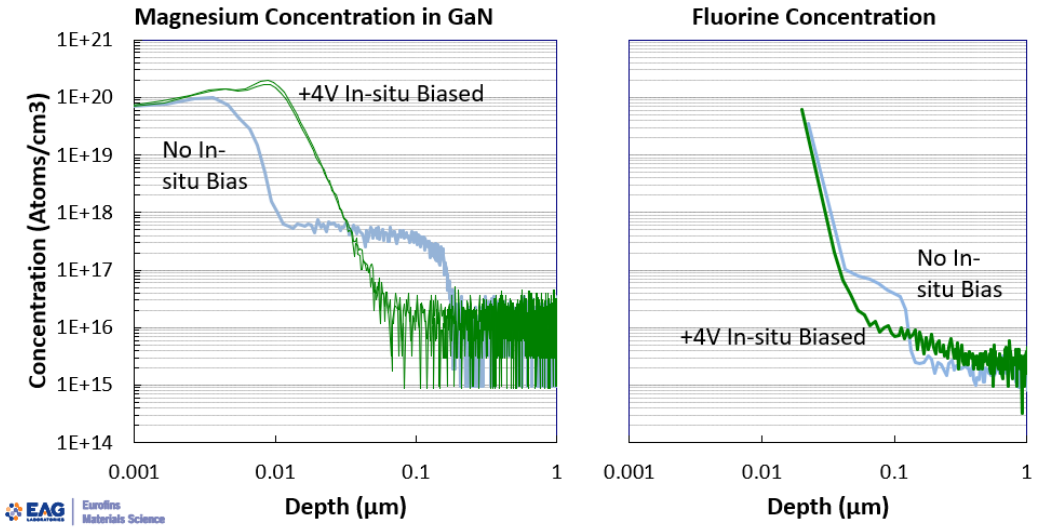


Figure 5. SIMS measurement results for the depth dependent (Left) Mg and (Right) F concentrations in

IQE GaN-on-GaN Diffusion Parameter Comparison

Recently, seven samples were prepared from the IQE wafers according to the legend below in Figure 6(A) where temperature, bulk concentration, and in-situ biasing conditions were compared. Here it can be observed that for most samples a high concentration of Mg is present at up to 10nm into the GaN surface, but samples annealed with a +4V in-situ bias show a larger tail down to 100nm. Interestingly, samples annealed either without or at negative bias reveal a shallower profile than those annealed under similar conditions but on material grown elsewhere. This implies that the MOCVD growth conditions play a large role in Mg diffusivity but can be mitigated by applying a bias while at temperature.

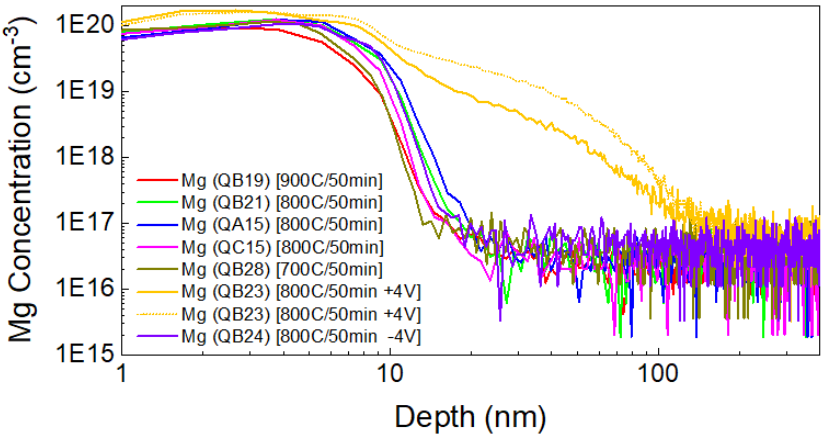
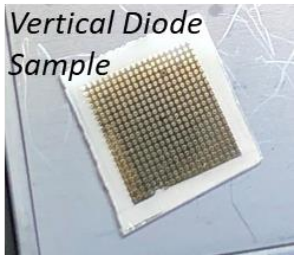


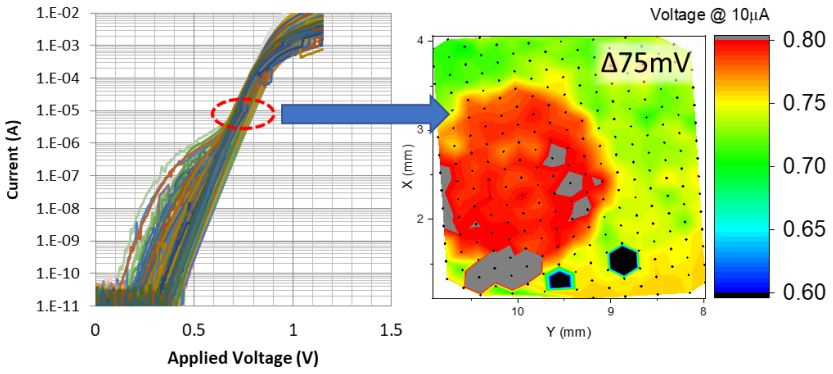
Figure 6. SIMS measurement results from IQE

Summary of Variable Diffusion Parameter Processing

Sample Fabrication and Testing

To ensure that electrical results were indicative of the bilayers role during diffusion, 5x5mm^2 samples were patterned with 100µm circular contacts composed of a Pd/Ni/Au stack. Assuming the diffusion resulted in a high concentration of acceptors at the surface, a PN diode could be formed under the 2mm circular bilayer region, otherwise a Schottky diode would be formed. Samples were then electrically measured and mapped with an automated probing setup. An example of a processed sample and generated data is shown below in Figure 7(A) and (B), respectively.





(A) (B)

Figure 7. (A) Patterned sample ready for measurement and (B) a sample of electrical results generated from 2D mapping

By extracting the voltage at which the diode reaches 10 uA for each contact, contour maps were created making it clear that the patterned bilayer does indeed alter the surface of the semiconductor such that the I-V characteristics are shifted on the voltage-axis. Additionally, a shift in the voltage required to reach 10uA while still maintaining the thermionic emission limited region (linear region on semi-log plot) suggest that the energy barrier at the M-S interface is varying. As discussed previously, TCAD simulations indicate that an increasing barrier can be described by varying the carrier concentration at this interface while still maintaining a Schottky contact.

Variable Diffusion Processing Condition Experiment

From this analysis, the voltage shift change, extracted from forward I-V measurements both within and outside of the bilayer region, were used as a method for comparing the effects of bilayer structure and diffusion conditions. Additionally, a similar process was followed to compare the effects on reverse leakage current. Below is a summary of the data extracted from fabricated devices. Thus far, results show that under certain conditions the forward IV curves can be shifted to higher voltages while lowering the reverse leakage current, implying near surface acceptor doping. Additionally, an in-situ bias has shown to improve these results further however, the results are inconsistent. This could be due to the incorporation of additional defects during the diffusion process that prevent incorporated Mg from presenting as a shallow acceptor at room temperature. Although PN diode behavior has not been observed under the tested conditions, these results indicate that progress is being made.

Table 1. Results from IV testing on Yale3 material

Material	Sample Name	Bilayer	Annealing Conditions			FWD IV ΔV @10uA	REV IV $\Delta log(I)$ @-50V
			Temp. (°C)	Time (min)	In-situ Bias		
Yale3 ($n \approx 5e16cm^{-3}$)	T19B	Au/MgF_2 100/100nm	700	5	No Bias	-	-
	T20B				+4V	-	-
	T21B			50	No Bias	*+75mV*	-
	T22B	Y/MgF_2 100/100nm			No Bias	*-30mV*	*1.58*
	T23B				+4V	*+20mV*	-
	T24B	Au/MgF_2 100/100nm	800	50	No Bias	*+150mV*	*-1.03*
	T25B		900	50	No Bias	*+60mV*	*1.38*

Table 2. Results from IV testing on first round of IQE material

Material	Sample Name	Bilayer	Annealing Conditions			FWD IV ΔV @10uA	REV IV $\Delta log(I)$ @-50V
			Temp. (°C)	Time (min)	In-situ Bias		
IQE - Variant 1 $N_{Si} \approx 5e16cm^{-3}$	QA2	Au/MgF_2 100/100nm	700	50	*No Bias*	*+60mV*	-
	QA3		800			*+150mV*	*-1.55*
	QA4		900			*-60mV*	*3.05*
	QA5		800		+4V	*+70mV*	*-2.12*
IQE - Variant 2 $N_{Si} \approx 2e16cm^{-3}$	QB2		700	50	*No Bias*	*+90mV*	*3.13*
	QB3		800			*+100mV*	-
	QB4		900			*-50mV*	*4.29*
	QB5		800		+4V	*+80mV*	-
IQE - Variant 3 $N_{Si} \approx 1e16cm^{-3}$	QC2		700	50	*No Bias*	*+80mV*	-
	QC3		800			*+120mV*	*2.84*
	QC4		900			-	-
	QC5		800		+4V	*+40mV*	-

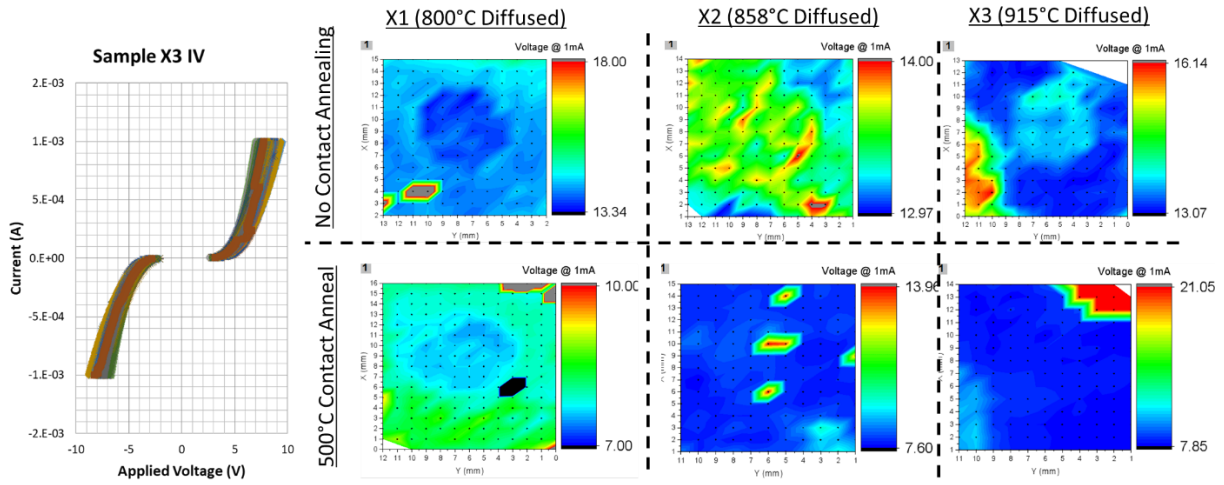
Table 3. Results from IV testing on second round IQE material

Material	Sample Name	Bilayer	Annealing Conditions			FWD IV ΔV @10uA	REV IV $\Delta log(I)$ @-50V
			Temp. (°C)	Time (min)	In-situ Bias		
IQE - Variant 1 $N_{Si} \approx 5e16cm^{-3}$	QA7	Au/MgF2 100/100 Full MgF2 Cover	900	50	No Bias	+100mV	-
	QA8		800		+4	-100mV	+3
	QA9		800	100	No Bias	**Fabricating**	
IQE - Variant 2 $N_{Si} \approx 2e16cm^{-3}$	QB7		900	50	No Bias		
	QB8		800		+4	-	-
	QB9		800	100	No Bias	-	-
IQE - Variant 3 $N_{Si} \approx 1e16cm^{-3}$	QC7		900	50	No Bias	-	-
	QC8		800		+4	+150mV	+3
	QC9		800	100	No Bias	-	-

Pattern Doped P-Type Ohmic Contact Experiment

Traditional means of lowering p-type contact resistance in GaN films is to slow the MOCVD growth rate such that more magnesium is incorporated from the gaseous dopant. Because this is accomplished with growth, it cannot easily be patterned across a sample. An experiment was performed whereby the GAID process was used as an alternative means for patterning these high magnesium concertation regions to lower p-type contact resistances. Here three samples were fabricated and diffused according to the table below. Once the reacted bilayer was removed, circular TLM patterns of varying separation were patterned in a grid. IV results indicated non-ohmic contact with the p-type surface however, extracting the voltage at which the curve reaches 1 mA the curves can be compared. Below in Figure 8 the annealed and unannealed voltage variation at 1 mA is compared for variably diffused samples. In the 800 °C diffused sample there is a clear enhancement of the IV curves extracted within the diffused region while the 858 and 915 °C show no change and degradation of conductivity, respectively.

Material	Sample Name	Bilayer	Annealing Conditions	
			Temp. (°C)	Time (min)
QROMIS (TO 5G2) 6x6mm^2	QT1	Au/MgF_2 100/100nm	800	5
	QT2		858	
	QT3		915	



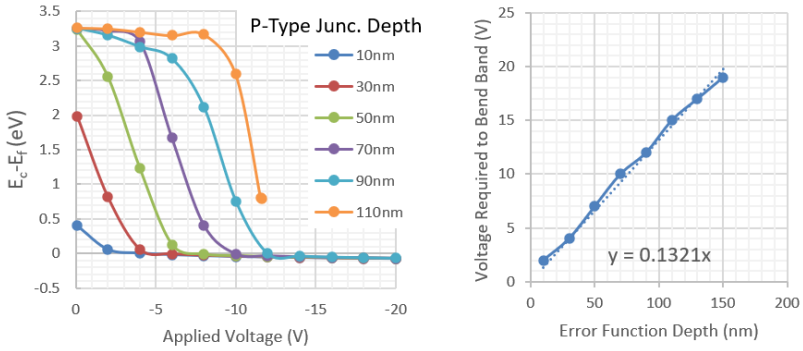
(A) (B)

Figure 8. (A) IV measurements of the 25µm TLM pattern on an 800°C diffused sample. (B) Mapped comparison of the voltage required to reach 1mA

Variable In-Situ Bias Experiment

Considering the first principles simulations of defect formation, the fermi-level at the surface of the GaN film is critical in the determination of incorporated impurities. TCAD simulations show that for an increasingly doped GaN film, voltage required to bend the conduction band to surface fermi-level will increase proportionally. Mg_{Ga} formation is preferential when the conduction band is closer to the valence band (E_C-E_F = *0*). TCAD simulations, shown below in Figure 9, reveal the

voltage vs. E_c-E_F dependence for increasingly deeper hole profiles. From these results samples were prepared whereby the in-situ diffusion bias was varied.

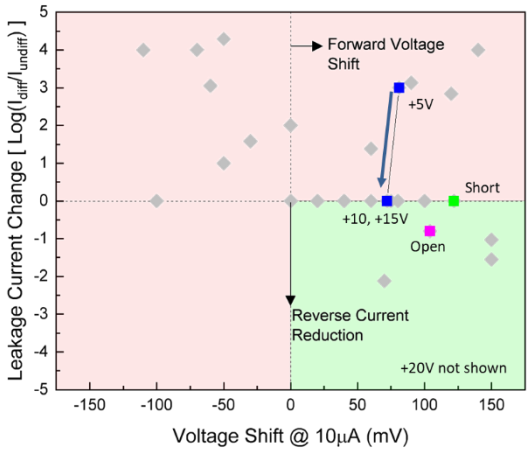


(A) (B)

Figure 9. Band lineup simulation for a metal-insulator-GaN interface. (A) Results show the surface fermi level offset for given applied voltages after p-type doping to variable depths. (B) The voltage required to reach E_c-E_f = 0 for varying p-type doping depths has been extracted.

The variable in-situ bias experiment is summarized below in Figure 10 along with the results from IV measurements. Although PN diode formation is not observed, results show an enhancement of the forward voltage shift without degradation of the reverse leakage current as compared with the undiffused region of the sample. Contrary to the hypothesis, the 'open' and 'short' circuit sample configurations show the greatest enhancement. The +5, +10 and +15 volt samples all revealed forward IV enhancement however the +5 volt sample had a 1000x larger reverse leakage current while the +10 and +15 volt samples showed no change in the reverse leakage current.

Material	Sample Name	Bilayer	Annealing Conditions		
			Temp. (°C)	Time (min)	In-situ Bias
IQE - Variant 2 $N_{Si} \approx 2e16cm^{-3}$	QB30	Au/MgF_2 (100/100nm)	800	5	Short Circuit
	QB31				Open Circuit
	QB32				+5V (~40nm)
	QB33				+10V (~75nm)
	QB34				+15V (~115nm)
	QB35				+20V (~150nm)
	QB36				Short Circuit
	QB37				0 to 10V Sweep
	QB38				0 to 20V Sweep
	QB39				No Bias



(A) (B)

Figure 10. (A) Summary of samples fabricated for the in-situ bias experiment and (B) the extracted forward voltage shift vs. relative reverse leakage ratio.

Summary of TCAD Device Simulation

SILVACO is used to both understand non-ideal electrical behavior in fabricated devices and predict geometries required to observe enhancement in fabricated devices. A Summer intern was successful in developing a testbed for evaluating the complex geometries needed to observe Superjunction behavior in simulation. TCAD Simulation work completed is summarized below:

Positive Voltage Shift in Diffused Devices

Two hypotheses were formed to explain the positive forward I-V voltage shifts (shown later) in the diffused region of processed samples. The first assumes that the surface of the semiconductor is doped p-type except for small patches which would allow parallel Schottky diode conduction. A second hypothesis was developed where the complete surface of the semiconductor was doped but the stringent requirements to make a p-type ohmic contact had not been met. From simulations it was concluded that the latter was the cause of the voltage shift indicating that the gallium assisted diffusion process is successful but will not yielded PN diode behavior until the acceptor concentration is increased.

Complex Geometry Testbed

Ideal functionality of a SJ-finFET relies on many parts working correctly. To help inform parameter selection for use in subsequent device fabrication procedures, a SILVACO simulation testbed was created where parts of the final devices could be tested in isolation. Work from a Summer intern realized the ability to simulate avalanche breakdown and forward operating points in complex structures.

Enhanced Device Geometry

Continuing where the Summer intern left off, device fabrication parameters in PN, JBS, SJ-JBS diodes were evaluated. Focus has been understanding the effects of device geometry and doping levels on avalanche breakdown. Results from these simulations will inform future device fabrication procedures.

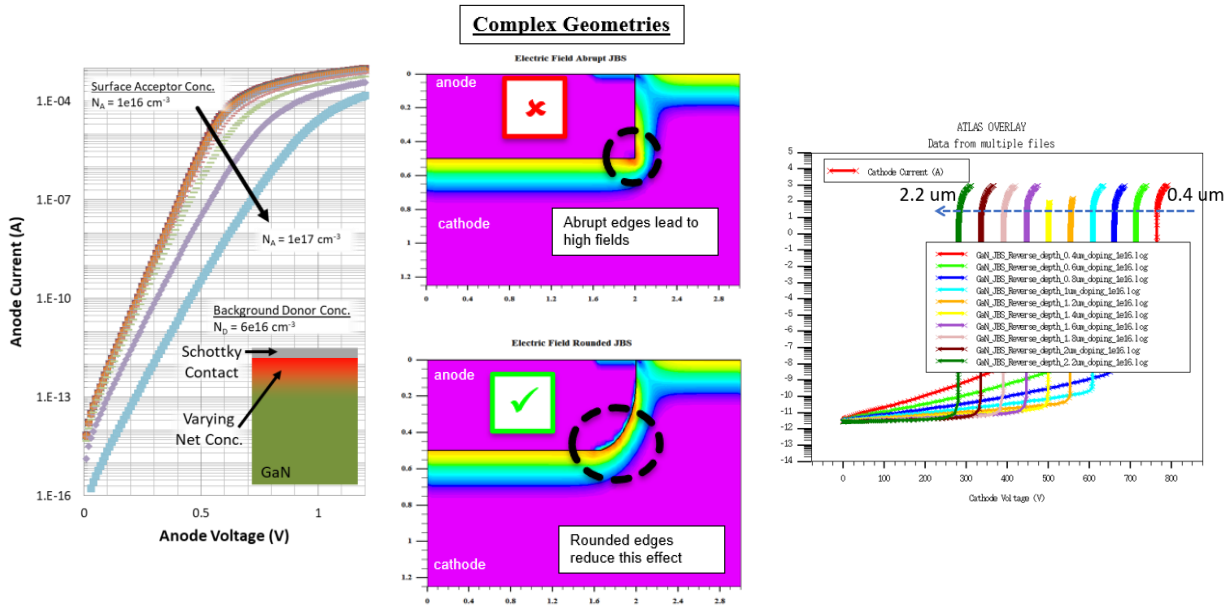


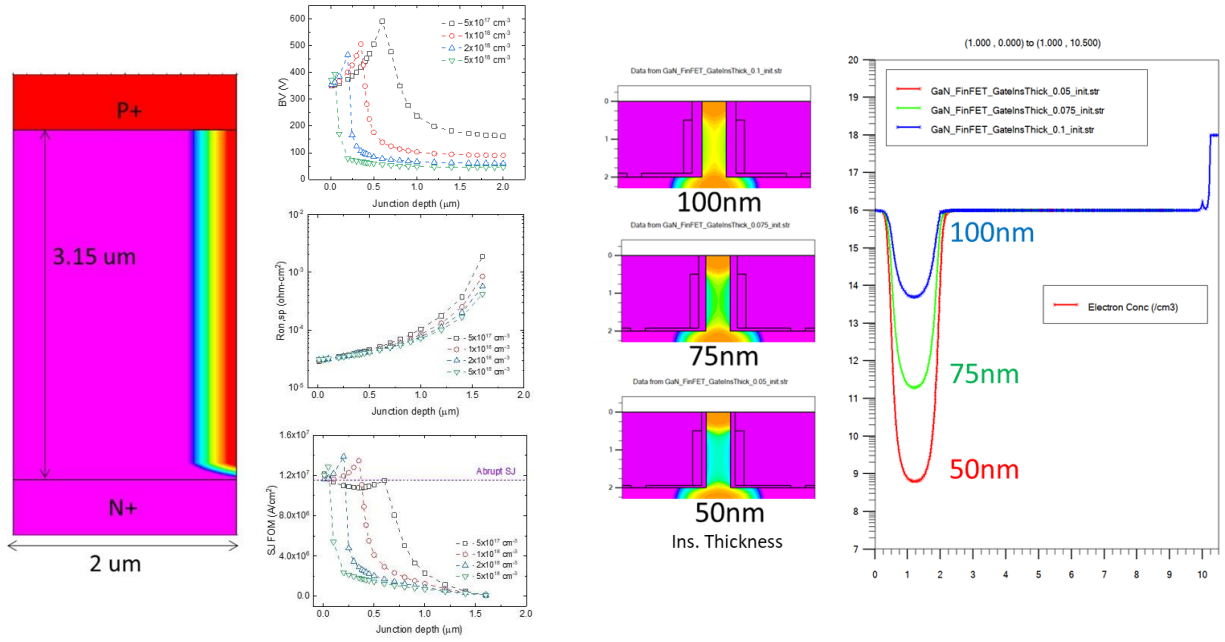
Figure 11. SILVACO TCAD simulation results show the (A) effects of donor compensation at a Schottky contact, (B) dispersion of electric field at a rounded interface and (C) breakdown characteristics of a JBS diode with varying Schottky diode areas.

GaN SJ Diode with ERF Profile CBL

Previously reported simulations of GaN-based Superjunction devices utilized an abrupt PN junction for the charge balance layer. By diffusing p-type dopants into the sidewall it is expected that the on-resistance and breakdown voltage characteristics will be changed. TCAD simulations have revealed a non-monotonic relationship between the diffusion depth and breakdown voltage. For a given surface concentration, there exists a single diffusion depth that would result in a maximum breakdown voltage. Around this point, the specific on-resistance does not vary much according to the plot below in Figure 12 (A). Comparing the figure-of-merit of these devices and abrupt Superjunction with identical active region doping concentrations, it has been shown that diffusion doped devices can outperform traditional SJ structures.

GaN SJ FinFET with ERF Profile CBL

The structure shown below in Figure 12(B) have been simulated to understand the effects of a diffused charge balance layer on the 3-terimal finFET. Currently, the structure is being optimized to understand the required fin and gate thicknesses to create a normally-off device. Once understood, the device characteristics under high voltage/current and switching capabilities will be simulated and compared to literature values.



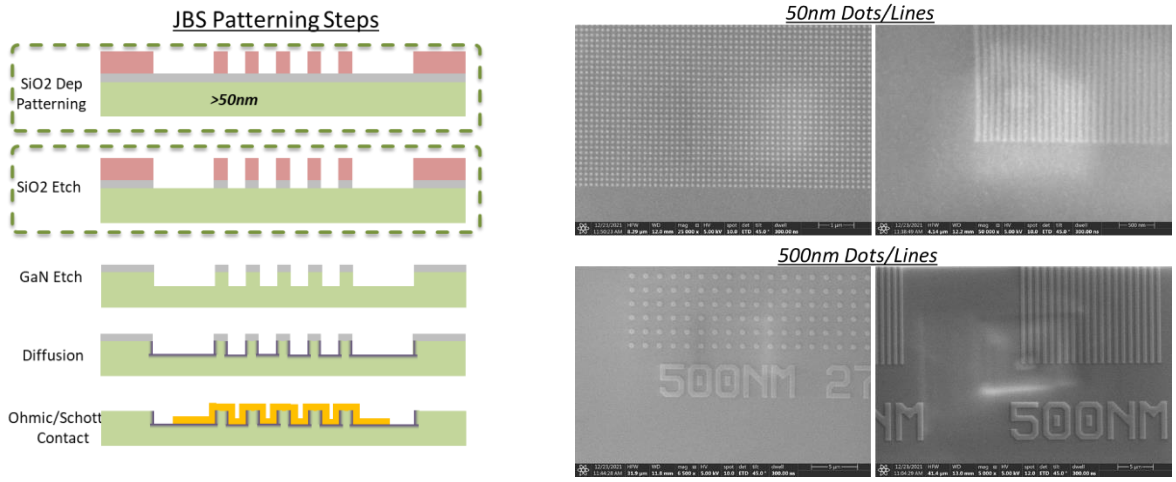
(A) (B)

Figure 12. (A) Optimized GaN SJ diode structure and the effect of varying the error-function depth on the breakdown voltage and specific on resistance. (B) Preliminary results of the GaN finFET structure showing the effect of decreasing gate insulator thickness on the electron concentration withing the channel

Summary Sub-Micron Device Processing

It was found from previous TCAD simulations that high power device enhancement is realized when the active region is <1um. For the example JBS process flow below in Figure 13(A), if the

pattern transferred pillar did not meet this critical dimension the IV characteristics would be dominated by the Schottky diode region on the top surface. Thus, the EBPG 5200 e-beam direct write system is utilized on this project to define patterns in resist that can be transferred into the GaN down to single nanometers. Currently, the EBPG has successfully been used to define features as small as 25nm but limits on sample throughput caused by tool downtime have limited process iterations. Currently, 250nm pillar and fin patterns have been transferred into GaN but further experimentation is needed to improve the etch mask.

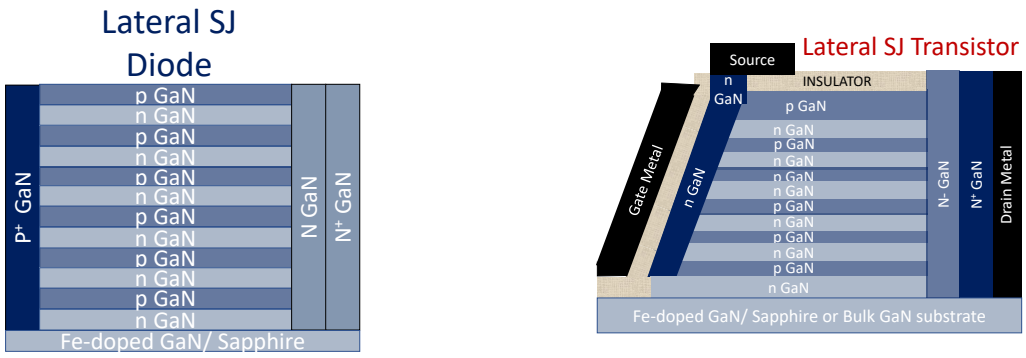


(A) (B)

Figure 13. (A) Example process flow for realizing JBS diodes and (B) SEM images of 50 and 500nm patterns realized in e-beam resist on GaN.

Charge Balancing by Epitaxial Growth

To ensure project deliverables are not delayed by the progress of the GAID process, external contributors have agreed to grow GaN films by MBE which are capable of lateral Superjunction device realization. With our current success modeling charge balanced structures and low damage deep etching in GaN, we will inform the growth and microfabrication processes to target explicit breakdown voltage and on-resistance values suitable for transition into industry. An example of the lateral SJ diode and lateral SJ transistor are shown below in Figure 14. With an ammonia-MBE system, alternating n and p-type doped layers will be grown according to TCAD simulations. These layers when contacted on the sidewall according to the figure below, will act as charge balanced layers for 2- and 3-terminal devices.



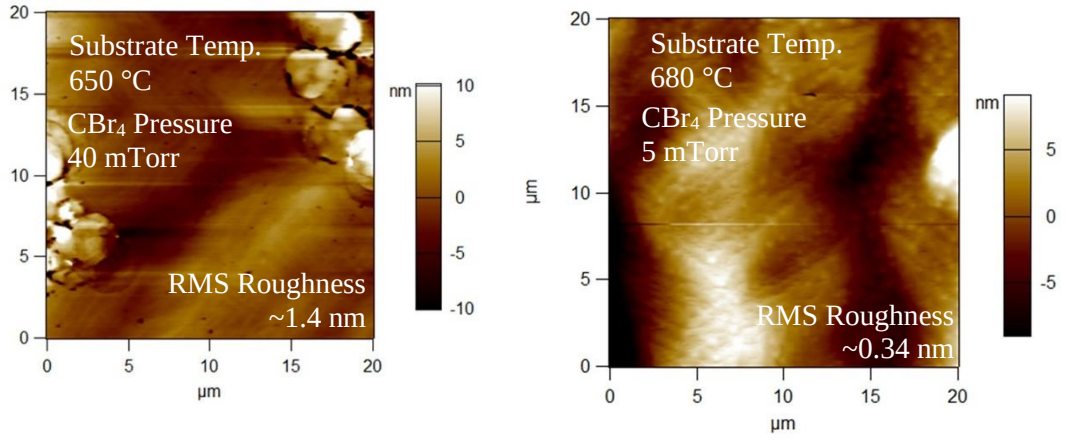
(A) (B)

Figure 14. MBE-grown layer structures for (A) lateral Superjunction diode and (B) lateral Superjunction transistor

Summary of Material Growth and Development

Semi-Insulating Buffer Layer Development

The lateral nature of these devices requires careful consideration into the substrate type and growth interface isolation where conductive underlayers can cause unwanted lateral conduction. Thus, to achieve breakdown voltages that are dominated by the anode-cathode spacing and not spurious conduction paths, iron-doped GaN layers are grown prior to the periodic charge balanced layers. AFM measurements on layers grown without optimization reveal RMS surface roughness non-ideal for subsequent active layer growths (1.4 nm), as seen below in Figure 15(A). Experiments with varying growth parameters including substrate temperature and CBr_4 flux has shown lower surface roughness (0.34 nm) of the Fe-doped buffer layers. With surface roughness within the range appropriate for subsequent charge balanced layer growth, the next step is to characterize the lateral conductivity.



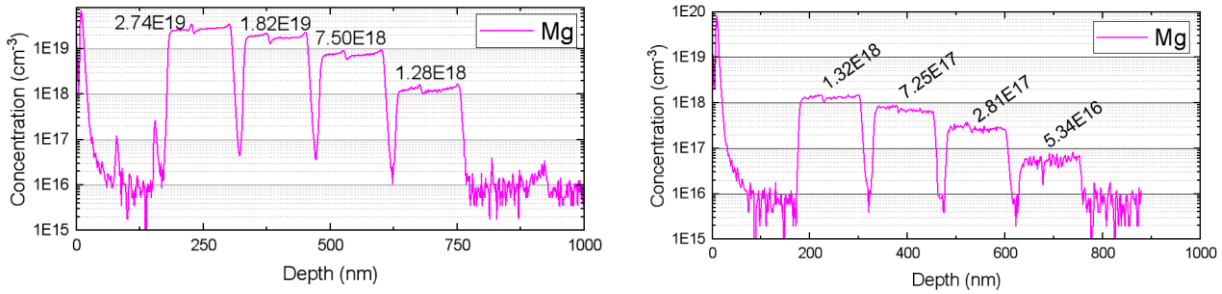
(A) (B)

Figure 15. AFM measurements on MBE-grown Fe-doped GaN films for lateral conduction isolation.

Mg and Si Doping Range Calibration

Charge balanced Superjunction structures require well controlled ionizable doping concentrations in both the n- and p-type regions. Due to the difficult nature of p-type doping in GaN, work has

been done to calibrate the effective ionizable dopant concentrations with SIMS and Hall measurements. SIMS measurements reveal a wide range of Mg concentrations controllable by growth parameters, shown below in Figure 16. Once a high resistivity Fe-doped buffer layer recipe has been established, layers with varying Mg concentrations and thicknesses will be measured for Superjunction charge balancing viability.



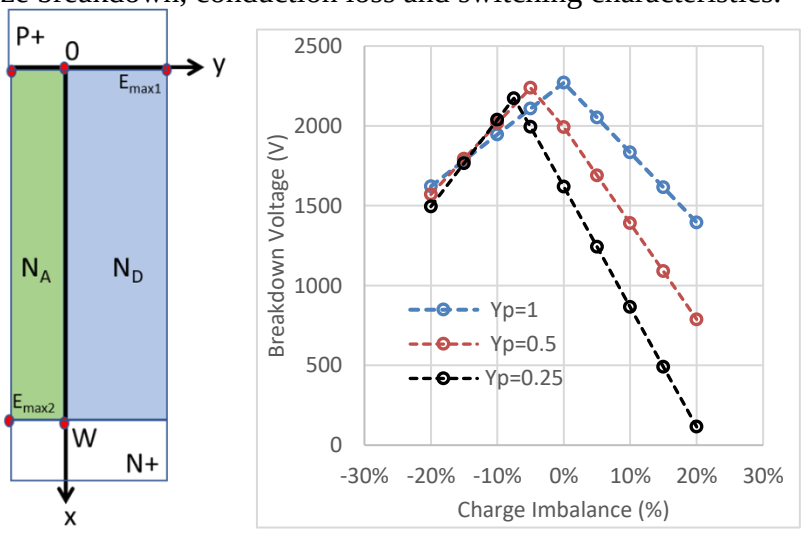
(A) (B)

Figure 16. Mg concentration measured in MBE grown GaN SIMS calibration stacks with varying Mg source temperatures.

Summary of Charge Balanced Parameter Modeling

Analytical Charge Imbalance Modeling

Both analytical and numerical models have been developed to rapidly represent the effect that growth and process variability have on lateral Superjunction device capabilities. For example, to reach full Superjunction capability, tight control of thickness and ionizable concentration levels are required. Analytical modeling revealed when charge balanced layers are not matched in thickness the ratio of volumetric ionizable charge concentrations should also not match, a point which is counterintuitive to the idea of charge balancing. This is shown below in Figure 17. With these models, a new understanding of device architecture paves the path for complex doping schemes to optimize breakdown, conduction loss and switching characteristics.



(A) (B)

Figure 17. (A) Half pillar Superjunction representation used to model effects of charge imbalance and (B) breakdown calculated for

Pillar Carrier Mobility Effect on Switching Characteristics

To increase conductivity in a single CBL period, the pillar with higher mobility could be emphasized while maintaining charge balance. Silvaco simulations were run to understand the effects that p- pillar thinning and low hole mobility have on a device switching performance. Here it was found that by limiting the aperture which slow holes can be removed, large switching losses during the 'on' to 'off' transition are induced. Currently, work is being done to develop mitigation methods to restore simulated switching performance.

Summary of Superjunction Device Modeling

Silvaco TCAD has been utilized to create device testbeds for the full/half stairstep Superjunction diode and the lateral Superjunction Schottky diode. Here we have utilized results from analytical models to optimize the Superjunction Figure of Merit (SJFOM) while testing effects of non-constant doping profiles and regrowth interfaces on lateral devices. Below in Figure 18(A) shows a progression of proposed devices along with (B) SJFOM simulations for the stair step SJ diode structure with varying anode-cathode spacings. The SJFOM simulations reveal that with a single optimized growth and fabrication run, devices with varying abilities can be fabricated so long as the anode to cathode spacing can be satisfied. Additionally, simulations of lateral Superjunction Schottky diodes reveal an exciting path toward low on-voltage rectifying devices like JBS structures but with full depletion of variable length channels. Here, models with a cathode contact formed with and without regrowth have been simulated.

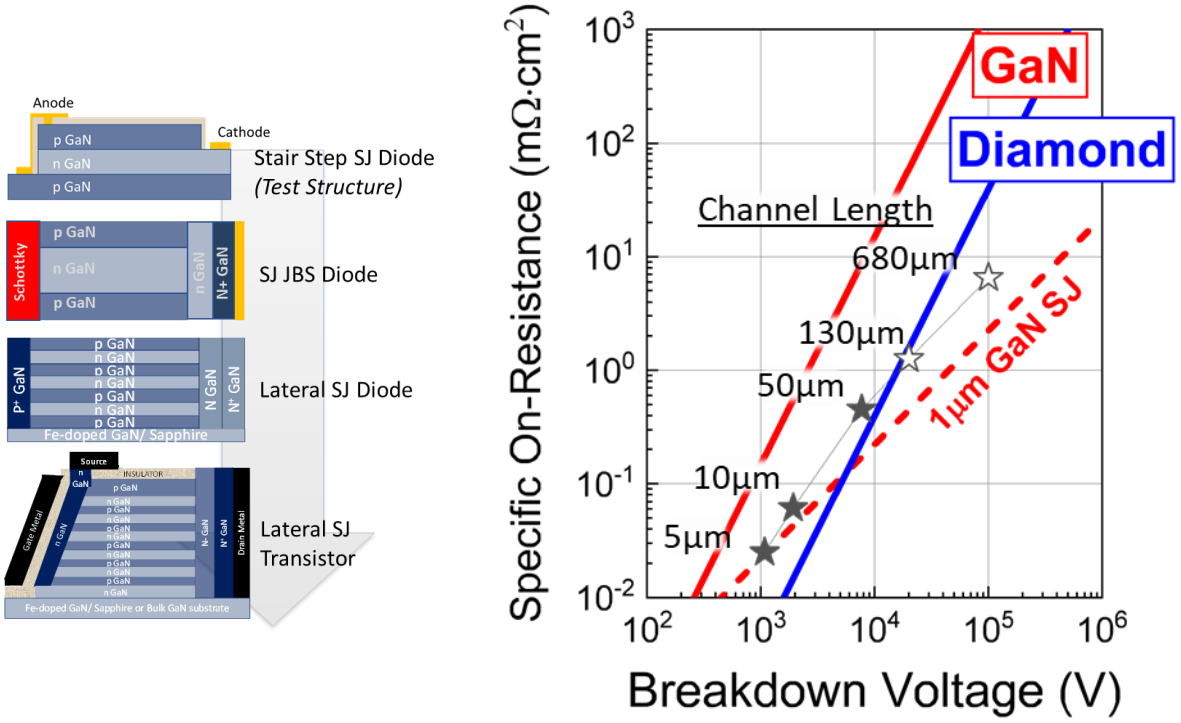


Figure 18. (A) Proposed SJ devices and (B) figure-of-merit plot for stair step SJ diode revealing breakdown control by anode-cathode spacing

Proposed Work for FY2023

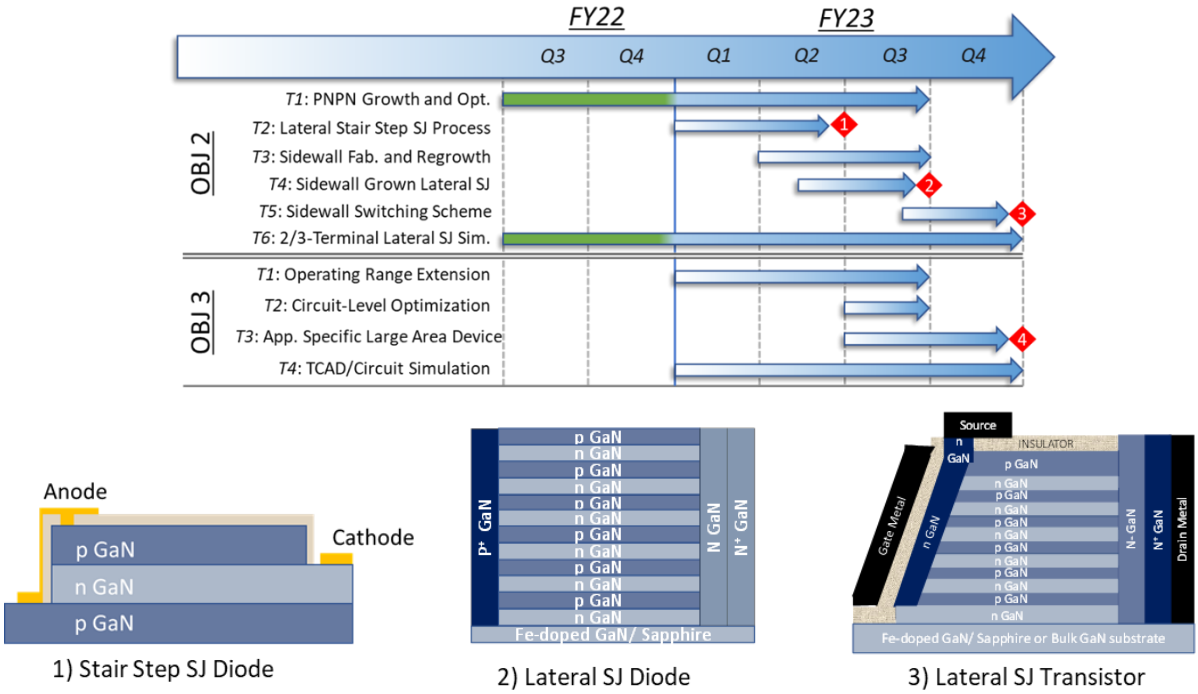


Figure 19. Gantt chart detailing proposed tasked and device realization for FY23

The above Gantt chart lays out the proposed work shared with the project collaborator, UCSB, for FY23. In summary, work in FY23 will focus on MBE growth optimization of charge balanced layers, TCAD device/circuit simulation of proposed SJ layers, diodes and transistor, microfabrication of proposed devices and demonstration of application specific large area devices.

Mission Impact

This project directly supports LLNL's Energy and Resource Security mission area. Because power electronic switches touch nearly aspect of electricity generation and consumption, even small gains in efficiency can drive outsized effects in energy consumption and improve United States energy security and reduce greenhouse gas emissions. It also falls with the Advanced Materials and Manufacturing core competency, as GaN is a next generation semiconductor material, and the project will be developing new manufacturing techniques for GaN devices.

Conclusion

Although SIMS analysis shows high concentrations of Mg at the surface of prepared samples, additional work is needs to improve the concentration of ionized acceptors at room temperature such that a PN diode can be formed. In the near-term, to mitigate the risk of not improving the hole concentration in GaN layers, external contributors have agreed to grow GaN P/N/P structures to form lateral GaN Superjunction devices. Here, we will expand our developed TCAD simulation-base and sub-micron processing techniques to define geometries and dopant concentrations needed to demonstrate Superjunction enhanced devices.

Publications, Presentations and Patents

- Varley, Joel Basile, Noah Patrick Allen, Clint Frye, Kyoung Eun Kweon, Vincenzo Lordi, and Lars Voss. "Field assisted interfacial diffusion doping through heterostructure design." U.S. Patent Application 17/166,962, filed August 19, 2021.

- Voss, Lars F., Clint D. Frye, Noah A. Allen, Sarah E. Harrison, Kyoung Kweon, Joel Basile Varley, Vincenzo Lordi, Rebecca Nikolic, Travis J. Anderson, and Jennifer K. Hite. "Moderate Temperature Mg Diffusion Doping of GaN." In *ECS Meeting Abstracts*, no. 26, p. 1810. IOP Publishing, 2020.

- [Invited Abstract] Voss, Lars F., Clint D. Frye, Noah A. Allen, Sarah E. Harrison, Kyoung Kweon, Joel Basile Varley, Vincenzo Lordi, Rebecca Nikolic, Travis J. Anderson, Jennifer K. Hite., Jung Han, and Bingjun Li. "Prospects for Magnesium diffusion doping of GaN" *ECS Meeting Abstracts, 2021*

- [Record of Invention Accepted] Noah A. Allen, Clint D. Frye, Kyoung E. Kweon, Vincenzo Lordi, Qinghui Shao, Joel Basile Varley, Lars F. Voss "Superjunction Devices by Field-Assisted Diffusion of Dopants" 2022

Upcoming Publications

- "Gallium Vacancy-Assisted Diffusion of Magnesium in GaN for P-Type Layer Formation"

- "Numerical Analysis of Performance of GaN Superjunction Devices Fabricated from Lateral Dopant Diffusion"