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ELECTRONICS RESURGENCE INITIATIVE SUMMIT & MTO Symposium

Xyce Circuit Simulator and Surrogate Modeling

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Posh Open Source Hardware (POSH)

Mitigating Design Costs

Topic

Xyce™ Parallel Electronic Simulator

Parallel Circuit Simulator

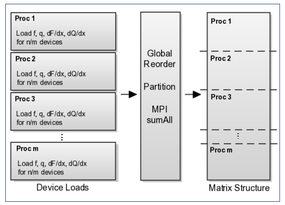
New Xyce Feature: PyMI: Python model interface

… **which enables:** Surrogate models via Dynamic Mode Decomposition (DMD)

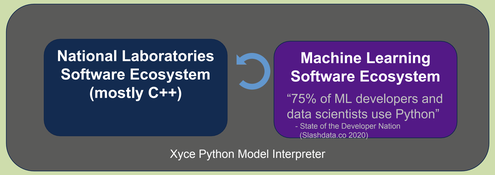
Background

The Xyce Parallel Circuit simulator is a SPICE-style analog circuit simulator, developed from-the-ground-up using a distributed memory paradigm, that provides a modular framework for developing state-of-the-art continuation algorithms, time-integration methods, preconditioned linear solvers, and parallel partitioning techniques

- **Xyce separates device distribution from matrix partitioning**
  - Cost of device evaluation unrelated to matrix partitioning
  - Enables each to separately determine the distribution that is efficient for communication and computation.
  - Hierarchical information leveraged in either distribution to enact efficiencies or integrate "fast-SPICE" techniques.



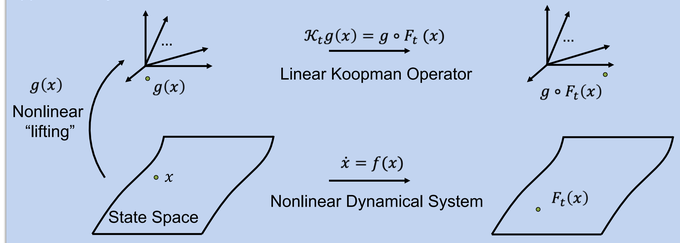
Xyce-PyMi (Paul Kuberry)



- Goal is to enable ML advancements to impact circuit design via data-driven models
- Leverages General External interface (C++) from Xyce, by Tom Russo
- Easily installable and callable capability for executing Python ML models in a production circuit simulation software (Xyce ←→ PyBind11)
- Actively engaged with compact model development groups and circuit designers at Sandia
- Provide data-driven compact device modeling approaches (GMLS, splines, deep neural networks, **Dynamic Mode Decomposition, see below**) from various ongoing research projects at Sandia

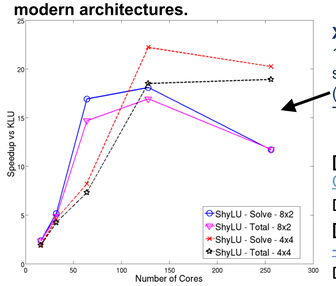
Model Abstraction via Koopman Operator

Koopman Operator: Infinite dimensional *linear* operator that fully describes the underlying evolution of scalar observables of a nonlinear (even chaotic) system. The Koopman operator can be approximated by **lifting** the state space to a higher dimensional space where its evolution is approximately linear.



Approach

Xyce has succeeded in performing scalable simulation of postlayout ASICs with >1M devices [1] and a history of developing specialized parallel linear solvers [2] to enable efficient simulation on modern architectures.



Xyce ASIC simulation scaling example. The circuit has 1.6M devices and 1.9M unknowns. Study is of strong scaling of Xyce simulation time and linear solve time (ShyLU) for different configurations of MPI Tasks X Threads per node.

[1] "A Hybrid Approach for Parallel Transistor-Level Full Chip Circuit Simulation," Thornquist et al.
DOI: 10.1007/978-3-319-17353-5_9

[2] "A parallel preconditioning strategy for efficient transistor-level circuit simulation," Thornquist, et al.
DOI: 10.1145/1687399.1687477

Xyce Xyce-PyMI to invoke an ML Python device or subcircuit

```
>> Xyce-PyMi example.cir
```

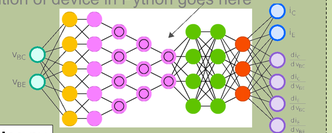
Xyce-PyMi (Xyce + **Py**thon **M**odel **I**nterpreter)

- Full Xyce functionality + devices / subcircuits / circuits defined in Python
- Python class defines how F, Q, B, dF/dX, and dQ/dX vectors/matrices are populated for Xyce DAE equation:
  - residual = f(x,t) + dq(x,t)/dt - b(t)
- Supports all popular machine learning frameworks such as TensorFlow, Keras, PyTorch, Jax, Numba, Numpy, etc…

* **example.cir** (Example of easy inclusion in a netlist)

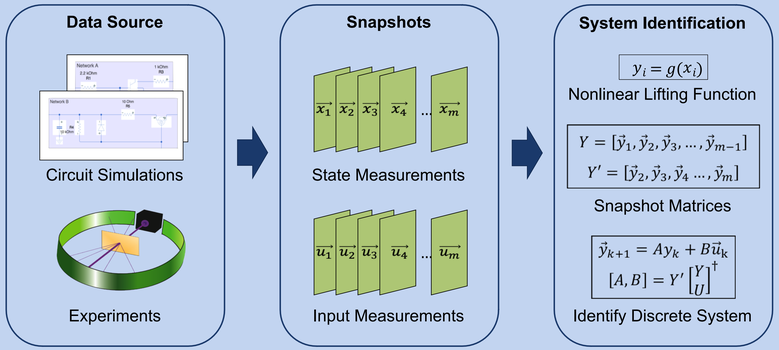
```
YGENEXT devicename terminal1 terminal2
+ SPARAMS={NAME=MODULENAME
+ VALUE=PythonDevice.py}
```

```
from BaseDevice import BaseDevice
class Device(BaseDevice):
    def computeXyceVectors(…):
        # definition of device in Python goes here
```



PythonDevice.py BJT DNN Compact Model

Extended Dynamic Mode Decomposition (EDMD)



Results and Impact

Obtaining Xyce

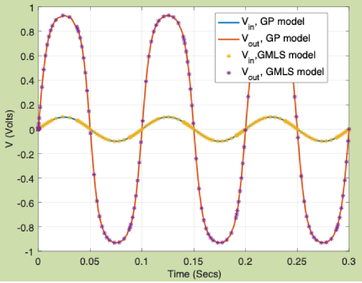
https://xyce.sandia.gov/ for Xyce binaries and documentation
https://github.com/Xyce for Xyce source code and regression tests

Recent developments

- Xyce version 7.3 released in May 2021
- Xyce Data Model (XDM) netlist translator version 2.3
- Support for 65nm 55nm, 14nm 12nm GF PDKs
- Support for Skywater 130 PDK
- Support for polynomial chaos expansion methods for uncertainty quantification
- Support for Verilog Procedural Interface (VPI) to support mixed signal simulation
  - Link to Yale discrete event simulator
- New Python model interface (PyMI). See below!
- Link to Synopsys analog assertions tool, Amstaff

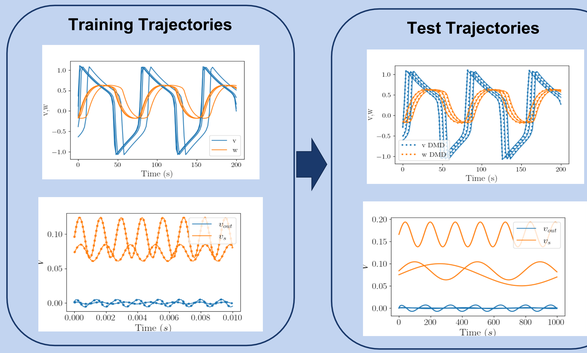
Xyce-PyMI example

Operational Amplifier with BJT models replaced by GMLS* models
GMLS = Generalized Moving Least Squares



* **from:** Development, Demonstration, and Validation of Data-driven Compact Diode Models for Circuit Simulation and Analysis K. Aadithya, P. Kuberry, B. Paskaleva, P. Bochev, K. Leeson, A. Mar, T. Mei, E. Keiter, arXiv:2001.01699

Simulations with EDMD Models



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