



CMOS FeRAM at Sandia MESA

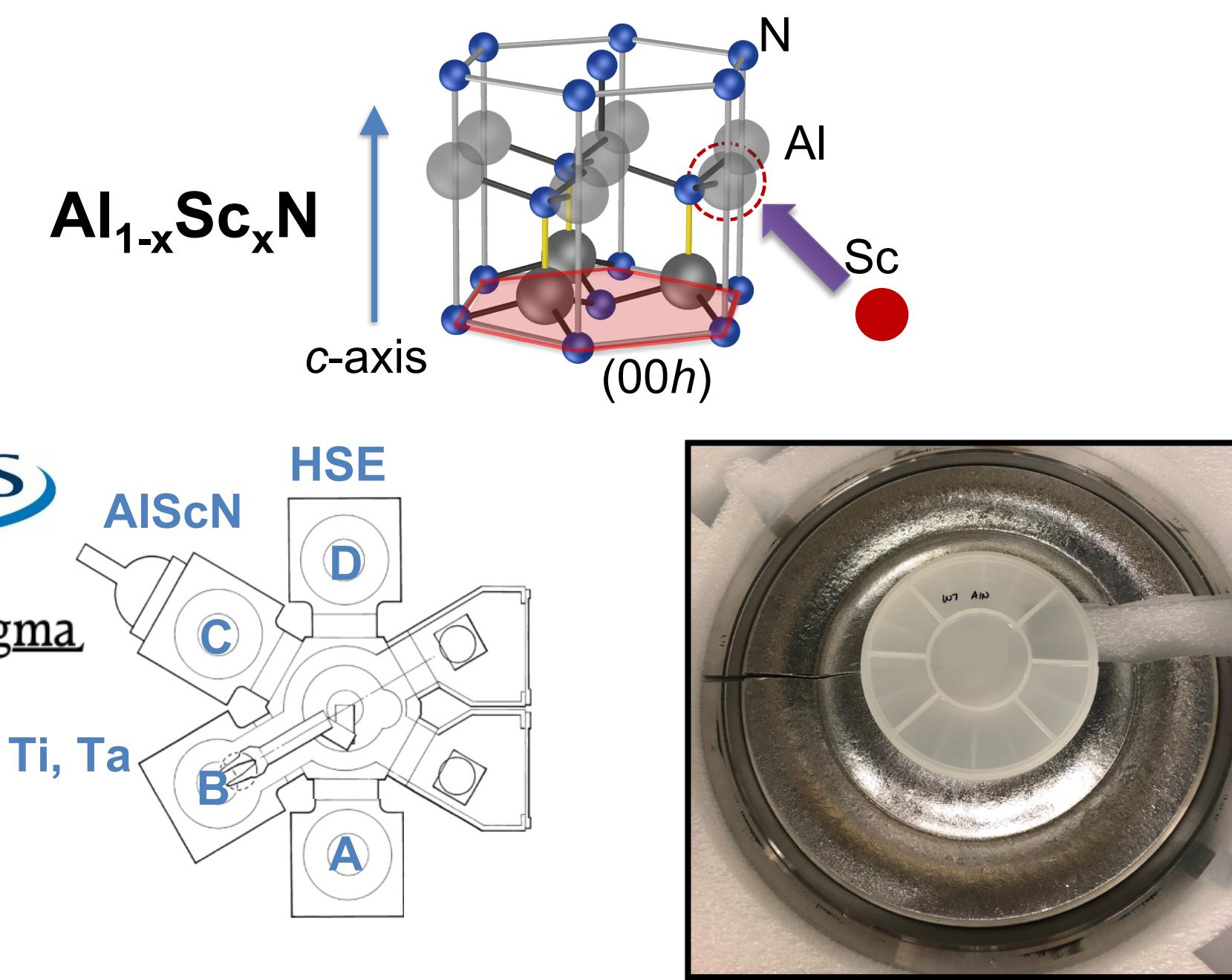
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Development of $\text{Al}_{1-x}\text{Sc}_x\text{N}$ Ferroelectric Films

Project summary: Fabricated ferroelectric AlScN capacitors at the 6" wafer-level for structure-property-processing relationships.

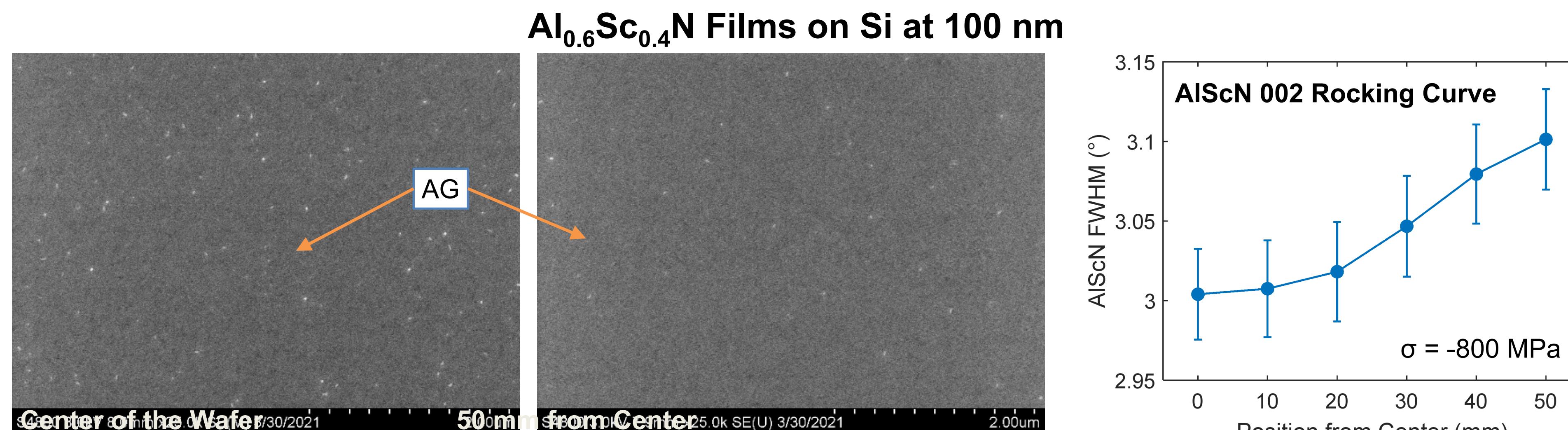
Goal: Develop AlScN (Sc 40%) sputtered films using single-alloyed target on a cluster deposition tool.

- Control film thickness and wafer-level stress.
- Achieve desired microstructure on metal templates.
- Chambers for AlScN, Metals, and Hot Sputter Etch (HSE).
- Target size is 330 mm diameter.
- $\text{Al}_{0.6}\text{Sc}_{0.4}$ single-alloyed target is used.
- Structure-property-processing relationship at the 6" wafer-scale yields insight into manufacturability.



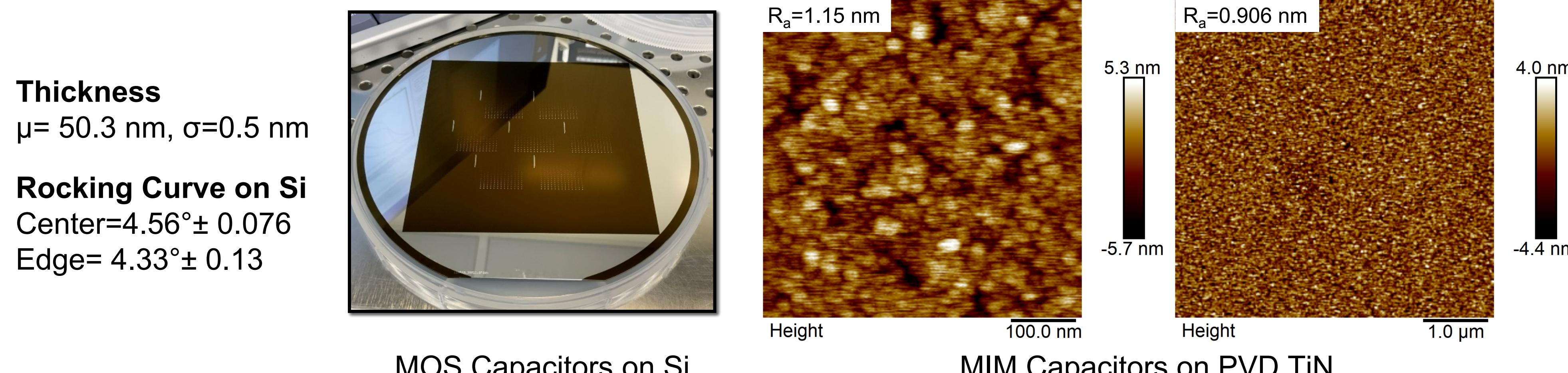
$\text{Al}_{1-x}\text{Sc}_x\text{N}$ Films at the Wafer-Level

- Films are characterized using scanning electron microscopy (SEM), ellipsometry, and X-ray diffraction (XRD) to gain insight into the microstructure of the film.
- Film development is scaling down from 100 nm to 50 nm film thickness.
- Leakage of 100 nm films is on the order of 10^{-6} A/cm^2 at $< 2 \text{ V}$ for MOS and MIM capacitors.
- Established processes will be available for device integration with other thrust members.
- Path forward** for film development involves using multistep depositions, sputter etching starting material, and using new templates such as Ta, W, TiN, TaN, and AlN.



The density of abnormal grains (AG) is higher in the center than on the edge of the wafer due to stress variation. The size of the AG are $\sim 35\text{-}45 \text{ nm}$, and they are detrimental to piezoelectric performance.

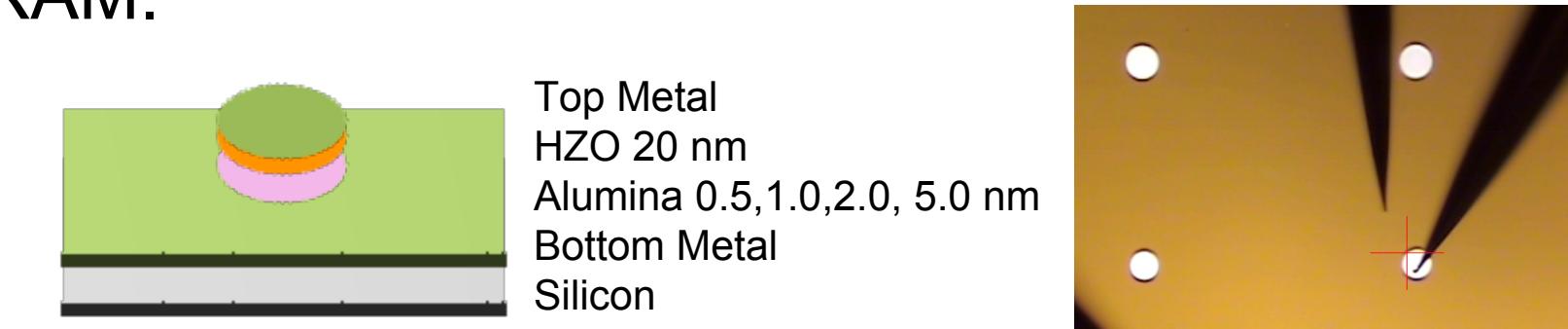
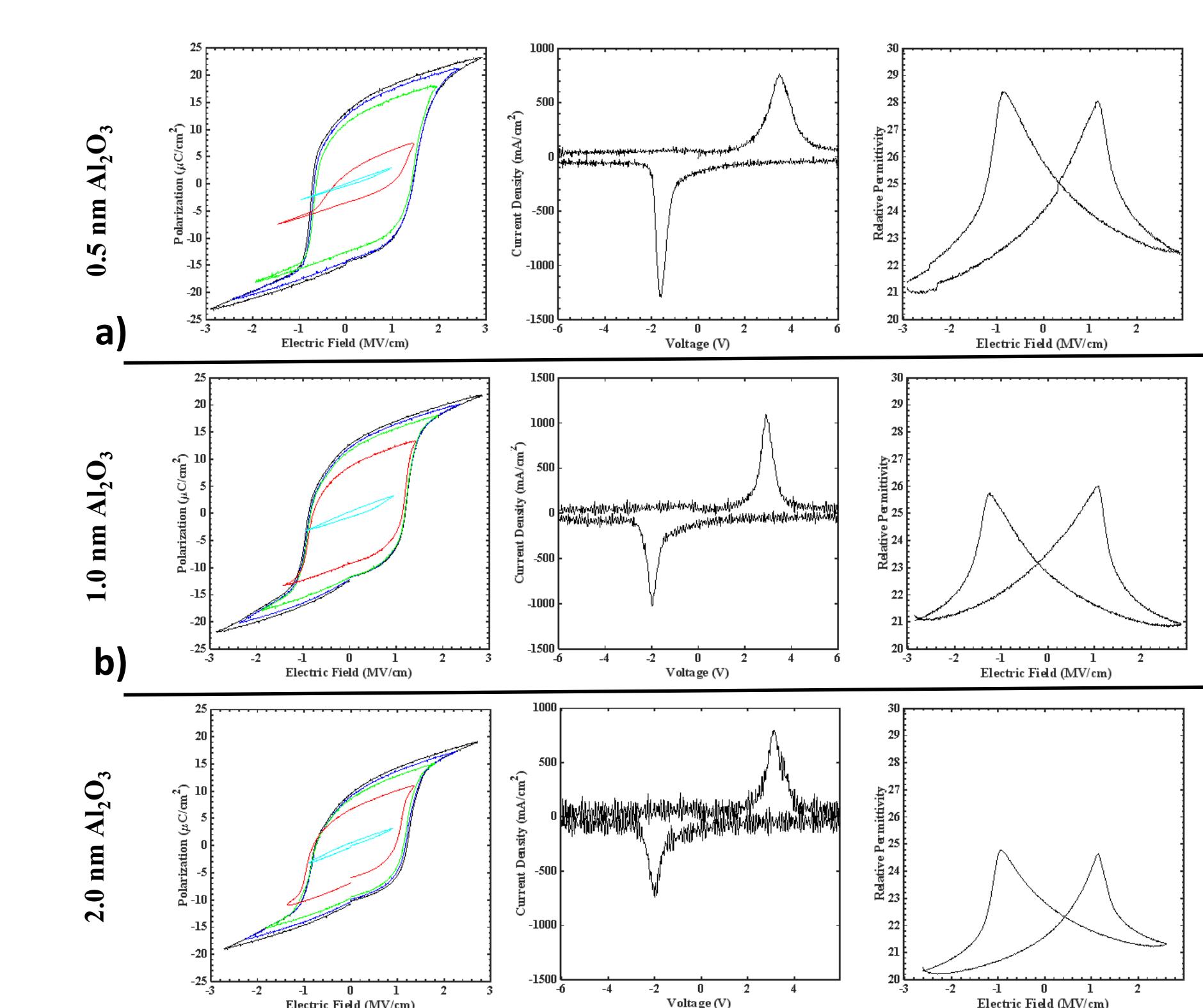
Scaling Down to 50 nm $\text{Al}_{0.6}\text{Sc}_{0.4}\text{N}$ Films



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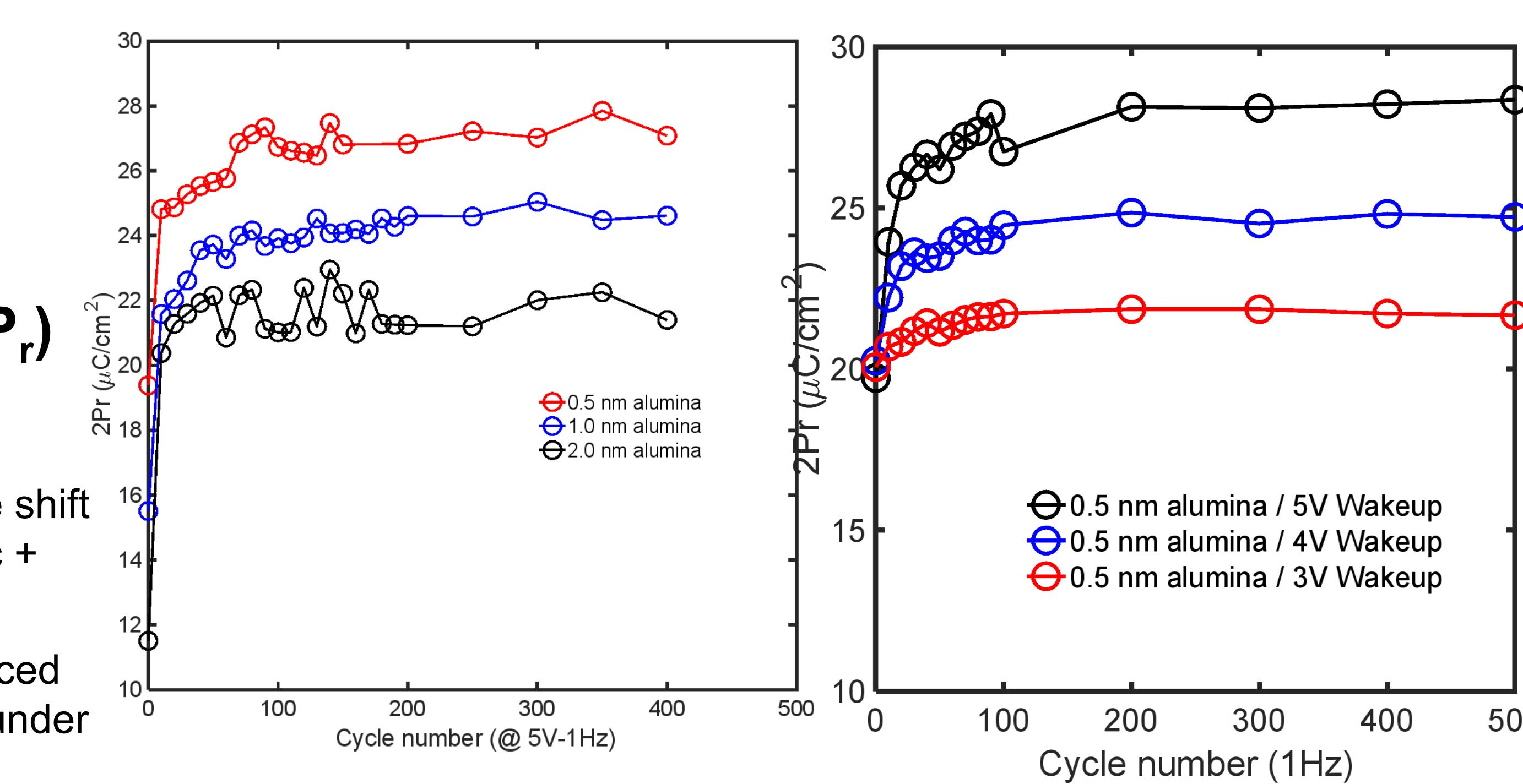
Evaluation of HfZrO_2 as a CMOS Integrable FeRAM Candidate

Ferroelectric memory has a high potential for high impact applications in the DOE and Sandia microelectronics. A new candidate that needs to be closely investigated is ALD hafnia/zirconia stacks in which an orthorhombic crystal phase can be stabilized at thickness of 5-20 nm, under CMOS compatible conditions (anneals at 400 – 600°C 30sec). In this work we utilize a CMOS compatible set of metal electrodes (niobium and niobium nitride) chosen to help establish the correct ferroelectric phase as well as having potential applications in superconductivity electronics (SCE) devices / architectures and in quantum computational devices. We examine devices where alumina layers of various thickness are inserted between the bottom electrode (BE) and the ferroelectric HZO films such that properties including leakage, memory retention, wake up and fatigue can be evaluated for integration into FeRAM.



Evaluation of NbN / Al_2O_3 / 20nm HfZrO_2 / NbN

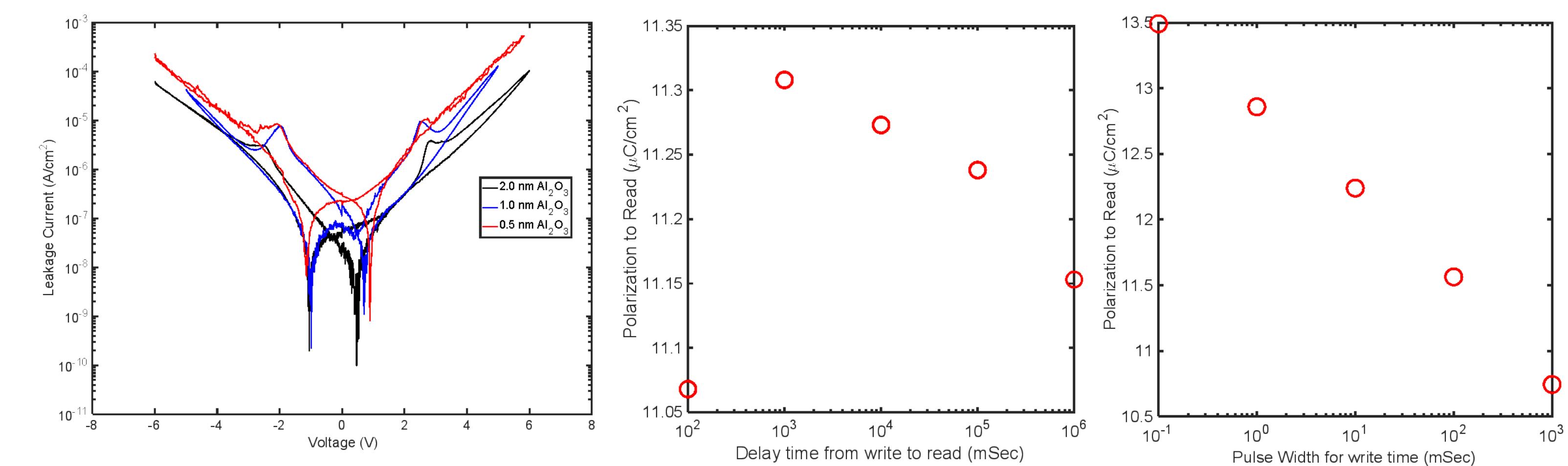
- Insertion of $\frac{1}{2}$, 1, and 2 nm alumina yielded modifications in the maximum achievable remanent polarization of 28, 25, 21 $\mu\text{C}/\text{cm}^2$ respectively.
- Relative permittivity of the composite stack is noted to decrease as the alumina thickness increases.
- 25% change in capacitance was observed – basis of FeRAM.



Wake-up and Remanent Polarization (P_r)

of the films were observed to shift (right).

- For a 1Hz / 5V wake up cycle, as the alumina thickness increased, the P_r decreased. It was expected that some shift could be attributed to switching dynamics of ferroelectric + dielectric sandwich physics.
- Cycling of the $\frac{1}{2}$ nm alumina + 20 nm HZO films at reduced bias demonstrate that a reduction of the P_r is achieved under lower fields.



Current work is examining the performance of using alumina under the HZO

- Leakage plots confirm modest logarithmic improvements.
- Investigations are current looking at memory aspects such as retention and required bit write times (for the 1 nm alumina shown left).

Recent work suggests exceptional ferroelectric performance of Nb / Al_2O_3 / 20nm HfZrO_2 / Nb (Right).

