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An Isolated Bidirectional DC-DC Converter with High Voltage Conversion Ratio and Reduced Output Current Ripple

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***Abstract*—This paper presents an isolated bidirectional dc/dc converter for battery energy storage applications. Two main features of the proposed circuit topology are high voltage-conversion ratio and reduced battery current ripple. The primary side circuit is a quasi-switched-capacitor circuit with reduced voltage stress on switching devices and a 3:1 voltage step down ratio, which reduces the turns ratio of the transformer to 6:1:1. The secondary side circuit has an interleaved operation by utilizing splitted magnetizing inductances of the transformer, which not only helps to increase the step down ratio but also reduces the battery current ripple. Similar to dual-active-bridge circuit, the phase shift control is implemented to regulate the operation power of the circuit. A 1 kW, 300 kHz, 380-420 V/20-33 V GaN based circuit prototype is currently under fabrication. The preliminary test results are presented.**

***Index Terms*—DC-DC power converter, isolated dc-dc converter, gallium nitride (GaN), switched capacitor circuits, interleaved boost circuit**

I. Introduction

In power distribution systems, lower voltage battery systems can provide higher reliability, safer operations, and reduced balancing losses. High voltage gain converters can interface these low voltage battery systems with standard inverter dc link voltages. To achieve high voltage gain, the isolated dc-dc converter with high-frequency magnetic components is commonly used[1][2]. CLLC and dual-active-bridge (DAB) are common circuit topologies for the isolated bidirectional dc-dc converter in battery storage system[3][4][5]. The CLLC circuit has the advantage of soft switching capabilities over the full load range. But it has high circulating energy, which introduces additional conduction losses in the transformer magnetizing inductance. The DAB circuit has lower circulating energy and lower conduction loss. However, the DAB circuit has difficulty in maintaining soft switching operation at light-load conditions. Voltage conversion ratios of the DAB and the CLLC are determined mainly by transformer turns ratios.As a result, the transformer turns ratios are high to achieve a high voltage ratio. High turns ratio can cause low coupling between windings, high power loss and manufacturing difficulties. A phase shift dc/dc converter with a quasi-switched-capacitor (QSC) circuit on the high voltage side was proposed in [6]. The QSC circuit on the high voltage side provides a voltage step-down ratio of 3:1 from the input side to the transformer primary side, which can reduce the transformer turns ratio and the voltage stress on the switching devices. For the low voltage side of the dc/dc converter, one of the challenges is to limit ripple current to the low voltage battery. This paper presents a study on an isolated bidirectional dc-dc circuit. With the QSC circuit on transformer primary side and new proposed transformer-interleaved circuit on low voltage side, the advantages are:

- Compared to the DAB circuit, the QSC and transformer-interleaved circuit can provide 6:1 voltage conversion ratio even if the transformer has a 1:1 turns ratio.
- Compared to previous proposed QSC phase shift circuit, it has a even higher voltage step-down ratio and lower output current ripple.

This paper consists of five sections. In Section II, circuit operation principle and detailed analysis are presented. Section III covers the circuit optimization and magnetic component designs. Section IV shows the simulation verification, the 1-kV, 400-V/20-33-V prototype in progress and preliminary experimental results. The conclusions are summarized in Section V.

II. Description and Operation Principle of the Circuit

A. Circuit Overview

As illustrated in Fig. 1, the proposed circuit diagram consists of a QSC circuit on high voltage side and a transformer-interleaved circuit on the low voltage side.

In the quasi-switched-capacitor circuit, S_{HV2} and S_{HV3} are switched simultaneously in a complementary manner with S_{HV1} with a duty ratio of 0.5. C_2 and C_3 are the two

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switched capacitors with equal capacitance. The voltage stress on each switch device is $\frac{2}{3}\ V_{dc}$. On the transformer primary side winding, the winding voltage stress is $\pm\frac{1}{3}\ V_{dc}$. A voltage conversion ratio of 3:1 is achieved from the input DC side to transformer side.

In the transformer-interleaved circuit, S_{LV1} and S_{LV3} are switched simultaneously as one switching pair, and S_{LV2} and S_{LV4} form another switching pair. Two switching pairs are switching in a complementary manner with a 0.5 duty ratio. The split transformer magnetizing inductance in secondary side windings together with two switching pair form two interleaving boost circuit . Thus, the capacitor C_{LV} voltage stress is $2V_{bat}$. A 1:2 voltage boost ratio is achieved from battery side to the transformer secondary side winding. Also, currents in two boost loops have same value but different polarities. They cancel with each other to mitigate the current ripple on battery side.

B. Circuit Analysis

1) High Voltage Side QSC Circuit: The QSC circuit consists of three switching devices and two switched capacitors. The voltage stress on each switching device is reduced to $\frac{1}{3}$ V_{dc}, and there exists a dc offset current in the magnetizing inductance of the transformer due to the asymmetrical structure and operation between three devices.

When S_{HV2} and S_{HV3} are on, S_{HV1} is switched off. Switched capacitor C_2 is connected to transformer with S_{HV2}in paralleling with the C_3 and S_{HV3}. These two paralleling switched capacitors are charging the transformer primary side windings.

When S_{HV1} is on, S_{HV2} and S_{HV3} are off. Switched capacitor C_2 and C_3 is connected in series with DC bus, S_{HV2} and transformer. In this mode, the switched capacitors are charged by dc bus and transformer.

2) Low Voltage Side Transformer Interleaved Circuit: In transformer-interleaved circuit, S_{LV1}, S_{LV4} and S_{LV2}, S_{LV3} are two switching pairs with the same switching manner. S_{LV1}, S_{LV4} and transformer winding w_2 form the boost circuit, similar forS_{LV2}, S_{LV3} and transformer winding w_3 This circuit's operation is similar to the interleaved boost circuit. The difference is that the transformer secondary side windings' magnetizing inductance replaces two coupled inductors. Two extra inductors are thus eliminated. Based on boost circuit operation mode, there exist dc offset currents in two secondary windings with different flowing direction.

C. Circuit Operation States

Circuit operation waveforms shown in Fig. 2 are divided into eight states based on the devices' on/off statuses in one switching cycle.

State 1($t_0 - t_1$): This state is the switching transient of the high voltage side QSC circuit. While the low voltage side circuit has no switching actions. Transformer secondary side voltages ($V_{w2},\ V_{w3}$) are fixed as V_{bat}. At the beginning of this state, all QSC-side devices are switched off. During ($t_0 - t_{01}$), the transformer primary winding current charges the output capacitance of S_{HV1} and discharges the output capacitances

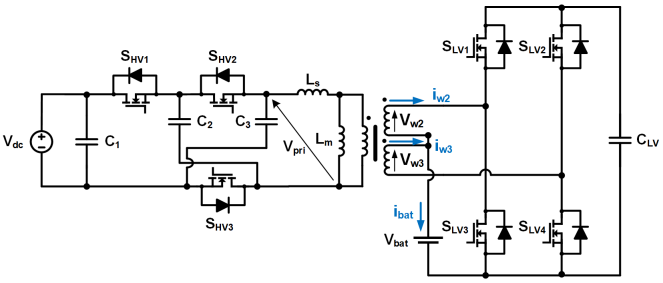

Fig. 1: Proposed topology with QSC circuit on high voltage side and transformer interleaved circuit on low voltage side.

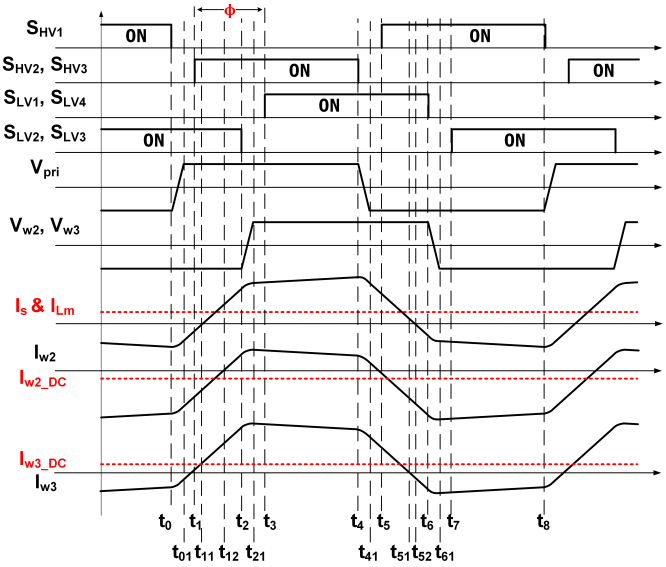

Fig. 2: Circuit operation waveform.

of S_{HV2} and S_{HV3}, as shown in Fig. 3 (1a). The equations for the resonant inductance current i_s and device S_{HV1} voltage v_{SHV1} can be derived as (1),(2) where C_{ossH} is the output capacitance of the high voltage side switching device, and $\omega_H = \frac{1}{\sqrt{3L_sC_{ossH}}}$.

After the output capacitances of S_{HV2} and S_{HV3} are fully discharged at t_{01}, the transformer primary winding current starts to flow through the body diode of S_{HV2} and S_{HV3}, as shown in Fig. 3(1b). The transformer primary winding current during ($t_{01} - t_1$) is derived as (3).

$$i_s(t) = -\sqrt{\frac{3C_{ossH}}{L_s}}\left(\frac{V_{dc}}{3} - 2NV_{bat}\right)\sin\omega_H(t-t_0) + I_{s(t_0)}\cos\omega_H(t-t_0) \tag{1}$$

$$v_{SHV1}(t) = -\sqrt{\frac{L_s}{3C_{ossH}}}I_{s(t_0)}\sin\omega_H(t-t_0) - \left(\frac{V_{dc}}{3} - 2NV_{bat}\right)\cos\omega_H(t-t_0) + \frac{V_{dc}}{3} - 2NV_{bat} \tag{2}$$

$$i_s(t) = I_{s(t1)} + \frac{V_{dc} + 6NV_{bat}}{3L_s}(t-t_1) \tag{3}$$

State 2($t_1 - t_2$): At t_1, high voltage side switch S_{HV2}, S_{HV3} are soft switched on. Switched capacitors C_2, C_3 are con-

nected in parallel with the transformer primary winding. The primary winding current i_s increases linearly derived as (3). At t_{11}, the primary winding current i_s changes the direction, as shown in Fig. 3(2b). Then at t_{12}, the secondary winding w_2 current i_{w2} changes direction, as shown in Fig. 3(2c).

State 3(t_2 – t_3): This state is the switching transient of the low voltage side transformer-interleaved circuit shown in Fig. 3(3a). At t_2, S_{HV2} and S_{HV3} are switched off. The transformer secondary winding current starts to charge the output capacitances of S_{LV2} and S_{LV3} and discharge the output capacitance S_{LV1} and S_{LV4}. The equations for the resonant inductance current i_s and device S_{LV1} voltage v_{SLV1}, can be derived in (4), (5). C_{ossL} is the output capacitance of the low voltage side switching device. I_{dc} is the dc offset current in QSC side and $\omega_L = \frac{N}{\sqrt{L_s C_{ossL}}}$.

$$i_s(t) = \sqrt{\frac{C_{ossL}}{L_s}}\left(\frac{V_{dc}}{3N} + 2V_{bat}\right)\sin\omega_L(t-t_2) + \left(I_{s(t_2)} - I_{dc}\right)\cos\omega_L(t-t_2) \; + I_{dc} \tag{4}$$

$$v_{SLV1}(t) = \sqrt{\frac{L_s}{C_{ossL}}}\left(\frac{I_{bat}}{4N} - \frac{I_{s(t_2)} - I_{dc}}{2}\right)\sin\omega_L(t-t_2) + \left(\frac{V_{dc}}{6N} + V_{bat}\right)\cos\omega_L(t-t_2) \; - \; \frac{V_{dc}}{6N} + V_{bat} \tag{5}$$

$$i_s(t) = I_{s(t_3)} - \frac{V_{dc} - 6NV_{bat}}{3L_s}(t-t_3) \tag{6}$$

State 4 (t_3 – t_4): At t_3, low voltage side switches S_{LV1} and S_{LV4} are soft switched on. There is no additional switching action. The current flow path is shown as Fig. 3(4). The resonant inductance current i_s can also be derived as (6).

For the circuit operation states 5 – 8 on another half of the period, the analysis is similar to those in states 1 - 4. Their voltage/current equations are shown in TABLE I.

D. Circuit Power Transfer Control

Due to the operation similarity between transformer-interleaved circuit and H-bridge circuit topology. The power transfer control of the circuit can be implemented with phase shift control. The phase shift angle ϕ is defined between the QSC side circuit S_{HV2} and transformer-interleaved circuit S_{LV1}. When the switching PWM deadtime is not considered, and the circuit power loss neglected. The phase shift operation for this circuit can be described as (7).

$$P = \frac{n\, V_{dc} V_{bat}\varphi(\pi - |\varphi|)}{3\pi^2 f L_s} \tag{7}$$

III. Circuit Design and Optimization

In this section, circuit design, optimization guideline will be illustrated. Considering the scenario with a 24-V nominal voltage rating battery connected to the low voltage side. A 400-V/20-33.3-V, 1000-W prototype is designed to present the performance of the proposed circuit topology. The battery side voltage ranges from 20 V to 33 V with nominal value of 24 V. In this design case, a power loss oriented circuit design process is performed.

A. Circuit Design Key Parameters

The converter design key parameters include switching frequency, transformer turns ratio, transformer winding structure and resonant inductance. The overall design target is to minimize the overall converter power loss given a load profile with weighted load condition within -1000-W to 1000-W range. Negative transferring power meaning the power flow through battery side to high voltage side.

1) Transformer turns ratio: With 133 V on transformer primary side and 24 V on transformer secondary side, the ideal transformer turn ratio is 5.5:1:1. Cases with more than two turns of secondary side windings are not considered. Fractional turns ratio is excluded as well. Hence, several discrete transformer turns ratios are included: 6:1:1, 5:1:1, 9:2:2 and 4:1:1.

2) Switching frequency: Switching frequency impacts the magnetic components dimensions, soft switching region and thus circuit switching loss. The design is targeting at the full range of load conditions. Three typical switching frequencies are selected: 300-kHz, 500-kHz, 1-MHz.

3) Resonant inductance: In practical design, planar transformer has a high coupling coefficient. Thus, the small leakage inductance functions as the resonant inductance and increases the control difficulty. An external inductor is designed and works as resonant inductance in a combination with transformer leakage inductance. The resonant inductance range can be calculated as (8),(9). The maximum phase shift angle is assumed as 70° at full load condition.

$$L_{s\_max} = \frac{NV_{pri\_min}V_{\text{sec}\_min}}{2\pi^2 f_{sw} P_{max}} \frac{\varphi_{max}(\pi - \varphi_{max})}{\pi} \tag{8}$$

$$L_{s\_min} = \frac{NV_{pri\_max}V_{\text{sec}\_max}t_{min}(1 - 2f_{sw}t_{min})}{\pi P_{min}} \tag{9}$$

B. Circuit Design Guideline and Trade-off

The final circuit parameters were selected based on two factors: weighted power loss and worst-case device loss. Weighted power loss is the indicator of the circuit efficiency at different load and voltage conditions. The worst-case device loss will decide the cooling requirements of the converter and thus affect the power density. Weighted power loss equation is shown as (10).W_p and W_v indicate the weights of different operation conditions.

$$P_{loss\ wt} = \sum_i \sum_j W_p(i)\, W_v(j)\, P_{loss}(N, f_{sw}, L_s, P_i, V_{bat,j}) \tag{10}$$

C. Magnetic Components

Switching frequency and transformer turns ratio are two key parameters in designing this transformer. With selected turns ratio and switching frequencies, the summarized circuit loss are shown in TABLE II. Two cases are considered as the final circuit parameters: 6:1:1 at 300 kHz and 9:2:2 at 300 kHz.

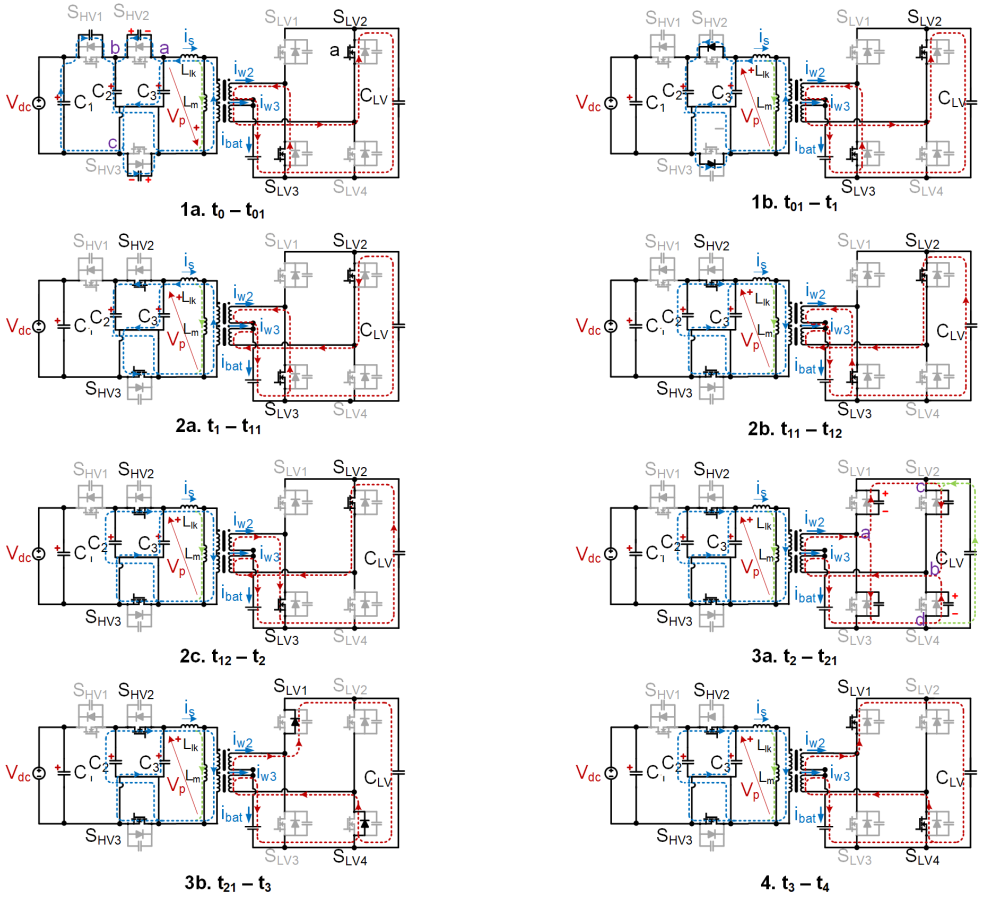

Fig. 3: Circuit operation states from t_0 to t_4.

TABLE I: Voltage/Current Equations of State 5 – 8

State	Duration	Equations
State 5	$t_4 - t_5$	$i_s(t) = \sqrt{\frac{3C_{ossH}}{L_s}}\left(\frac{V_{dc}}{3} - 2NV_{bat}\right)\sin\omega_H(t-t_4) + I_{s(t4)}\cos\omega_H(t-t_4)$ $v_{SHV1}(t) = -\sqrt{\frac{L_s}{3C_{ossH}}}I_{s(t4)}\sin\omega_H(t-t_4) + \left(\frac{V_{dc}}{3} - 2NV_{bat}\right)\cos\omega_H(t-t_4) + \frac{V_{dc}}{3} + 2NV_{bat}$
State 6	$t_5 - t_6$	$i_s(t) = I_{s(t5)} - \frac{V_{dc}+6NV_{bat}}{3L_s}(t-t_5)$
State 7	$t_6 - t_7$	$i_s(t) = -\sqrt{\frac{C_{ossL}}{L_s}}\left(\frac{V_{dc}}{3N} + 2V_{bat}\right)\sin\omega_L(t-t_6) + \left(I_{s(t6)} - I_{dc}\right)\cos\omega_L(t-t_6) + I_{dc}$ $v_{SLV1}(t) = \sqrt{\frac{L_s}{C_{ossL}}}\left(\frac{I_{bat}}{4N} - \frac{I_{s(t6)}-I_{dc}}{2}\right)\sin\omega_L(t-t_6) - \left(\frac{V_{in}}{6N} + V_{bat}\right)\cos\omega_L(t-t_6) + \frac{V_{in}}{6N} + V_{bat}$
State 8	$t_7 - t_8$	$i_s(t) = I_{s(t7)} + \frac{V_{dc}-6NV_{bat}}{3L_s}(t-t_7)$

When the transformer turns ratio is 9:2:2 and the switching frequency is 300 kHz, the weighted power loss is minimum, but the worst-case device losses are high. This is because the power loss distribution at different load conditions and battery voltages are highly non-uniform. As a result, the case with turns ratio of 6:1:1 and switching frequency of 300 kHz is selected.

The transformer design is implemented with ER32/6/25 – 3F36 ferrite core. The transformer winding is built with four identical PCB boards. Each PCB board has four layers with 4 oz copper thickness. The primary side and secondary side windings are interleaved to reduce the winding ac resistance. The planar inductor design is implemented with EQ25/LP – 3F35 ferrite core. The inductor winding has 4 layers of PCB to be integrated with planar transformer on the same PCB boards.

D. Optimization results

Weighted power loss and worst-case device loss at different resonant inductance Ls values are shown in Fig. 4. It can be seen that increasing resonant inductance Ls can have a lower weighted power loss. The impact of the resonant inductance

TABLE II: Weighted power loss and worst-case device loss

Turns Ratio	f_{sw}	Weighted P_{loss}	HV P_{loss}	LV P_{loss}
6:1:1	300 kHz	13.43 W	10.23 W	11.83 W
	500 kHz	16.14 W	11.14 W	11.83 W
	1000 kHz	23.34 W	16.16 W	11.83 W
5:1:1	300 kHz	15.51 W	12.27 W	15.01 W
	500 kHz	13.43 W	12.27 W	15.01 W
	1000 kHz	16.58 W	12.27 W	14.01 W
9:2:2	300 kHz	15.51 W	12.27 W	15.01 W
4:1:1	300 kHz	11.86 W	16.37 W	25.89 W

change on the worst case device power loss is limited. So the resonant indutance Ls value is selected as 6 µH. The converter efficiency is calculated as shown in Fig. 5. The efficiency at full load conditions (±1000 W) and nominal dc bus and battery voltages is above 98%.

IV. Simulation Verification, Prototype Design and Experimental Results

A. Simulation Verification

A PLECS simulation model was built to verify the circuit analysis. Simulation model main parameters are listed in TABLE III. On the battery side of the simulation model, a pure resistive load is connected. Fig. 6 shows the circuit simulation waveforms at 1 kW. In the simulation waveform, voltage stress on transformer primary side is 1/3 of the input voltage. On secondary side windings, each winding has a voltage stress of

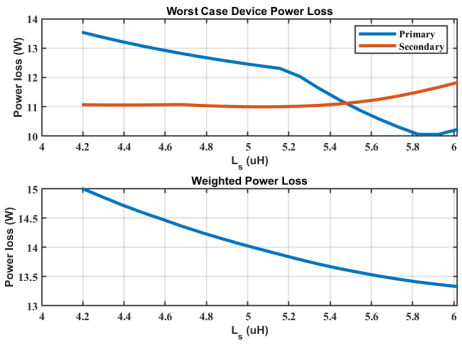

Fig. 4: Weight converter power loss and worst-case device power loss.

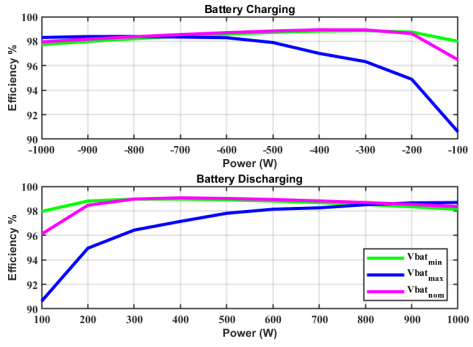

Fig. 5: Weight converter power loss and worst-case device power loss.

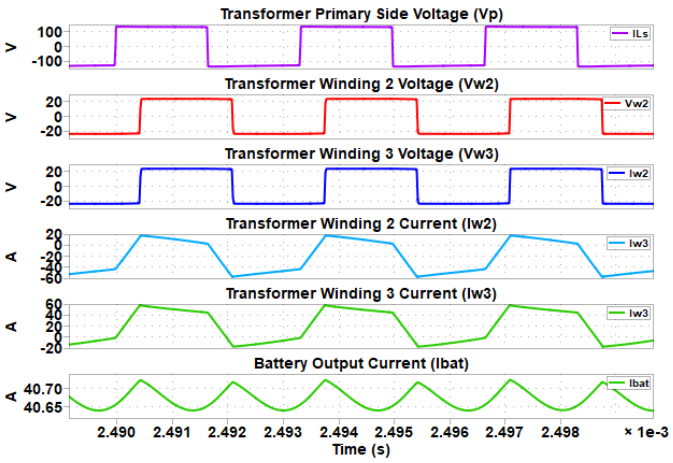

Fig. 6: Weight converter power loss and worst-case device power loss.

24 V. DC offset current can be found in transformer primary and secondary side windings. DC offset current in secondary side windings has same value but different directions. Current ripple in transformer secondary side windings cancelled with each other at the battery output side, which is consistent with the results described in circuit analysis.

TABLE III: Simulation Model Main Parameters

Parameter	Variables	Values
DC input/battery voltages	V_{in}/V_{bat}	400 V/24 V
Switching frequency	f_{sw}	300 kHz
Transformer turns ratio	N	6:1:1
Inductance	L_m/L_s	64 µH/ 6 µH
Switched capacitor	C_2/C_3	5 µF

B. Circuit Prototype and Test Setup

To verify the circuit analysis and simulation results, a 1-kW 400-V/20 - 33-V QSC transformer interleaved converter prototype is built, with 650-V GaN System GS66506T on QSC side, 100-V EPC2022 on low voltage side. The prototype 3D rendering model is shown in Fig. 7. Its overall size was 130 mm x 74 mm x 53 mm. Fan integrated heatsinks are implemented on QSC side and low voltage side for cooling. The 6:1:1 planar transformer was built with two ER32/6/25 - 3F36 cores. A 2.7-mil air gap was applied, resulting in a magnetizing inductance of 36 µH. The planar inductor was built with two EQ25/LP - 3F35 cores. 5.8 µH inductance was achieved with a 5.4-mm air gap. For the switched capacitor, two 450-V rating, 2.2-µF capacitors was connected in parallel to give 3 µF in 133-V DC bias condition. On the low voltage side capacitor, two 100-V. 22-µF capacitors are connected in parallel.

For the test setup, the input power was from a Magna dc power supply. Battery side load was a resistive load bank. The controller card was Ti TMDSCNCD28379D.

C. Experimental Results

The prototype in working is shown in Fig. 8. The QSC side circuit with transformer has been tested in light load condition.

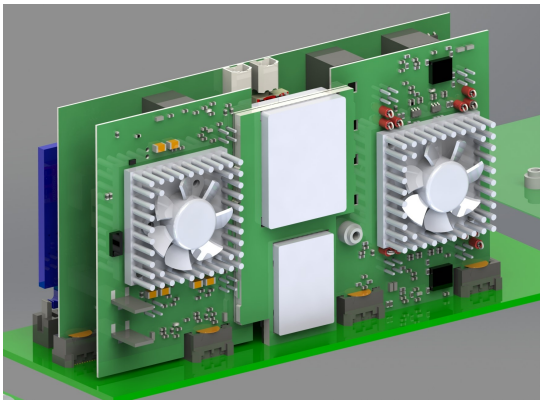

Fig. 7: 3D rendering prototype assembly.

Transformer secondary side is connected to a 6-Ω resistor to verify the QSC side circuit and transformer design. Test results are presented in Fig. 9 and Fig. 10.

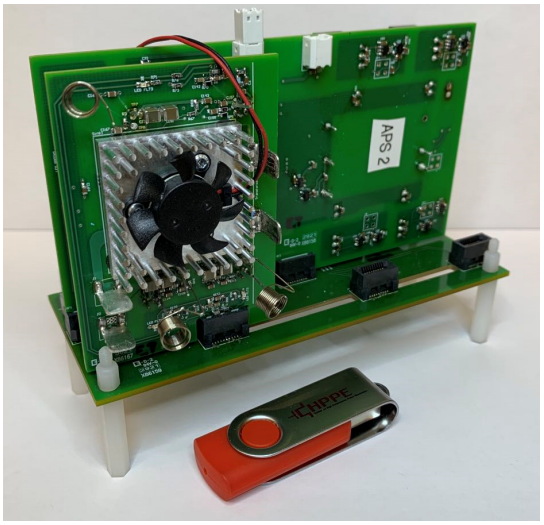

Fig. 8: Prototype in construction.

V. Conclusion

The operation principle, circuit operation states analysis, design guideline and circuit optimization of the proposed high conversion ratio dc/dc converter are presented. The simulation and test results verify the analysis. The high voltage side of the converter has a QSC circuit which provides 3:1 step down ratio and reduced voltage stresses on switching devices. Low voltage side transformer interleaved circuit provides a 2:1 step-down ratio and output current ripple cancellation. A 1-kW, 300-kHz, 400-V/24-V circuit prototype is current under construction. Preliminary test results are shown. More detailed experimental results will be presented in the follow-up paper.

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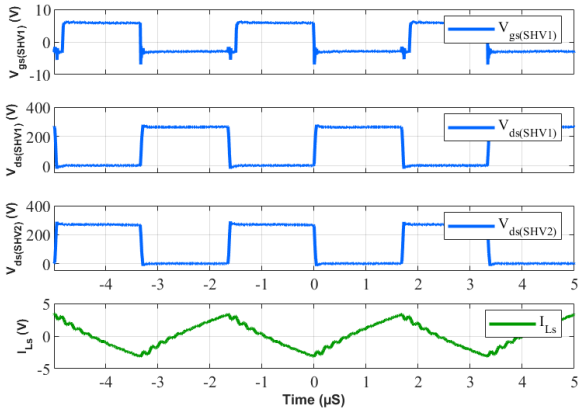

Fig. 9: Test waveform at light load condition.

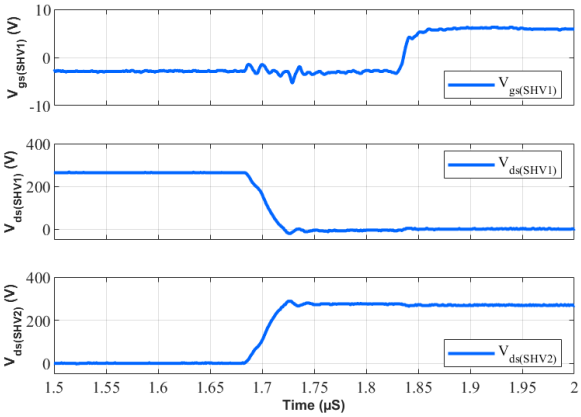

Fig. 10: Zoomed test waveform at light load condition.

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