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A Comparative Study of SiC JFET Super-Cascode Topologies

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***Abstract*—In spite of several advantages of SiC JFETs over enhancement mode SiC MOSFETs, the intrinsic normally-ON characteristic of the JFETs can be undesirable for many industrial power conversion applications due to the negative turn-OFF voltage requirement. This prevents normally-ON JFETs from being widely accepted in industry. However, a cascode configuration, which uses a low voltage (LV) Si MOSFET can be used to enable a normally-OFF behavior, making this approach an attractive solution to utilize the benefits of SiC JFETs. For medium-, and high-voltage applications that require larger blocking voltage than the rating of each JFET, additional devices can be connected in series to increase the overall blocking voltage capability, creating a super-cascode configuration. This paper provides a review of several super-cascode topology variations and presents a comprehensive comparative study, evaluating similarities and differences in operating principles, equivalent circuits, and design considerations and limitations.**

***Index Terms*—silicon carbide (SiC) junction field-effect transistor (JFET), wide-bandgap (WBG), medium voltage (MV), cascode, super-cascode, super cascode, cascaded switch**

I. Introduction

Wide-bandgap (WBG) semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN) have demonstrated superior performance in terms of efficiency, power density, and high-voltage-blocking capability [1] – [3]. In exploit of the WBG materials, different SiC-based power semiconductor device structures, such as lateral or vertical junction-gate-field-effect transistors (JFET) and planar and trench metal-oxide-field-effect transistors (MOSFET) have been manufactured for power applications [4] – [6]. SiC JFETs and MOSFETs are commercially available with voltage ratings in low kV range [7] – [8]. Due to the design convenience and safety with normally-OFF devices, the enhancement mode has been the preferred device structure over the depletion mode. However, SiC JFETs can provide distinct benefits over SiC MOSFETs in terms of smaller input and Miller capacitances, lower ON-resistance from high-channel density, long-term stability of the pinch-OFF voltage at elevated temperatures, and increased ruggedness and reliability from the absence of a gate-oxide layer [9] – [13].

Though JFETs are depletion type transistors, the normally-ON behavior can be overcome using a cascode configuration, which consists of a low-voltage (LV) silicon (Si) MOSFET along with a JFET, as shown in Fig. 1(a). The cascode configuration operates by biasing the gate and source terminals of the Si MOSFET; if a small voltage-drop across the ON - resistance ($R_{M,ds(on)}$ of the Si MOSFET) is discounted, the conduction mode of the cascode is achieved by essentially creating a short between the gate and source terminals of the JFET. In contrast, the blocking mode is realized by biasing the drain-source voltage of the Si MOSFET to a level lower than the JFET's pinch-OFF voltage, V_{po}.

As for applications that require a large blocking voltage, one way to meet the desired voltage requirement is to connect an appropriate number of SiC JFETs in series, controlled by a LV Si MOSFET through the cascode configuration. This is known as a super-cascode (SC) circuit, which has been proposed and evaluated in [14] – [15] for medium- and high-voltage (HV) applications. Such a circuit construction is shown in Fig. 1(b) with additional JFETs, J_2 and J_3 connected in series to the cascode configuration of J_1 and M. Moreover, to ensure the static and dynamic balancing, a balancing network is required, which is composed of a combination of diodes, resistors, and capacitors. There are several examples of balancing networks and these are presented and further analyzed in the following sections. However, for the context of introducing the super-cascode concept, the balancing network is represented as a block diagram and the intricacies of different balancing circuits

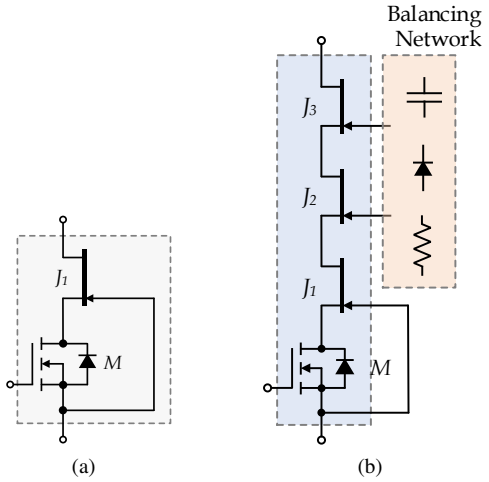


Fig. 1. Circuit schematic of (a) a cascode connection of a SiC JFET with a LV Si MOSFET, and (b) a super-cascode with multiple SiC JFETs with an arbitrary balancing network for static and dynamic balancing.

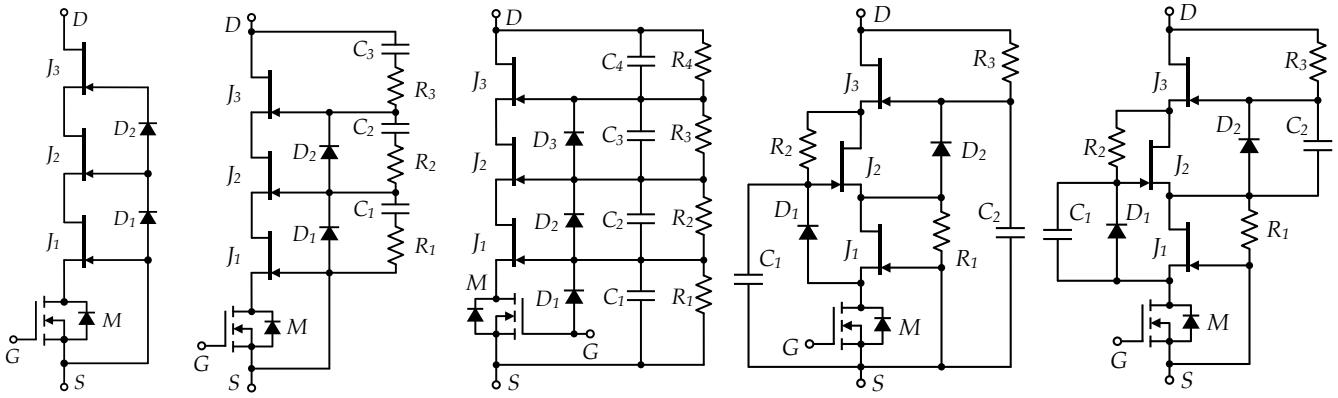


Fig. 2. Circuit topology progression and comparison of SC structures: (a) SC1 [14], (b) SC2 [15] – [16], (c) SC3 [23], (d) SC4 [30], and (e) SC5 [34].

have been omitted in Fig. 1(b).

The super-cascode configuration is a simple, low-cost solution to designing a HV chopper as it only requires a network of passive balancing elements and a single gate driver, potentially reducing power density and control complexity. Because the configuration requires auxiliary elements for balancing of voltage distribution across multiple power devices, a balancing network becomes an essential, yet challenging design task to ensuring safe operation of the super-cascode. Hence, the main objective of this paper is to present a comprehensive summary of different super-cascode topologies; analysis of the operating principles with equivalent circuits, the dynamic and static balancing behaviors, and evaluation of the design parameters and unique challenges associated with each super-cascode topology are examined and discussed.

II. Review of Super-Cascode Circuit Topologies

Based on a thorough literature search, there is a number of well-established ways to stack multiple SiC JFETs in the super-cascode configuration. The references related to [14], [15], [23], [30], and [34] are the five exemplars of super-cascode topology variations selected for comparison. There are also a few other super-cascode derived examples that propose techniques to solve the unique challenges associated with this circuit structure, such as controlling leakage current, thermal distribution, voltage rise and fall timing, and distribution of blocking voltages during transient and steady-state [17] – [19], [24], and [31].

Fig. 2 illustrates five slightly varied super-cascode circuit topologies, $SC1$ – $SC5$, corresponding to Fig. 2(a) – Fig. 2(e), respectively; these five circuit structures use appropriate number of SiC JFETs along with passive and/or active elements to build a HV super-cascode chopper. Fig. 2(a), introduced in [14], is documented as one of the early designs and constructions of the super-cascode configuration. An 8 kV switch was developed by cascading four 3 kV rated vertical JFETs along with a 55 V rated Si MOSFET and three additional 2.2 kV avalanche diodes. This topology is simple to build and requires only JFETs and avalanche diodes that connect the gate terminals of the JFETs. However, the selection of the JFET-diode pair is crucial as the clamping voltage is predetermined by the diode avalanche breakdown bias point.

Biela et al. [15] – [19] describe a couple of methods to control the dynamic balancing of the voltage distribution of the JFETs in the cascode or super-cascode structure. As illustrated in Fig. 2(b), the passive snubber elements consist of resistors and capacitors, which improve the turn-ON and turn-OFF dynamic transients of the JFETs. The avalanche diodes are still employed to clamp the voltage of the JFETs' gate to gate terminals, biasing the drain terminals of the JFETs. Biela et al. [15] – [16] developed a 5 kV switch with five 1.5 kV, 5 A SiC JFETs along with 1.3 kV avalanche diodes and a 55 V LV Si MOSFET. This topology provides a methodology for controlling the dynamic voltage balancing of the JFETs, but controlling the leakage current during the blocking state remains a challenging task, leading to thermal distribution imbalance in the package [20] – [21].

Fig. 2(c) shows the topology presented in [22] – [23], which proposes a slight modification to the balancing network from Fig. 2(b) of [15] – [16]. For instance, the circuit proposed in [23] uses a SiC MOSFET for the cascode device rather than a LV Si MOSFET, which conceptually distributes the voltage evenly in all FETs, including the bottom control cascode device. Zhang et al. [25] utilizes all SiC MOSFETs in the same manner as in [23] to build a 7.2 kV, 60 A switch. To enhance the steady-state balancing during the OFF state, the balancing resistors, denoted as R_1 – R_4 in Fig. 2(c), are added in parallel to the dynamic balancing capacitors, C_1 – C_4. This topology is advantageous in terms of equal voltage sharing across all devices, thus improving the switching and thermal stresses. Furthermore, by using a SiC MOSFET with the same rating as the JFETs, one less HV JFET is needed compared to the rest of the super-cascode topologies.

Nonetheless, designing the super-cascode with higher blocking voltage and high efficiency can be challenging as the balancing resistors can increase the overall power loss with

increasing blocking voltage. To counteract the loss, the resistor values can be increased, but this can result in unequal distribution of leakage currents, leading to voltage imbalance in the HV transistors. A novel resistor balancing network is proposed in [24], adding an additional path for the leakage currents to flow, lowering the OFF-state power loss while maintaining the voltage balancing even at high voltage.

Fig. 2(d) shows another super-cascode topology with every other JFET staggered. The circuit topology is introduced and studied in [27] – [33]. Like many super-cascode designs, the topology uses a LV Si MOSFET and clamping diodes (D_1 – D_4) to limit the voltage stress of each JFET, the balancing capacitor network (C_1 – C_4) and the resistor network (R_1 – R_4) are used in a similar fashion to control the dynamic and static behaviors of the super-cascode. However, the main difference from $SC1$ – $SC3$ in Fig. 2(a) – (c) is that the balancing capacitor charging paths are different, causing different dynamics of the charging and discharging behaviors and resulting in unique equivalent circuits during transients. A limitation to this topology is that the balancing capacitors are referenced to the source of the LV Si MOSFET; with sufficiently large blocking voltage, e.g. >10 kV, the selection of the capacitors can be challenging in terms of volume and availability as the capacitance is inversely proportional to voltage potential. In addition, it can also be difficult to find the right form-factor capacitors for high power density designs. However, one theoretical advantage of $SC4$ is that the steady-state balancing is achieved with two leakage paths, leading to a better management of the leakage current and voltage balancing in the the OFF-state. In practice, though, the design process involves laborious steps to properly adjust values of the balancing network to limit while balancing the leakage currents.

Fig. 2(e) shows a modified version of $SC4$ with the balancing capacitors connecting between the gates of every other JFETs [34] (similar to $SC2$ – $SC3$) rather than being tied to the source of the LV Si MOSFET. With this modification, the requirement of the voltage rating of the balancing capacitors is greatly reduced from that of $SC4$ while conserving the benefit of having two leakage current paths in $SC4$.

There are other super-cascode based circuits besides the topologies introduced. For instance, Table I summarizes a variety of the super-cascode configurations based HV modules found in literature. The table provides the authors claimed voltage and current ratings of the modules as well as the specific HV devices used to construct the module along with the devices' specifications and manufacturers. It can be noted that many have demonstrated large blocking voltage capability, much higher than the rating of a single SiC JFET device, 1.2 or 1.7 kV.

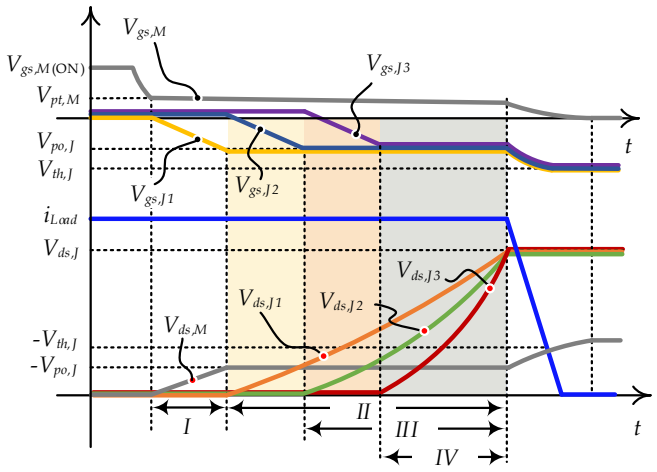


Fig. 3. Turn-OFF timing diagram of a super-cascode, describing *Interval I*, LV Si MOSFET delay time, *Interval II*, J_1 blocking voltage rise time, *Interval III*, J_2 blocking voltage rise time, *Interval IV*, J_3 blocking voltage rise time.

III. Circuit Analysis of Super-Cascode Topologies

The fundamental principles of the sequential cascaded operation are the same across all super-cascode topologies. There are different ways to implement the static and dynamic balancing networks between the five versions, and each distinct balancing mechanism results in different equivalent circuits. Therefore, the design considerations vary from one topology to another.

However, there are largely two separate underlying operation theories that are shared amongst the super-cascode designs. For the static balancing techniques, $SC1$ and $SC2$ share the same concept of utilizing only the avalanche diodes to bias the balancing voltage while $SC3$, $SC4$, and $SC5$

TABLE I
Literature Review of Super-Cascode Applications and Device Comparison

Super-Cascode (SC)	**Topology**	**SC Total Rated Voltage & Current**	**HV Device Manufacturer & Part #**	**Single HV Device Rating & # of Devices**
Stacked HV SiC VJFETs [14]	$SC1$	8 kV, 10 A	SiCED GmbH & Co.KG, N/A	3-4 kV, 10 A, 55 mΩ, 4
ETH Pulsed-Power SiC JFET [15]	$SC2$	5 kV, 5 A	SiCED GmbH & Co.KG, N/A	1.2 kV, 5 A, N/A, 6
NCSU FREEDM Super-Cascode [23]	$SC3$	15 kV, 40 A	United SiC, UJN1205K3	1.2 kV, 38 A, 45 mΩ, 11
NCSU FREEDM Super-Cascode 2 [21]	$SC2$	6.5 kV, 100 A	United SiC, UJ3N1701Z	1.7 kV, 100 A, 6mΩ, 6
Austin SuperMOS [25] – [46]	$SC3$	7.2 kV, 60 A	CREE/Wolfspeed, C2M0025120D	1.2 kV, 63 A, 25 mΩ, 6
WEMPEC SiC JFET Super-Cascode [36]	$SC2$	12 kV, 20 A	United SiC, UJN1208K	1.2 kV, 21 A, 80 mΩ, 12
OSU SiC JFET Super-Cascode [30]	$SC4$	4.5 kV, 40 A	United SiC, UJN1205K	1.2 kV, 38 A, 45 mΩ, 5
UnitedSiC SiC JFET Super-Cascode [34]	$SC5$	40 kV, 1 A	United SiC, UJN171K0Z	1.7 kV, 1 A, 80 mΩ, 30
UnitedSiC SiC JFET Super-Cascode [35]	$SC4$	4.5 kV, 40 A	United SiC, UJN1205Z	1.2 kV, 38 A, 45mΩ, 5
SNL Cascaded SiC JFETs [24]	$SC3$	3.5 kV, 60 A	United SiC, UJ3N120035K3S	1.2 kV, 63 A, 35 mΩ, 4

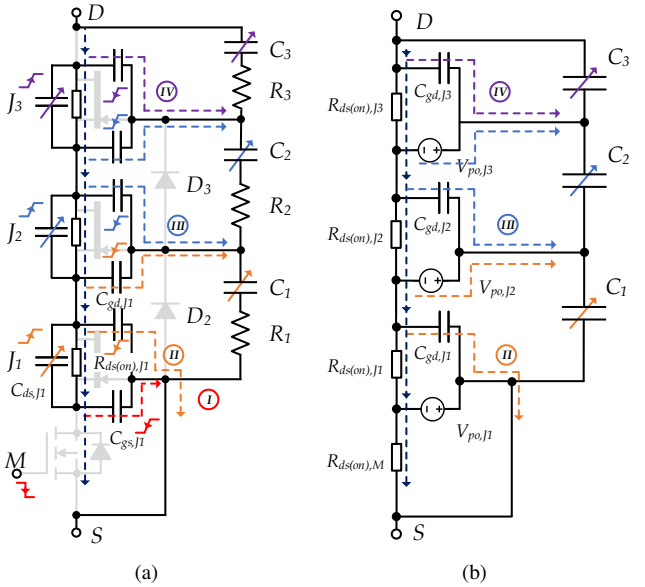


Fig. 4. Circuit schematic of $SC2$, illustrating: (a) turn-OFF current paths corresponding intervals in Fig. 3 with charging and discharging of parasitic junction capacitances, and (b) turn-OFF transient equivalent circuit during *Interval* $II - IV$.

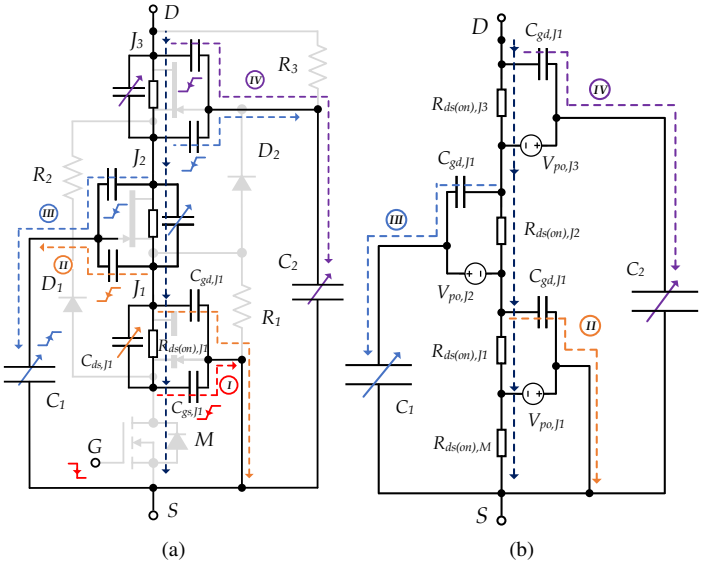


Fig. 5. Circuit schematic of $SC4$, illustrating: (a) turn-OFF current paths corresponding intervals in Fig. 3 with charging and discharging of parasitic junction capacitances, and (b) turn-OFF transient equivalent circuit during *Interval* $II - IV$.

employ resistor networks to balance the steady-state voltage. For the dynamic balancing analysis, $SC2$ – $SC5$ share the same concept of using the balancing capacitors to control the charging and discharging of the total gate charge, Q_g of the JFETs. The charging and discharging paths of the capacitors in $SC2$, $SC3$, and $SC5$ are different from those of $SC4$. Due to the distinct differences in the capacitor charging paths, $SC2$ and $SC4$ have been selected to compare in the circuit analysis through equivalent circuits during turn-OFF transient.

Fig. 3 shows the time intervals $(I - IV)$ of the gate-source voltages ($V_{gs,Ji}$ for JFET i and $V_{gs,M}$ for the Si MOSFET), the drain-source voltages of the bottom MOSFET ($V_{ds,M}$), and the cascaded JFETs ($V_{ds,Ji}$) during the turn-OFF transition. The Si MOSFET starts turning OFF at the applied gate voltage, $V_{gs,M(ON)}$ until the plateau point, $V_{pt,M}$. During this time, the MOSFET drain voltage is applied to the gate of J_1 and drives the gate-source potential up until the JFET pinch-off voltage, $V_{po,J}$. J_1 starts turning OFF and the drain voltage starts to increase (*Interval* II), which in turn decreases the gate voltage of J_2 to $V_{po,J}$. J_2's drain voltage starts to increase during *Interval* III. The following JFETs, J_{i+1} follow the same procedure in sequence until the equal balancing is achieved. Then the load current, i_{Load} starts to decrease when the gate terminals of the JFETs reached the threshold voltage, $V_{th,J}$.

The diagram for the turn-ON transition is not included in this paper as it is the opposite process of the turn-OFF transition, though the proper equations for the time intervals are not exactly interchangeable.

Fig. 3 shows generalized waveforms for a super-cascode. The exact turn-ON and -OFF times as well as the design parameter values differ from one topology to another. Fig. 4(a) shows the junction capacitor charging paths and Fig. 4(b) illustrates the equivalent circuits during the turn-OFF process for $SC2$. Note that the current path numbers defined in Fig. 4 are equivalent to the time intervals $(I - IV)$ in Fig. 3.

Fig. 4(a) describes the discharging of the gate-source capacitance of J_1, denoted as $C_{gs,J1}$ during *Interval* I. This is after the MOSFET, M has been turned OFF and blocks the gate-source voltage of J_1 until the $V_{gs,J1}$ reaches its pinch-OFF voltage. At pinch-OFF, the JFET starts to charge the output capacitance, $C_{oss,J1}$ while simultaneously charging the balancing capacitor, C_1, increasing the drain-source voltage of J_1 at the onset of *Interval* II.

The drain node of J_1 is tied to the source terminal of J_2 and therefore, a voltage increase in the drain of J_1 results in a decrease in the voltage potential of the gate-source voltage J_2 until its pinch-OFF voltage is reached at *Interval* III. The drain-source voltage of J_2 starts to increase in the same manner as J_1 while charging C_2 and C_1. The last JFET, J_3 also follows this sequential turn-OFF progression until the voltage balancing has reached its equilibrium.

Fig. 4(b) shows the combined equivalent circuit within the time interval II and IV. Note that the specific equivalent circuit to each interval can be derived easily based on the time interval of interest. Based on the equivalent circuit and under the assumption that the charge balance applies between the total gate charge, Q_g of a JFET and the balancing capacitors, (1) can be derived.

$$C_i = Q_g(V_{ds,J})/V_{ds,J} \times (n - i + 1), 1 \leq i \leq n. \quad (1)$$

Note that the total gate charge, $Q_g(V_{ds,J})$ is expressed in terms of the blocking voltage of the device where $V_{ds,J}$ is

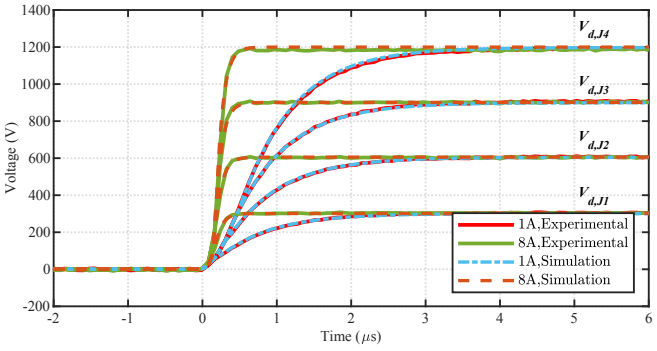
the ideal distributed blocking voltage for each JFET. n is the required number of JFETs to withstand the source voltage.

The same principle applies to $SC4$; Fig. 5(a) shows the turn-OFF current paths of $SC4$ specific to time intervals notated in Fig. 3. When the MOSFET is turned OFF, J_1 starts to turn OFF by discharging the gate current up until the pinch-OFF voltage level or *Interval I*. J_1 gate-drain junction capacitance starts to charge, pulling down the source potential node of J_2 during *Interval II*. This results in discharging the gate current through J_2, eventually leading to the charging of the output junction capacitance as well as C_1. The upper JFETs follow the same successive charging and discharging current paths as the lower JFETs.

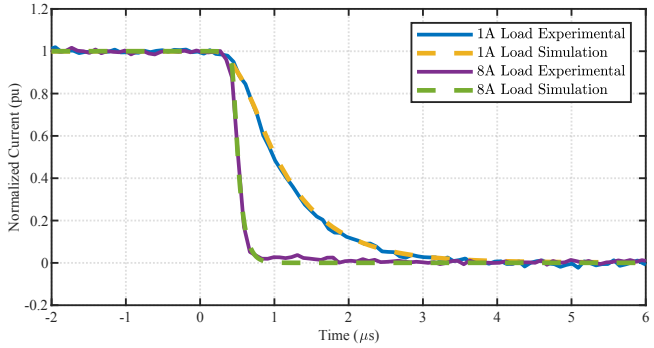
Fig. 5(b) shows the combined equivalent circuit between intervals II through IV for $SC4$. Note that the specific equivalent circuit to each interval can be derived easily based on the time interval of interest. Based on the equivalent circuit and under the assumption that the charge balance applies between the output capacitances of the JFETs and the balancing capacitors, (2) can be derived.

$$C_i = Q_g(V_{ds,J})/[(V_{ds_J}) \times (1+i)]. \tag{2}$$

Based on the derived capacitance values using (1), a modified $SC3$ topology has been design and developed using four 1.2 kV SiC JFETs. Fig. 6(a) shows the experimental results of the voltage balancing across the JFETs versus the simulation results at different load current levels. In addition, Fig. 6(b) illustrates the matching load current behaviors at turn OFF between the experimental data and the simulation. The comparable results between the experiments and the simulation studies can be used to demonstrate the validity of the equations based on the derived equivalent circuit models.



(a)



(b)

Fig. 6. Experimental results of a modified $SC3$: (a) turn-OFF drain voltages of $V_{d,J1}$ – $V_{d,J4}$ for 1A and 8A and (b) load current turning-OFF for 1A and 8A.

IV. Evaluation of Super-Cascode Design Parameters

Table II describes the rating of the design difficulty in various design aspects, including circuit design, static and dynamic balancing, and layout. The rating for each category is relative from one topology to another. Moreover, based on the observation and analysis of each super-cascode topology, the unique advantages and limitations have been documented and can be used for further design considerations and evaluation.

As briefly described in Section *Section III*, $SC1$, $SC2$, $SC4$, and $SC5$ require careful selection of the avalanche diodes as the operation of the super-cascode depends on the breakdown voltage of the clamping diodes, ultimately distributing the voltage across the HV switches. Hence, the voltages across the JFETs, capacitors, and diodes depend on the breakdown rating of the diode, V_{BR}. This is a design parameter that requires careful selection of breakdown diodes

TABLE II
Super-Cascode Design Parameters and Considerations Comparison

Topology	**MOSFET Stress,** $V_{ds,M}$	**JFET Stress,** $V_{ds,J}$	**Cap. Stress,** V_{C_i}	**# of HV Switches**	**Total # of Components**	**SC Rating**
SC1	$-V_{th,J}$	$\begin{cases} V_{BR} \text{ for } J_1 - J_{n-1} \\ V_{DC} - (n+1)V_{BR} + V_{th,J} \text{ for } J_n \end{cases}$	N/A	n	$2n$	$nV_{ds,J}+V_{th,J}$
SC2	$-V_{th,J}$	Same as SC1	V_{BR}	n	$3n$	$nV_{ds,J}+V_{th,J}$
SC3	$V_{DC}/(n+1)$	$V_{DC}/(n+1)$	V_{BR}	$n+1$	$4n+1$	$nV_{ds,J}+V_M$
SC4	$-V_{th,J}$	$V_{BR}-V_{th,J}$	$i(V_{BR}-V_{th,J})$	n	$4n-1$	$nV_{ds,J}+V_{th,J}$
SC5	$-V_{th,J}$	$V_{BR}-V_{th,J}$	V_{BR}	n	$4n-1$	$nV_{ds,J}+V_{th,J}$

V_{DC} is the total operating voltage of super-cascode
V_{BR} is the avalanche breakdown voltage of the diodes
$V_{th,J}$ is the threshold voltage of the JFETs
n is the required number of JFETs

TABLE III
SUPER-CASCODE CIRCUIT DESIGN DIFFICULTY RATING AND ADVANTAGES AND LIMITATIONS COMPARISON

Topology	Overall Circuit Design	Static Balancing Design	Dynamic Balancing Design	Layout Design	Advantages & Limitations
SC1	●	♦	♦	●	• Easy circuit design with minimal number of components required • Difficult to control dynamic and static balancing • Bias voltage is leakage current dependent
SC2	■	♦	■	■	• Moderate difficulty rated circuit design • Requires design selection of RC damping network for dynamic balancing • Bias voltage is leakage current dependent
SC3	■	■	■	■	• LV Si MOSFET replaced with a SiC MOSFET, requiring one less JFET • Potential reliability and robustness issue with SiC MOSFET • Less restriction on the selection of the avalanche diodes
SC4	♦	■	♦	♦	• Better leakage current control • PCB board or module layout can be difficult due to the balancing capacitors • High voltage rated capacitors are required
SC5	♦	■	■	■	• Hybrid of static balancing from $SC4$ and dynamic balancing from $SC2$. • High voltage capacitors are not required • High component counts

Legend: ● easy, ■ moderate, ♦ difficult

that evenly distribute the voltage across the HV switches and prevent over-voltage stress.

In reality, selecting the diodes with the same breakdown rating as V_D/n can be challenging if the blocking voltage is changing or an odd number and thus the top JFET will see the leftover voltage from the lower diodes. On the other hand, the $SC3$ eliminate the need for the avalanche diodes for the steady-state voltage hold-OFF and they can be placed for preventive and protection purposes.

The combination of the gate leakage current and the reverse leakage current from the diode avalanche breakdown mechanism can be controlled by the balancing resistors, R_1 – R_4 in $SC1$, $SC2$, and $SC3$. However, excessive leakage can cause a steady-state voltage imbalance and thermal stress, which becomes more prominent when the super-cascode is in the blocking stage for a long period of time (in ms range or longer). This issue is less susceptible for $SC4$ and $SC5$ as the leakage current takes two separate paths: one path through even numbered R_n and another through odd numbered R_n balancing resistors.

Lastly, the selection of the balancing capacitors can be more challenging for certain super-cascode topologies over others. Because the capacitance is inversely proportional to voltage potential, designing super-cascodes that require a large voltage rating of the capacitors, like $SC4$ can be challenging.

To further quantify the differences stated in Table I, Table II compares each super-cascode topology in terms of the voltage stress on the FETs, including the JFETs and MOSFETs, balancing capacitors, and the required number of total components, including the balancing network elements and HV switches. The selected parameters are critical in regards to design complexities, cost, and robustness of the super-cascode module.

Due to the use of SiC MOSFET for $SC3$, the MOSFET voltage stress is $V_{DC}/(n+1)$, which is the same voltage stress as the JFETs. The upper capacitors experience higher voltage stress for $SC4$ than the lower JFET balancing capacitors. The voltage increases linearly and therefore, a design constraint when building a tens of kilo-volts or higher without having to increase the volume of the module significantly.

V. CONCLUSION AND FUTURE WORK

Super-cascodes have been evaluated and designed for a wide range of applications. Table III describes the difficulty rating of a few design aspects related to each super-cascode topology. It also summarizes the advantages and limitations to each topology selection option. However, thorough analysis of the advantages and limitations between the explored topologies have yet to be compared in greater details.

One active research application area in which SiC JFETs pose a promising solution is medium- and high-voltage circuit breaker applications [38] – [45]. The unique characteristics of SiC JFETs, such as robustness and reliability over repetitive cycles of switching makes the device an attractive choice for enduring large energy stress during short circuit events.

Nonetheless, there are other passive and active balancing approaches for IGBTs [49] – [52] and SiC MOSFETs [53] – [60].

In essence, the comparative-study nature of this paper aims to inform, analyze, and make a comprehensive comparison between the five super-cascode topologies. The similarities and differences gathered and analyzed could enhance a designer's understanding beyond the circuit operations and ultimately contribute to making an informed decision for designing or selecting a unique super-cascode architecture. For future work, other factors will be explored and compared, such as volume, manufacturability, reliability, and sensitivity analysis between the five super-cascodes.

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