



AlGaN High Electron Mobility Transistors for Power Switches and High Temperature Logic

B.A. Klein, A.M. Armstrong, A.A. Allerman, C.D. Nordquist, J.C. Neely, S. Reza, E.A. Douglas, M. Van Heukelom, A. Rice, V. Patel, B. Matins, T.R. Fortune, M. Rosprim, L. Caravello, R. DeBerry, J.R. Pipkin, V.M. Abate, R.J. Kaplar

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Goals: Al-rich AlGaN Channel E-mode power transistors and high temperature digital logic circuitry

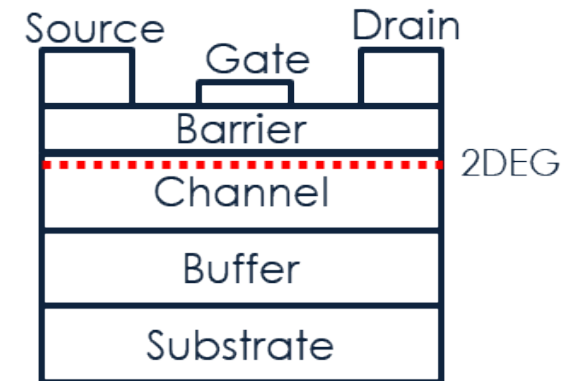
1. Background / Motivation

2. Experiments

- Threshold voltage – Enhancement Mode Power Switches
- Epitaxial design – Mobility and Charge Density
- Ohmic contacts
- High temperature gate metals

3. High Temperature AlGaN HEMTs

4. Summary



Nomenclature

$\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier / $\text{Al}_y\text{Ga}_{1-y}\text{N}$ channel
=
X/Y HEMT

Why AlGaN HEMTs?

High power

$$P_{\max} = I_{\max} V_{\max} / 8$$

$$J_{\max} = q \mu n_s E_c \quad J_{\max} = q v_{\text{sat}} n_s$$

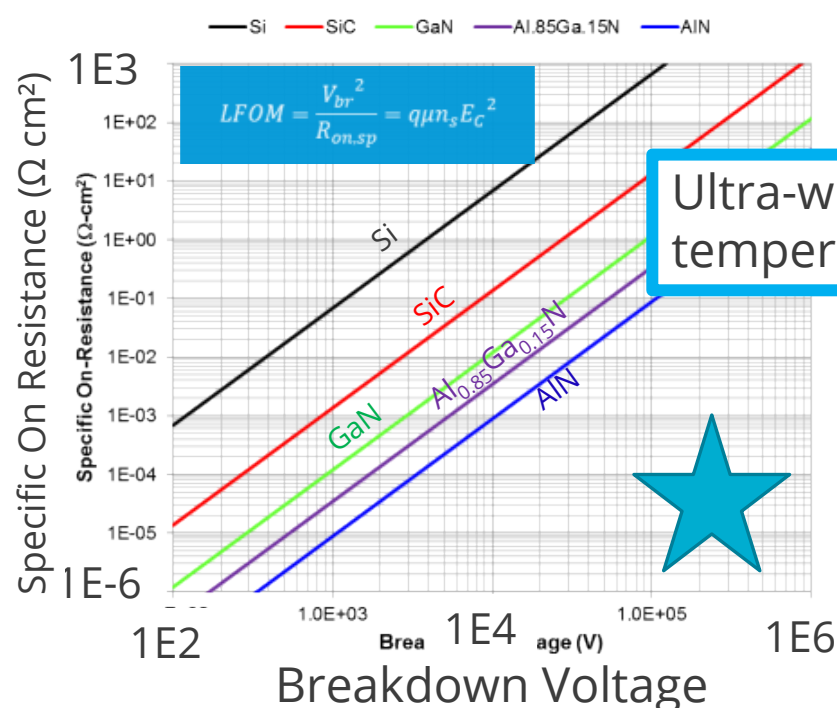
High temperature

- Wide band gaps suppress intrinsic carrier density effects and thermionic emission-induced leakage

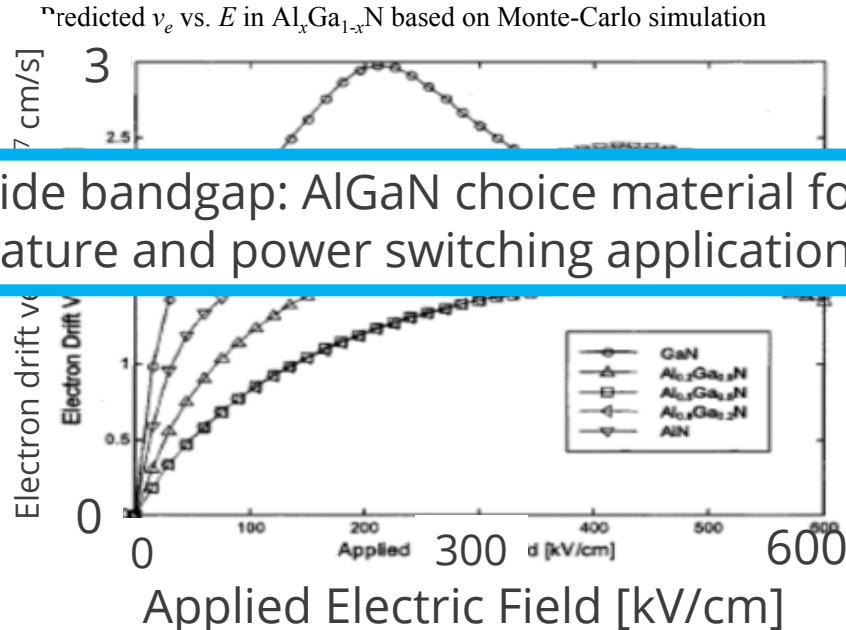
P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1065 - 1076, 2002.

Estimated properties of wide band gap materials

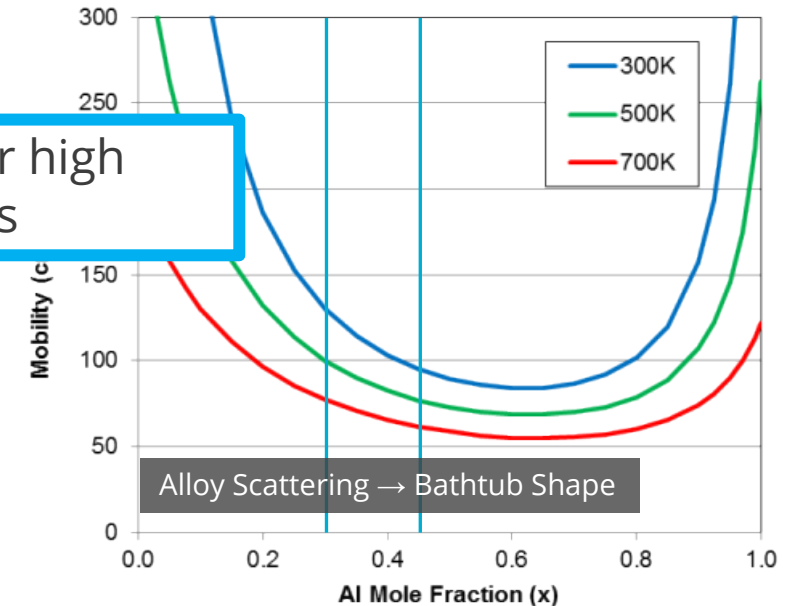
Material	E_G (eV)	E_c (MV/cm)	Electron mobility (cm ² /V s)	v_{sat} (10 ⁷ cm/s)	Thermal conductivity (W/m·K)
SiC	3.3	2.5	1000	2.0	370
GaN	3.4	4.9	1000	1.4	253
AlN	6.0	15.4	426	1.3	319
$\text{Al}_x\text{Ga}_{1-x}\text{N}$ (x>0.7)	5.0-6.0	13.5-15.4	~150-400	Interpolation	Interpolation
b-Ga ₂ O ₃	4.9	10.3	180	1.1	11-27
Diamond	5.5	13.0	4500-7300	1.9-2.3	2290



Ultra-wide bandgap: AlGa_xN choice material for high temperature and power switching applications



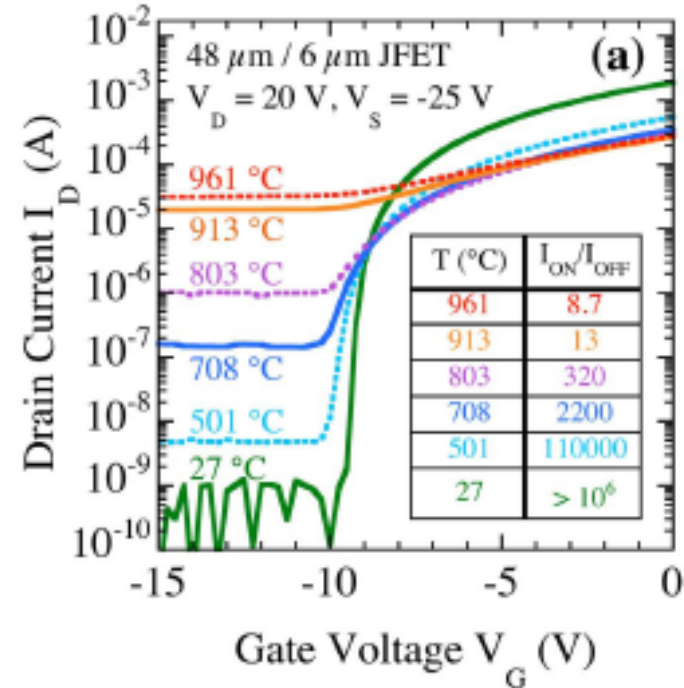
M. Farahmand et al., *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 535-542, 2001.



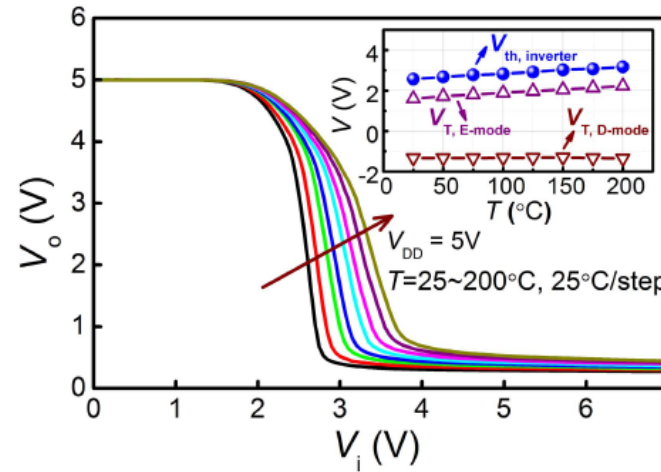
M. E. Coltrin and R. J. Kaplar, *Journal of Applied Physics*, vol. 121, no. 055706, 2017

High temperature device background

NASA: SiC JFET^[1]
Characterized to 961°C

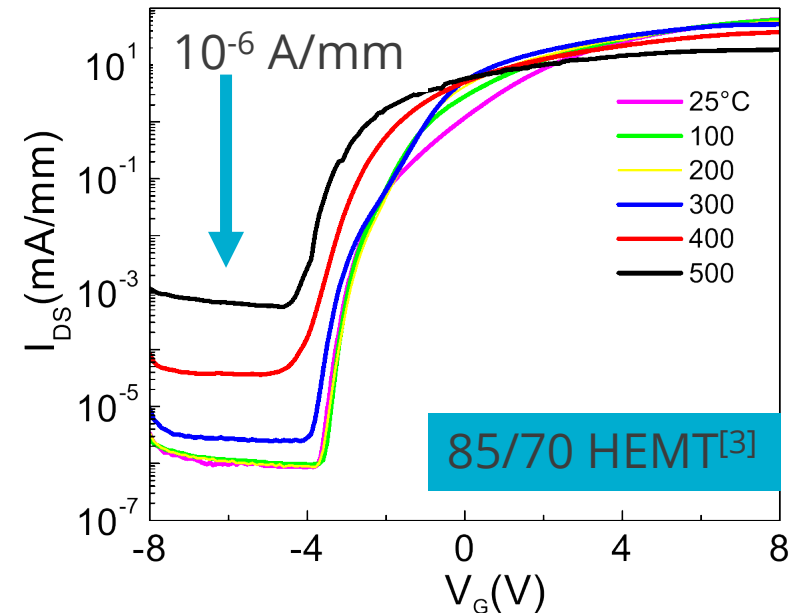
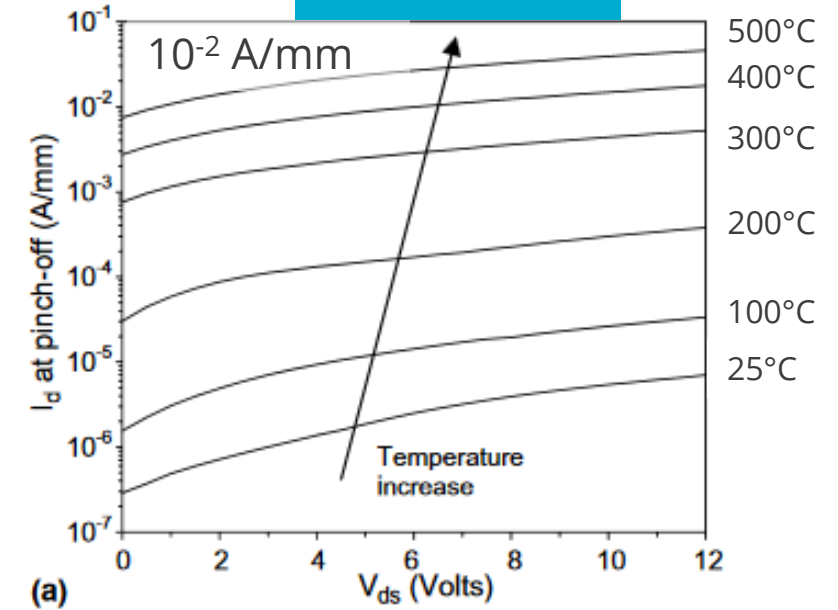


GaN HEMT inverter^[2]
25 – 200°C



Low off-state leakage for high temperatures:
 10^{-6} A/mm for $\text{Al}_{0.85}\text{GaN}/\text{Al}_{0.7}\text{Ga}_{0.3}\text{N}$ HEMTs (Sandia),
 compared to
 10^{-2} A/mm for $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ HEMTs (1)

25/0 HEMT^[4]



^[1] P. G. Neudeck, *IEEE Electron Device Letters*, vol. 38, no. 8, (2017).

^[2] G. Tang, *IEEE Electron Device Letters*, vol. 38, no. 9, pp. 1282-1285 (2017).

^[3] P. H. Carey, *Journal of the Electron Devices Society*, vol. 7, pp. 444-452, 2019.

^[4] W. S. Tan, *Solid-State Electronics* **50**: 511-513 (2006).

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- **Threshold voltage – Enhancement Mode Power Switches**
- **Epitaxial design – Mobility and Charge Density**
- **Ohmic contacts**
- **High temperature gate metals**

3. High Temperature AlGaN HEMTs

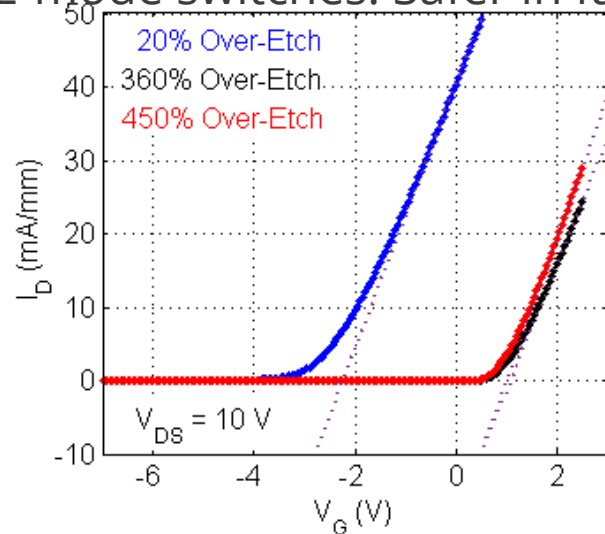
4. Summary

Enhancement-Mode AlGaN-channel HEMTs

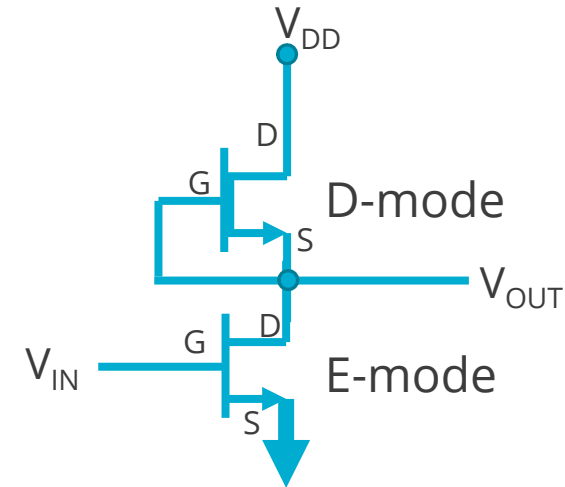


Depletion-Mode (normally on)			AlGaN HEMTs are innately D-mode
Enhancement-Mode (normally off)			Two approaches for E-mode already successfully implemented at Sandia

E-mode switches: Safer in failures



Currently complimentary pFET and nFET not practical
→ Combine e-mode and d-mode for logic



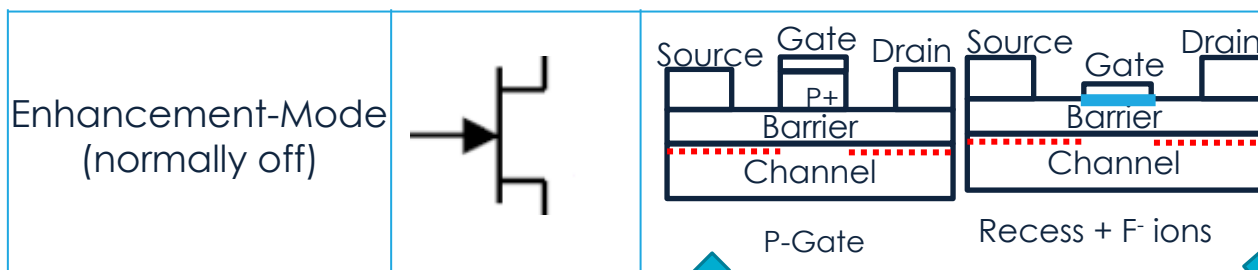
Depletion-mode load inverter

Masahito Kanamura, et al. (2010). *IEEE Electron Device Letters* **31**(3): 189-191.

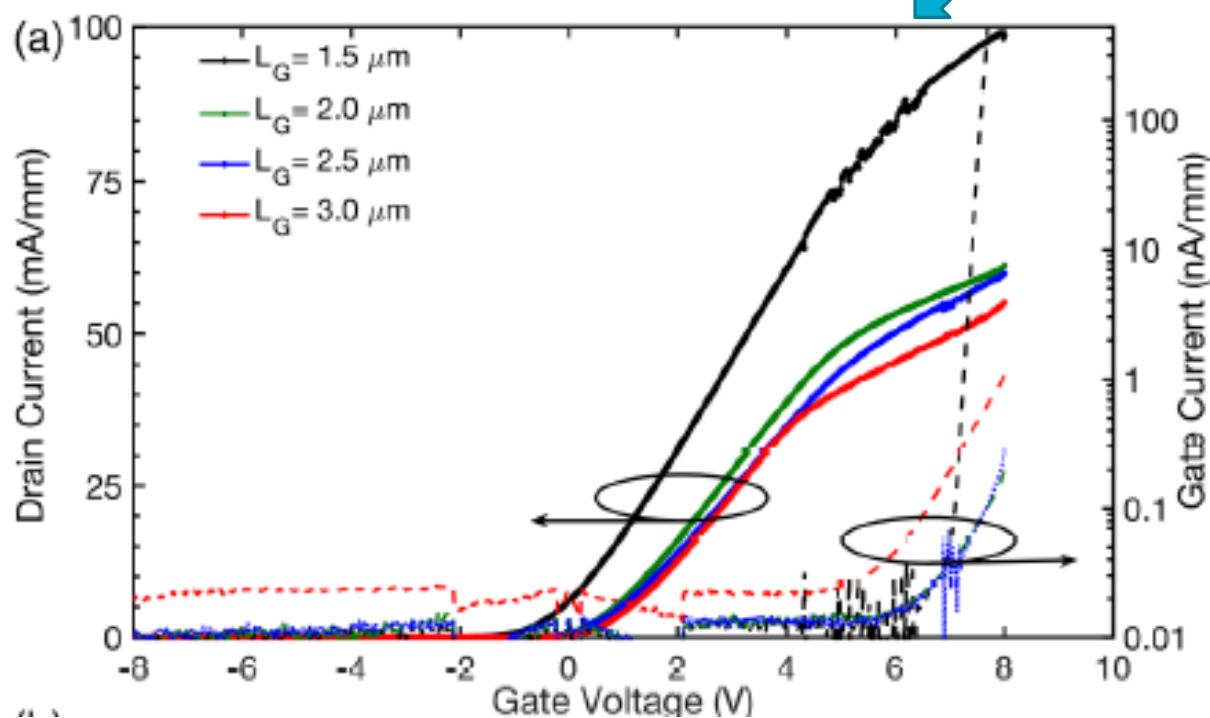
Hilt, O., et al. (2010). Proceedings of the 22nd International Symposium on Power Semiconductor Devices & ICs, Hiroshima, Japan, IEEE.

Yong Cai, et al. (2006). *IEEE Transactions on Electron Devices* **53**(9): 2207-2215.

Enhancement-Mode AlGaN-channel HEMTs

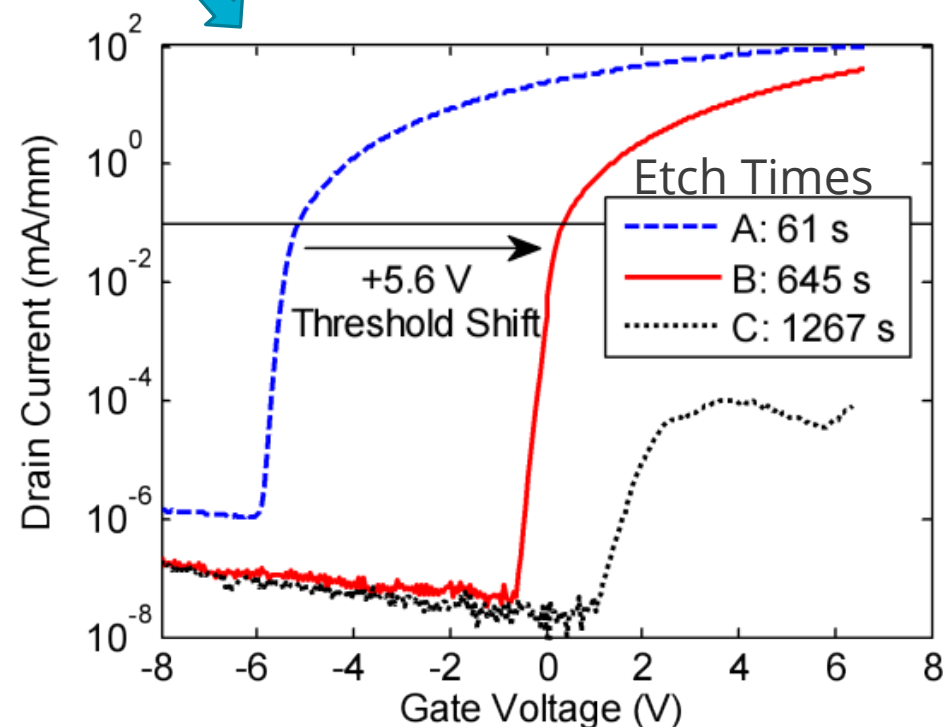


Two approaches for E-mode successfully implemented at Sandia



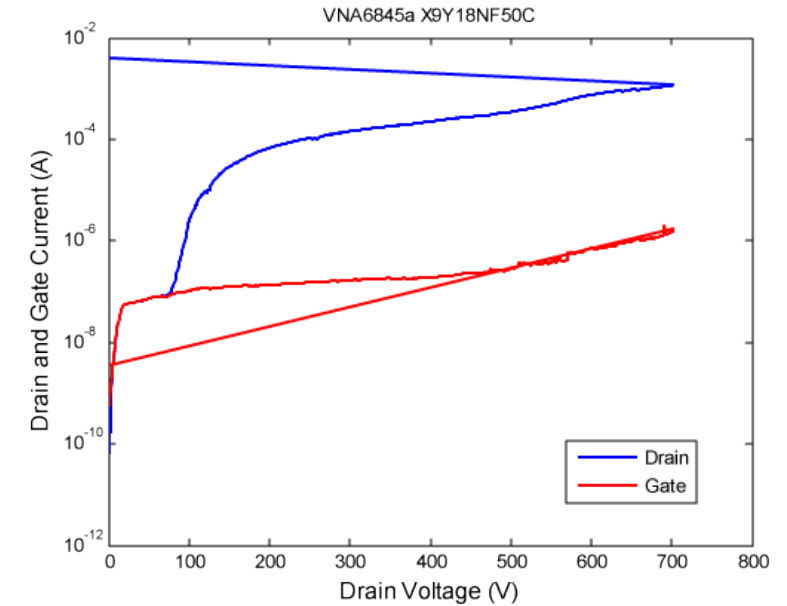
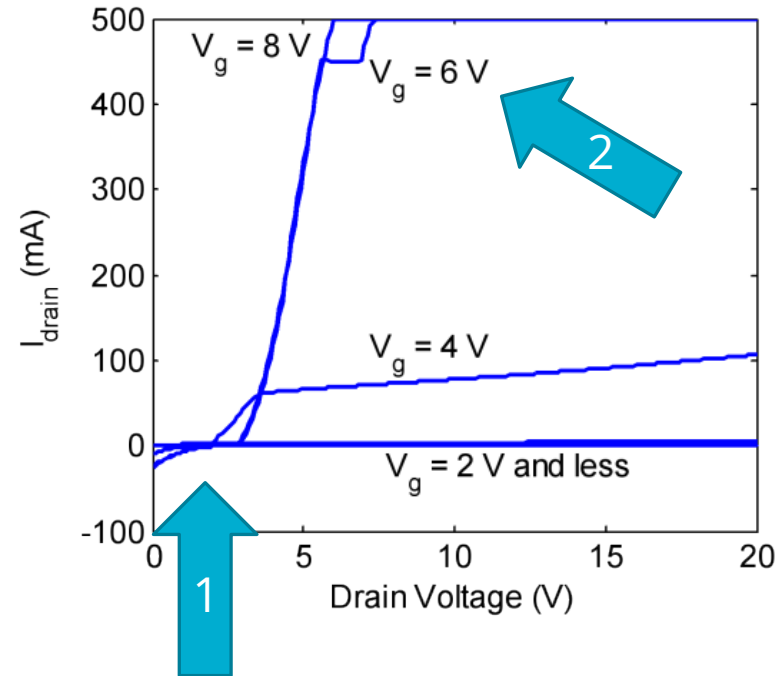
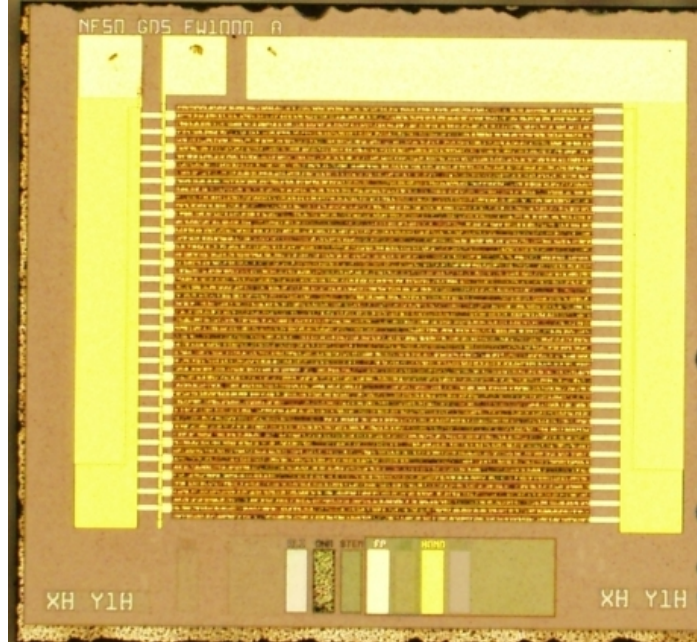
JVSTB, vol. 37, no. 021208, 2019.

45/30 HEMT + p-AlGaIn cap



Appl. Phys. Lett. **114**, 112104 (2019)

85/70 HEMT: Recess + F⁻ ions



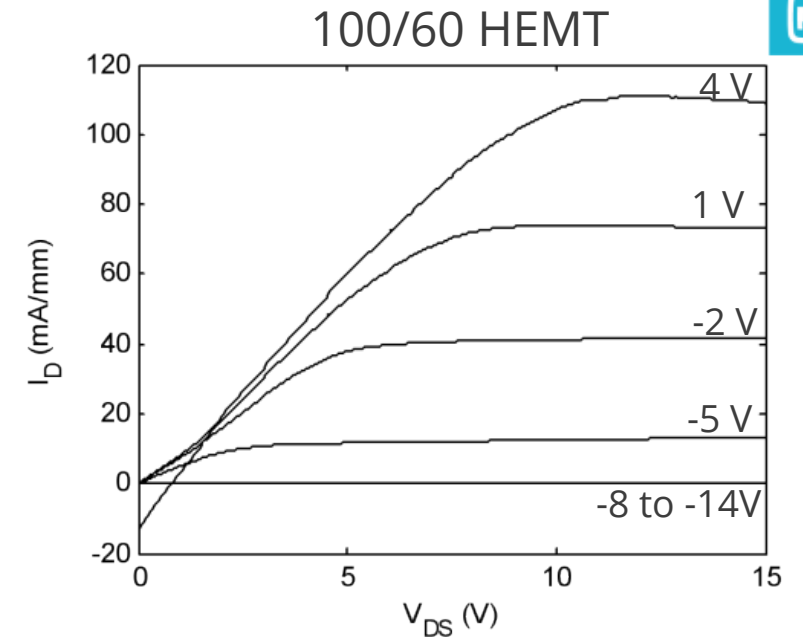
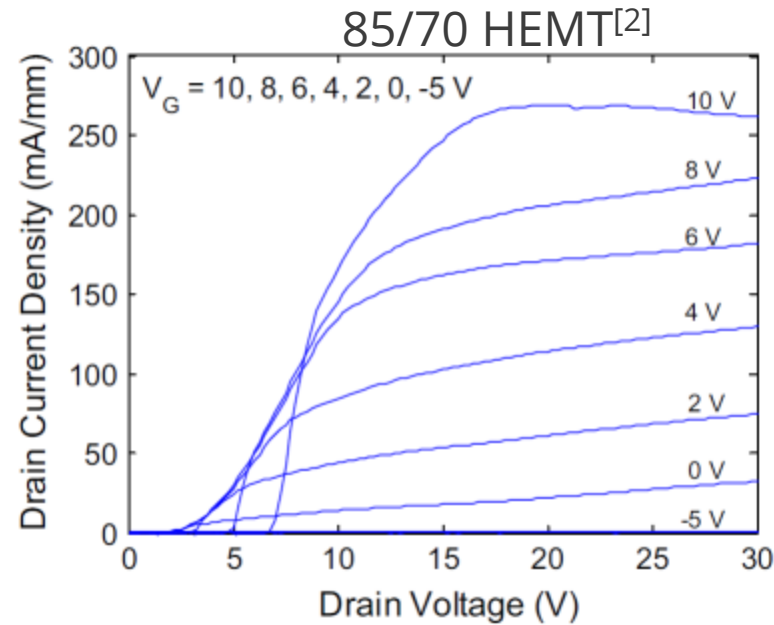
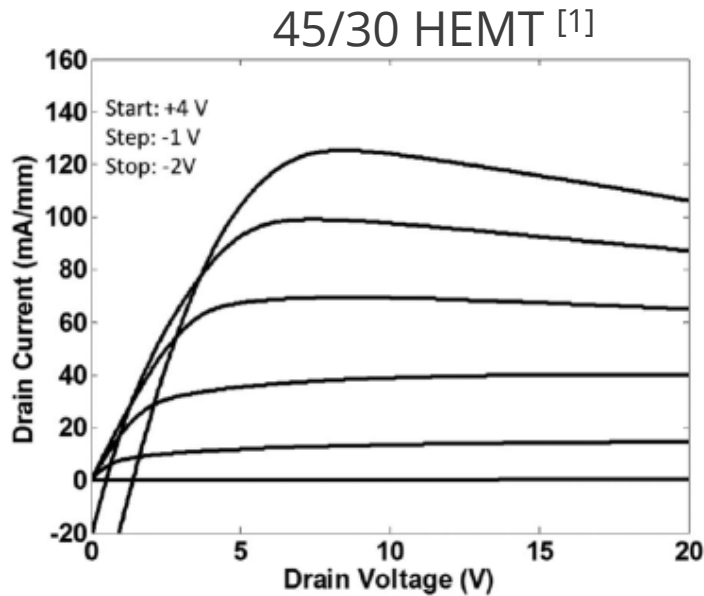
Threshold voltage = 1.5 V
 Drain Current = 500 mA (DC), 1.5 A (pulsed)
 Breakdown voltage = ~650 V

What needs more work?

1. Offset voltage
2. High gate bias

Need to change epitaxy design
 Ohmic contact needs improvement

Epitaxial Design



- Could repeatably make good contacts to a 45/30 HEMT
- For a long time we worked off the assumption that the high barrier composition was limiting our ohmic contacts
- ...Until we observed Ohmic contacts on a 100/60 HEMT → Channel composition dependence → What was going on?

45/30 HEMT

100/60 HEMT

86/70 HEMT

26/0 HEMT

Motivated transport study^[3]

$\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ (50 nm)
$\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ (270 nm)
$\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ (3.9 μm)
AlN (1.6 μm)
Sapphire Substrate

AlN (30 nm)
$\text{Al}_{0.6}\text{Ga}_{0.4}\text{N}$ (150 nm)
$\text{Al}_{0.73 \rightarrow 0.6}\text{Ga}_{0.27 \rightarrow 0.4}\text{N}$ (10 nm)
$\text{Al}_{0.73}\text{Ga}_{0.27}\text{N}$ (50 nm)
$\text{Al}_{1 \rightarrow 0.73}\text{Ga}_{0 \rightarrow 0.27}\text{N}$ (50 nm)
AlN (1.6 μm)
Sapphire Substrate

$\text{Al}_{0.86}\text{Ga}_{0.14}\text{N}$ (30 nm), $2.5 \times 10^{18} \text{ Si}$
$\text{Al}_{0.7}\text{Ga}_{0.3}\text{N}$ (500 nm)
$\text{Al}_{1 \rightarrow 0.7}\text{Ga}_{0 \rightarrow 0.3}\text{N}$ (10 nm)
AlN (2.5 μm)
Sapphire Substrate

$\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ (20 nm)
GaN (50 nm)
GaN:C (1.7 μm), $1 \times 10^{18} \text{ C}$
AlN nucleation
SiC substrate

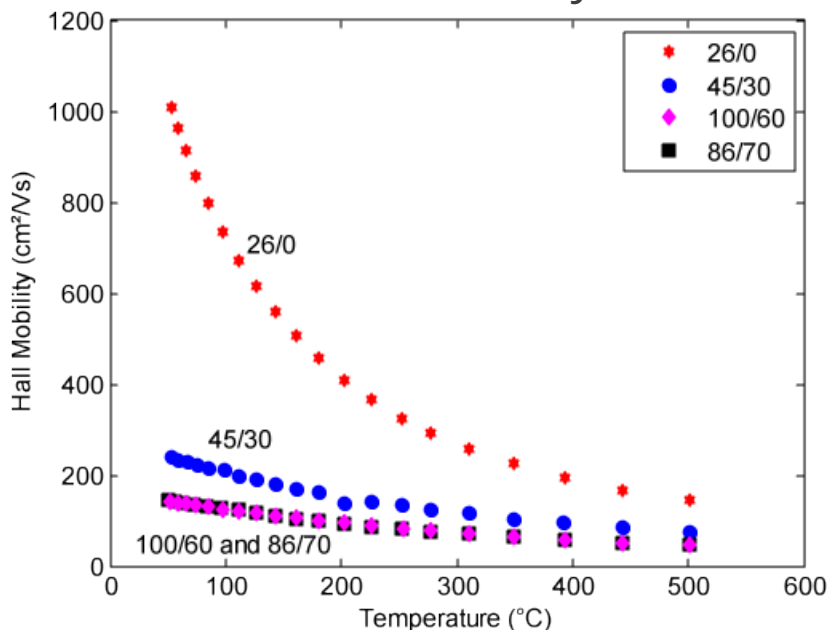
[1] *ECS Journal of Solid State Science and Technology*, vol. 6, no. 11, pp. S3010-S3013, 2017.

[2] *Journal of Electronic Materials*, vol. 48, pp. 5581–5585, 2019.

[3] B. A. Klein, *Journal of Applied Physics* (submitted).

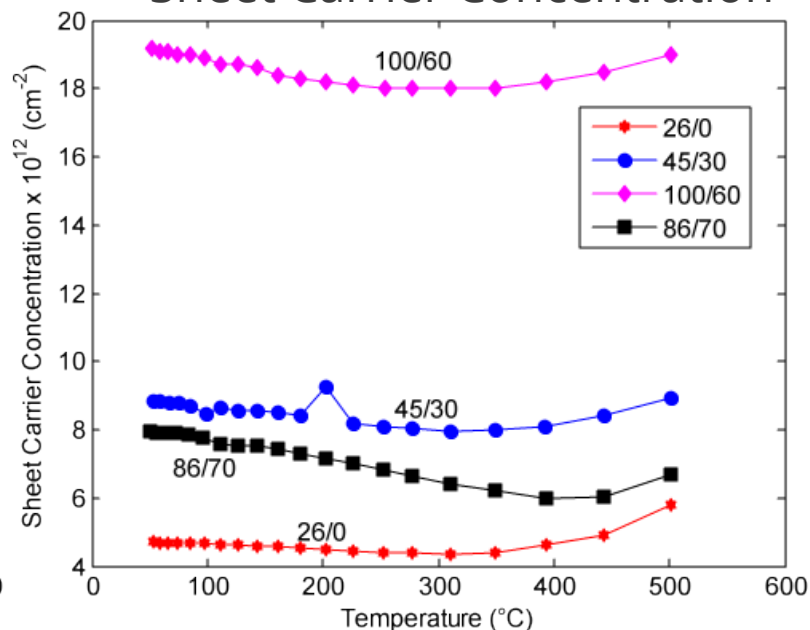
Epitaxial Design

Hall Mobility


 μ

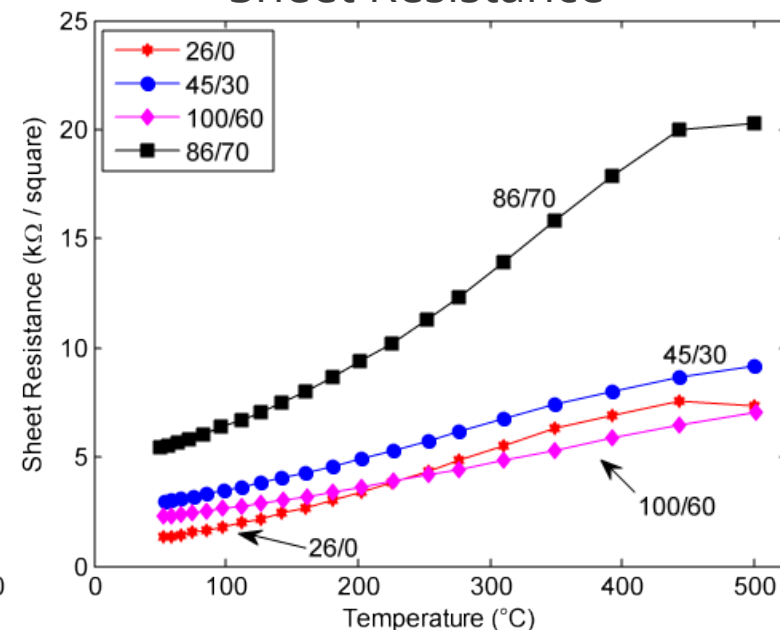
- Lower Al% channel = higher mobility
- Mobility less variable over temperature compared to GaN HEMTs
- Over the 500°C range
 - AlGaAs channels: 3.1x reduction
 - GaN channel: 6.9 x reduction
- Improved stability over T

Sheet Carrier Concentration


 n_s

- High barrier/channel Al contrast increases carrier concentration

Sheet Resistance


 $= 1/qR_{SH}$

Good combination for high temperature epitaxy:

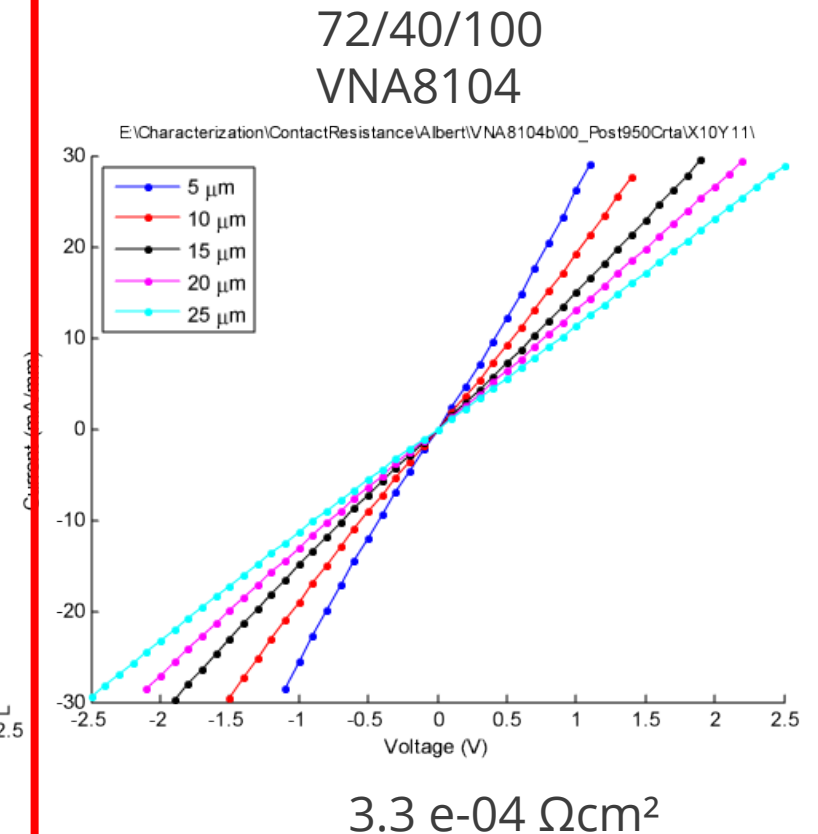
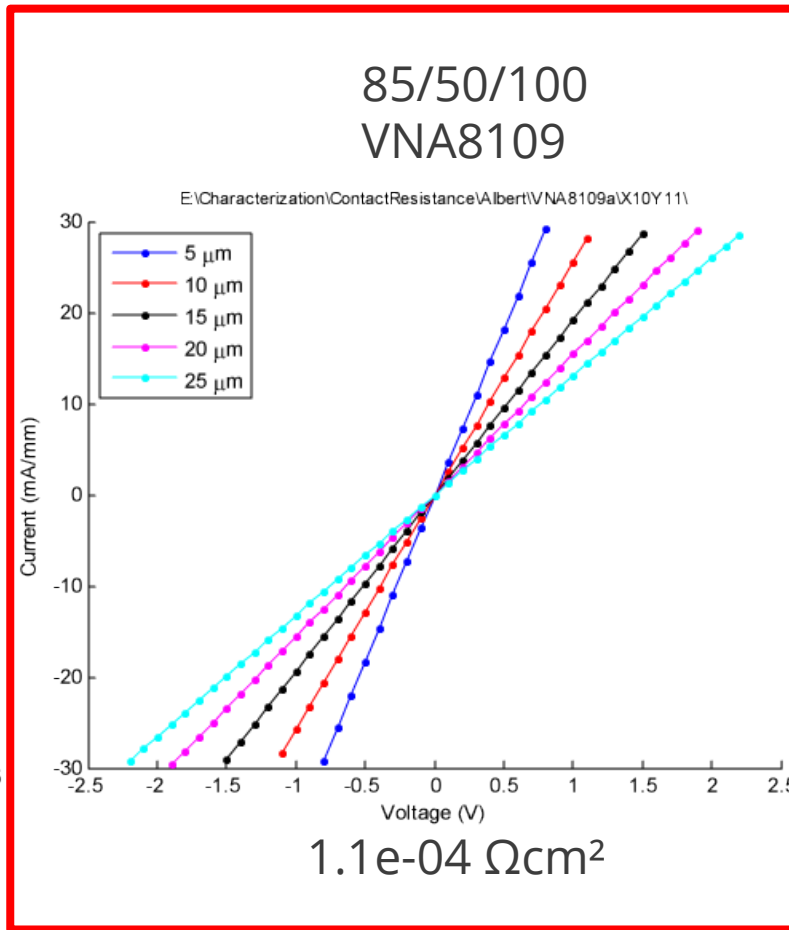
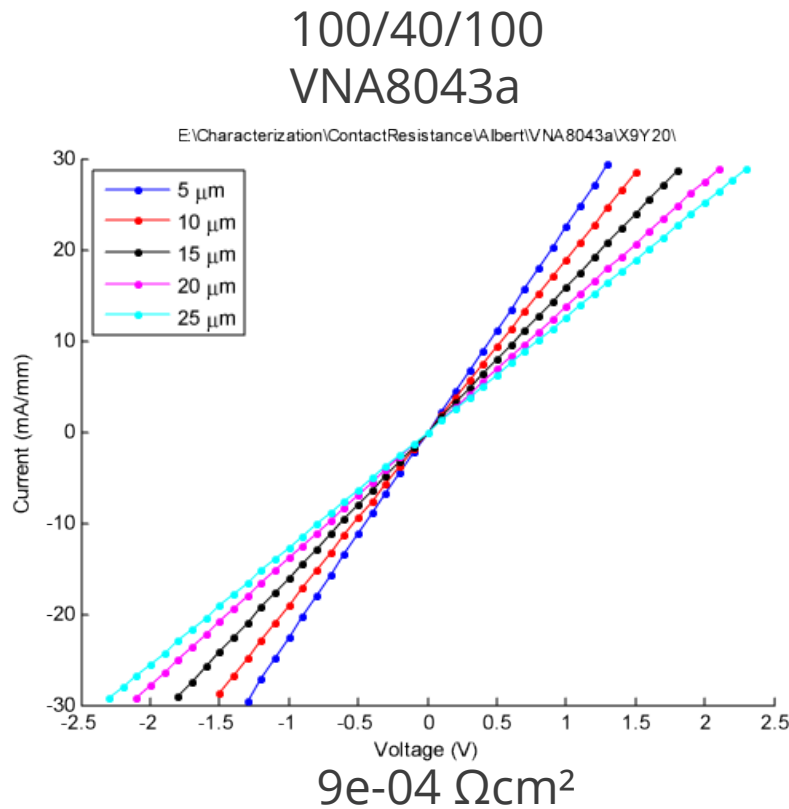
1. Low mobility variation
2. High carrier concentration

Guidelines

Reduced channel Al% → higher mobility

Increased Barrier/Channel Al% contrast → higher n_s

Epitaxial Design → Ohmic Contacts



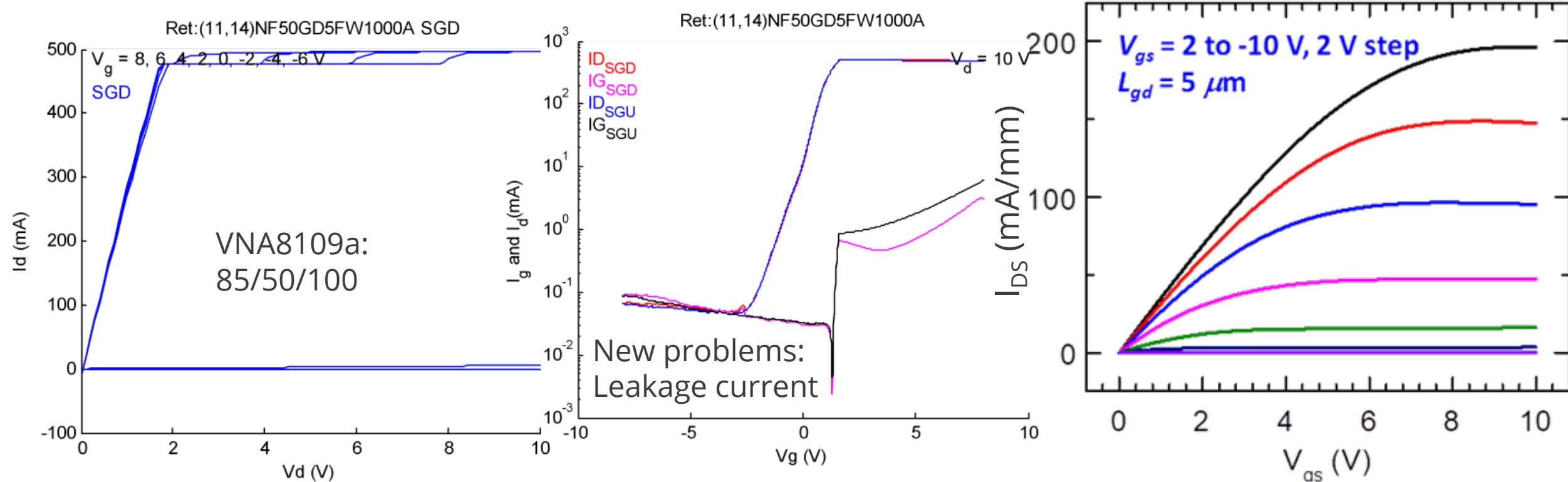
Design Principles

1. Keep the Al-rich barrier – Want to keep for benefits in power and high temperature

2. Increase the Al contrast between barrier and channel – Reduce sheet resistance

Epitaxial Design → Ohmic Contacts

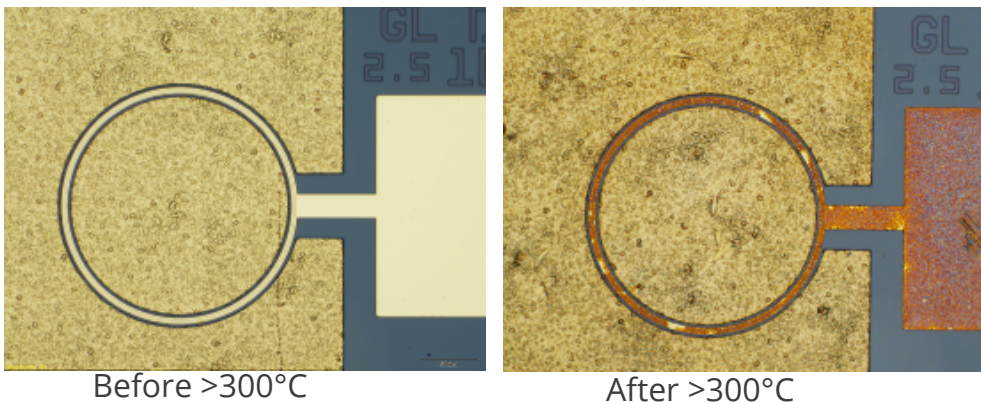
Planar Ohmic contacts
85/50 HEMT



- Reduced specific contact resistance by 2×:
 5×10^{-3} to $1 \times 10^{-4} \Omega\text{cm}^2$
- Reduced sheet resistance by over half:
4.7 k Ω /sq to 1.7 k Ω /sq
- Increased current density by over 6×:
30 mA/mm to 200 mA/mm (long channel devices)

- ✓ Threshold voltage control
- ✓ Epitaxial design
- ✓ Ohmic contacts
- **High temperature gate metals**

High Temperature Gates



“Standard” Gate: 200 Å Ni / 4500 Å Au

- Nickel metal migration
- Changes to electrical properties
- Metal pads don’t survive
- Need high temperature gate metal

Properties of Candidate Metals

Metal	Resistivity, ~25°C (Ωm)	Melting Point (K)	Thermal Expansion ($\times 10^6$) (cm^{-1})
Au	2.35	1337	14.2
Mo	5.34	2896	5
W	5.6	3695	4.5 ←
Ni	6.84	1726	13
Pt	10.6	2042	9 ←
Ta	12.4	3293	6.5
Nb	12.5	2742	7
Cr	12.9	2130	6
Pd	20	1825	←
V	25	2163	8
Zr	40	2128	5.7

Pattern standard Ohmic contacts



Gate Metal Experiment



Characterization

- 85/70 HEMT
- 250 Å Ti / 1000 Å Al / 150 Å Ni / 500 Å Au
- Anneal: 1100°C, 30s, ~1mT nitrogen

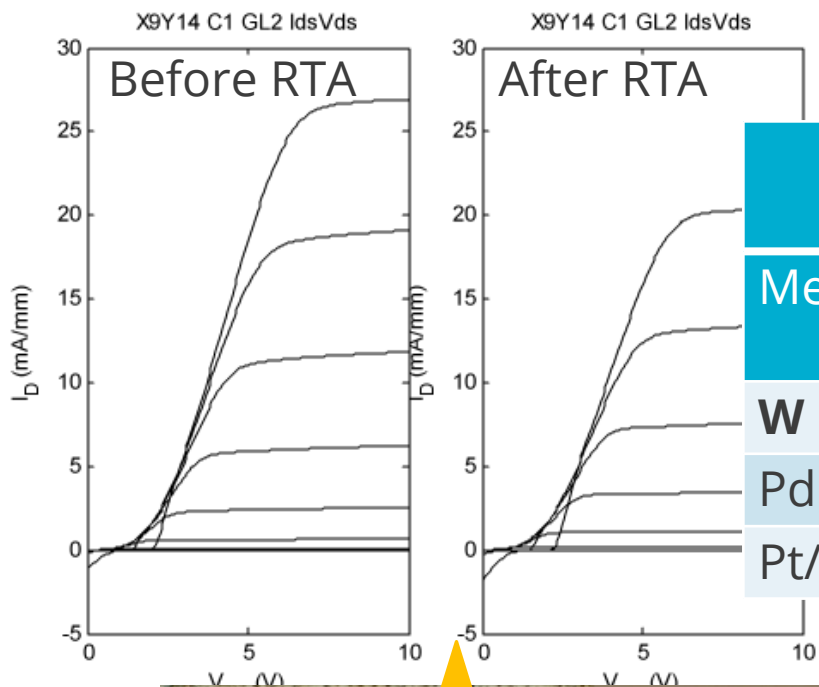
1. 2000 Å W (sputter)
2. 2000 Å Pd (evap)
3. 200 Å Pt / 2000 Å Au (evap)

1. Pre-high temperature I-V sweeps
2. Multiple Cycles: Anneal at 500°C → I-V sweeps

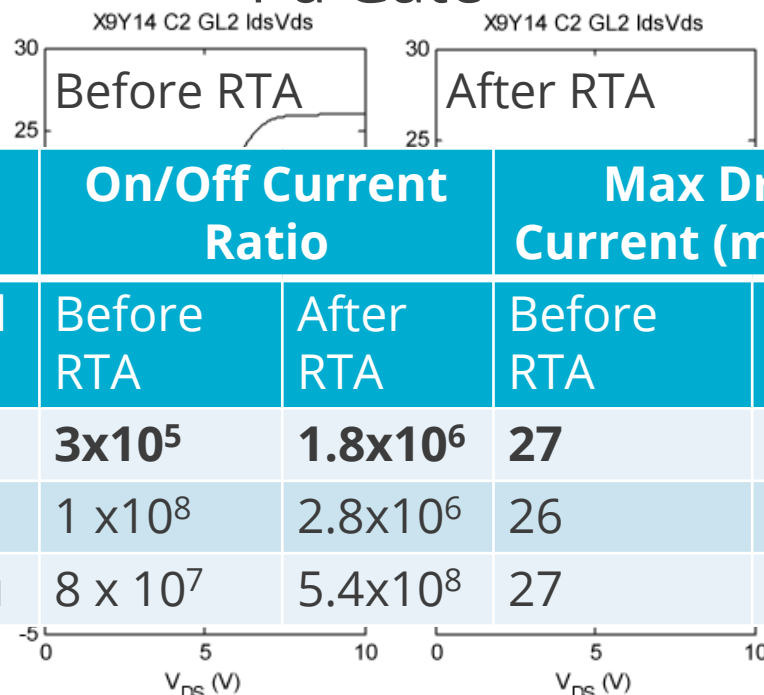
High Temperature Gates



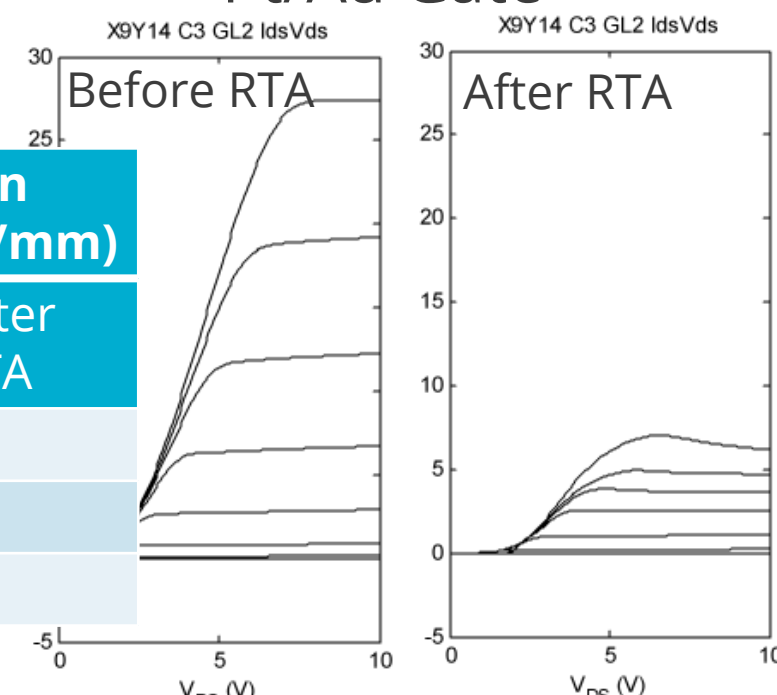
W Gate



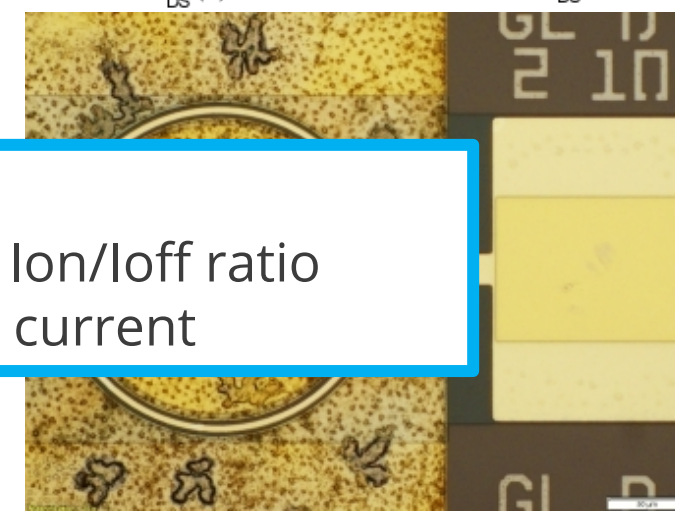
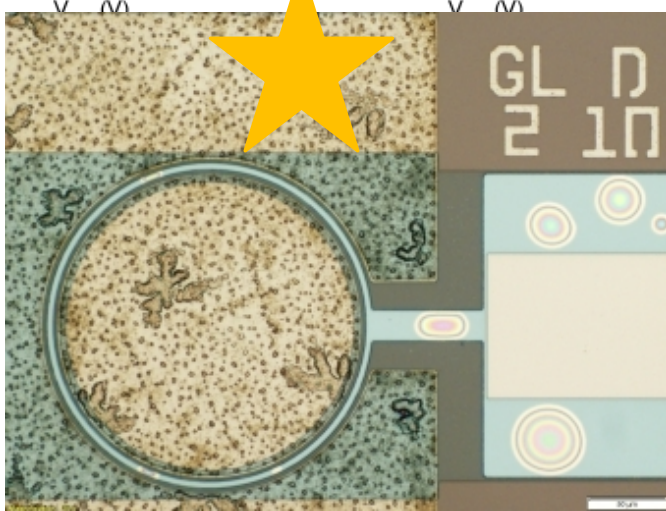
Pd Gate



Pt/Au Gate



Metal	On/Off Current Ratio		Max Drain Current (mA/mm)	
	Before RTA	After RTA	Before RTA	After RTA
W	3×10^5	1.8×10^6	27	21
Pd	1×10^8	2.8×10^6	26	13
Pt/Au	8×10^7	5.4×10^8	27	7



Best Results: W gate

- Burn-in for improved Ion/Ioff ratio
- Maintains good drain current

Goals: Al-rich AlGaN Channel E-mode power transistors and high temperature digital logic circuitry

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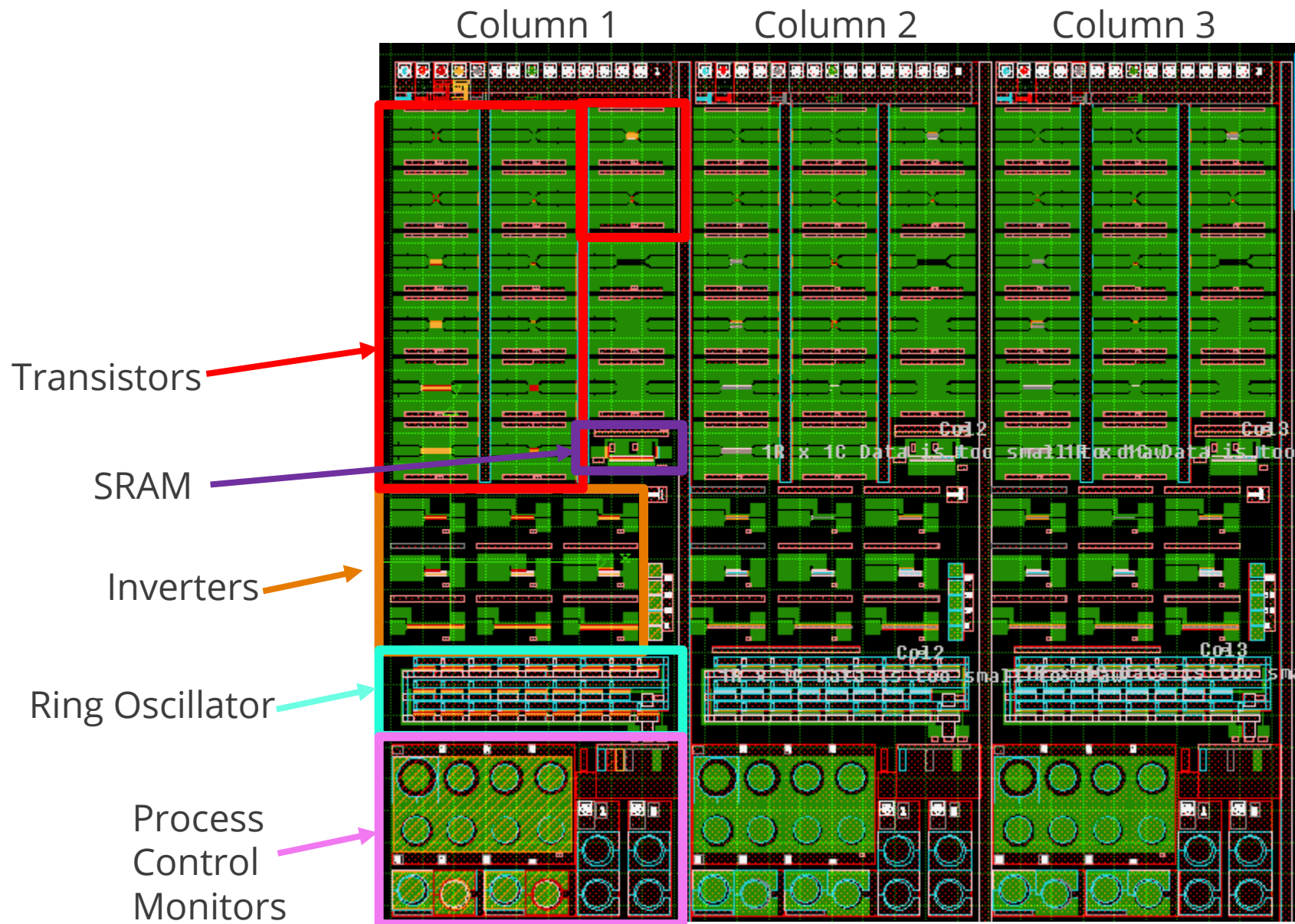
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High Temperature Mask Set



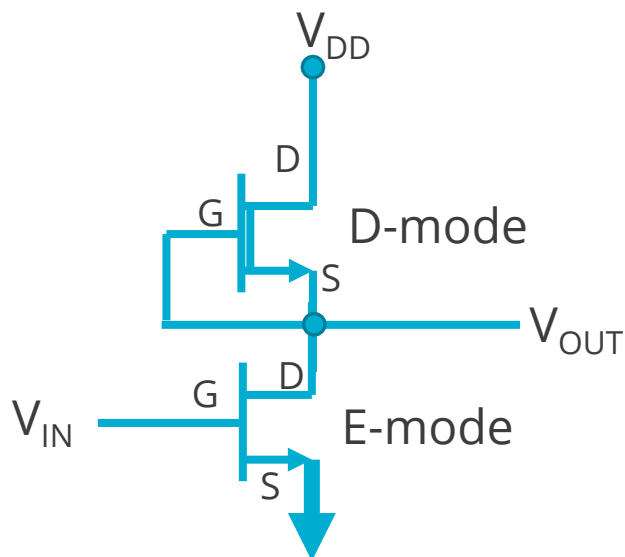
3 Columns

Use for 3 different barrier etches

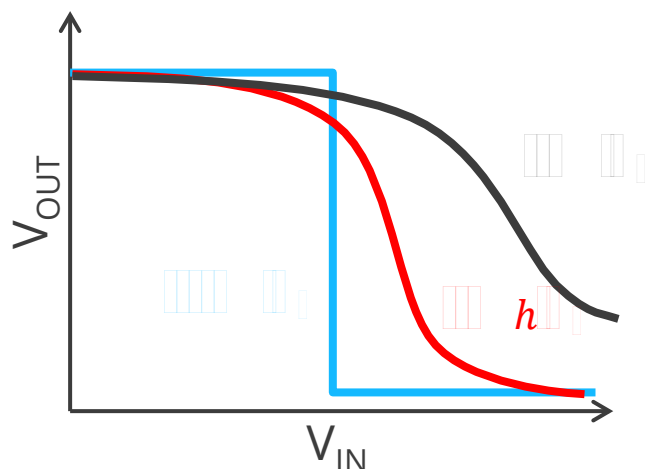
OR

Use for 3 different p-(Al)GaN etches

High Temperature Mask Set: Inverter design



Inverter Characteristic Plot



See for example: J. Uyemura, *Fundamentals of MOS Digital Integrated Circuits* (1988).

Column 1

Vary β_R (driver-load ratio) by E/D gate width ratio. Vary gate length.

GL 1.5 μm	GL 2.5 μm	GL 5 μm
$\beta_R = 1.5$	$\beta_R = 1.5$	$\beta_R = 1.5$
$\beta_R = 6$	$\beta_R = 6$	$\beta_R = 6$
$\beta_R = 16$	$\beta_R = 16$	$\beta_R = 16$

Column 2

Vary β_R (driver-load ratio) by E/D gate width ratio. Vary gate length.

GL 1.5 μm	GL 2.5 μm	GL 5 μm
$\beta_R = 1.5$	$\beta_R = 1.5$	$\beta_R = 1.5$
$\beta_R = 6$	$\beta_R = 6$	$\beta_R = 6$
$\beta_R = 16$	$\beta_R = 16$	$\beta_R = 16$

Column 3

Vary β_R (driver-load ratio) by E/D gate width ratio. Vary gate length.

GL 1.5 μm	GL 2.5 μm	GL 5 μm
$\beta_R = 1.5$	$\beta_R = 1.5$	$\beta_R = 1.5$
$\beta_R = 6$	$\beta_R = 6$	$\beta_R = 6$
$\beta_R = 16$	$\beta_R = 16$	$\beta_R = 16$

$$\beta_R = \frac{W_{Emode}/L_{Emode}}{W_{Dmode}/L_{Dmode}}$$

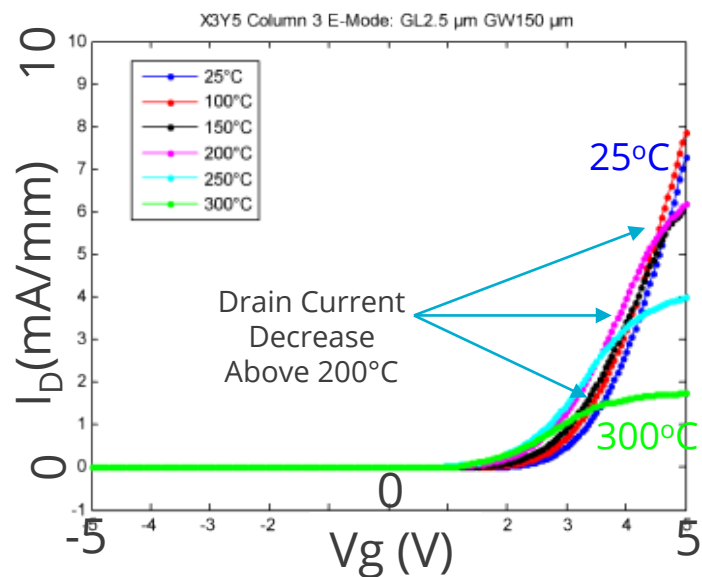
Mask Features

- Increasing $\beta_R \rightarrow$ Increasingly abrupt transition
- Multiple columns \rightarrow Vary recess etch time

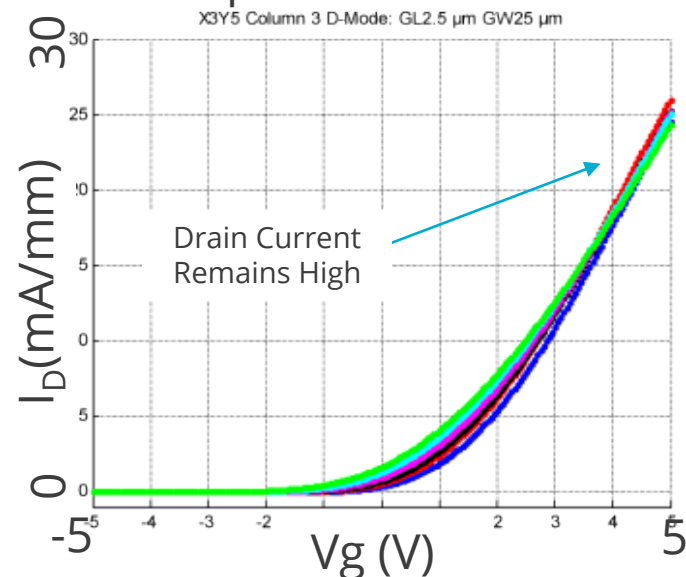
High Temperature Devices: Transistor



Enhancement Mode

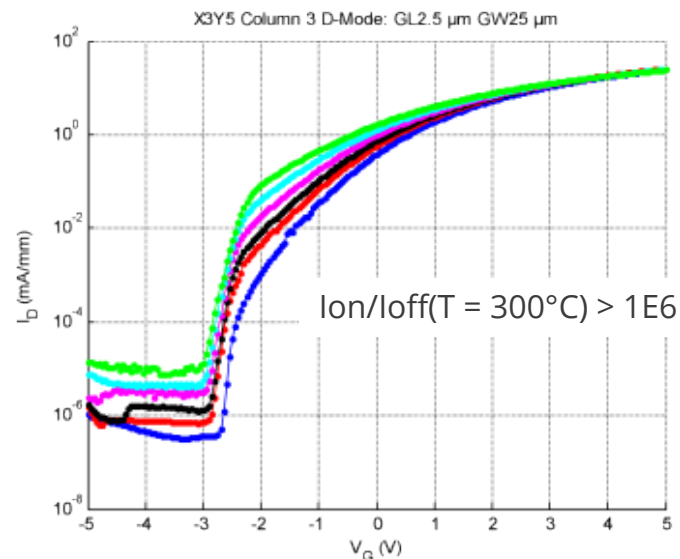
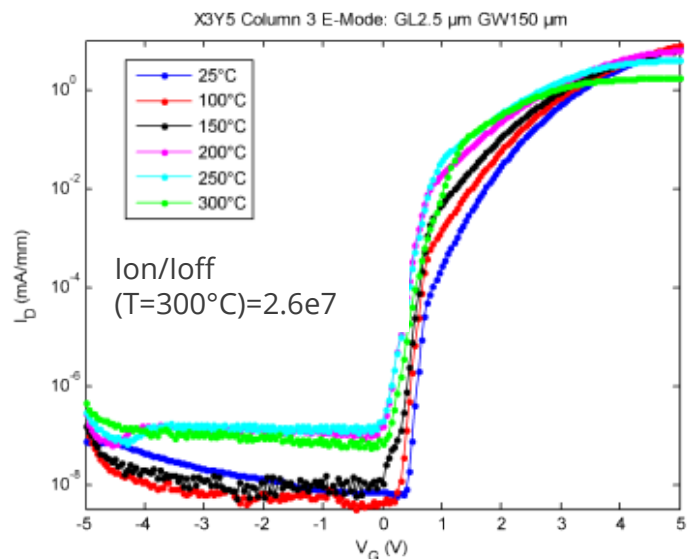


Depletion Mode



D-mode: drain current stable 25-300°C
E-mode: drain current decreases >200°C

E-mode resistance increases \rightarrow inverter $V_{\text{out,Low}}$ rises

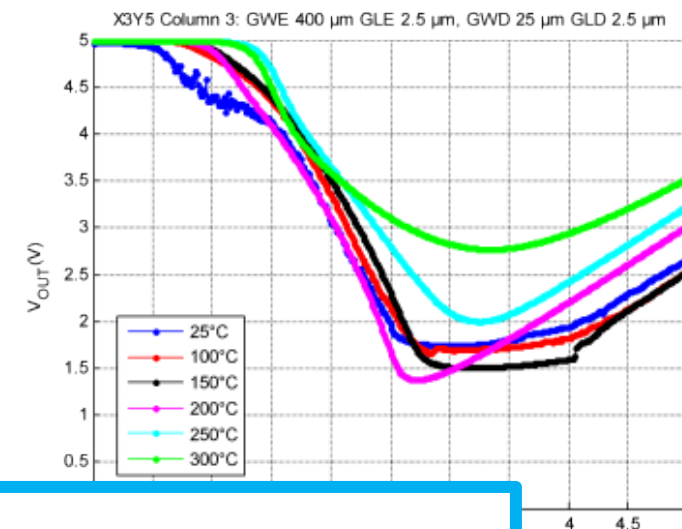
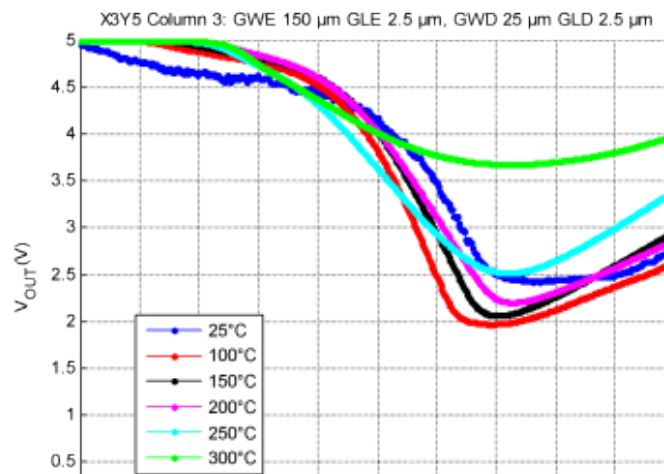
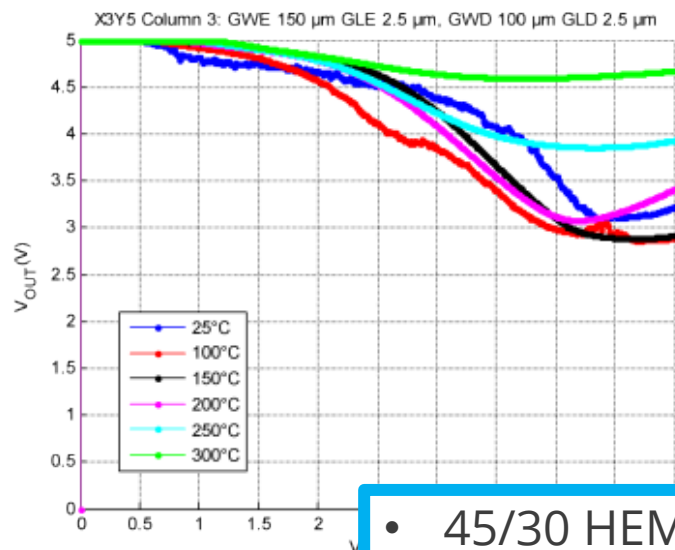


On/Off ratio stable 25-300°C for both e- and d-mode transistors

High Temperature Devices: Inverter Results

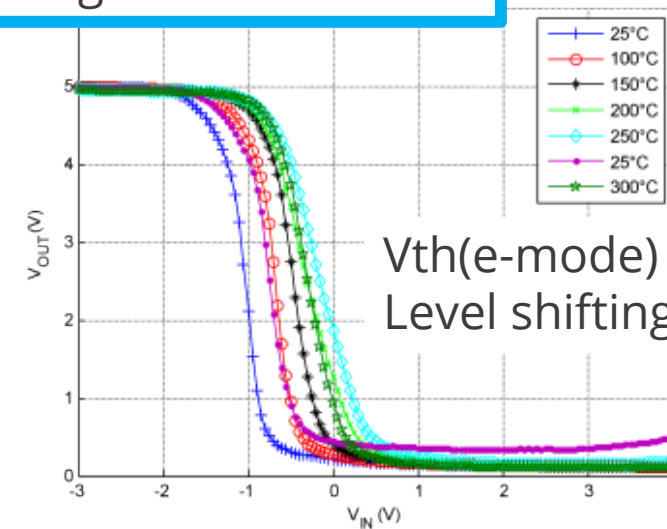
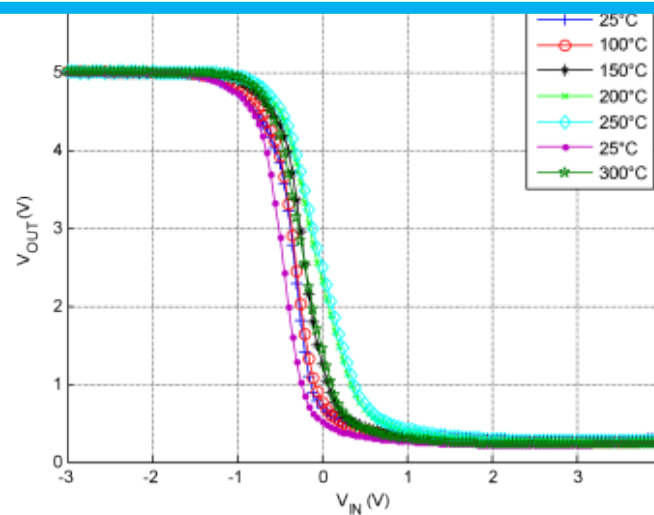
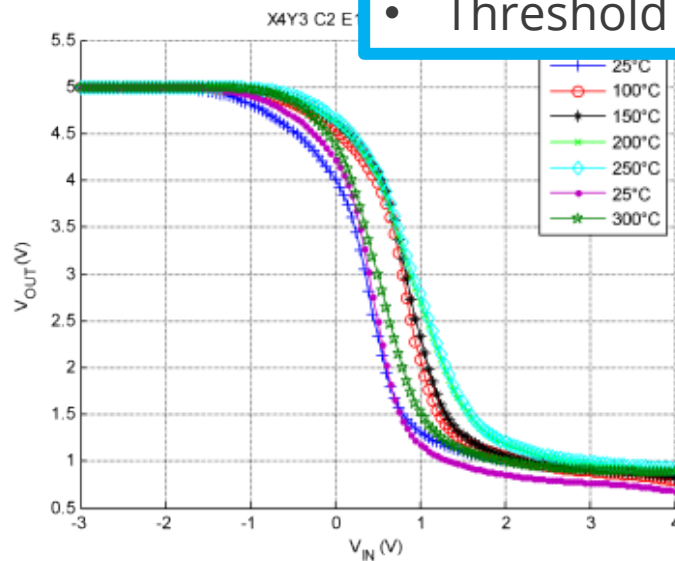

 $\beta_R = 1.5$
 $\beta_R = 6$
 $\beta_R = 16$

85/70 HEMT



- 45/30 HEMT with p-AlGa_N Cap
- Lower e-mode resistance than 85/70 \rightarrow Improved inverter performance
- Threshold voltage of e-mode is too low \rightarrow Level shifting needed

45/30 HEMT

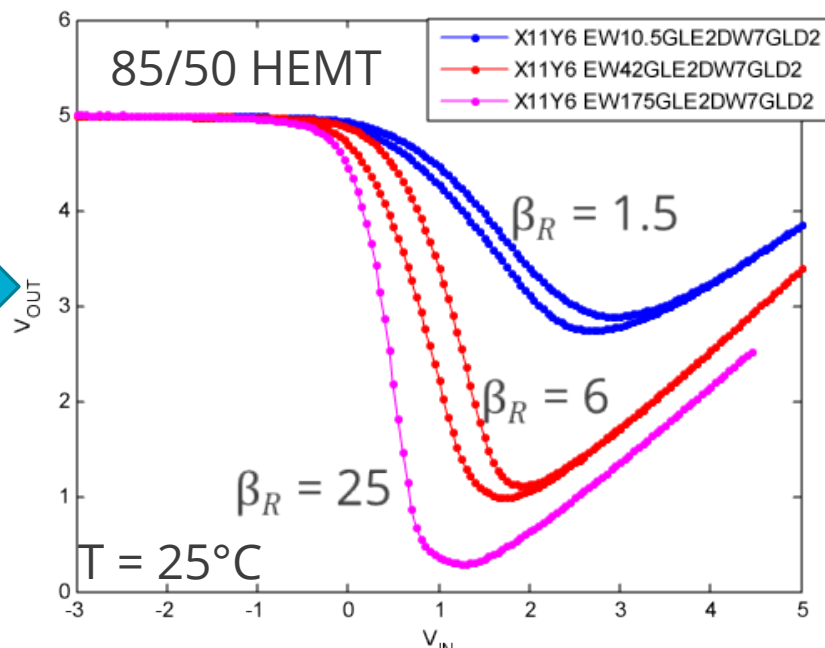
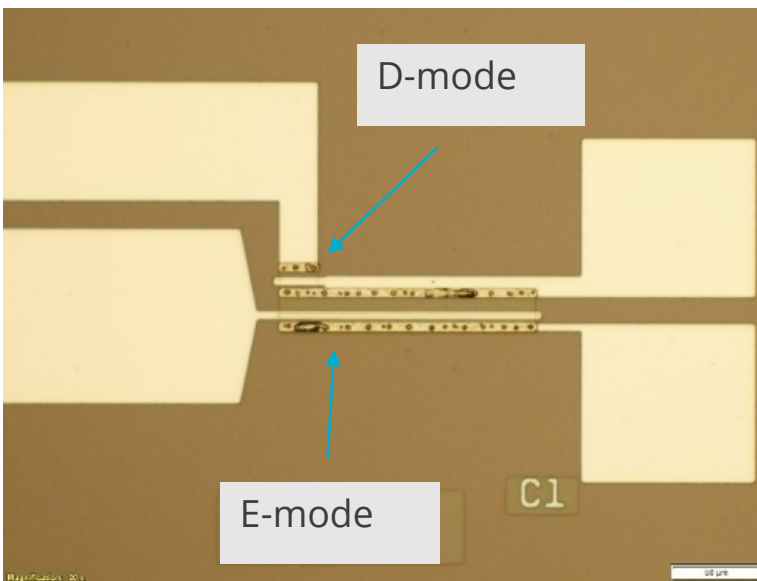
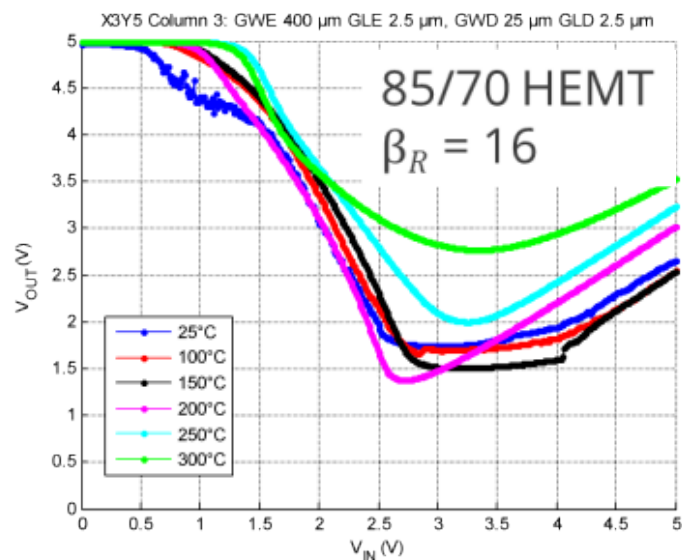
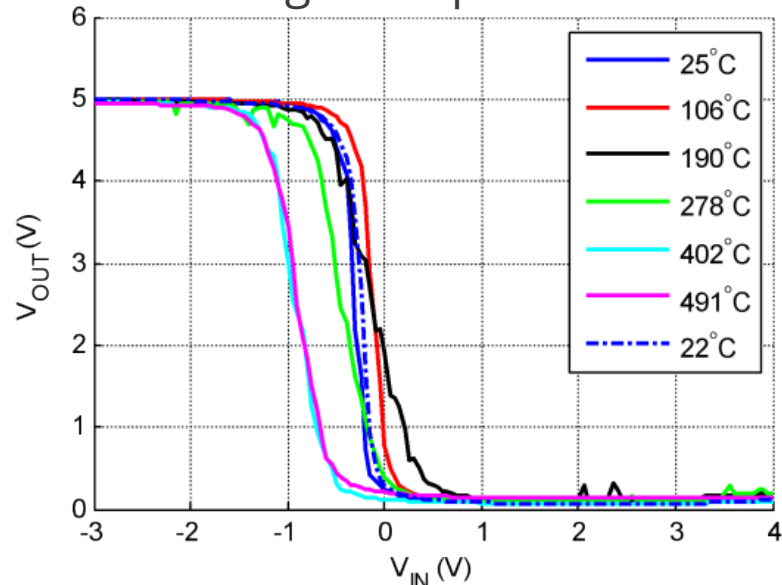


V_{th}(e-mode) bad
Level shifting

High Temperature Devices: Inverter Results



AlGaN High Temperature Inverter



45/30 HEMT + p-AlGaN gate cap

- Operation up to 491°C
- Requires level shifting
- E-mode threshold wasn't shifted positive enough

85/70 HEMT

- Increasing resistance of e-mode → Degradation of inverter characteristics with increasing temperature

85/50 HEMT

- Room T performance improvements from reduced sheet resistance.
- Needs testing over T
- Need to minimize leakage for high V_{in}

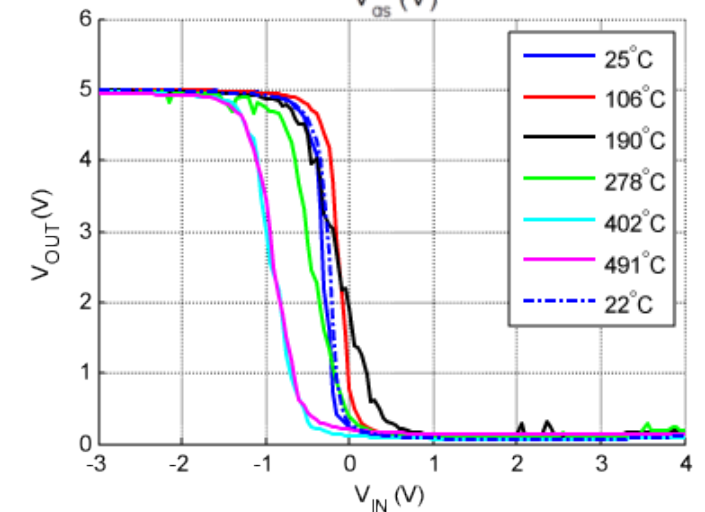
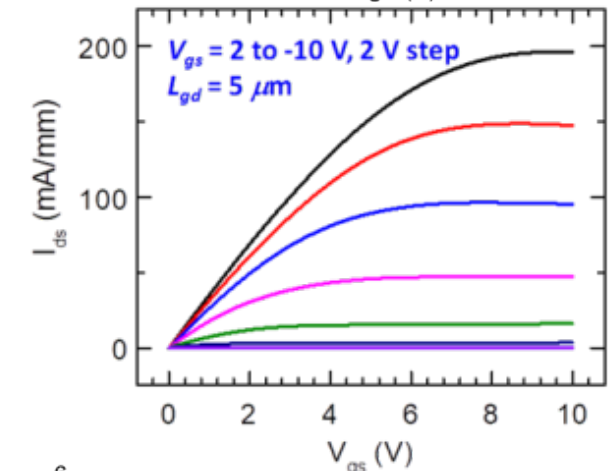
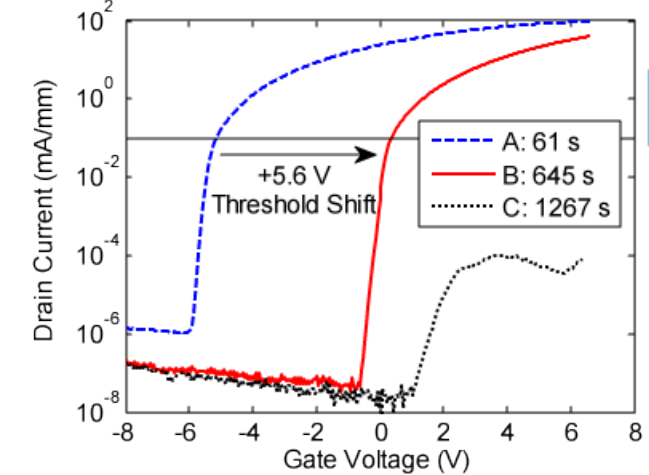
Summary

Ultra-wide bandgap: AlGaN choice material for high temperature and power switching applications

- E-mode: Two approaches for threshold voltage control
- Transport study: Needed high barrier/channel Al contrast
- Ohmic contacts: Improved by modifying epitaxy 85/70 HEMT \rightarrow 85/50 HEMT
- High temperature Gate Metals: Tungsten (2000 Å)

High Temperature Devices

- E-mode/D-mode logic gates
- 45/30 HEMT Inverter tested up to $\sim 500^\circ\text{C}$



AlGaN High Electron Mobility Transistor for Power Switches and High Temperature Logic

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