Invited journal article accepted for publication in upcoming Special Issue on Ion Trap Technology.

Hybrid MEMS-CMOS ion traps for NISQ computing

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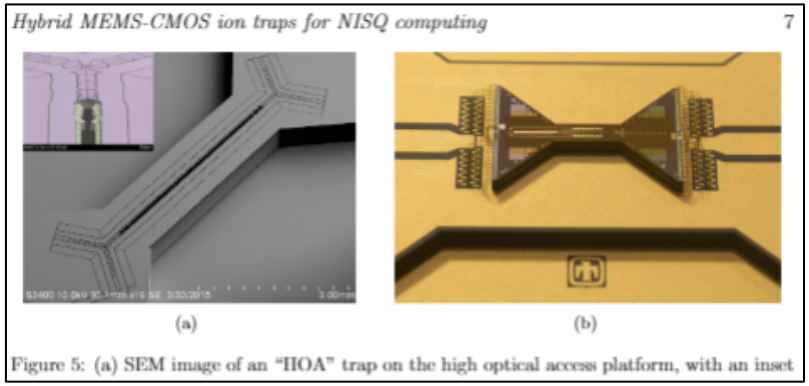

Figure 5: (a) SEM image of an "HOA" trap on the high optical access platform, with an inset

Scientific Achievement

Invited IOP Quantum Science and Technology journal article describing the key requirements and design attributes of microfabricated ion trap devices for NISQ computing has been accepted.
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Significance and Impact

This invited paper describes present limitations and the approaches needed to overcome the challenges facing ion trap device design and fabrication for the NISQ computing regime.

Research Details

- We give an over-view description of Sandia's hybrid MEMS-CMOS ion trap device
- The issues addressed in our article include:
  - How geometric complexity drives the number of metal levels required for ion trap chips
  - How and why routing congestion affects the size and location of shunting capacitors on chip
  - How RF power dissipation can limit the size of the trap array.
- Finally, we give recommendations for future research needed to accommodate the demands of NISQ scale ion traps integrated with additional technologies such as photonic waveguides, modulators and detectors.

U.S. DEPARTMENT OF ENERGY | Office of Science

Work was performed at Sandia National Labs

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- **QSCOUT program directly funded, in part, the fabrication and packaging of, and the experimental work using, Peregrine and Phoenix devices, including the publication of the results of that work.**

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