SAND2021-9884PE

Sandia National Laboratories

Process Development & Forensics of SOI Nanoscale Membranes

Ryan Stewart | Tom Harris | John Nogan | Don Bethke

Introduction & Motivation

Motivation: Understand and measure thermopower in a P-doped quantum material.

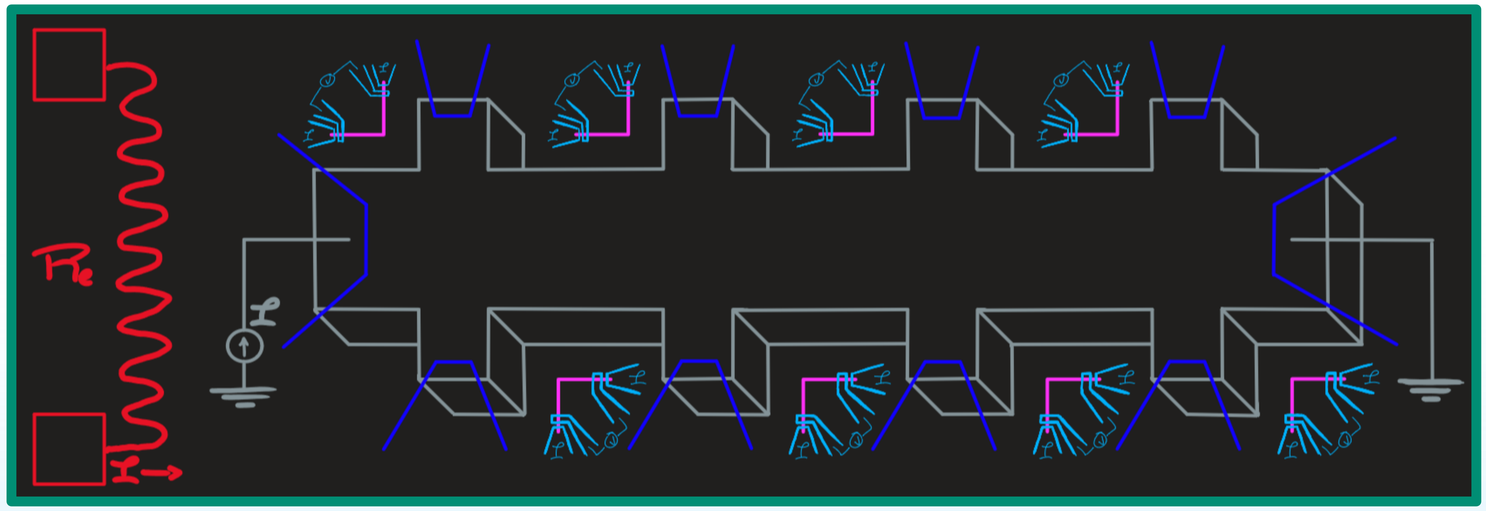
Michelle Simmons: Queen of Quantum Computers

SNL: Shashank Misra & Ezra Bussman

Measurements of Interest:

- Carrier Type, Density, and Mobility
- Seebeck Coefficient

Hall Bar with a Heater and a ton of Thermometers



The Seebeck Coefficient

$$\mathbb{S} = \frac{\partial V}{\partial T} = -\frac{\Delta V}{\Delta T}$$

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Introduction & Motivation Continued

Why SOI?

Thermal Ohm's Law

$\Delta T = R_{th}\dot{Q}$

Where $R_{th} = {}^{L}/_{kA} = {}^{L}/_{kwt}$

$$\Rightarrow R_{th,Si} = \frac{10\mu m}{\left(10\frac{W}{m\cdot K}\right)(500\mu m)(10\mu m)} = 200\,{}^{K}/_{W}$$

Therefore, to achieve a temperature difference of 1 K we will need

$$\Rightarrow \dot{Q}_{Si} = {}^{\Delta T}/_{R_{th,Si}} = \frac{1K}{200\frac{K}{W}} = 5mW$$

Cryogenic System Power Output Limits:

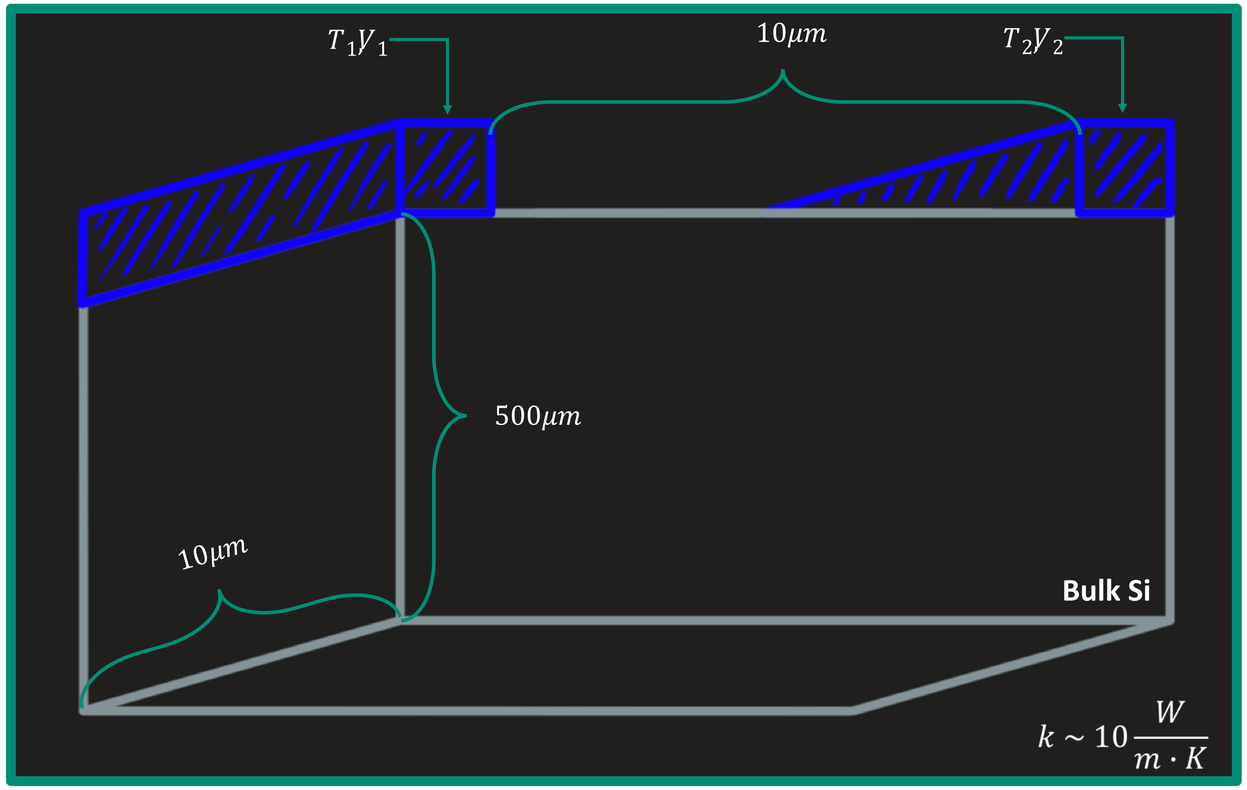
➔ ^{3}He can produce $40\mu W$ of cooling power

➔ Dilution Fridge can produce between $200\mu W$ and $400\mu W$ of cooling power

& if we compare

$t_{Si} = 500\mu m$ vs. $t_{SOI} = 250nm$

Nominal Dimensions for Optical Lithography Patterning



$\Rightarrow \dot{Q}_{SOI} = 2.5\mu W$ (2000 times less!!)

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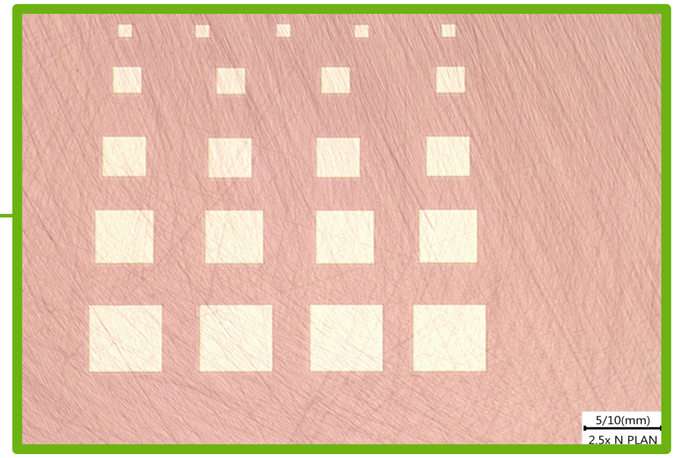
Approach

QUESTION: How big of a membrane can we make?

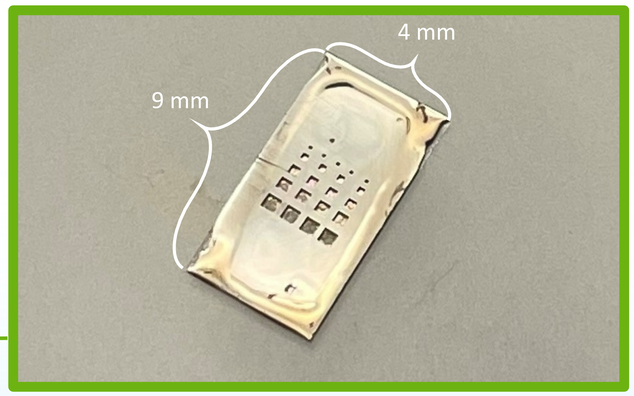
My Process Flow

- Clean & Strip
- Spin Coat & Soft Bake
- Expose & Develop
- Attach to a Sapphire Carrier
- Bosch Etch
- Analyze Results



Developed Pattern on the Handle prior to sub mounting

Substrate attached to Sapphire Carrier before Etching



Substrate attached to Sapphire Carrier after Etching

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Process Development & Forensics of SOI Nanoscale Membranes

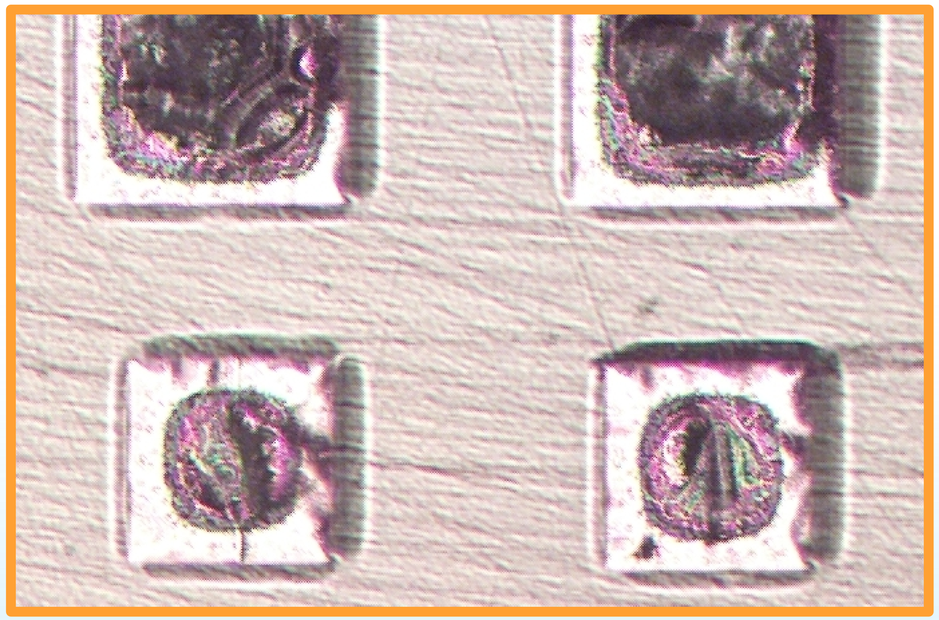
Challenges

1.) Depleted Resist & Blown Out Membranes

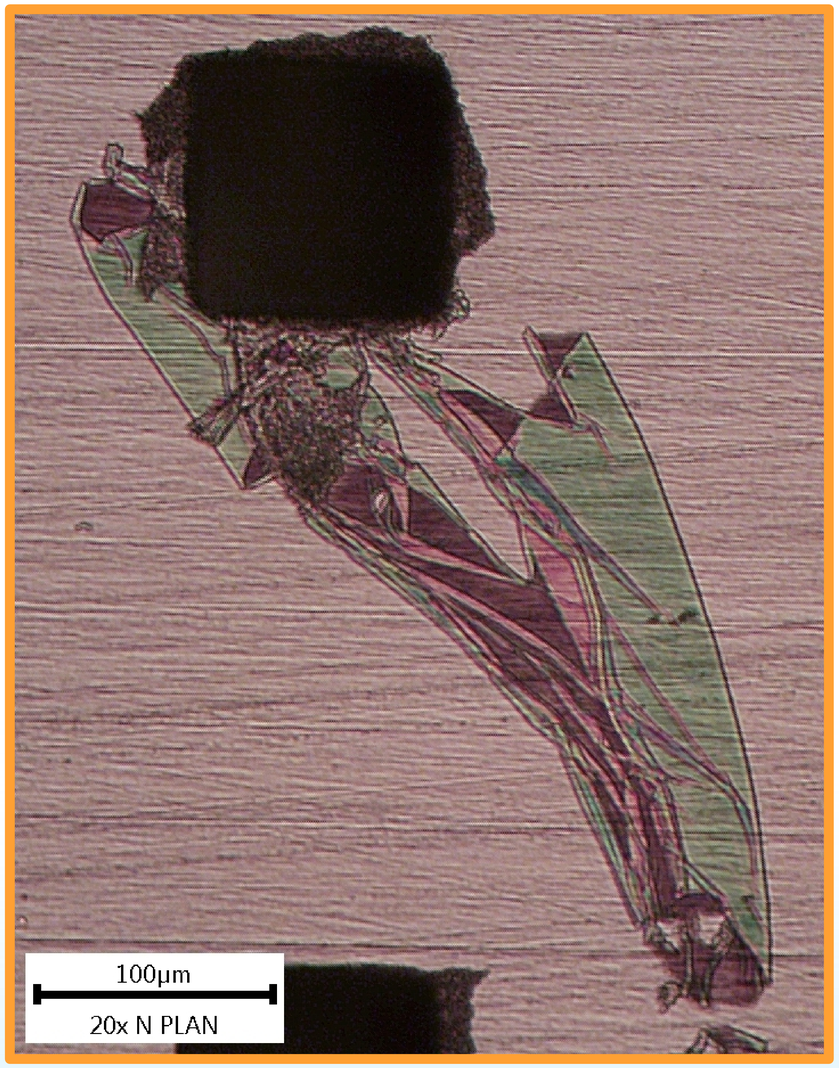
Our Response:

1) Thicker Resist & Si Etch Rate Test
2) Bosch Etch with a 2 Phase Process
3) Add Protective Coating to the Device Layer, such as ProTEK B3

2.) Directional Control Issue



3.) Mechanical Failure Evidence



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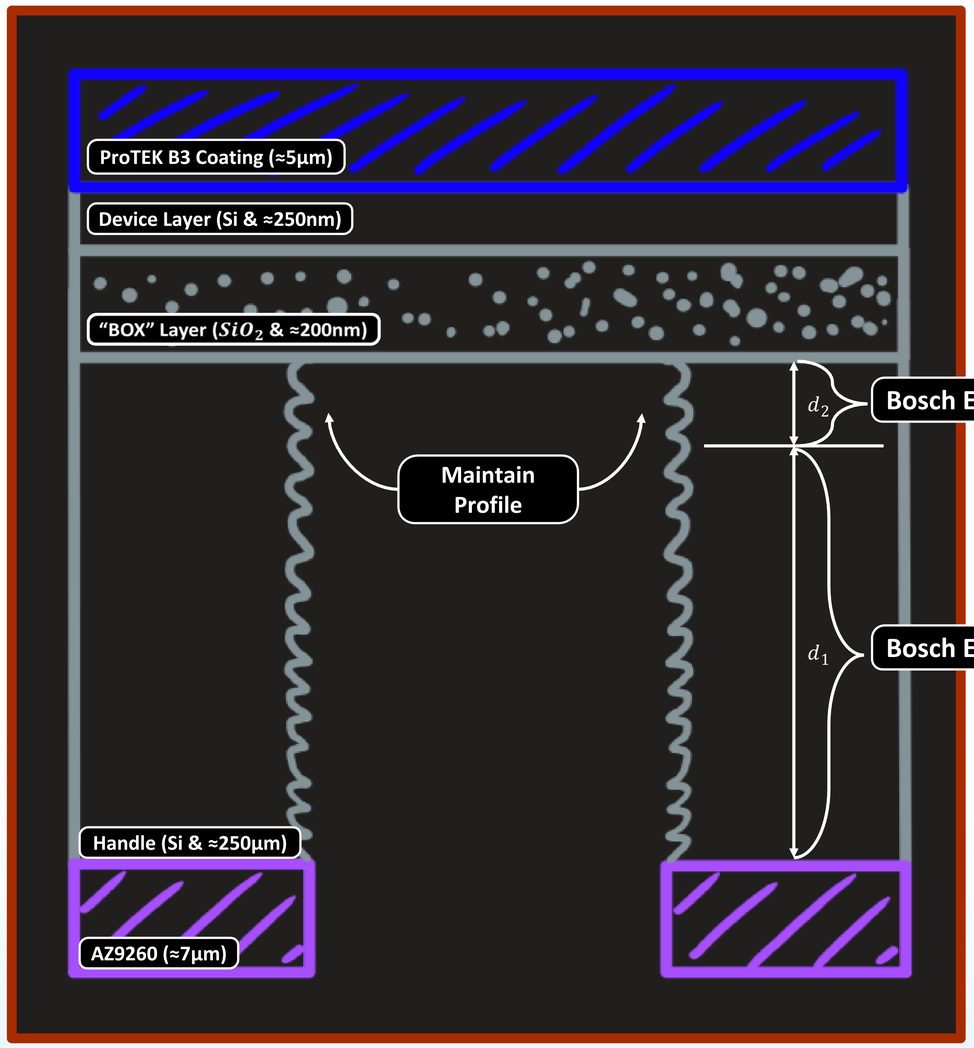
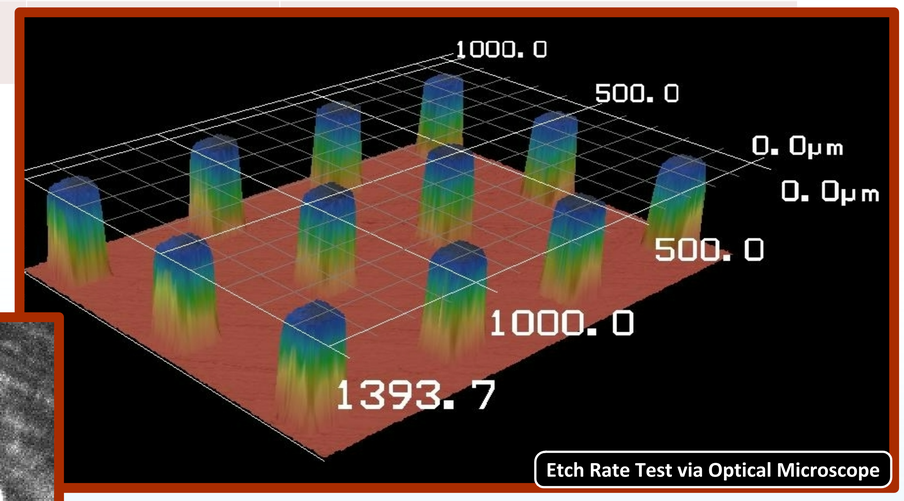
Results

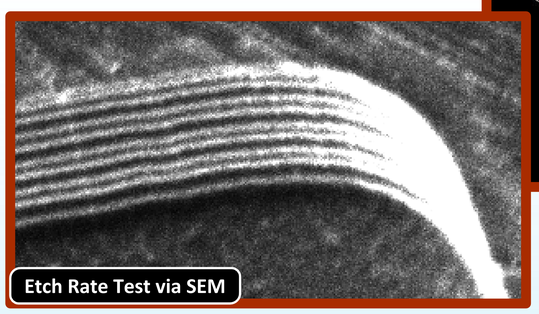
Quantified Etch Rates & Developed Lithography and Etching Recipes



Test	Phase	Material	Etch Rate
#2	#1	Si	$\sim 0.604 \frac{\mu m}{cycle}$
#6	#1	SiO_2	$\sim 4.3 \frac{nm}{cycle}$
#6	#1	$AZ9260$	$\sim 15 \frac{nm}{cycle}$
#7	#1	Si	$\sim 0.623 \frac{\mu m}{cycle}$
#11	#2	Si	$\sim 0.762 \frac{\mu m}{cycle}$
#13	#2		



Etch Rate Test via Optical Microscope


Etch Rate Test via SEM

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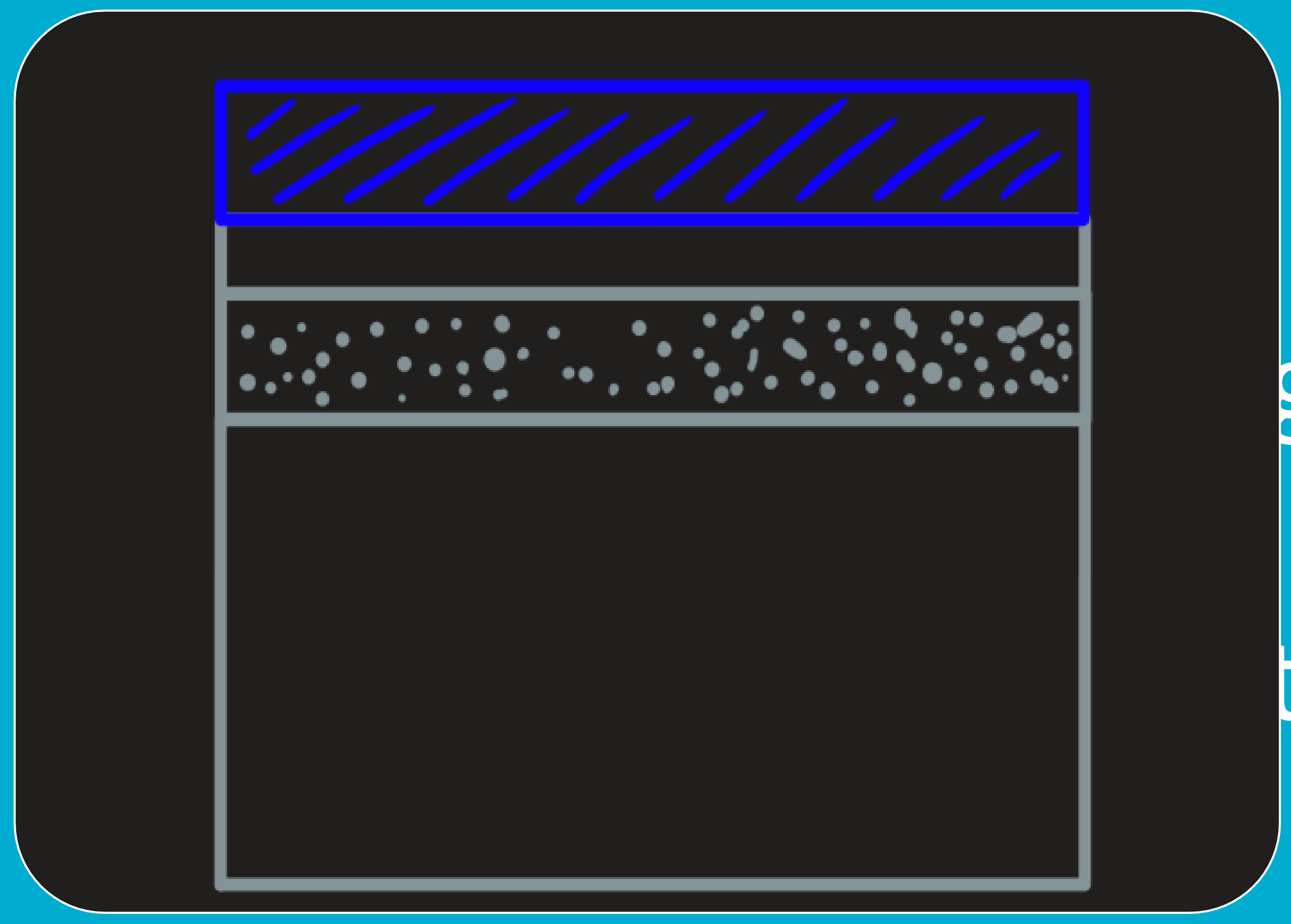
Ongoing & Future Work

Using a Polymer as Structural Support



- ➔ Spin coat the device layer before spin g the resist on the handle.
- ➔ For Example, a ProTEK B3 Coating is used tect delicate front-side circuitry during back-side micromachining.

Use an SOI with a thicker BOX and Device

- ➔ Pro: Increases the structural integrity
- ➔ Con: New process needed for embedding Phosphine

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