A MEMS Gyroscope for Reliable Long Duration Measurement While Drilling at 300°C

Final technical report draft

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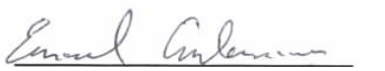
Signature  _____ Date__1/24/2022_____

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Disclaimer

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Executive Summary

The 300°C Microelectromechanical system (MEMS) gyroscope project aims to contribute to DOE's goal of increased geothermal drilling efficiency by 2025 through the development of a 300°C MEMS gyroscope for Measurement While Drilling (MWD). At the conclusion of the 2-year project, the team will develop a 300°C capable MEMS gyroscope containing GE's patented Multi-Ring Gyroscope Transducer (MRGT) design, custom Silicon-On-Insulator (SOI) based frontend and feedback control electronics, and with demonstrated functionality and lifetime beyond 1000 hours.

The project is divided into two budget periods with Go/No-Go decision at the end of the first budget period. The goal for the first budget period is to establish the feasibility of the MRGT and electronics design for meeting the 300°C performance requirements. The goal for the second budget period is to integrate the MRGT with the SOI-based application specific integrated circuit (ASIC) and demonstrate capability to operate at 300°C for 1000 hours.

In Budget Period 1 we met the phase 1 goal. We successfully validated the combined MRG, electronics and packaging capability entitlement to achieving 0.5 degrees azimuth uncertainty while enabling operation at significantly higher temperatures than the state-of-the-art.

In Budget Period 2, we successfully completed the integration of the MRGT and ASIC with associated high temperature, high reliability packaging to demonstrate the performance and functionality of the integrated gyroscope across the temperature range from room temperature to at 300°C. Furthermore, the team demonstrated operating life of >1,000 hours at 300°C, thus providing a validation of application-relevant lifetime capability.

Significant findings of project include:

- **10X performance improvement over state-of-the-art**
  - The GE team has achieved a bias instability of 0.01 °/hr at 25°C and angular random walk of 0.003°/rt(hr). This is a 10X improvement over state-of-the-art MEMS gyroscopes that are limited to 0.1 °/hr and 0.01°/rt(hr), and enables azimuth accuracy <0.25°.
  - This substantial achievement positions this MEMS-based solution to compete with conventional, high-cost gyroscope technology but with the size, cost, and reliability advantage of MEMS.
- **300°C operation, >600°C survivability**
  - The GE team validated the design of GE's gyroscope by demonstrating operation at 300°C. Furthermore, survivability of the packaged gyroscope was demonstrated to 600°C during which we observed no hysteresis or any sign of performance degradation. These results exceed the temperature capability of existing MWD tools for oil and gas drilling and

enabled the successful demonstration of 1,000-hour operation at 300°C of the integrated gyroscope system comprising the MRGT and ASIC.

- **New gyroscope package with high reliability, 10X volume reduction**
    - We developed a new wafer-level package (WLP) whose integrity improves with exposure to high temperatures (during processing the package is annealed at 1100°C to form covalent silicon-silicon bonds, subsequent annealing improves vacuum integrity by gettering residual oxygen). Besides enabling high reliability and long lifetime, this package has the added benefit of a small form factor (approximately 10X reduction in volume relative to state-of-the-art MEMS gyroscopes using metal-can lids).
- **Highly integrated, high temperature capable SOI-based electronics design**
    - GE in collaboration with Inertial Wave has successfully designed and simulated the silicon-on-insulator based control ASIC. The design incorporates advanced algorithms and analytics that enable temperature compensation in addition to modern control algorithms (e.g., quadrature tuning). The design requirements and capabilities were validated using board-level electronics. Simulations show our design meets all application requirements. The control ASIC design has been fabricated and tested across the full temperature range of interest up to 300°C.
- **High temperature, high reliability MEMS gyroscope system, >150°C temperature capability increase over state of the art.**
    - The integrated functionality and lifetime of the developed MRGT and ASIC devices was shown to function as intended across the temperature range of interest and >1,000 hours of operating lifetime at 300°C was demonstrated.

In addition to the significant findings highlighted here, the team has also contributed to DOE's goal of advancing scientific understanding and industry knowledge through several publication and conference presentations that are covered in detail in Publications, Abstracts and Presentations section.

Project Overview

Directional drilling is the practice of steering a wellbore along a predefined trajectory leading to a subsurface target (1).The 300°C MEMS gyroscope project aims to advances the state of the art, contributing to DOE's goal of increased geothermal drilling efficiency by 2025 through the development of a 300°C gyroscope for Measurements While Drilling (MWD) orientation tool, while alleviating the magnetic interference, temperature limitation, size and power constraints imposed by today's magnetometer-based systems. At the conclusion of the 2-year project, the team has developed and demonstrated a 300°C capable gyroscope containing a high temperature optimized Microelectromechanical system (MEMS) Multi-ring Gyroscope Transducer (MRGT) and Silicon-On-Insulator (SOI) based frontend and feedback control Application Specific Integrated Circuit (ASIC), and with functionality and lifetime beyond 1000 hours.

The project was divided into four tasks spanning two budget periods with Go/No-Go decision at the end of the first budget period, and regularly scheduled Status Update meeting every six months.

The goal for the first budget period is to establish the feasibility of the MRGT and electronics design to meet functional and performance requirements at 300°C, and validate gyroscope component performance capabilities. The technical work was organized into two main tasks and a number of subtasks under each. Task 2 constituted the analysis and design aspects of the MRGT and ASIC development. Task 3 covered the component fabrication and testing. The task structure of the first budget period is shown in Table 1.

Table 1: First budget period task description

Task/Subtask		Description
2.1		Assess High Temperature Performance, Reliability Risks and Requirements for MEMS Gyroscopes
	2.1.1	Azimuth uncertainty definition will be defined and flow-down to critical MRGT and electronics angular random walk, bias instability and noise specifications).
	2.1.2	Benchmark commercial devices including performance and temperature capability.
2.2		Assess MRGT Characteristics and Performance at High Temperature
	2.2.1	Perform high temperature characterization of MRGT at probe station.
	2.2.2	Develop a 300°C device testing platform using localized heating of MRGT device.
	2.2.3	Evaluate temperature performance of MRGT.
2.3		Design High Temperature Optimized MRGT
	2.3.1	Perform design optimization and modeling of MRGT for 300°C operation.

2.3.2 Assess the process improvement and risk required by the MRGT design improvement.

2.4 Develop Requirements for MRGT Frontend, Control and Compensation ASIC

2.4.1 Identify key electronics performance metrics for MRGT interrogation, control and compensation electronics.

2.4.2 Design and build of electronics process evaluation test circuits.

2.4.3 Conduct electronics design tradeoffs and define electronics architecture given system requirements and process constraints.

2.4.4 define electronics performance entitlement and compare with the electronics requirements.

3.1 Fabrication and Testing of High Temperature MRGT

3.1.1 Fabricate high temperature MRGT.

3.1.2 Perform die level characterization of the fabricated device at room temperature.

3.1.3 Perform die level characterization of the fabricated device at high temperature.

3.2 Develop High Temperature Frontend and Control Electronics

3.2.1 Conduct interrogation and control electronics functional modeling.

3.2.2 Complete Transistor level design and validation through circuit simulation.

3.2.3 ASIC layout and fabrication.

3.2.4 Package ASIC and build evaluation platform.

3.2.5 ASIC performance and functionality evaluation.

3.3 Design and Build High Temperature System Test Environment

3.3.1 Package and assemble high temperature gyroscope for testing.

3.3.2 Develop functionality and reliability test plan and define performance metrics and success criteria.

3.3.3 Design and build temperature capable test platform for system evaluation.

In the second budget period, the integrated gyroscope system (MRGT, Electronics and high temperature capable packaging) performance and capability to operate for 1000 hour at 300°C were tested and the capability of a high temperature gyroscope system was demonstrated.

The technical work for the second budget period was organized into a single technical task (Task 4) that included the integration and test of the components developed in the first budget period. Task 4's three main objectives are:

1. System integration of MRGT and ASIC components
2. Functional and performance testing of the integrated gyroscope
3. Lifetime testing of the integrated system

The task structure of the first budget period is shown in Table 2.

Table 2: Second budget period task description

Task/Subtask	Description
4.1	Demonstrate High Temperature Gyroscope System in Laboratory Test Environment
4.1.1	Conduct Integration testing of the gyroscope system.
4.1.2	Performance characterization versus temperature (20°C to 300°C).
4.1.3	Reliability testing at 300°C for a minimum of 1000 hours

During the period of performance of the project, the high temperature MRGT and ASIC were developed and validated on a component level. The MRGT and ASIC components were then integrated with high temperature packaging and supporting passive devices to further advance the technology readiness level (TRL) and demonstrate lifetime and temperature capability of the gyroscope system as seen in Figure 1.

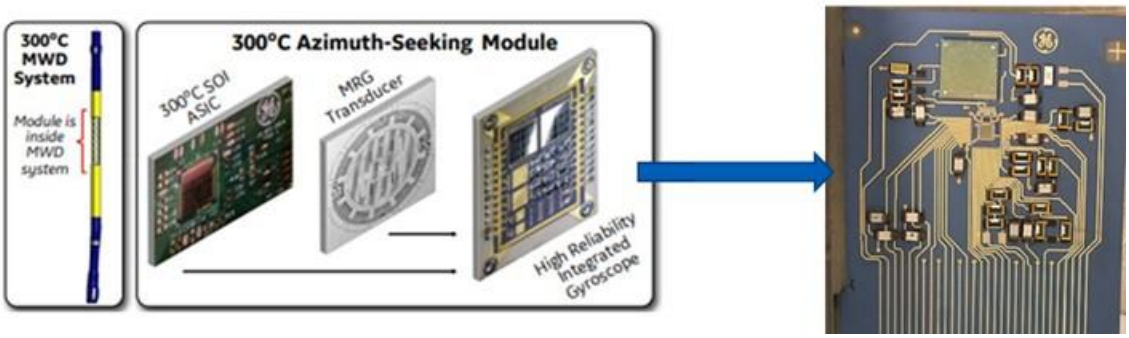


Figure 1 Progress and TRL advancement from concept to 300°C capable gyroscope with demonstrated >1000 hours of lifetime

Summary of project accomplishments.

Performance entitlement validation

- ✓ MRGT device design
- ✓ Achieved state of the art room temperature navigation grade capability
- ✓ Developed physics -based model of performance dependence on temperature
- ✓ Validated model with temperature measurements

Electronics capability

- ✓ Developed electronics architecture to support driving, sensing and control of MRG

- ✓ Validated performance in board-level electronics
- ✓ Achieved design electronics noise below mechanical noise

Packaging capability

- ✓ Developed 300°C+ capable packaging approach
- ✓ Validated device packaging in high temp tests to 300°C
- ✓ Mapped packaging design to 300°C for 1000 hours capable design rules established in prior work

Fabrication capability

- ✓ Developed reliable wafer level packaging process capable of surviving 600°C
- ✓ Achieved device yield of 80%

Project achievements significance and impacts are summarized in Table 3

Table 3 Project accomplishments and significance

Aspect	Improvement	Significance	Impact
MRGT design	GE's Optimized multi-ring gyroscope design	Achieved state-of-the-art room temperature bias instability of 0.01deg/hr and ARW of 0.003deg/rt(hr), an order of magnitude better performance than commercially available MEMS gyroscopes	System accuracy
System	Demonstrated functionality to 300°C	~200°C higher operating temperature than commercially available devices	Temperature capability
Packaging	WLP wafer bonding packaging process	Increased quality factor by >4X. Achieved quality factor of 13,000 --> Reduced device noise by 2x	System accuracy
Fabrication	MEMS/ASIC process	System size reduction: MRGT is 10mmx10mm, ASIC is 3mmx3mm	Compatibility with downhole tool size
MRGT design + Electronics	In situ frequency matching and quadrature nulling	Increase scale factor by >100x	System accuracy

Electronics	Drive level temperature compensation	reduced scale factor deterioration over temperature by >4x from 25°C to 200°C	System accuracy over temperature
Fabrication	Fabrication bonding and etch process improvements	Increased device yield from 50% to 80%	Commercial viability
Fabrication	High temperature capable fabrication process	Demonstrated survivability to 600°C	Reliability at temperature
Packaging	High temperature capable substrate, attach and interconnect	Reliable long-term operation at 300°C	Reliability at temperature
Electronics	Silicon-On-Insulator electronics	Reliable 300°C + capable electronics >150°C increase over conventional Si electronics, and 100°C increase over HT optimized Si electronics	Temperature capability
Fabrication and packaging integration	MRGT signal redistribution routing layer	Demonstrated routing simplification between ASIC and MRGT. Low crosstalk, compact footprint routing minimizes signal crossovers and parasitics	Reliability, performance and system miniaturization
Packaging	High temperature multi-layer substrate	Substrate size reduction and signal routing simplification	System performance and temperature capability
Integrated system	MRGT, ASIC and packaging design	Demonstrated functionality and performance from room temperature to 300°C	Technology demonstration
Integrated system Lifetime	High temperature, high reliability MRGT and ASIC components + packaging	Demonstrated >1500 hours of operating life at 300°C	Technology viability for long term operation

Significant findings and achievements

10X performance improvement over the state-of-the-art

The GE team has successfully developed the MEMS based MRGT capable of azimuth-seeking in MWD applications at 300°C. The MRGT prototype has been demonstrated to achieve bias instability of 0.01 deg/hr and angular random walk (ARW) better than 0.003 °/rt(hr), capable of meeting azimuth finding accuracy better than 0.25° at room temperature (the azimuth accuracy at 300°C is expected to be better than 0.5°, which we'll discuss in more detail below). A picture of the MRGT wafer after processing and a single MRGT die is shown in Figure 2 A-B, and an example Allan deviation measurement showing this level of performance is shown in Figure 2C.

To put this level of performance in perspective, part of Task 1 was dedicated to benchmarking state-of-the-art commercial-off-the-shelf gyroscopes (COTS). From our survey results shown in Figure 3, the highest performing MEMS gyroscopes have bias instabilities of approximately 0.1 °/hr and angle random walk of 0.01 °/rt(hr) at room temperature. Therefore, the performance demonstrated by the GE MRGT on this program represents a 10X improvement over the state-of-the-art COTS devices.

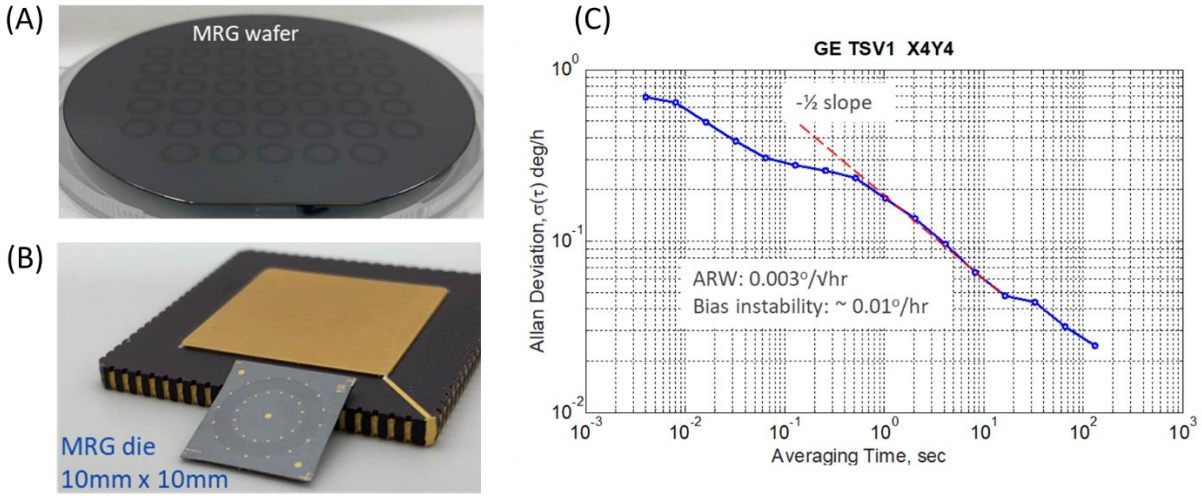


Figure 2 (A) Wafer containing 45 MRGT die. (B) Single MRGT die. (C) Allan Deviation measurement on GE's MRGT prototype, showing angle random walk of 0.003 °/rt(hr) and bias instability of 0.01 °/hr.

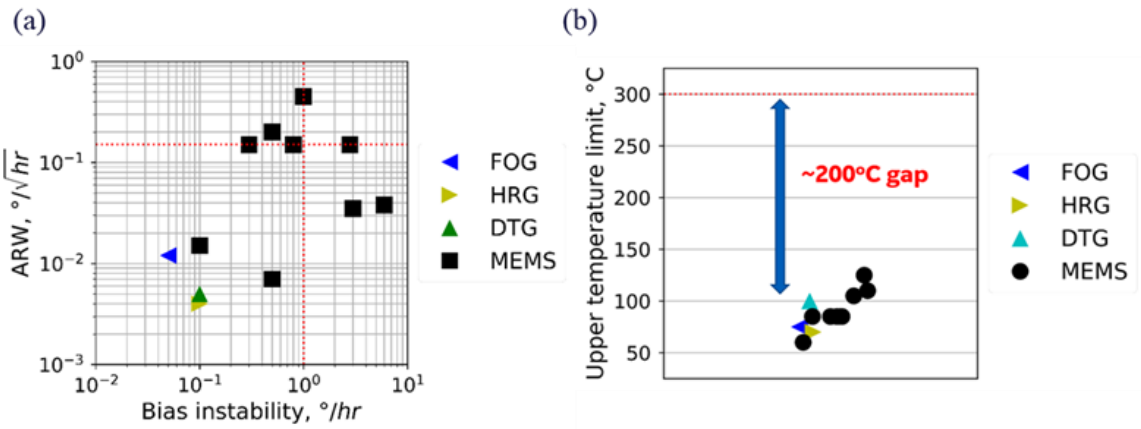


Figure 3 Performance and temperature capability of COTS devices surveyed. (a) Best performing devices have bias instabilities approaching 0.1 deg/hr at room temperature. (b) None of the devices can operate at 300°C - there is ~200°C capability gap

Another important observation in the COTS survey is the temperature capability of COTS MEMS gyroscopes. All the devices we surveyed are based on conventional silicon processing and are therefore limited to low temperature operation (<120°C). Our discussion of performance requirements and survey of the published MEMS devices has led to the discovery that no existing commercial MEMS gyroscope can reliably operate at 300°C for 1000+ hours while maintaining the sub-degree-per-hour accuracy needed for MWD. This is a critical technology that needs to be invented and developed.

The demonstrated performance improvement over state of the art is achieved through the combination of the MRGT device design and the sensing, tuning and control capabilities enabled by the electronics architecture as is described below in the MRGT Device Design and Capability and the High Temperature ASIC design sections.

300°C operation, 600°C survivability

We validated the temperature design of the MRGT by completing tests at elevated temperatures. The MRGT scale factor has been measured from room temperature to 300°C validating functionality and response to rotation rate across the temperature range and illustrated in Figure 15. The WLP package was tested from room temperature to 600°C, and device resonance was recorded across the temperature range as can be seen in Figure 4 and Figure 20 below. The observed resonance across the temperature validated the WLP capability to maintain vacuum and the device's robustness at extreme temperature.

New gyroscope package with high reliability and 10X volume reduction

The bare die-on-board packaging approach developed, coupled with the WLP vacuum package and a highly integrated readout and control ASIC architecture has enabled a highly miniaturized, high temperature capable gyroscope. The elimination of second level packaging for the MRGT and the ASIC results in an MRGT device that is approximately 10mmx10mm in size and an ASIC that is approximately 3mmx3mm. The combined substrate and MRGT and ASIC thickness is approximately 1mm in thickness compared to approximately 18mm for gyroscopes and associated electronics utilized in oil and gas application. Additional detail on packaging is addressed more fully in the Device packaging advancements and the ASIC packaging sections.

Highly integrated, high temperature capable SOI-based electronics design

In the first budget period, the team completed the development of the electronics architecture capable of meeting the excitation, sensing and control requirements, while achieving the system noise and performance across the temperature range of operation. The electronics architecture capabilities were first corroborated through functional simulations, and further refined and implemented utilizing board-level electronics. Performance testing conducted during the first budget period utilized these board-level electronics to further validate the functionality and performance. The validated board-level design was then converted to an integrated ASIC design in an SOI process capable of operating at 300°C. Functional simulations across operating temperatures and fabrication corners were utilized to validate the ASIC design prior to release to fabrication. The highly integrated ASIC comprises the functionality of the board level electronics in a 3mmx3mmX0.5mm semiconductor chip.

Detailed technical achievements

This section covers the detailed technical achievement for the major project components which include the MRGT device design, fabrication, electronics, component test, system integration and system test.

MRGT Device Design and Capability

This section of the report details the design and development steps and advancements achieved in the MRGT device to enable the performance needed to support the geothermal downhole navigation and orientation needs.

MRGT Device critical performance parameters to meet requirements

MRGT is a type of Coriolis Vibratory Gyroscope (CVG) that uses a vibrating multiple-ring structure to determine the rate of rotation. MRGT takes advantage of a pair of degenerate resonance modes of a multiple-ring structure, so called 'wineglass modes' (specifically, wineglass mode 3). By design, these two resonance modes have identical frequency and identical mode shape, rotated 30° from each other. In operation, one of the modes is excited into resonance (drive mode). Rotation about the sensitive axis will produce a Coriolis force which transfers the energy from one of the wineglass modes to the other. The rate of rotation is determined by measuring the amplitude of the 2nd wineglass mode (sense mode) induced by the Coriolis force. Because the two wineglass modes have identical frequencies, this kind of gyroscope architecture is also called mode matching operation. However, due to manufacturing and material imperfections, the MRGT fabricated could have a small frequency split between the two wineglass modes. The amount of frequency split can directly affect the gyroscope scale factor, as shown in Eq. (1)

$$Scale\ factor\ = \mathrm{A}\mathrm{X}_d Q_{eff}$$

$$Q_{eff} = \frac{1}{\sqrt{\left[1-\left(\frac{\omega_d}{\omega_s}\right)^2\right]^2+\left(\frac{1}{Q}\frac{\omega_d}{\omega_s}\right)^2}} \qquad (1)$$

where A is the geometrical factor, dependent on design, X_d is the drive amplitude, ω_d is the drive mode resonant frequency, ω_s is the sense mode resonant frequency. Q is the quality factor. As can be seen from Eq.1, in order to maximize the gyroscope scale factor, the gyroscope will should have large drive amplitude, high mechanical Q and small frequency split. For the gyroscope which is limited by the electronics noise,

increasing the scale factor will directly improve the signal-to-noise ratio (SNR), resulting in lower gyroscope ARW.

In practice, drive amplitude is limited by the device geometry. Having a low frequency split between drive and sense modes is critical to maintain high sensitivity. For example, if Q is 10,000, a frequency split of only 10 Hz will reduce Q_{eff} to 1500.

In order to be able to measure the earth rotation, the MRGT will also need to be designed to have low noise. The noise characteristics of the CVG is indeed quite complex, consisting of different noise spectral density at different frequency ranges. However, for the targeted application of azimuth finding for geothermal drilling, with a carouseling time of less than 5 minutes, our previous test data (refer to the Allan Deviation data) on MRGT devices shows the noise of MRGT is dominated by white noise within that target integration time of 5 minutes.

For the gyroscope which is limited by the thermal mechanical noise of the transducer itself, ARW can be calculated as

$$\Omega_n = \frac{1}{\mathrm{k}_a X_d}\sqrt{\frac{k_B T}{mQ\omega_d}} \qquad (2)$$

Where Ω_n is the Angle Random Walk (ARW), X_d is the modal amplitude, k_a is angular gain (Bryan factor) which is related to the MRGT geometry and resonance mode, k_B is the Boltzmann constant, T is the operating temperature, m is the modal mass, Q is the quality factor, ω_d is the drive mode resonant frequency.

To achieve <1^o azimuth finding accuray at 300°C and 5 minutes integration time, the targeted ARW of MRGT is estimated to be < 0.03^o/√hr. We estimate that such target can be achieved with 0.5um gyroscope drive amplitude and quality factor >3500.

Figure 4 shows the Q-factor variation for a wafer-level sealed MRGT up to 600^{o}C. Two high temperature cycles were performed to show the device had no degradation and the device sealing integrity has not been compromised. For reference, the curves of TCQ (thermal coefficient of quality factor) of -0.5 and -3.5 were also shown on the same plot. Literature suggests the TCQ of -0.5 is related to the air damping inside the gyroscope cavity due to imperfect vacuum. TCQ of -3.5 is related to the TED loss (2). Based on Figure 4, the MRGT Q-factor at 300°C will decrease to be approximately 1/3 of the Q-factor at room temperature. According to (1), the ARW will degrade by 2.4 times when going from room temperature to 300°C.

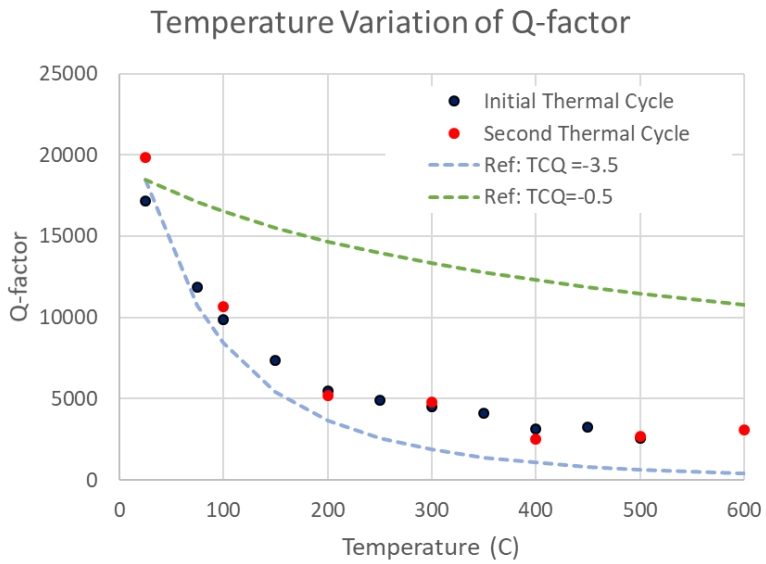


Figure 4 Wafer-level packaged MRGT Q-factor characterization over temperature

The accuracy of azimuth finding is directly related to the gyroscope bias instability. We have used two transfer functions for azimuth finding; the first is the ISCWSA error model and the second is a custom transfer function that uses a GE proprietary carouseling algorithm. The results from both algorithms are shown in Figure 5. According to our algorithm study, we need 0.2 °/hr bias instability to support 0.5 degree azimuth uncertainty.

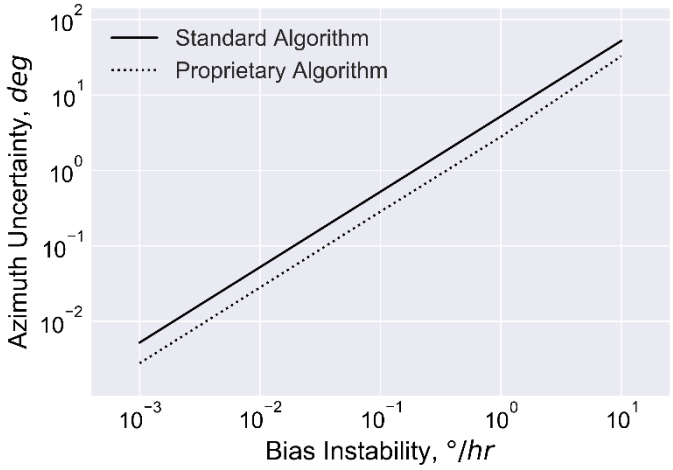


Figure 5 Azimuth uncertainty as a function of the bias instability of the gyroscope

Figure 6 showed the test results of the Allan Deviation of the GE MRGT at room temperature. In Figure 6, the bias instability of a gyroscope can be found as the lowest point while ARW is obtained by typically finding the -1/2 slope line at 1 second point. For practical application, the total azimuth finding operation will need to be finished in less than 5 minutes. Therefore, we require the Allan Deviation of bias at 100 second point support 0.5-degree azimuth uncertainty.

Our test data, as shown in Figure 6, suggested the MRGT is dominated by thermal-mechanical noise (white noise, -1/2 slope in Allan Deviation plot) within the 100 seconds of integration time needed to complete azimuth finding operation. In order to reach 0.2 °/hr at 100 seconds at 300°C for 0.5-degree azimuth uncertainty, we need to reach 2 °/hr at 1s at 300°C or 0.83 °/hr at 1s at room temperature (with the expected 2.4x ARW degradation from room temperature to 300°C). The MRGT test data suggests the Allan Deviation at 1s at room temperature is within this range.

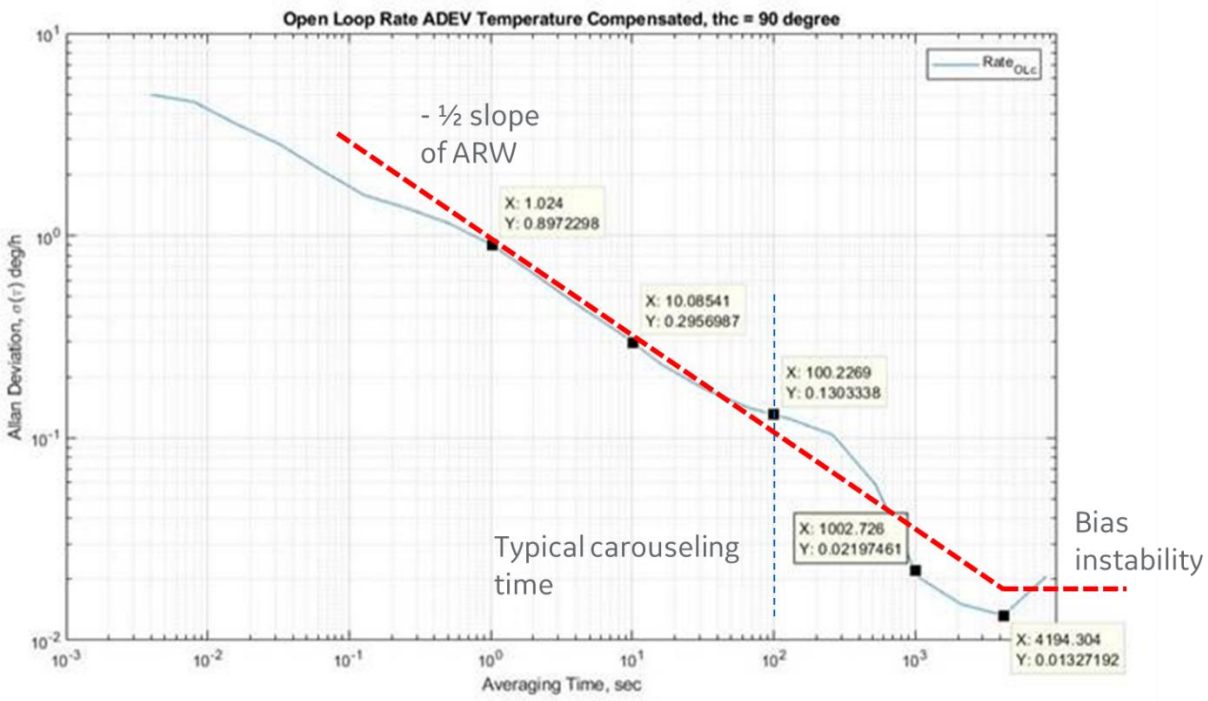


Figure 6 Allan Deviation of the MRGT at room temperature showing the relationship between ARW, -1/2 slope, bias instability and the 100s integration time for carouseling

MRGT design parameters

As seen from Eq.1 and Eq.2, the quality factor of the gyroscope directly impacts the gyroscope scale factor and ARW. In order to maximize scale factor and achieve lower

ARW, the quality factor of the gyroscope would prefer to be >3500. Q-factor is related to the damping of the gyroscope resonator. Multiple mechanisms will contribute to the energy loss. Among those, the leading damping loss mechanisms are air damping, thermoelastic damping (TED), anchor loss and surfacing loss. Air damping is a well know energy dissipation mechanism, caused by the collision of air molecules with the resonator. The MRGT is sealed in a vacuum cavity in order to minimize the air damping. TED is due to energy dissipation cause by the thermal transport across the thermal gradient caused by the strain gradient in the resonator. Figure 7 shows the finite element analysis modeling result of the quality factor for the MRGT caused by TED at room temperature (Q_{TED} = 22,000).

The total Q-factor of MRGT resonator can be written as

$$\frac{1}{Q_{total}} = \frac{1}{Q_{air}} + \frac{1}{Q_{TED}} + \frac{1}{Q_{others}} \qquad (3)$$

The anchor loss and surface loss are complex to model so that a quantitative predictive model is not available. Nonetheless, we can infer the contributions from different damping mechanism by the experimental testing. Experimental data shows the MRGT has a quality factor of 12,000 in a vacuum chamber which is evacuated to pressures less than 10mTorr. Under those conditions, assume $1/Q_{air} << 1/Q_{TED}$. In this case, the combined anchor loss and other loss mechanisms contribute to slightly less than half of the total energy loss, while TED makes up slightly more than half of the total energy loss (Q_{others} = 26,400). When the MRGT was sealed in a LCC84 package, the Q-factor degraded to 7,500. From Eq. (3), the Q-factor cause by air damping (due to the imperfect vacuum inside the LCC84 package) was calculated to be Q_{air} = 20,000).

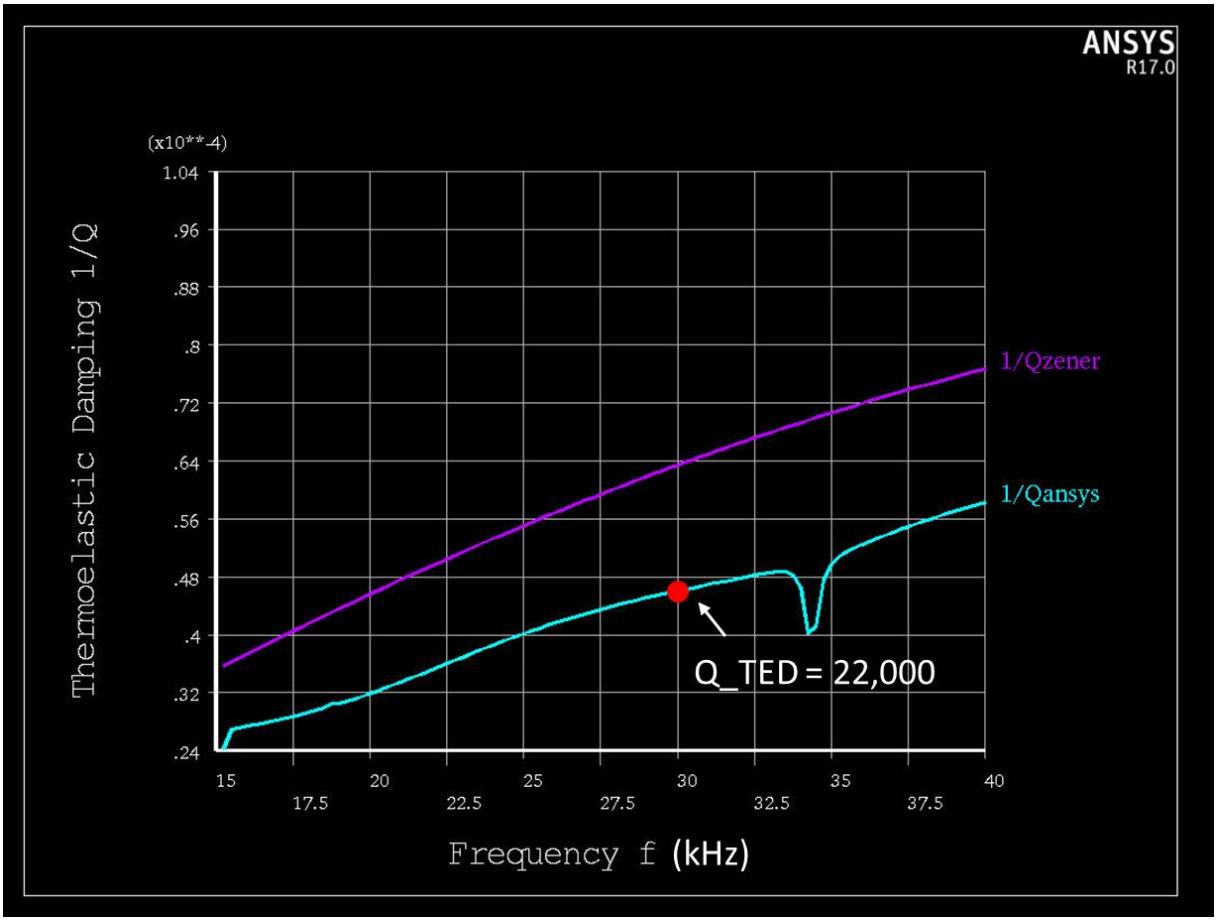


Figure 7 Finite element simulation of the MRGT thermoelastic damping.

Temperature will have negative impact to the MRGT quality factor. Reference (3) suggested the different relationship between Q-factor and temperature among the different damping mechanism where

$Q \propto \frac{1}{T^{0.5}}$, for air damping (TCQ = -0.5)

$Q \propto \frac{1}{T^{3.5}}$, for thermoelastic damping (TCQ = -3.5)

The literature did not list the temperature coefficient of Quality (TCQ) factor for other mechanisms, but from our test data (shown in Figure 8), we conclude the TCQ for other damping mechanisms should fall within -0.5 and -3.5. Figure 8 shows our measurement of Quality factor in the vacuum station from room temperature to 200°C. For comparison, two separate curves (TCQ=-0.5 and TCQ=-3.5) are also included. The TCQ of our MRGT was measured to be -1.63. We can therefore extrapolate with TCQ of -1.63 to predict the quality factor of 4,000 at 300°C. This meets our design target Q of 3,500 at 300°C.

A more conservative estimation will be to extrapolate from the Q_{TED} = 22,000 at room temperature with the worst case TCQ of -3.5, resulting Q_{TED} of 2, 200 at 300°C. The impact of air damping over temperature can also be extrapolated from Q_{air} = 20,000 at room temperature with TCQ of -0.5, to Q_{air} =of 14,400 at 300°C. Therefore, our conclusion is that the TED will be the dominant damping mechanism at 300°C if there are no other outgassing mechanisms induced by the high temperature.

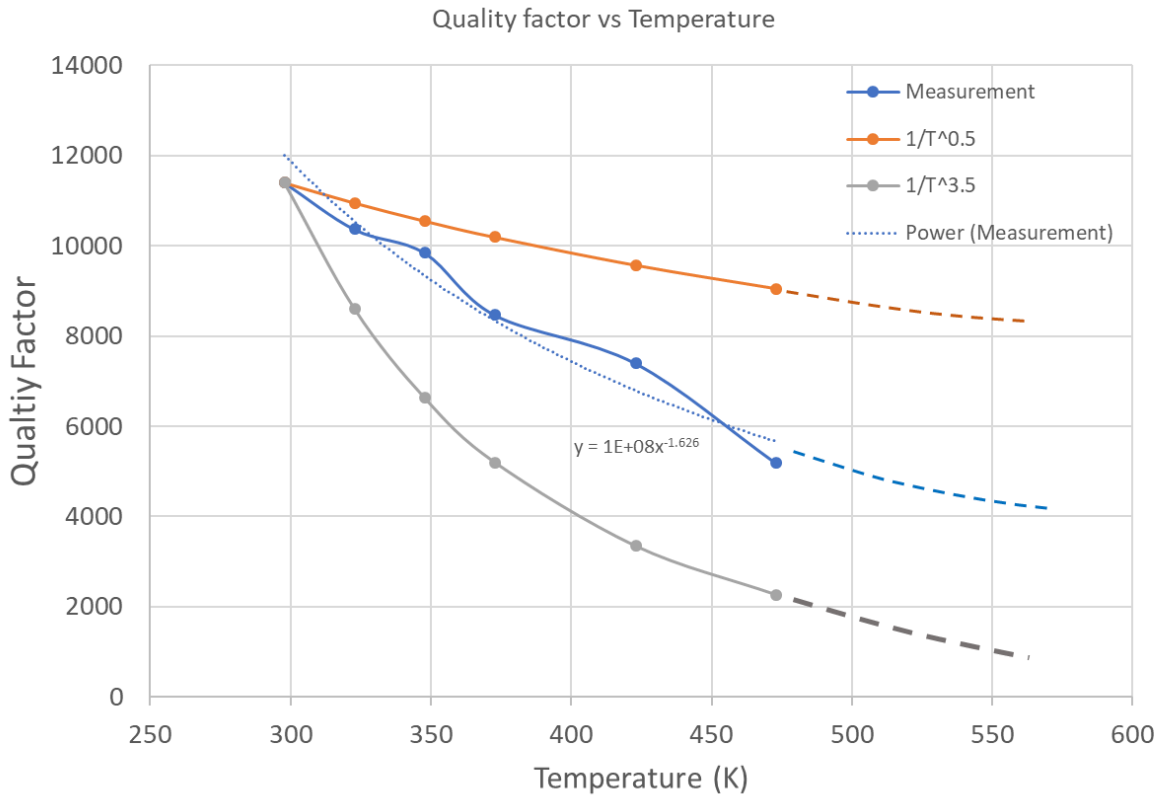


Figure 8 Measurement of Temperature dependence of MRGT quality factor

The preliminary temperature test data suggested DetX, which is a measure of the drive amplitude, degraded from 75mV at room temperature to 18mV at 300°C, with excitation voltage kept constant. The device scale factor was degraded from 15.3uV/dps at room temperature to 2.2uV/dps at 300°C.

Comparing the degradation of DetX (approximately 4x) with the Q-factor degradation shown in Figure 8, it can be concluded that the majority of DetX degradation is due to the Q degradation over temperature.

The device scale factor is directly proportional to the drive amplitude and the effective Q-factor as shown in Eq.1. With 4x degradation in drive amplitude and 7x degradation in total scale factor, we inferred that there is a 1.75x degradation in Q_{eff}. For comparison, considering an initial Q-factor of 7,500 at room temperature which was degraded to 1880 at 300°C and a frequency split of 3Hz, Q_{eff} is calculated to be 4,350 at room temperature and 1,770 at 300°C (approximately 2.5x reduction).

The initial experiments were performed with open drive loop. Once integrated with the ASIC, the device was operated in closed loop to keep the drive amplitude constant further reducing the dependence of scale factor on temperature by more than 2x from room temperature to 300°C.

MRGT device testing approach

A testing approach as developed to enable multiple levels of screening and characterization of the devices. MRGT device testing was primarily divided into two approaches, wafer level and packaged device level testing.

Wafer Level Testing

Wafer level testing was conducted on individual MRGT devices prior to packaging. These tests are primarily concerned with screening parts for functionality. The first generation of MRGT devices were uncapped, and therefore required testing in a vacuum probe station. This limited testing to a few devices at a time and changing devices required waiting for the chamber to reach a sufficient vacuum level to enable the measurement. The vacuum probe station is shown in Figure 9.

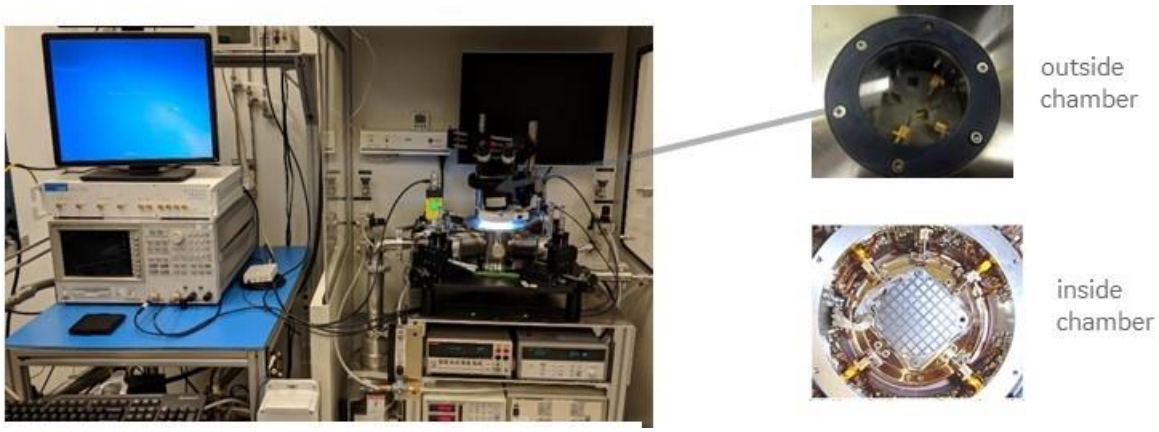


Figure 9 Vacuum probe station with test instrumentation

Figure 10 shows the Q-factor measurement results of an unsealed MRG at room temperature. The vacuum level of the vacuum probe station was adjusted from 0.1mTorr to 2.8mTorr while the MRG Q-factor remained constantly at 14,000-15,000. Because the Q-factor did not vary with respect to the vacuum level change, it can be safely assumed that the air damping is not the dominant damping mechanism for MRG at this vacuum level. To explain using (3), Q_{air} is much higher than Q_{TED}, so it can be ignored from the Q_{total} calculation. By using the simulated QTED of 22,000, the Q_{others}, which includes combined anchor loss and other loss mechanisms, can be estimated to be at 42,400. This verifies the effectiveness the MRG design approach in minimizing the anchor loss.

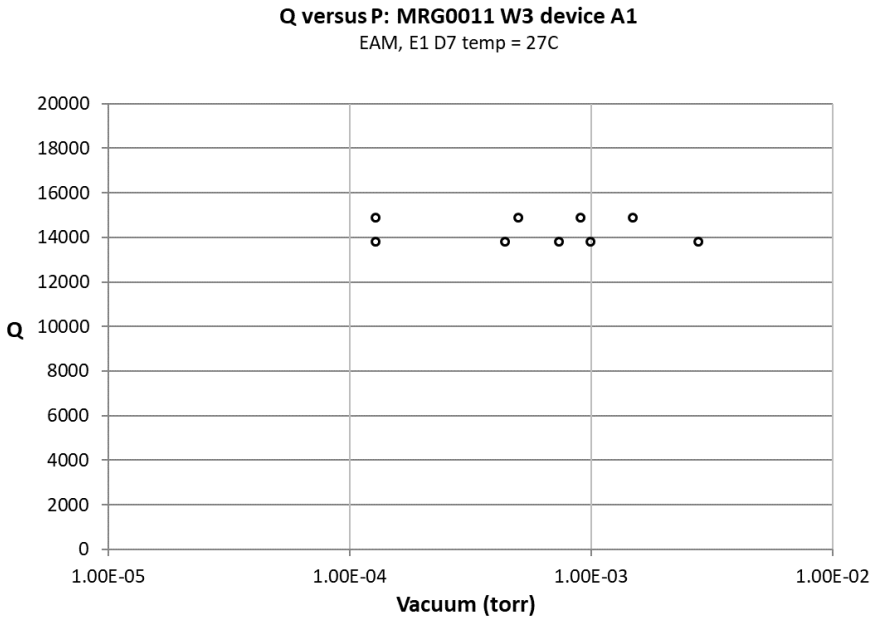


Figure 10 Q-factor measurement of an unsealed MRG in vacuum chamber

For comparison, a wafer-level sealed MRG was fabricated in the GE-MEMS fabrication process known as the Polaris process. The Polaris process incorporates high aspect ratio, deep etch capability along with wafer level vacuum sealed cavity capability. The wafer-level sealed MRG was characterized with the same electrical testing conditions at room temperature. The results are shown in Figure 11. The direct measurement refers to the method of exciting and measuring from electrodes belonging to the same wineglass mode. The indirect measurement will excite from the electrodes belong to one wineglass mode and measure from the electrodes belonging to the other wineglass mode. The direct method provides more accurate measurement of resonant frequency and Q-factor while the indirect method provides the measurement of frequency split and cross coupling errors between the two degenerated wineglass modes.

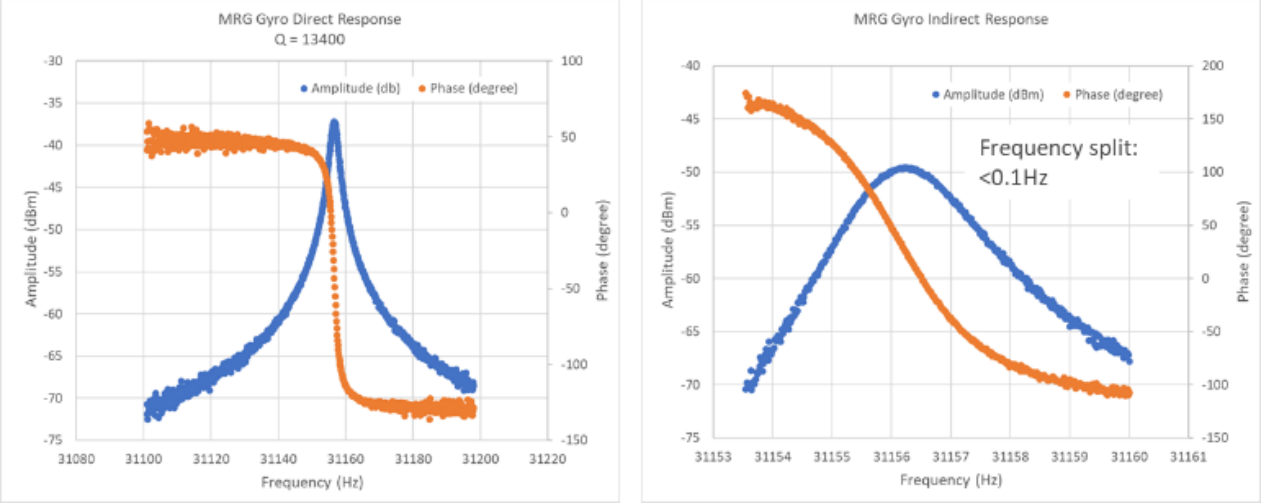


Figure 11 Frequency characterization of an MRG sealed at wafer level

Figure 11 shows the Q-factor the sealed MRG is 13,400, which is in good agreement with vacuum chamber test results. This proves the Polaris' capability in producing good vacuum in the wafer-level sealed cavity, enabling MRG to achieve the highest possible Q-factor. The indirect measurement shows the frequency split between of the degenerated wineglass modes is less than 0.1Hz. This proves the capability of Polaris process flow to achieve high quality silicon etching with high symmetry and low anisoelastic coupling.

The sealed MRG is further characterized to 600ºC to check the device integrity and understand how the MRG dynamic response might change at extremely high temperature. Figure 12 shows the change of MRG frequency over the temperature, measured by the 2nd wineglass mode. As expected, the frequency decreases with temperature due to the negative temperature coefficient of the silicon Young's modulus. The temperature coefficient of frequency (TCF) is measured to be at ranging from -25 to -34ppm/ºC from room temperature to 600ºC. Reference (2) reported similar TCFs of -27ppm/ºC and -33ppm/ºC based on the characterization of a silicon resonator from -10ºC to 80ºC. The MRG test results suggest there is no drastic change or degradation in the silicon resonator up to 600ºC, which opens up potential for MEMS devices to be used in extreme temperatures such as hypersonic flight and turbine engine hot gas path. Furthermore, the trend of increasing TCF with temperature is also observed, which means the temperature compensation technique used for high temperature will need to consider high order nonlinear terms.

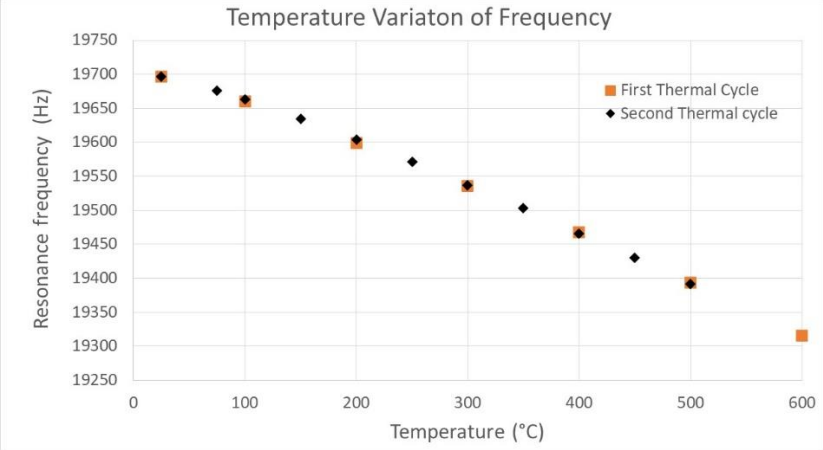


Figure 12 Sealed MRG frequency characterization over temperature

As noted previously, temperature will have negative impact to the MRG quality factor. Reference (3) suggested the different relationship between Q-factor and temperature for some damping mechanisms but it is noted that it only covered a limited temperature range up to 80ºC. In our work, the MRGs were tested to a much higher temperature range. Figure 4 shows the Q-factor variation for a wafer-level sealed MRG up to 600ºC. Two high temperature cycles were performed to show the device had no degradation and the device sealing integrity has not been compromised. For reference, the curves of TCQ of -0.5 and -3.5 were also shown on the same plot. It can be seen the MRG Q-factor follows the TCQ= -3.5 curve more closely. This confirms our previous conclusion that TED is likely the dominant damping mechanisms for the MRG. It also reaffirms our belief that for TED is a crucial design consideration for high temperature gyroscope because Q_{TED} tends to degrade very quickly over temperature. It is also observed the MRG TCQ curve tends to not degrade as rapidly when temperature increases. For example, MRG TCQ of MRG is -2.66 from room temperature to 200ºC while the TCQ is -1.29 from 200ºC to 600ºC. Whether or not this indicates a new physical phenomenon for damping at higher temperature remains as an interesting topic for future study.

During the project execution, the WLP process was developed that enabled testing unpackaged devices outside of a vacuum probe station. This enabled testing of full wafers for functionality and produce wafer maps of device characteristics variation across the wafer as can be seen in Figure 21 and Figure 22 in the *Fabrication Process Capability Advancement* section. The WLP process is discussed in more detail in the fabrication section of the report.

Packaged device test and characterization

Much of the device characterization in the project's first budget period was conducted using a high temperature capable package, die attach and wirebonding in commercially available high temperature ceramic packages. Conventional temperature circuit boards with sockets are utilized for testing. Parts can be swapped into the test board socket and therefore enables more easily testing multiple devices. Testing over temperature was accomplished by locally heating the device package while maintaining the rest of the test board at lower operating temperatures. Figure 13 shows the characterization test approach, the MRGT was packaged in a high temperature capable ceramic LCC package with high temperature die attach and interconnect. The part was inserted in a socket to facilitate testing of multiple parts. The test board contains the electronic circuitry designed as part of the Budget Period 1 effort and utilized in characterization of the overall system performance. This approach also enabled validation of the electronics approach and capabilities.

The test board and heater assembly were designed to be compatible with attaching to the rate table to enable gyroscope scale factor characterization.

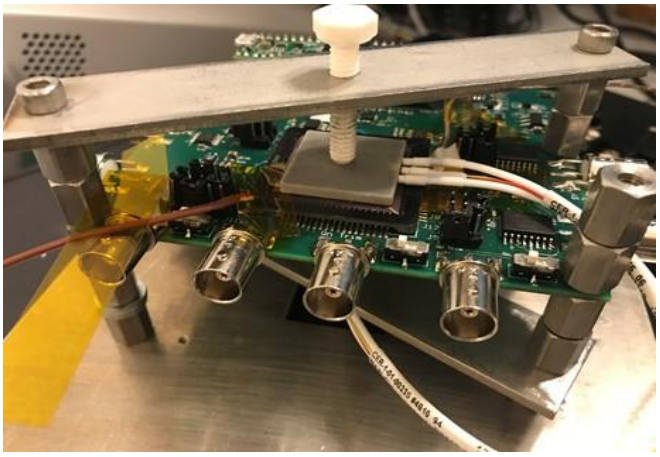


Figure 13 Test and characterization packaging approach

Figure 14 shows the MRGT rotation rate response characterization utilizing the test board and the rate table. As expected, the response is proportional to the rotation rate.

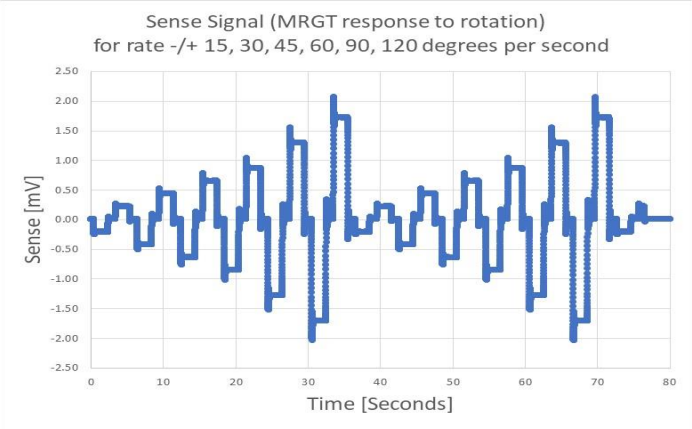


Figure 14 Response to rotation rate

The characterization approach enables testing critical performance metrics across temperature. Figure 15 shows response characterization test results at multiple temperature points from room temperature to 300°C

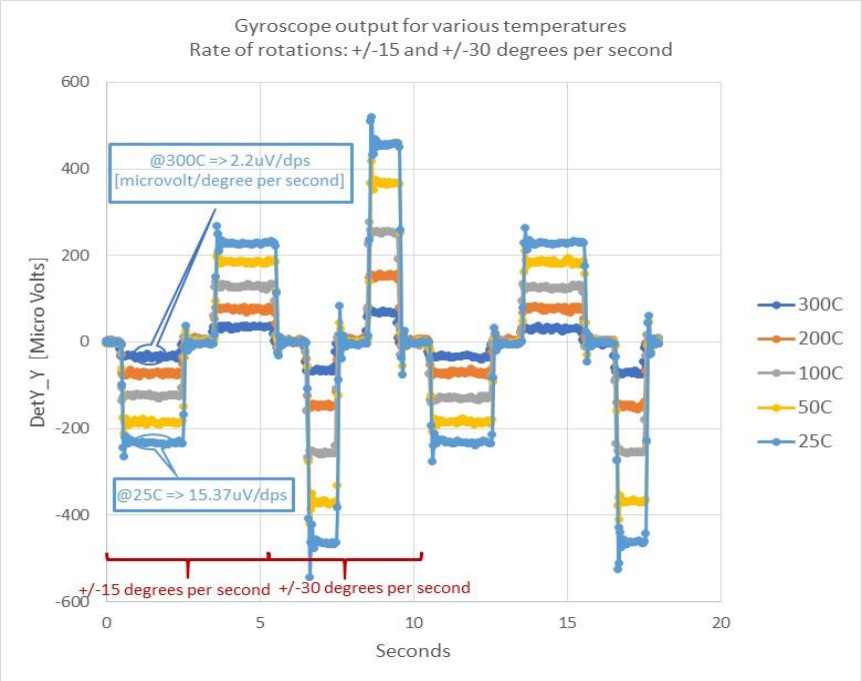


Figure 15 Rotation rate response from room temperature to 300°C

MRGT device characteristics over temperature

Testing conducted during the device design tasks aimed to further validate the device design parameters and temperature dependence. Initial testing was conducted with

fixed excitation voltage. The MRGT exhibited 6x scale factor deterioration between room temperature and 200ºC due to the loss of mechanical drive amplitude resulting from the reduced device quality factor.

A first iteration of a temperature compensation algorithm was devised in which the drive voltage is controlled over temperature to provide a constant mechanical drive amplitude. With the compensation algorithm implemented, the scale factor loss was reduced to approximately 2.25x. Figure 16 shows significant reduction in scale factor deterioration over temperature with temperature compensation implemented.

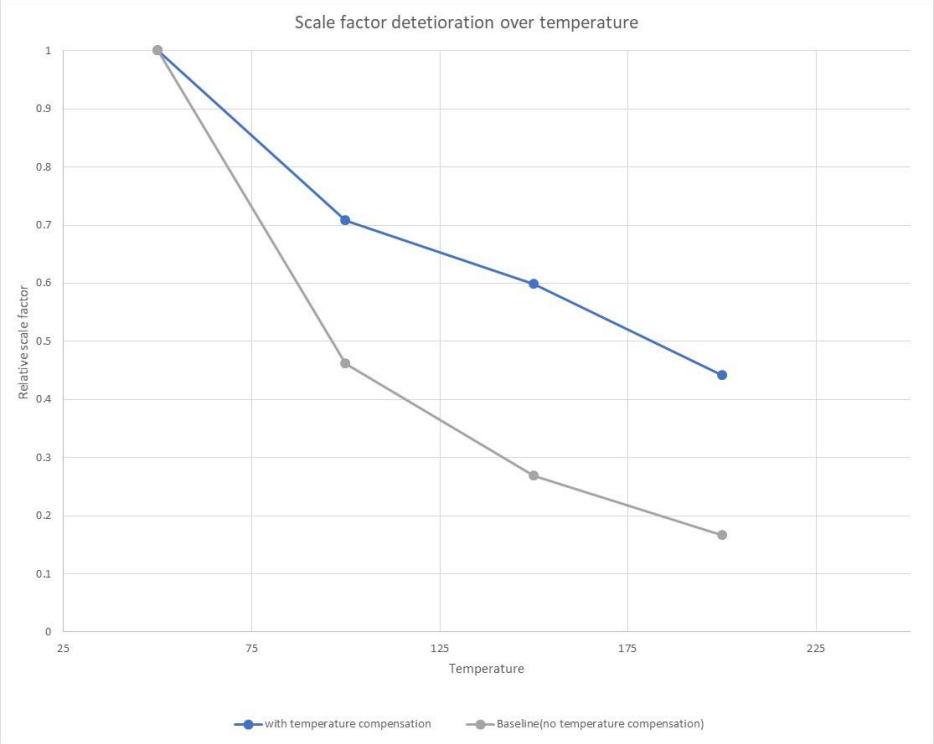


Figure 16 Scale factor deteriorating over temperature with and without temperature compensation

The characterization test setup initially exhibited a limited temperature range of operation to approximately 200°C, limited primarily by the temperature capability of the test socket in which the MRGT is inserted as well as the circuit board material and electronics components selected to support the testing. A modification to the test setup was conducted to remove the test socket and separate the MRGT from the lower temperature-capable components as shown in Figure 17. Additionally, to overcome leakage current at temperatures above 250°C, the input gain stage of the electronics

was reduced to alleviate signal saturation due to leakage. The modified test setup and electronics configuration enabled the extension of the characterization testing to 300°C.

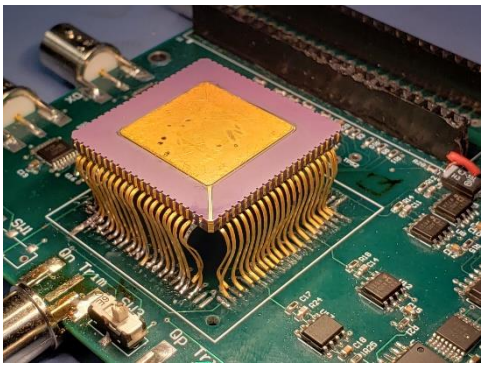


Figure 17 Modified test setup to enable 300°C testing

The modified test setup and approach was utilized to successfully characterize the noise and scale factor of the MRGT device from room temperature to 300°C . As seen in Figure 18, the device under test achieves 9 degrees/hour Allan variance at 1 second and 0.9 degrees/hours at 100 seconds at 300°C.

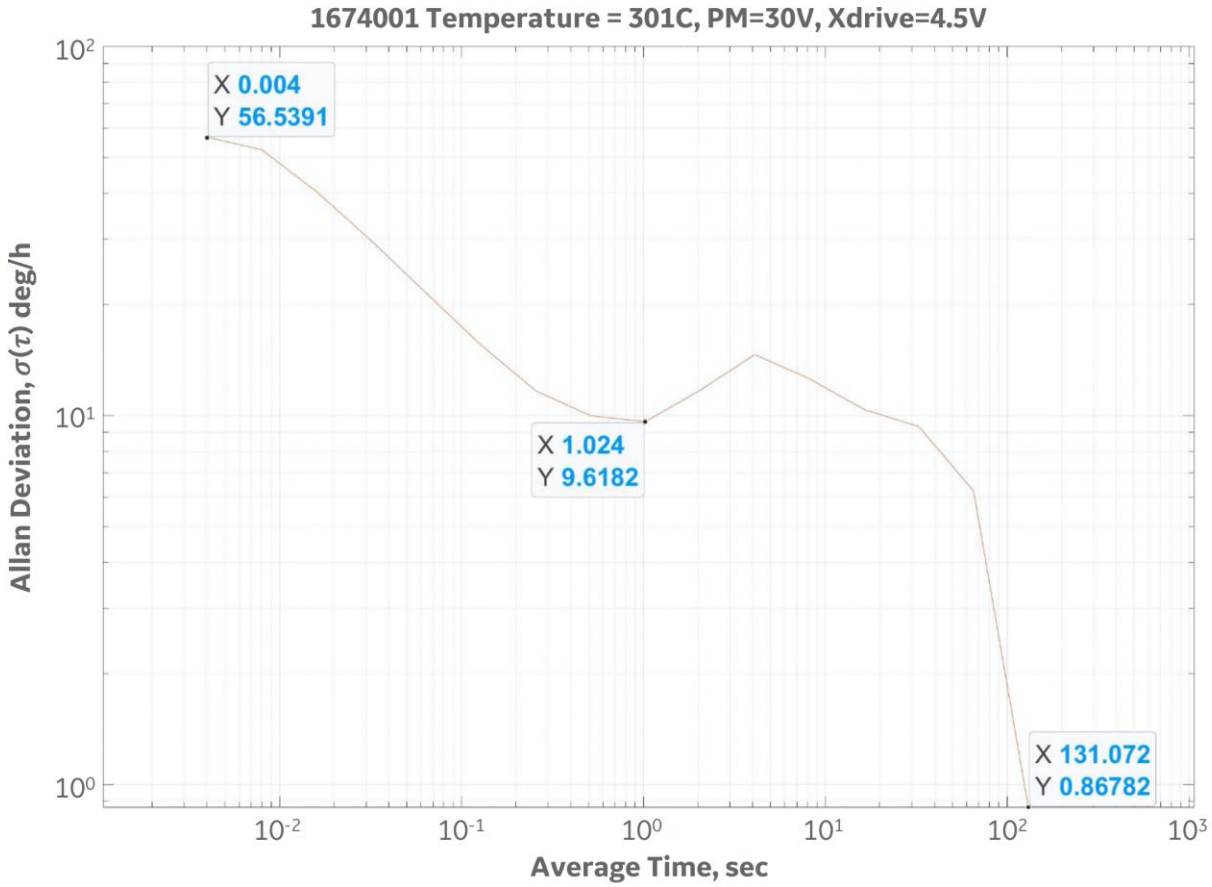


Figure 18 Allan deviation of MRGT device at 300°C

Table 4 summarizes the MRGT testing over temperature from room temperature (22°C) to 300°C. The device continues to operate and exhibit sensitivity to rotation rate across the full temperature range of operation.

Table 4 MRGT measurement summary from room temperature to 300°C

Temperature (°C)	MRGT drive quality factor	MRGT sense quality factor	Adev@ 1 second (degrees/hour)	Scale Factor (mV/degrees/sec)
22	16,079	16,044	2.05	1.63
50	11,805	11,817	3.75	1.15
100	8,028	8,055	11.56	0.71
150	5,868	5,881	15.53	0.50
200	4,639	4,632	18.22	0.58
250	3,810	3,820	25.40	0.24
300	3,272	3,281	27.69	0.20

Prior test data to 225°C is show in Table 5. This data is prior to test setup modification to enable 300°C measurement. Note that the device exhibits less than one third of the noise and more than double the sensitivity. This is attributed to a combination of increased parasitics on the 300°C setup, and the limited control voltage range of the tuning voltages. Both constraints are overcome in the setup utilized for the subsequent gyroscope system testing to be conducted in budget period 2. The ASIC utilized in the next phase of the project is itself 300°C capable, allowing for tight integration between the MRGT and electronics, resulting in significantly lower noise due to interconnect and routing parasitics and coupling. Additionally, the existing test electronics is limited to <5Volt excitation of the MRGT drive mode. The ASIC allows for supply voltages up to 30 volts, therefore allowing for 6x higher mechanical motion amplitude.

Table 5 MRGT measurement summary to 225 prior to temperature compensation and test setup modification

Temperature (°C)	MRGT drive quality factor	MRGT sense quality factor	Adev@ 1 second (degrees/hour)	Scale Factor (mV/degrees/sec)
25	12,777	12,774	0.70	11.40
50	10,587	10,595	1.07	6.65
100	7,790	7,801	2.50	3.07
150	5,469	5,483	4.50	1.78
200	4,580	4,614	5.00	1.11
225	4,063	4,098	7.00	0.95

MRGT device design summary

GE's Multi-Ring Gyroscope Transducer (MRGT) has been optimized to ensure reliable 300°C operation in geothermal applications. These innovations include optimizing ring geometry to reduce thermoelastic damping (TED), optimizing the anchor location and the anchor attachment design to reduce anchor loss, and improving MRGT robustness against temperature-induced stress.

Integration with the high temperature ASIC and further testing and performance validation of the integrated gyroscope system comprising the MRGT, ASIC and associated packaging is covered in subsequent portions of this report.

Fabrication Process Capability Advancement

The MRGT is fabricated using GE's Polaris process which has been enhanced during the first budget period to enable the following key project milestones:

1. Non-WLP die fabrication: Provided capability to assess modal resonate behavior on vacuum probe station. Enabled characterization of resonator versus vacuum level and resonance characteristic over temperature.
2. Package level vacuum non-WLP die: This includes die attach, wirebond, and critically vacuum bonding. Devices packed with this technology achieved Q of 3000, and enabled board level characterization with electronics. Provided data required for requirements flow-down to MRGT and electronics designs.
3. Wafer level vacuum packaging using an all silicon Through Silicon Via technology. WLP-TSV. The critical improvement to Polaris enabled by this project was the addition of the cap wafer. As shown in Figure 19, the process starts with two silicon-on-insulator wafers. The cap wafer is processed to have the through silicon vias. This is fusion bonded to the device wafer. In fusion bonding, all the residual gas is removed by gettering to the silicon walls creating a high vacuum. Finally, the metal routing is applied.

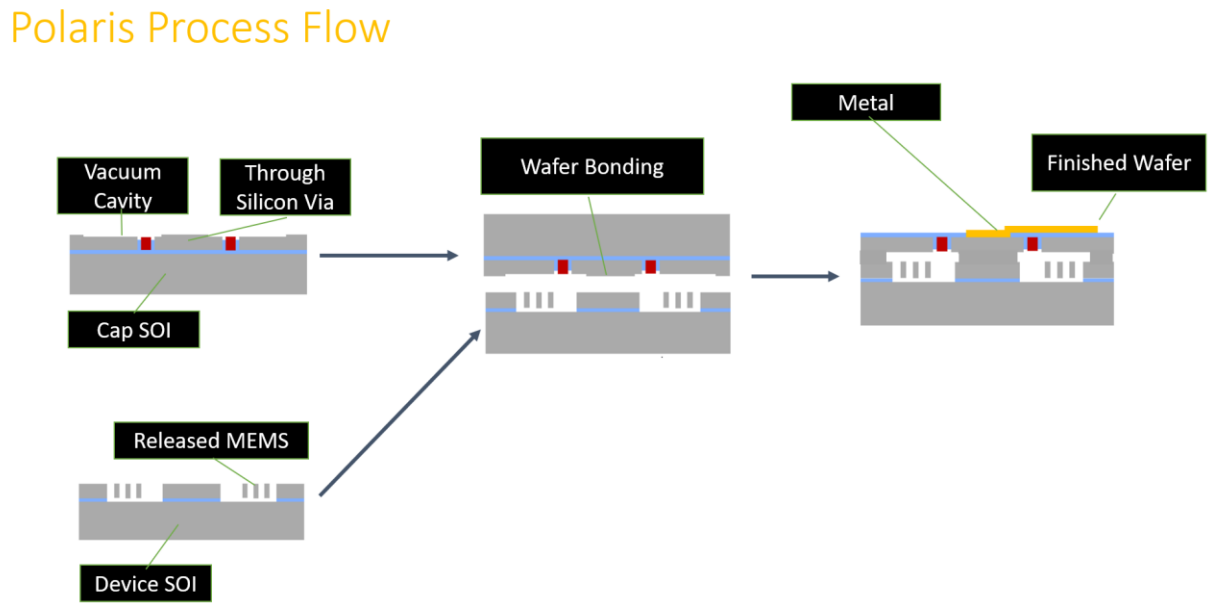


Figure 19 The Polaris process flow.

4. This critical technology advancement enabled:
    a. Full integration of Metal 1 with a redistribution layer on the Sense Element (SE), this is critical because it means that the wire-bond pads can be physically removed from the MEMS electrodes.
    b. Achieved Q of 13,000, significantly higher than was achievable with package-level vacuum packaging approach, which enabled significant improvement in device performance.

c. Supported wafer level probing, which is critical to understand the manufacturing process, yield and device characteristics variation across full wafers.
d. Robust wafer level vacuum packaging process that can withstand extreme temperatures to >500ºC. The frequency sweep in Figure 20 shows an MRGT's resonance characteristics from room temperature to 500ºC.

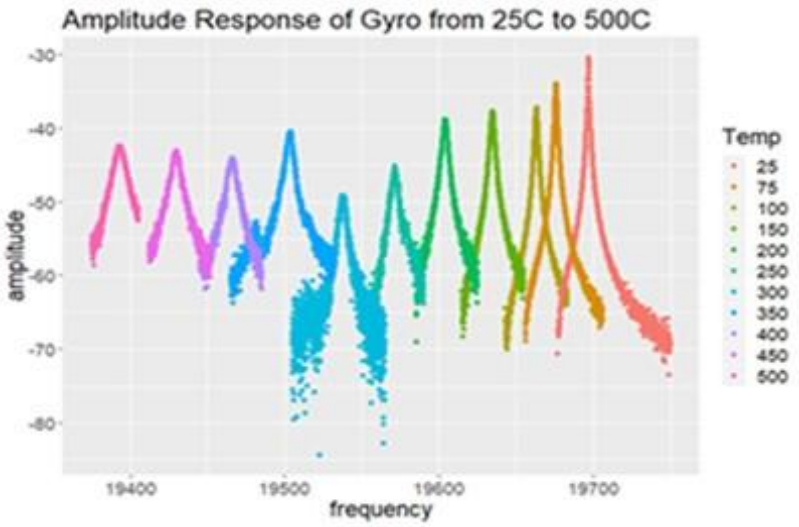


Figure 20 WLP device frequency sweep from room temperature to 500ºC

5. Process capability improvements. Along with the advancements achieved through wafer level packaging, improvements to the fabrication process controls and refinement of the process parameters have resulted in a number of significant improvements
    a. Yield improvements:
    Consistent effort to improve the wafer process, including the critical bonding step was undertaken during the first budget period. In the bonding step, the two parts must come into intimate contact, as hydrogen bonding must happen across the wafer surfaces. Thus, advances in cleaning and surface preparation are believed resonsible for improved WLP process. The yield improvement can be seen in comparing the wafer map of the MRGB007 wafer shown in Figure 21 where only 23/45 parts resonated with the wafer map from the MRGB008 wafer as seen in Figure 22 where 36 resonated. This improvement has resulted in a yield increase from approximately 50% to 80% with additional improvements in device quality and performance consistency.

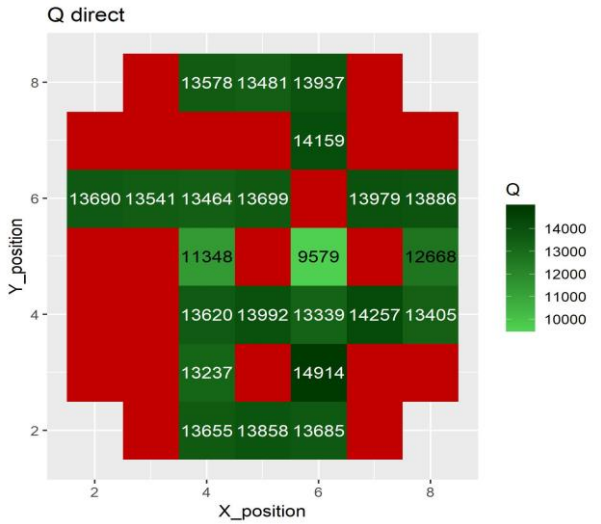


Figure 21 Wafer map of device resonance frequency for MRGB007

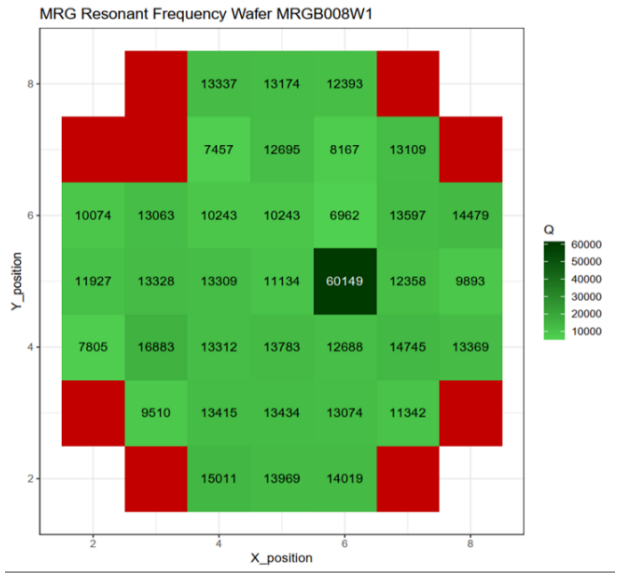


Figure 22 Wafer map of device resonance frequency for MRGB008

b. Trench etch quality improvement

The formation of the actual device requires a single photo-lithographic etch step using industry standard Deep Reactive Ion Etching (DRIE). This is technically challenging for two reasons. First, at the end of the step, the surface must be bond ready, smooth and free of defects that can be caused by handling, such as scratches. Second, the etch itself should achieve the highest possible aspect ratio in order to maximize the device sensitivity. Using our existing tooling and processes, we have discovered

the presence of subtle defects in the etched sidewall. As shown in Figure 25, ‘micro-needles’ or ‘grass’ can be formed at the trench bottom.

Wafer fabrication improvements

The wafer fabrication improved over the project. As the output improved, the requirements for success on a die were tightened. In particular, as it became clear that quality factors in excess of 10,000 were achievable, these fabrication process improvements became critical to the performance entitlement budget. Figure 23 shows the growth in fab output across the project.

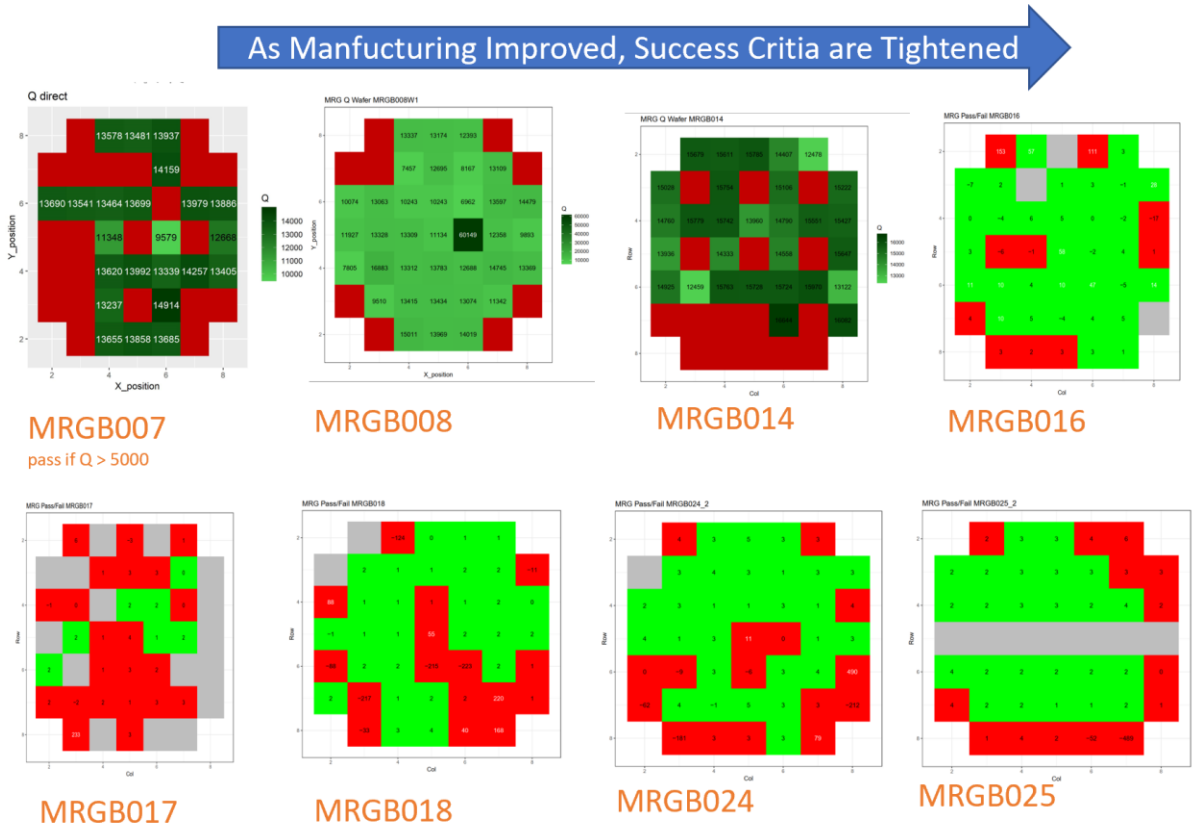


Figure 23 As the project proceeded, the MRG wafers improved. The criteria for success were tightened along with this, with requirements for higher Q driving success.

Device packaging advancements

In addition to our wafer fabrication abilities, the packaging we used to run some tests improved. In Figure 24 we see the improvement in the package from the start of the project to the end. In the beginning, the die was not wafer level packaged. The top image shows a die in a much larger package with wirebonds flying out from electrodes to pads. With wafer level package and TSV metal routing allowed us to use fewer

wirebonds to fewer pins. In addition, there was no longer a requirement for vacuum packaging.

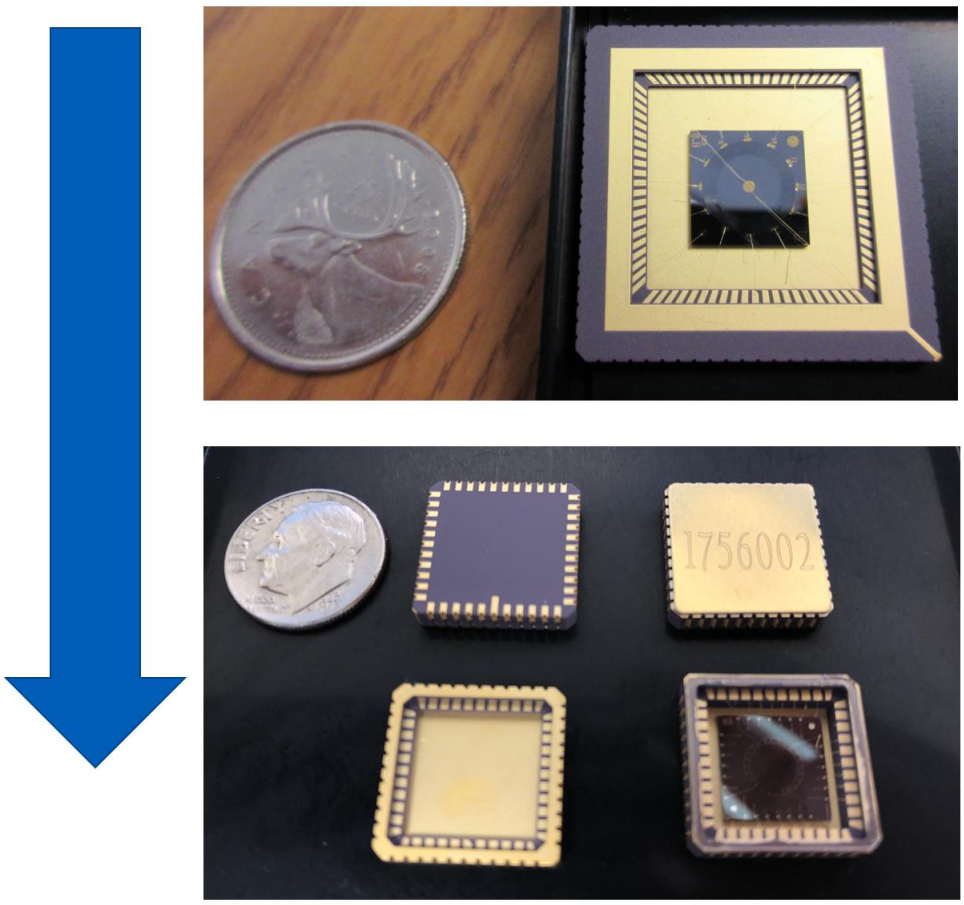


Figure 24 In addition to improvements in wafer fabrication, we made improvements in packaging. The upper image is our initial package. The lower image is improved package.

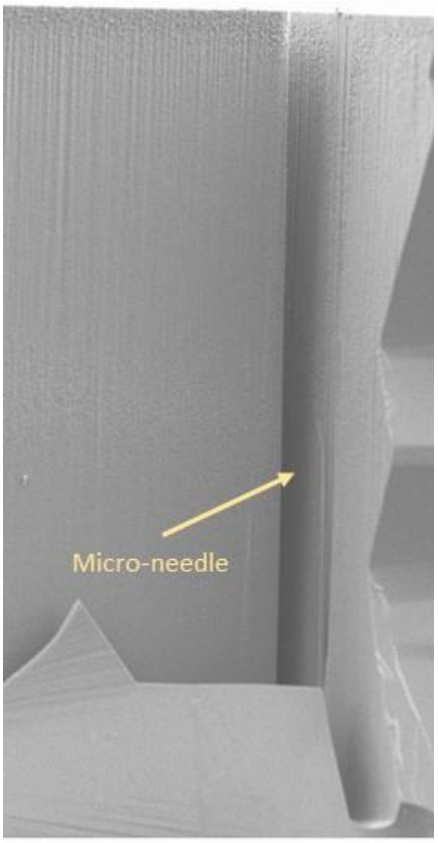


Figure 25 Trench sidewall showing micro-needle formation

In the image we see a small fiber clinging to the side of the gyroscope device. This fiber, or ‘needle’ is composed of the base silicon material. It is a defect known in DRIE. These micro-needles sometimes dislodge and cause intermittent shorts and other time-varying behavior during testing. A study of DRIE etch conditions was implemented to alleviate these defects.

Fabrication process capability advancement summary

A summary of fabrication process capability advancements undertaken during Budget Period 1 is summarized in Table 6.

Table 6 Process capability Advancements

Topic	Impact	Improvement process	Outcome
Wafer Bonding quality	Vacuum level, device quality factor (Q)	Chemical Mechanical Polishing (CMP), Cleaning, Dry process optimization	Reliable WLP process
Device Robustness	Wire bond on TSV can cause electrical shorting	Implemented Metal Redistribution to remove wire bonds from TSV	No wirebonding induced failures detected
Device Etch Quality	Q, Cross Gain, device-to-device variation	DRIE etch process optimization	Yield improvement, state-of-the-art device performance
Foreign object debris Generation	Micro-needle formation, Intermittent shorting	DRIE process optimization.	SEM images showed no micro-needles in trench. Performance improvement validation in progress

Electronics requirement development:

MRGT 2-DOF Analytical Model

The 2-degrees of freedom (DOF) mechanical oscillator model consists of the linear time invariant (LTI) ordinary differential equations (ODE) for the GE MRG resonator with its two degenerate (X,Y) Coriolis-coupled modes, as shown in Figure 26.

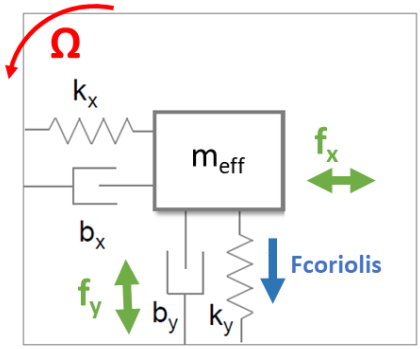


Figure 26: 2DOF mechanical oscillator model of GE MEMS MRG

The MRG analytical equations can be described in a non-inertial frame with rotating at inertial rate as (Figure 27) [IEEE Std1431-2004].

$$\ddot{x} - 2k\Omega\dot{y} + \frac{2}{\tau}\dot{x} + \Delta\left(\frac{1}{\tau}\right)\left(\dot{x}\cos 2\vartheta_\tau + \dot{y}\sin 2\vartheta_\tau\right) + \omega^2 x - \omega\Delta\omega\left(x\cos 2\vartheta_\omega + y\sin 2\vartheta_\omega\right) = f_x$$

$$\ddot{y} + 2k\Omega\dot{x} + \frac{2}{\tau}\dot{y} - \Delta\left(\frac{1}{\tau}\right)\left(-\dot{x}\sin 2\vartheta_\tau + \dot{y}\cos 2\vartheta_\tau\right) + \omega^2 y + \omega\Delta\omega\left(-x\sin 2\vartheta_\omega + y\cos 2\vartheta_\omega\right) = f_y$$

$$\omega^2 = \frac{\omega_1^2 + \omega_2^2}{2}, \quad \omega\Delta\omega = \frac{\omega_1^2 - \omega_2^2}{2}, \quad \frac{1}{\tau} = \frac{1}{2}\left(\frac{1}{\tau_1} + \frac{1}{\tau_2}\right), \quad \Delta\left(\frac{1}{\tau}\right) = \frac{1}{\tau_1} - \frac{1}{\tau_2}$$

Ω, k, inertial rate, angular gain, respectively

$\vartheta_\tau, \vartheta_\omega$, principal damping and stiffness axes, respectively

f_x, f_y, input acceleration or force normalized to unit modal mass

Figure 27: 2DOF CVG LTI ODE Analytical Model Equations

A state space model was formulated from the 2DOF CVG LTI ODE analytical model equations in order to more easily implement a time domain simulation model for MATLAB, and the capacitive transducer interface was implemented in state space form.

The ASIC analog electronics analytical model that captures relevant gain, bandwidth, and noise characteristics was also incorporated into the overall state model as shown in Figure 28.

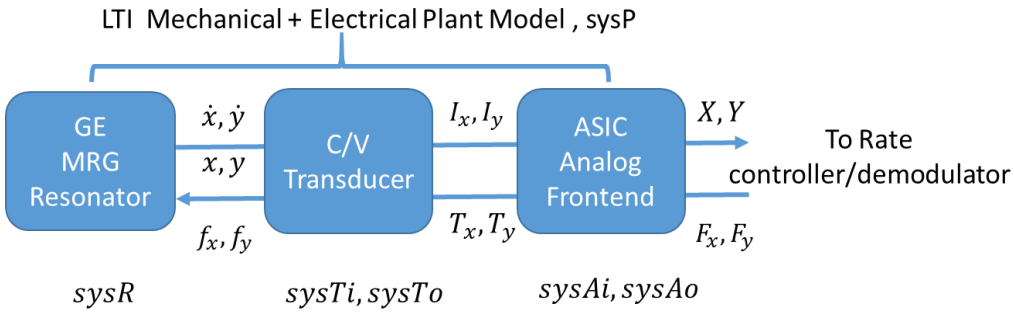


Figure 28: State Model Block diagram MRG CVG with Mechanical Resonator (sysR), capacitive transducer interface (sysT), and ASIC analog frontend electronics (sysA) analytical model blocks

The state space model (sysP) incorporating MRGT CVG with Mechanical Resonator (sysR), capacitive transducer interface (sysT), and ASIC analog frontend electronics (sysA) analytical model blocks was then simulated in MATLAB for transfer functions to verify expected transfer function performance, Figure 29. The model diagram does not show cross-channel feedthrough, but it was implemented.

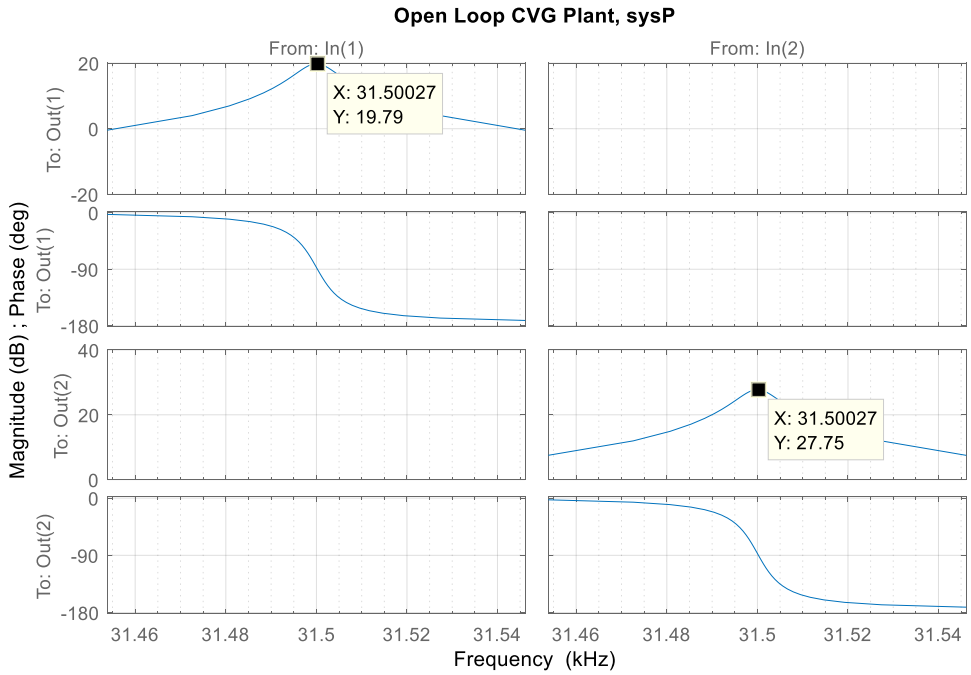


Figure 29: Predicted transfer function (in(1)→X channel drive, in(2)→Y channel drive, out(1)→X channel sense, out(2)→Y channel sense) for the GE MRG with IW ASIC AFE

The state space model (sysP) was also simulated in MATLAB for noise performance to predict Angular Random Walk (ARW) noise performance, Figure 30.

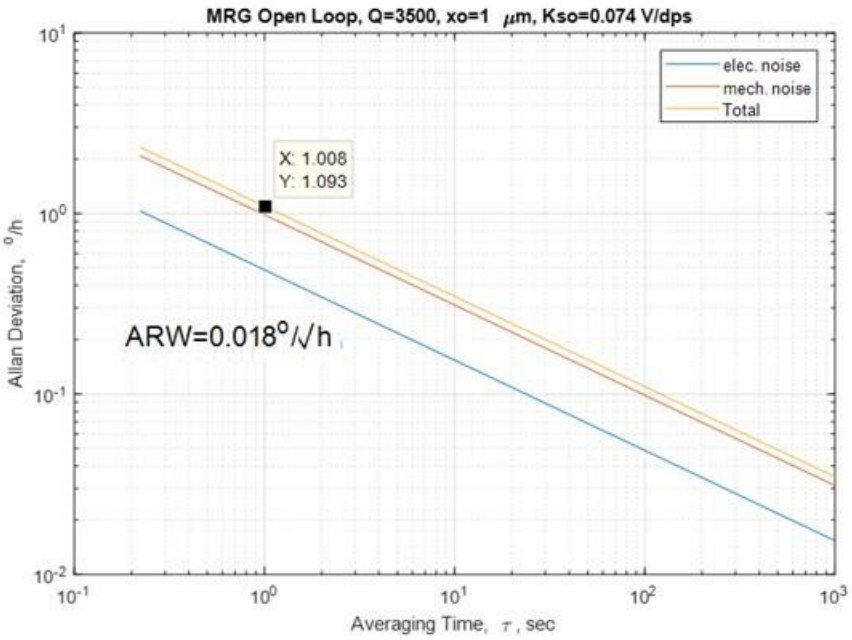


Figure 30: Predicted GE MRG with current InertialWave ASIC Frontend Electronics Allan Deviation Bias Stability and ARW

The Allan Deviation plots the predicted MRG Mechanical Thermal Noise (MTN) component (mech. noise red curve), ASIC analog frontend thermal noise component (elec. noise blue curve), and the total noise (Total, yellow curve). A conservative quality factor (Q) of 3500 was used in the model with an expected electronic drive level of 1um displacement in the MRG. The associated open loop baseband sense gyroscope scale factor was analytically predicted by the model Kso=74mV/°/s. The overall analytical model performance predicts that the overall ARW noise = 0.018°/√hr performance is MTN limited by the MRG mechanical noise and the there is significant margin in the current ASIC AFE frontend electronics noise floor.

ASIC Interface Requirements

Preliminary GE temperature testing on MRG die produced a series of transfer functions and measured Q-factors from ~25°C→200°C, Figure 31.

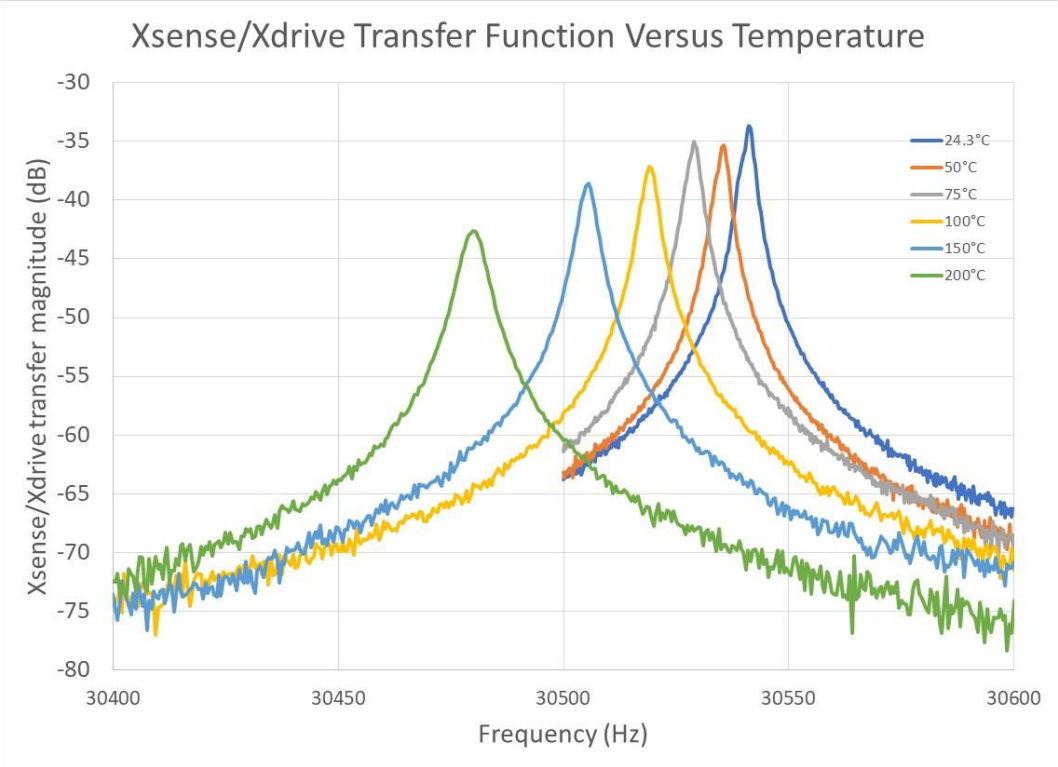


Figure 31: GE MRG Die Level Transfer Function (Xsense/Xdrive) vs. swept die temperature (25°C-blue/right, 50°C-orange, 75°C-grey, 100°C-yellow, 150°C-blue/left, 200°C-green)

The following Table 7 summarizes the frequency and Q factor at each temperature point.

Table 7: GE MRG Die Level Transfer Function (Xsense/Xdrive) vs. swept die temperature summary

Temperature (°C)	MRG frequency (Hz)	MRG Q-factor
25	30541	8320
50	30536	8200
75	30529	7250
100	30520	6780
150	30506	4200
200	30481	3580

InertialWave designed and fabricated an Analog Frontend Electronics control board to test with available packaged GE MRG devices (Figure 32). The board includes the frontend gain/noise parameters described in the previous model.

Figure 32: InertialWave Analog Frontend electronics board with attached LCC vacuum packaged GE MRG

The AFE board is connected to InertialWave's CVG Test System product test equipment (Figure 33, Figure 34, Figure 35 and Figure 36) that provides a real-time MATLAB controller environment and InertialWave's proprietary software product modules for taking transfer functions, PLL-based frequency tracking and open loop operation, closed loop Force Rebalance operation, and advanced electronic compensation (digital temperature compensation and switched mode drive operation).

Figure 33: InertialWave CVG Test System Product used for GE MRG testing with InertialWave AFE electronics

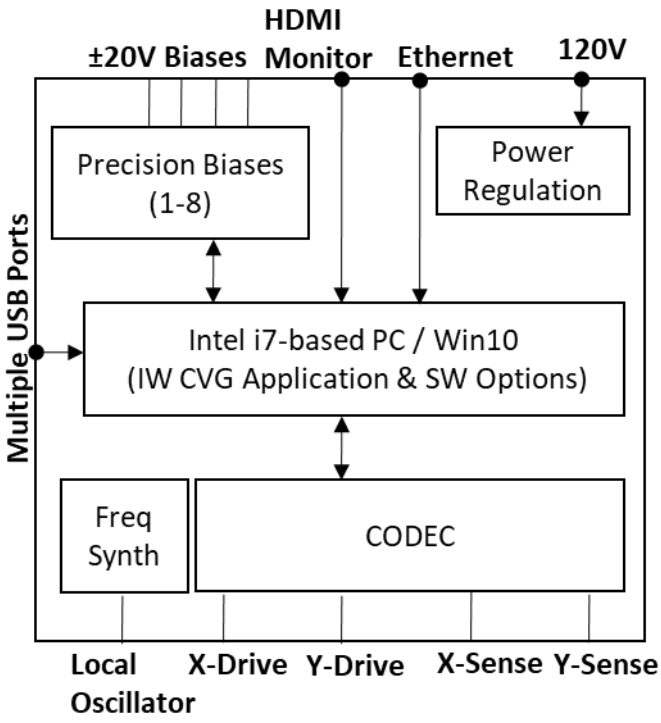


Figure 34: InertialWave CVG Test System functional block diagram

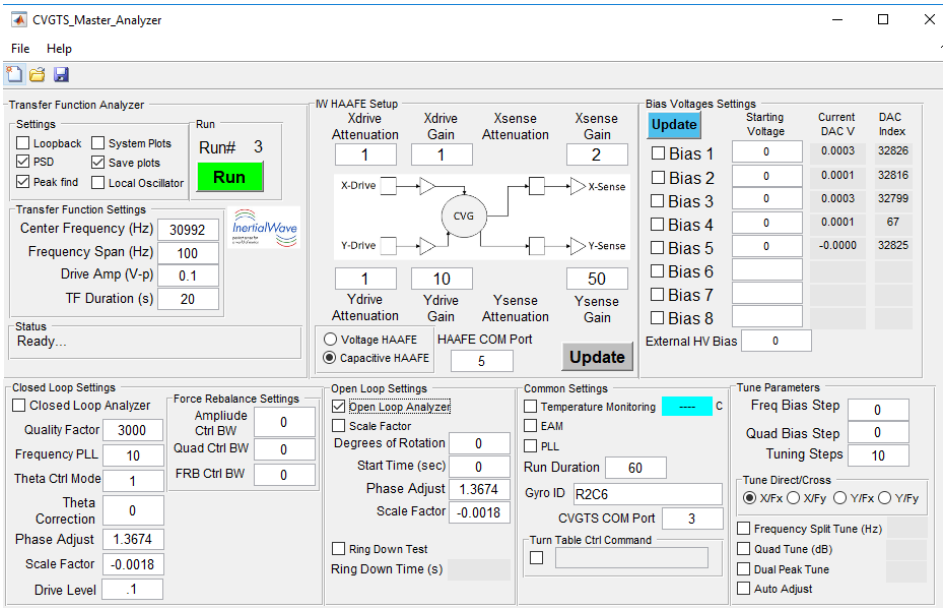


Figure 35: InertialWave CVG Test System Product associated GUI used for GE MRG testing with InertialWave AFE electronics

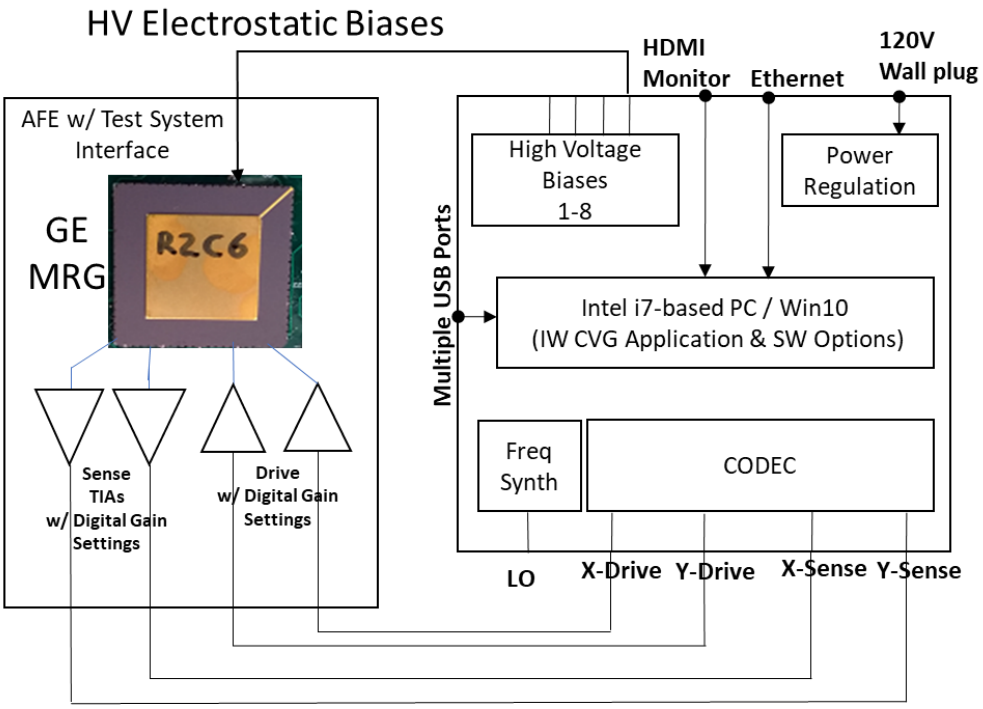
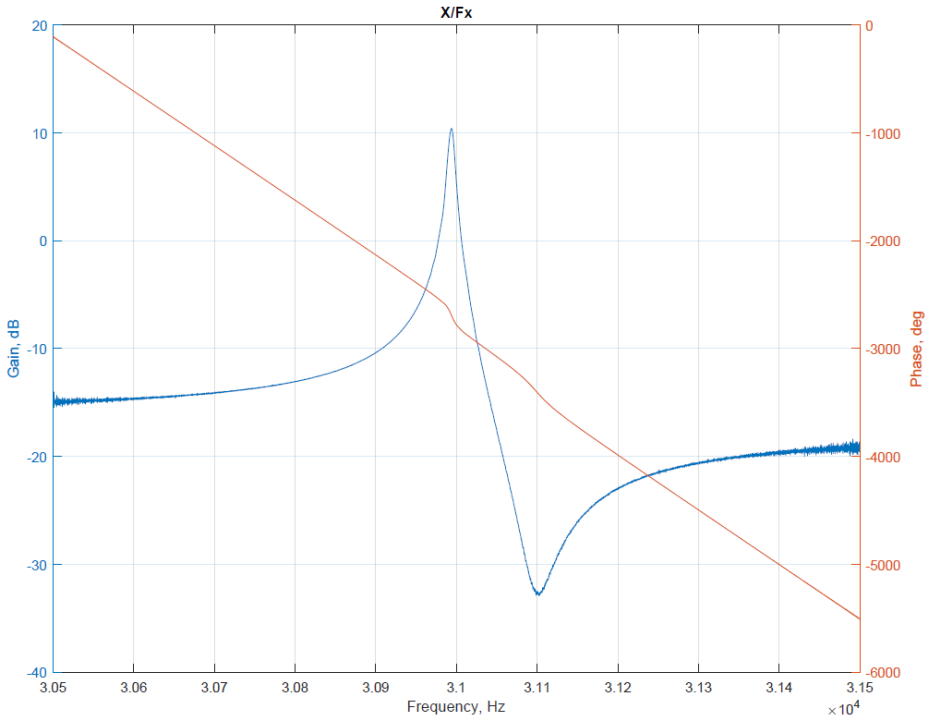


Figure 36: InertialWave CVG Test System connected to GE MRG functional block diagram

Transfer functions from the MRG (Part# R2C6) are summarized in Figure 37. The device exhibits expected center frequency, excellent untuned frequency mode split, conservative room temperature Q-factor, transfer function peak gains consistent with some tuning adjustments to InertialWave analytical model prediction, and relatively large cross gain (Y/Fx, X/Fy) attributable to quadrature leakage and/or drive misalignment in the MEMS MRG.


X/Fx
Gain, dB
Phase, deg
Frequency, Hz
×10^4
20
10
0
-10
-20
-30
-40
0
-1000
-2000
-3000
-4000
-5000
-6000
3.05
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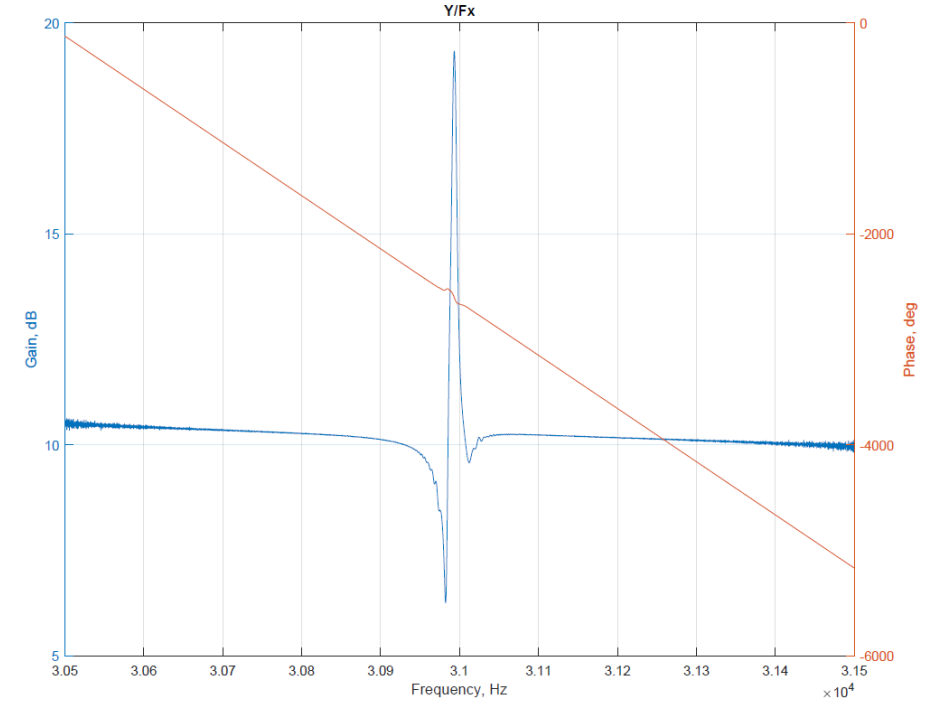
A


Y/Fx
Gain, dB
Phase, deg
Frequency, Hz
×10^4
20
15
10
5
0
-2000
-4000
-6000
3.05
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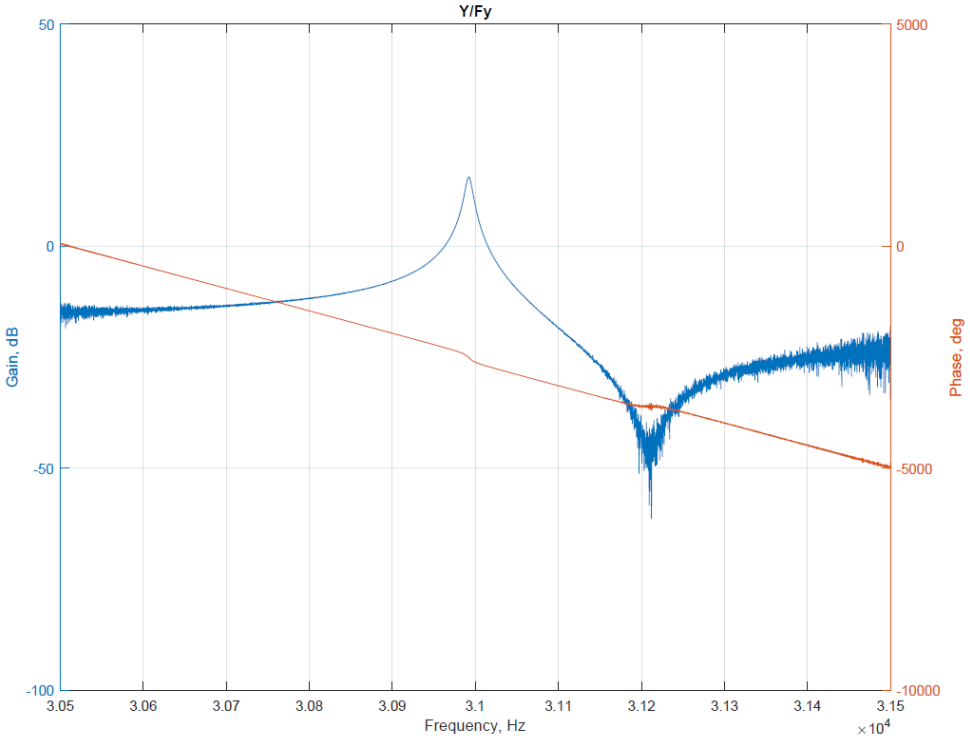
B



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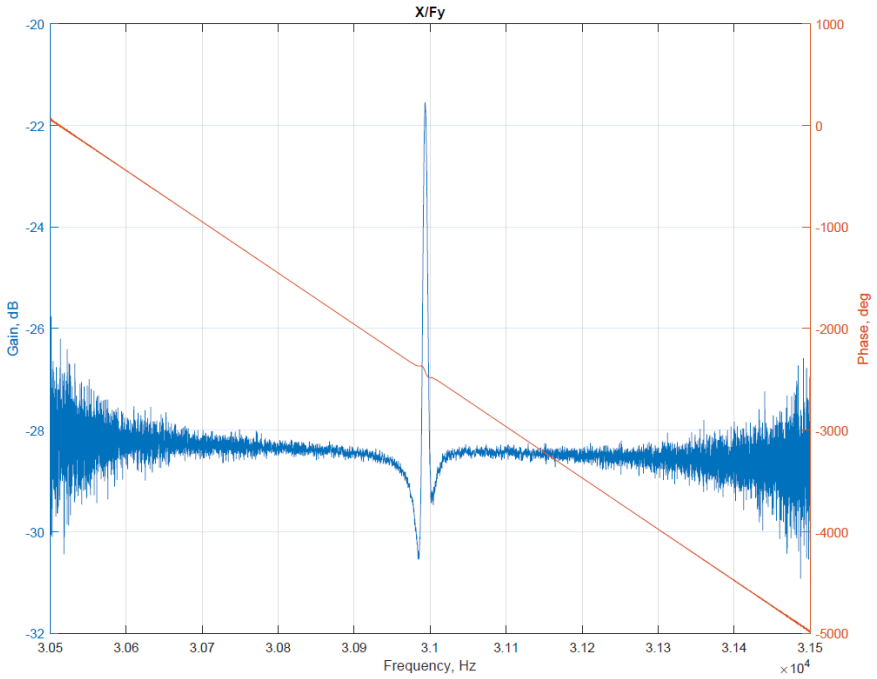

D

Figure 37: InertialWave measured 2-port Xdrive and Ysense transfer functions on GE MRG R2C6 part

A summary of measurement results auto-generated from the CVG-TS is shown in Table 8.

Table 8: GE MRG R2C6 Measured Transfer Function Summary

Test Results

Y: Fpky: 30992.1, Pkdby: 17.7, Qmy: 3548

X: Fpkx: 30993.8, Pkdbx: 9.8, Qmx: 3324

Frequency Mode Peak Split (Hz): -1.7262

Drive to Sense (Y/Fx) Cross gain (dB): 19.3257

The measurements were re-compared to the InertialWave analytical model and showed good prediction of direct transfer function gains in Figure 38. Sources of cross gain are due to device asymmetry and are removed during MRG gyroscope operation using electrostatic biasing.

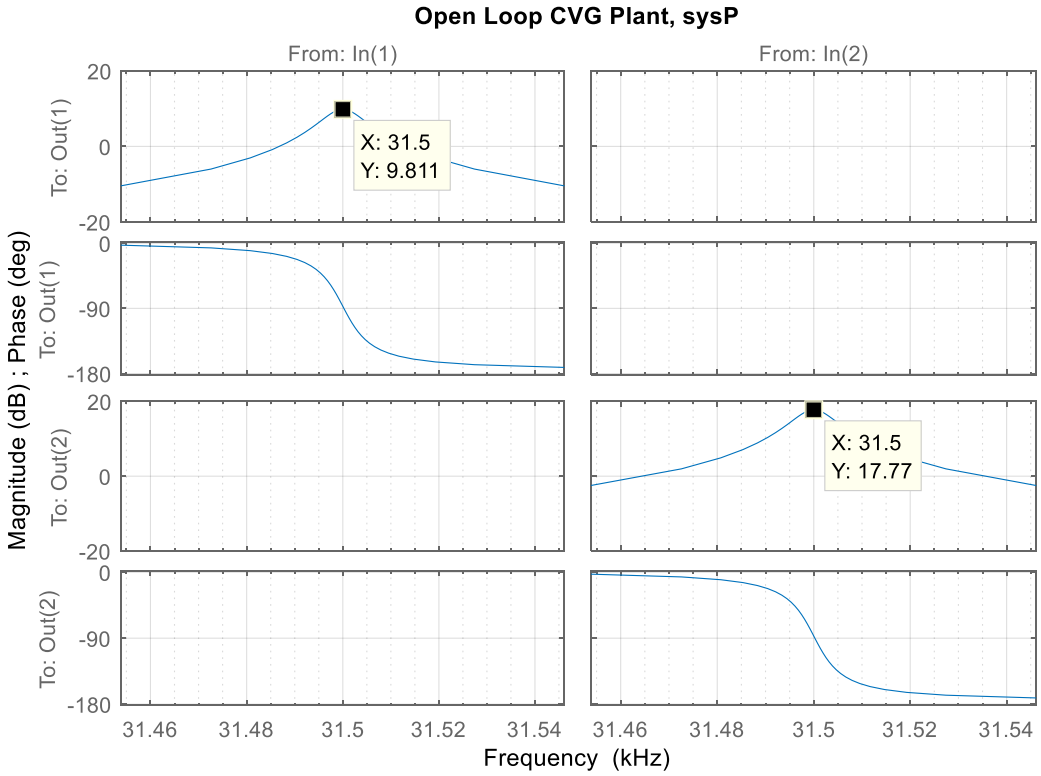

Figure 38: Predicted transfer functions (in(1)→X channel drive, in(2) →Y channel drive, out(1)→X channel sense, out(2)→Y channel sense) for the GE MRG R2C6 with IW ASIC frontend electronics

Results from testing to confirm transfer function measured Q-factor are consistent with a ring down test using closed loop drive PLL tracked MRG center frequency (Figure 39). Slight differences are due to the discretized transfer function frequency step size.

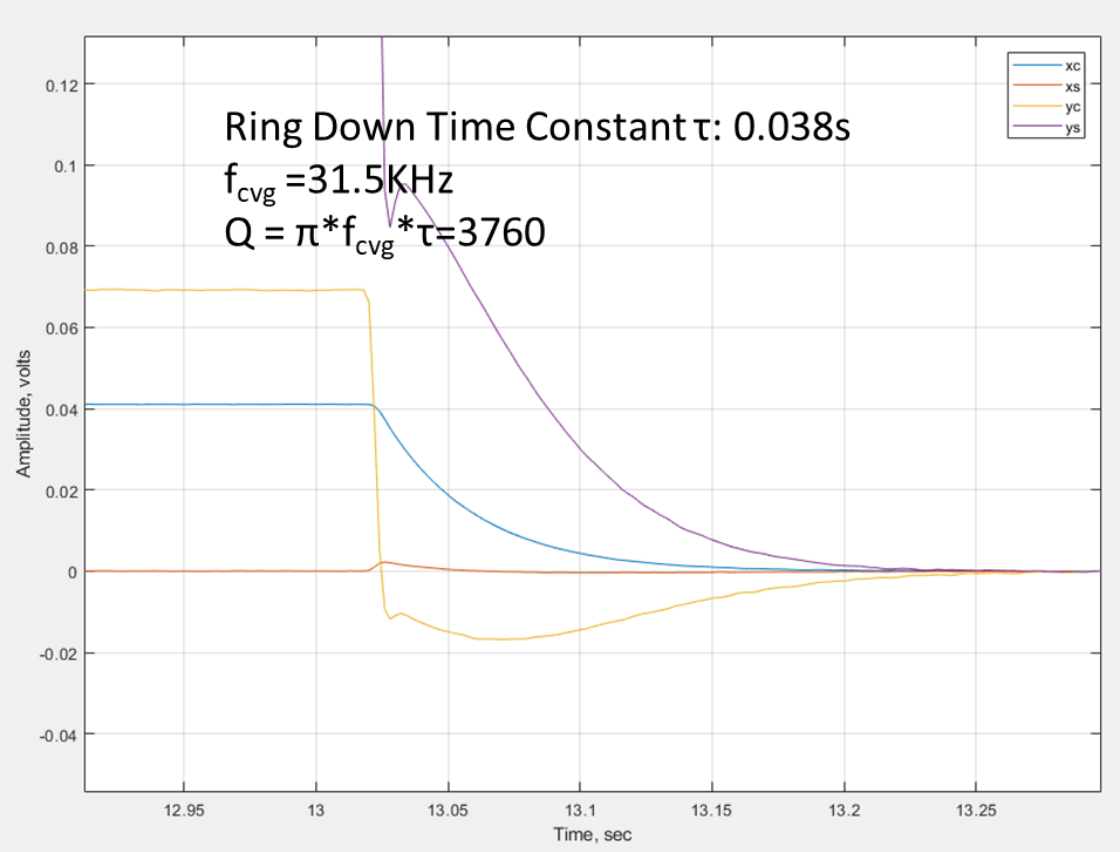

Figure 39: Closed loop drive with PLL tracking ring down test on R2C6 calculated Q-factor=3760 is consistent with measured transfer function Q-factor=3548.

Based on promising measured versus predicted model a preliminary ASIC interface specification was created (Table 9). This was used to move forward with ASIC controller architecture board level demonstration. Further work on closed loop noise measurements and demonstration of MRG 1um drive displacement to achieve predicted ARW<0.01°/√hr was completed using the ASIC architecture board level demonstrations using GE's new higher Q-factor MRG packaged devices and ASIC interface requirements were finalized.

Table 9: ASIC Interface Specifications for GE MRG to achieve Mechanical Thermal Noise limited performance and ARW<0.01°/√hr at 1um MRG drive displacement

Parameter	Value	Definition
Vb	≥30V	Proof mass bias generation
Vdrive_xy	±10V	MRG drive AC level max.
Kinstx.y	2 - 100	Instrumentation amp gain (programmable range)
Kax/y	1 - 10	Drive Output Buffer gain (programmable range)
Rfx	100Mohm	TIA feedback resistance
Cfx	1pF	TIA feedback capacitance
fa	>250KHz	TIA gain-bandwidth
Css	<1pF	Parasitic input capacitance
Vny	<5uV/√Hz	AFE/MRG Sense input referred noise
Vnda	<1uV/√Hz	Controller drive noise density

Board-level testing and validation of electronics design.

The electronics design was advanced to enable control and signal conditioning architecture of the MRGT. The electronics architecture and performance requirements were validated utilizing room temperature board-level electronics. The MRGT characterization was conducted using the electronics architecture devised to validate the performance and interface capability between the MRGT and the electronics. Further iterations on the electronics design were conducted to accommodate improvements on the MRGT design including the addition of the frequency tuning and quadrature nulling capabilities. The combined MRGT and electronics improvements achieved sensitivity enhancements of greater than two orders of magnitude compared to the baseline performance achieved with the first iteration of the MRGT and electronics as can be seen in Figure 40.

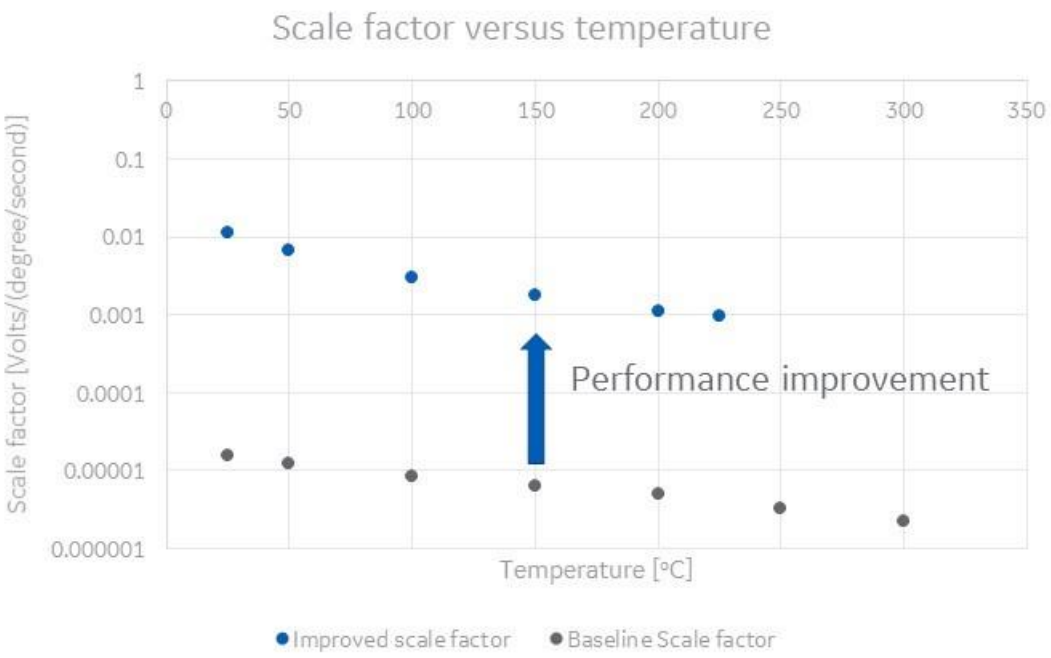

Figure 40 Baseline and improved scale factor versus temperature

Testing with the combined room temperature electronics and MRGT was used to validate required drive levels, electrostatic tuning and control levels. The validated design was used to derive the requirements for the ASIC.
ASIC electronics development

High Temperature ASIC design

Objective and scope

To support the development of a high temperature gyroscope for geothermal drilling, InertialWave (IW) is tasked with developing a high temperature 300°C capable gyroscope controller Application Specific Integrated Circuit (ASIC). The ASIC, along with for the MEMS Multi-Ring Gyroscope transducer (MRGT) must achieve sub-earth rate sensitivity necessary to operate as a gyrocompass (gyroscope-only inertial north-finding) for downhole geo-thermal drill tool navigation.

Building upon the electronics requirements, functional and performance models Functional board-level validation hardware was developed and tested showing good correlation between model and measurement results and further validating the

requirements and performance of the overall gyroscope operation and providing the necessary inputs to the ASIC electronics development tasks.

The ASIC electronics development tasks expanded the work conducted in the prior tasks to include simulations across process and temperature corners. The corner simulations cover fabrication variations, operating condition variations, and device characteristic changes across the temperature range from 20ºC to 300°C . Functional and performance validation across process corners and temperatures provide ability to validate the design's robustness against process and temperature variations and validate the ability of the design to maintain critical parameters such as gain and noise performance to within required specifications imposed by the overall gyroscope system requirements.

The ASIC electronics development task established the testability approach, the functional and performance risk mitigation features and validated the ASIC readiness for fabrication.

The high temperature gyroscope controller ASIC was designed in a high temperature capable, 1um Silicon On Insulator (SOI) process capable of 300°C operation. The ASIC enabled the combined MRGT to successfully be operated as a gyroscope up to 300°C . The ASIC design has the following features:

- 300°C capable Analog Frontend (AFE) design
    - Enable testing of MRG w/ AFE at 300°C for representative noise performance
    - Perform closed loop amplitude control of the MRG drive
    - Phase Locked Loop tracked MRG operation
    - Low power consumption
- Meet Mechanical Thermal noise limited performance
    - Maintain sub- 1degree hour @ 1s performance
- Performance optimized layout chip to minimize parasitics
    - Improved noise performance over current board level design
- Digitally controllable low noise gain settings
    - Enable high drive level (low gain)
    - Enable high sensitivity rate sense (high gain)

The ASIC interface signals were designed to match the signal interface requirements and signal pad locations of the MRGT device. The signal ordering was co-optimized between the MRGT and the ASIC to maximize performance. This includes separation

of sensitive signals from high drive signals, and routing differential signals together to maintain common mode noise immunity.

The ASIC floorplan showing the location of the various functional blocks within the die is shown in Figure 41.

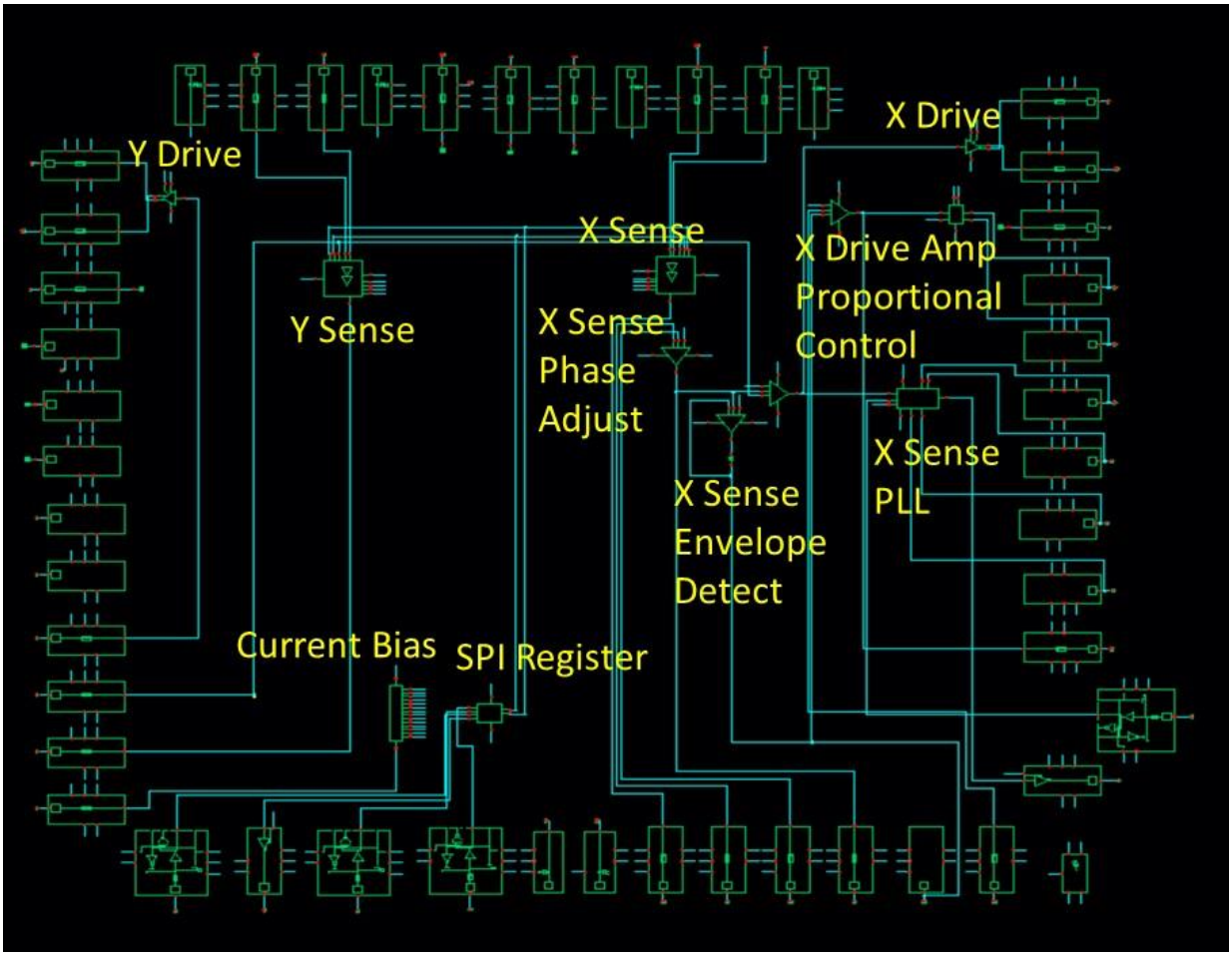

Figure 41 MRG controller ASIC floorplan

Simulation results

Validation of the robustness of the design to fabrication process and operational variation was accomplished using corner simulations with the XFAB SPICE models. The corner simulations cover the full range of expected ASIC characteristic variations. The controller ASIC circuits were simulated across temperatures from 20ºC to 300°C, and across supply voltages from 4.5V to 5.5V, which represents a worst case 10% power supply variation. The circuits were also simulated across the worst speed (ws)

and worst power (wp) corners which represent opposite ends of expected device performance across process variations. Simulations were also conducted utilizing the typical device model (tm). The design was shown to operate within required specifications across the simulation corners, therefore providing a high degree of confidence in successful operation and yield across the range of expected fabrication variations. The simulations across temperature validated the circuit design robustness to device characteristic changes over temperature and the ability of the design to meet performance requirements across the full temperature range of operation up to 300°C.

A subset of simulation results for critical circuit blocks are shown and discussed in the following sections.

High voltage driver

The driver circuit is responsible for providing the excitation to the MRGT. The board level design was limited to 5V excitation. While sufficient to provide enough mechanical displacement to achieve the desired MRGT performance, little margin remained to ensure sufficiency across fabricated devices. The ASIC design extended the operating range of the excitation circuit to produce up to 30V of excitation. The extended range provides the ability to ensure sufficient mechanical displacement of the MRGT can be achieved and maintained across the temperature range and across MRGT device variations. The driver accepts a single ended low voltage signal, and generates a differential high voltage signal to drive the MRGT.

The driver was simulated to validate operation. Example simulation results are shown in Figure 42 and Figure 43. These results show the driver differential output for voltages of 1V and 30V respectively at the 300°C extreme temperature condition.

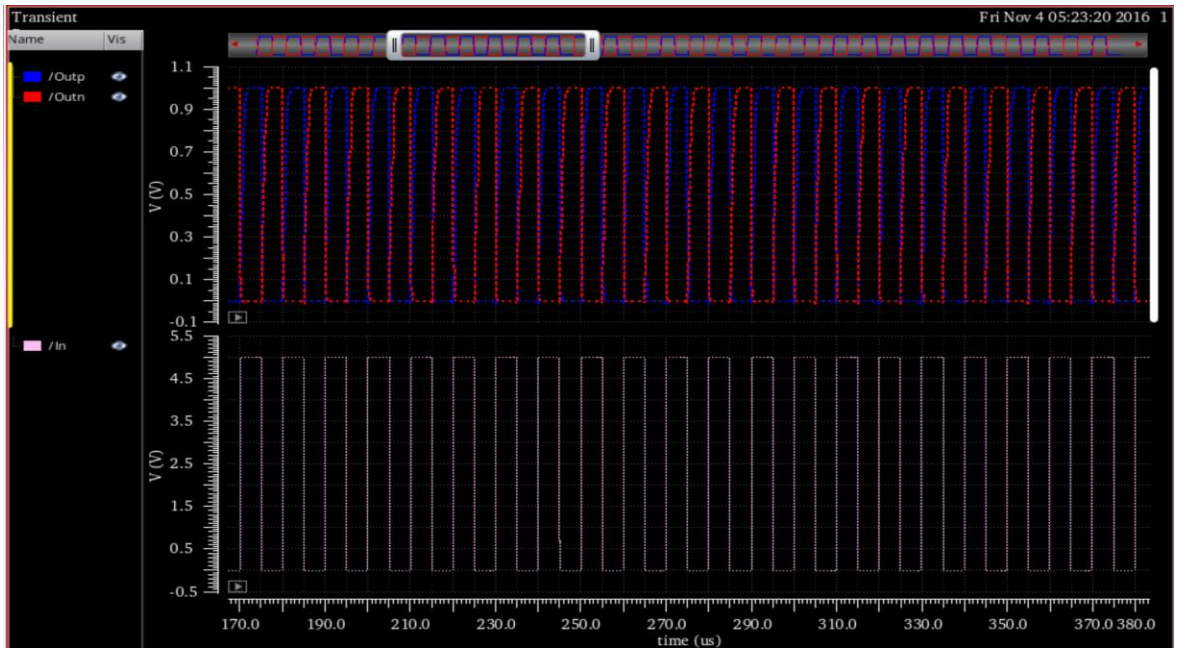

Figure 42 simulated driver output: 1V level at 300°C

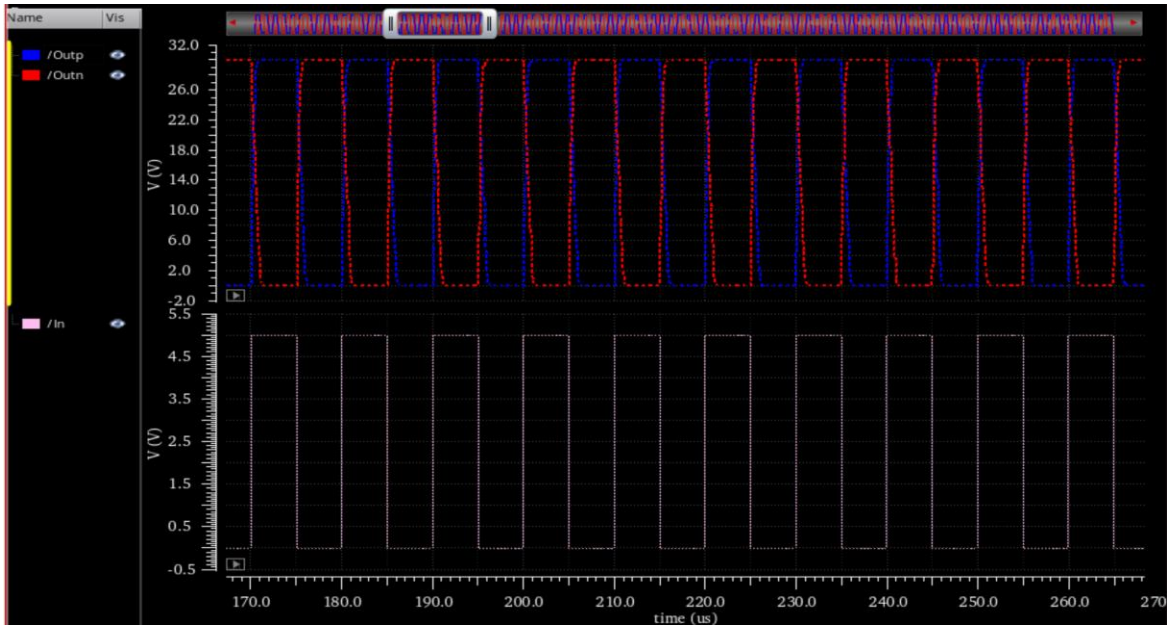

Figure 43 Simulated driver output: 30V level at 300°C

Closed loop controller

The closed loop controller modulates the drive level to maintain a constant sensed drive amplitude. This ensures that a constant mechanical displacement is achieved at the MRGT in the presence of operational and temperature variations and parameter drift.

The controller functionality was simulated to ensure proper operation. Figure 44 is a simulation at 300°C that shows the controller maintaining constant sensed amplitude (left) for MRGT gain characteristics that are varying by as 4x over a 200Hz time scale. While the 200Hz rate of variation is extreme compared to what is expected in real operation, the 4X characteristic change ensures that any device changes across the full temperature range of operation can be tracked and accommodated within the design. While gain and bandwidth of the controller are adjustable with on-chip programable settings, to further reduce risks, off chip means of adjustments are also provided if a change of the range of adjustment is deemed necessary or desirable.

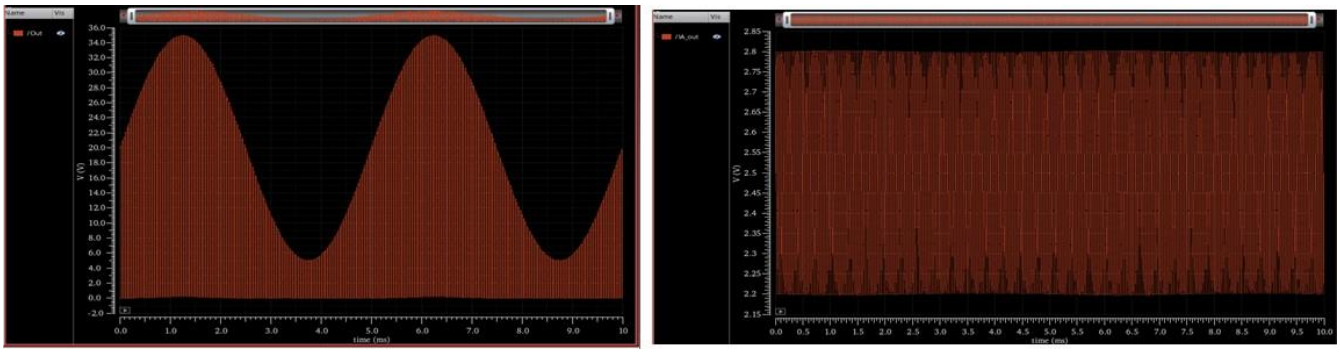

Figure 44 300°C functional simulation results of the closed loop controller

The closed loop controller comprises a number of sub-blocks, each of which were separately simulated across corners to ensure their proper operation. Example of the envelop detector simulation in the worst power corner at 300°C is shown in Figure 45.

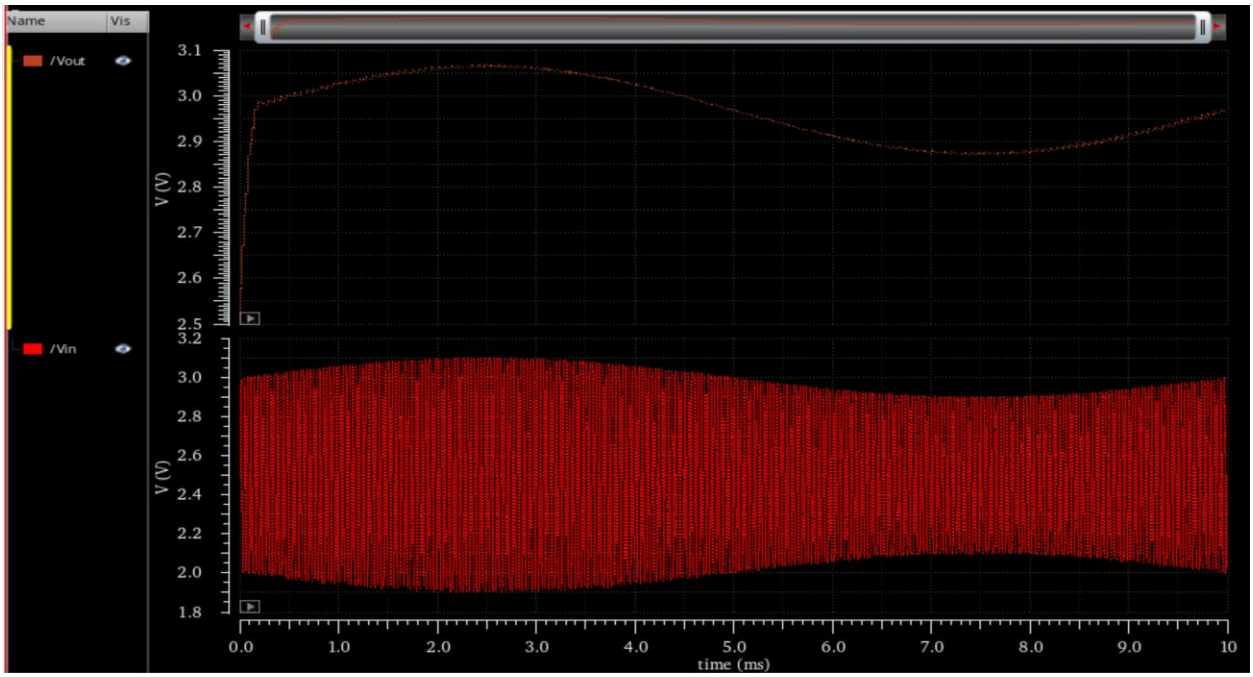

Figure 45 Envelop detector simulation (wp, 300°C)

Analog front end (AFE)

The AFE is responsible for interfacing with and amplifying the input signal from the MRGT. Gain and noise in the AFE are critical parameters to achieving the operational performance needed. The AFE consists of an input charge amplifier followed by an instrumentation amplifier. Example results of the AFE corner simulations are shown in Figure 46. This simulation exercises the worst speed and low supply corner in which slow devices and low power supply are applied, and therefore exercising a highly constrained performance corner. A 3dB gain reduction from 145dB to 142dB, and a noise increase from 400nv/rtHz to approximately 900nV/rtHz are seen across the temperature range.

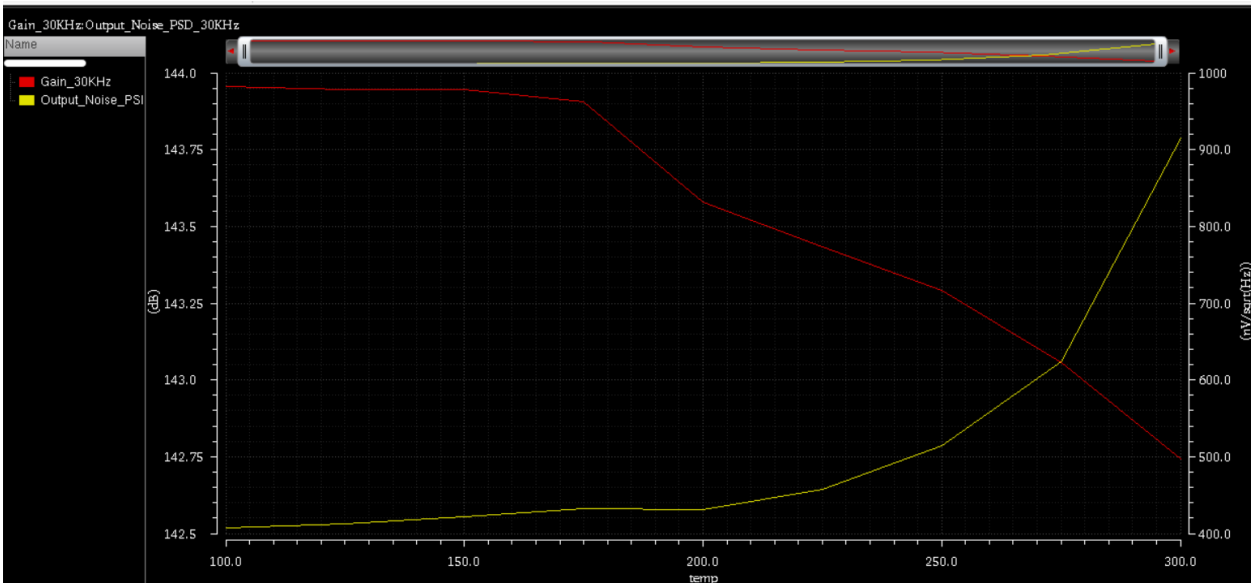

Figure 46 AFE gain and noise over temperature (ws, 4.5V vdd)

The worst case and gain points were then analyzed against the mechanical noise of the MRGT. The analysis in Figure 47 shows that the worst-case electronics noise remains well below that of the mechanical noise, therefore posing an insignificant deterioration to the overall performance of the gyroscope system.

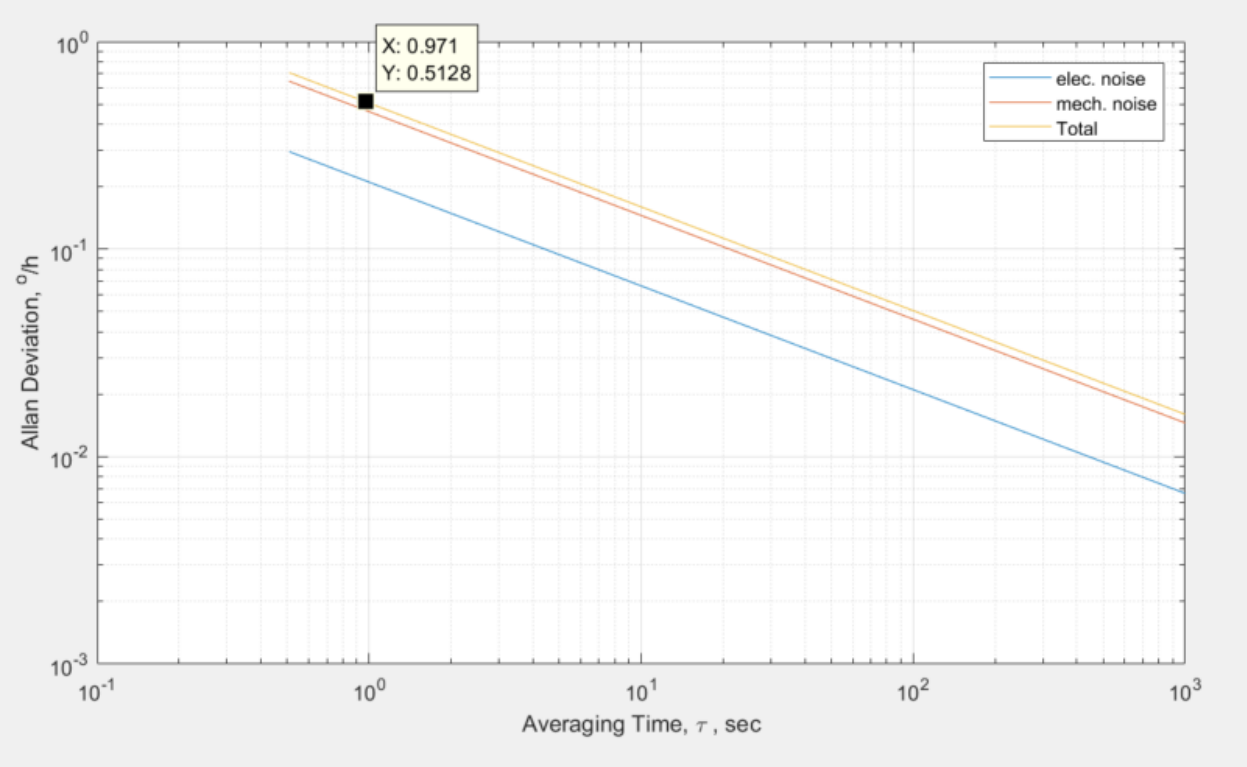

Figure 47 Allan Deviation analysis of MRGT and AFE noise

Table 10 shows the AFE performance summary across corners. The simulations spanned 25-300°C temperature, power supply range from 4.5V to 5.5V and ws, wp and tm process corners. The simulation results met the performance requirements across all corners.

Table 10 AFE performance summary across corners

Performance Summary	Min	Max	Units
VDD	4.5	5.5	V
IDD	1.4	2.6	mA
Operating Temperature	25	300	C
Gain (dbV)	118	152	dbV
Output Noise	269	994	nV/rt-Hz
Output Swing	2.7	3.2	Vp-p
PSSR	-32	-62	dB
Input Common Mode Rejection	-13	-37	dB

Phase locked loop (PLL)

The PLL is responsible for tracking the resonance frequency of the MRGT. The PLL is designed to cover MRGT frequency range from approximately 10KHz to approximately 50KHz and therefore covers the MRGT nominal resonance frequency of 30KHz while allowing for the ASIC to remain compatible with any future MRGT device changes.

The PLL phase noise at 300°C ranges from -99dBc to -112dBc at 1MHz over the wp, tm and ws corners with an integrated jitter of ~300fs rm. The PLL noise and jitter support the noise performance needed to meet overall system noise.

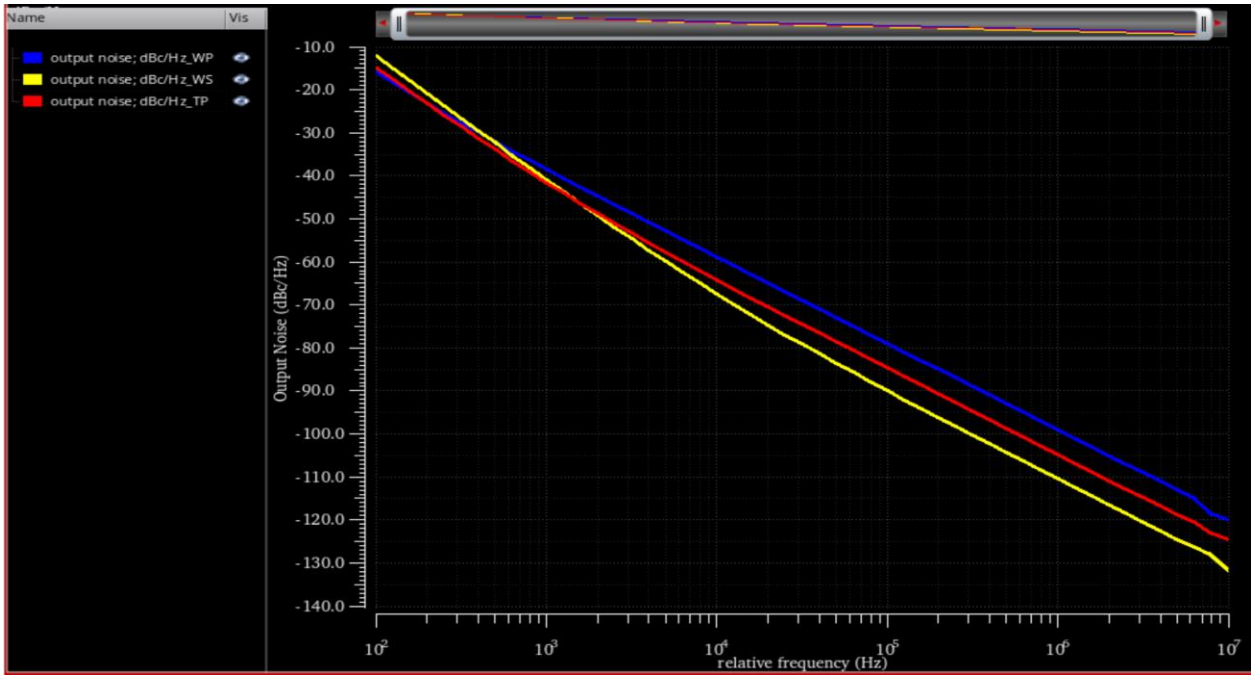

Figure 48 PLL phase noise at 300°C over ws, wp and tm corners

ASIC testability features

Three chip designs have been implemented to facilitate testing and provide additional risk mitigation. The block diagram of each of the three are shown in Figure 49, Figure 50, and Figure 51.

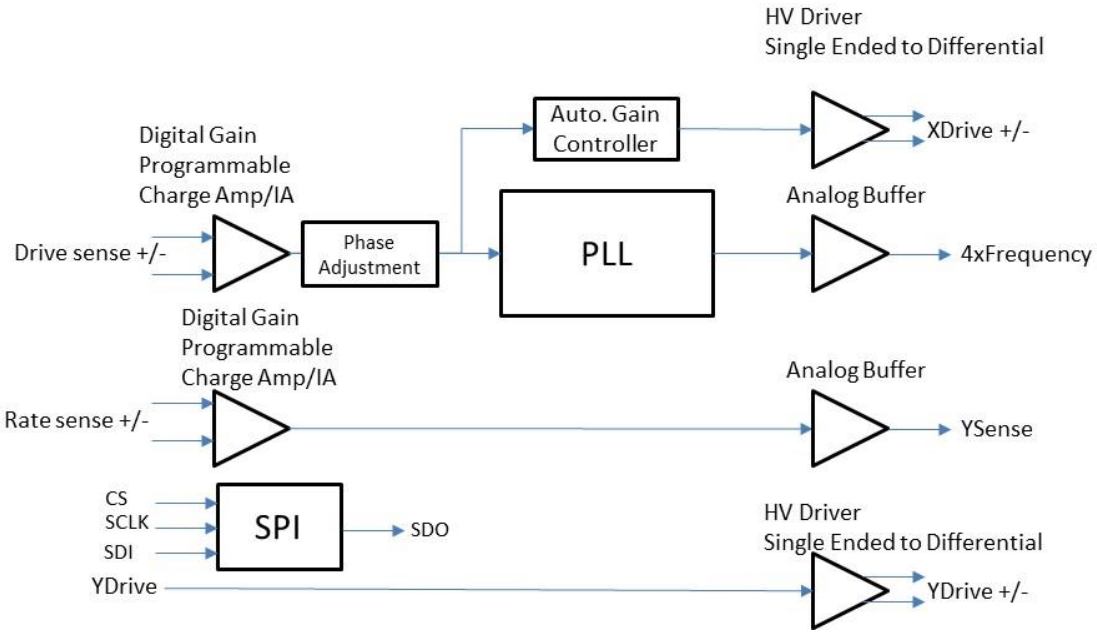

Figure 49 ASIC full controller chip #1

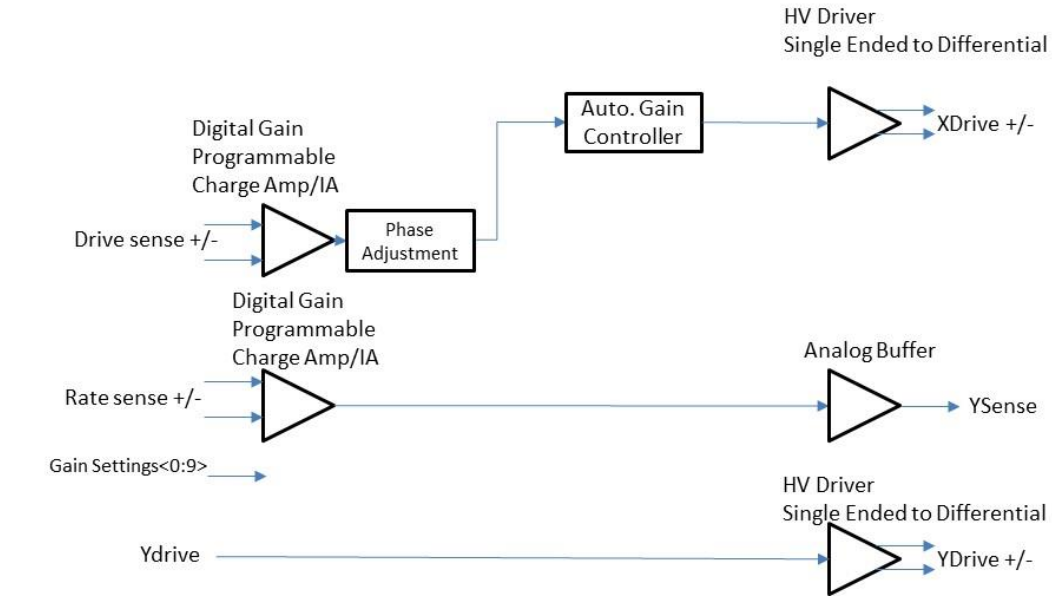

Figure 50 ASIC Receive chain with controlled X-channel drive chip #2

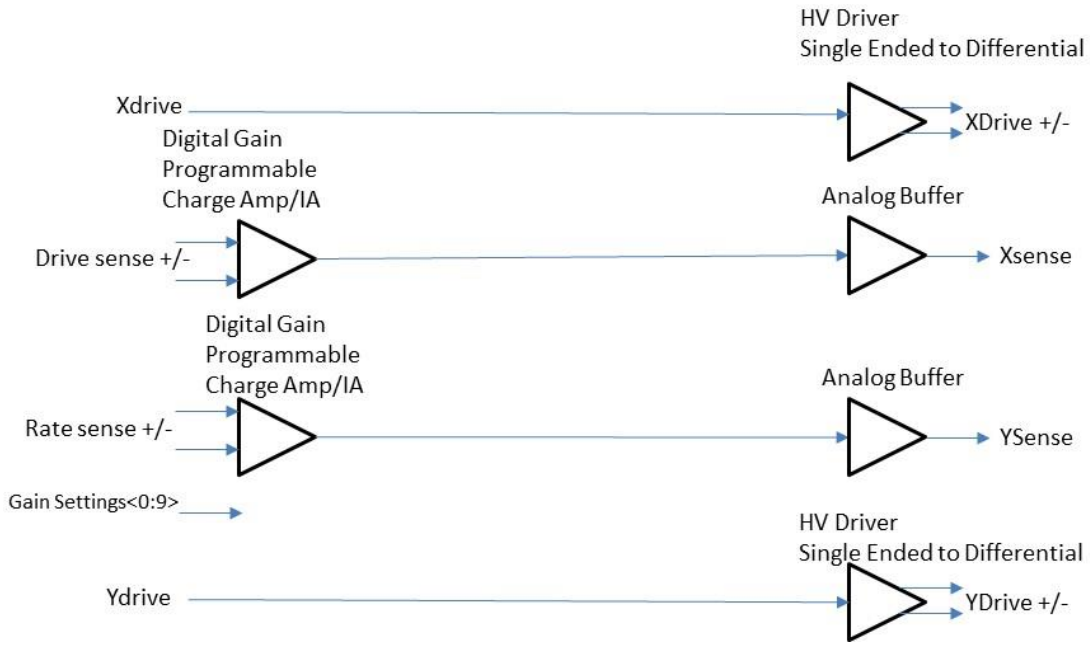

Figure 51 ASIC Receive chain with direct X-channel drive chip #3

The first is of the full controller design. The second is of the receive signal chain and the drive controller, and the third is of the receive signal chain with external direct drive capability. The three designs improve visibility into various functional blocks and provide capability to bypass some functions.

To further facilitate testing, the three chip designs maintain a common IO pad definition and a common chip size. This enables simple swapping for the chips on the test board to facilitate testing and debugging without the need to change the test setup. The three-chip layout is shown in Figure 52 with the full ASIC chip 1 on the bottom, chip 2 in the middle and chip 3 on top. Each of the three chips is 2.8x2.8mm. The common size of the chips also facilitates wafer dicing.

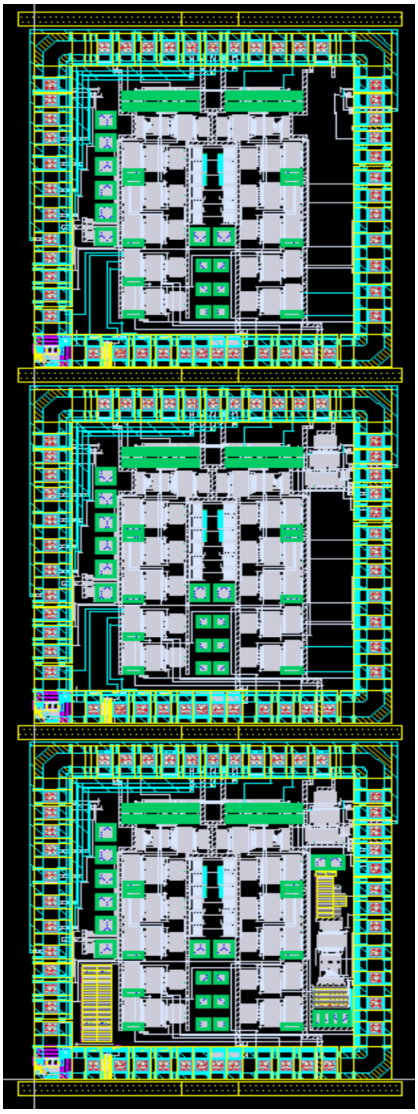

Figure 52 3-chip layout

In addition to the register programable settings supported by the ASIC, additional testability features include external adjustment capability for critical functions such as the closed loop controller gain and bandwidth, phase shifter phase and envelop detector RC filter are controller by external resistors and capacitors to further increase flexibility, improve testability and mitigate risks imposed by limited adjustment range of on-chip components.

ASIC electronics development summary

The ASIC design utilized the electronics requirements that were refined and validated through testing. The ASIC design applied further enhancements to provide additional

operation margins and further reduce risks. One such enhancement is the selection of drive voltages for exciting the MRGT drive mode. The high temperature ASIC was partitioned into two power domains, one operating on 5-volt power domain, where the low noise, high performance analog front-end, signal conditioning, and control loops are performed, and high voltage (25 – 30 volt) domain where the MRGT drive and tuning voltages are derived.

The room temperature electronics allowed for a maximum of 5-volt excitation voltage on the device. The drive voltage increased as a function of temperature to counteract the effect of quality factor loss. To accommodate device-to-device variations, performance changes over time, and to enable larger mechanical displacement which lowers angular random walk noise, the ASIC implemented the drive generation circuitry in the high-voltage power domain allowing for excitation of up to 25 volts of operation. This 5x margin over the board-level electronics ensured sufficient margin to accommodate device-to-device variations, and variations over time and retains sufficient margin from the maximum operating voltage to minimize signal distortions and non-linearities that can increase system noise. Similarly, the electrostatic tuning voltages are controlled from the high voltage domain allowing for wider tuning ranges than the board-level electronics, and therefore accommodating wider MRGT characteristics variations. The ASIC block diagram and layout are shown in Figure 53.

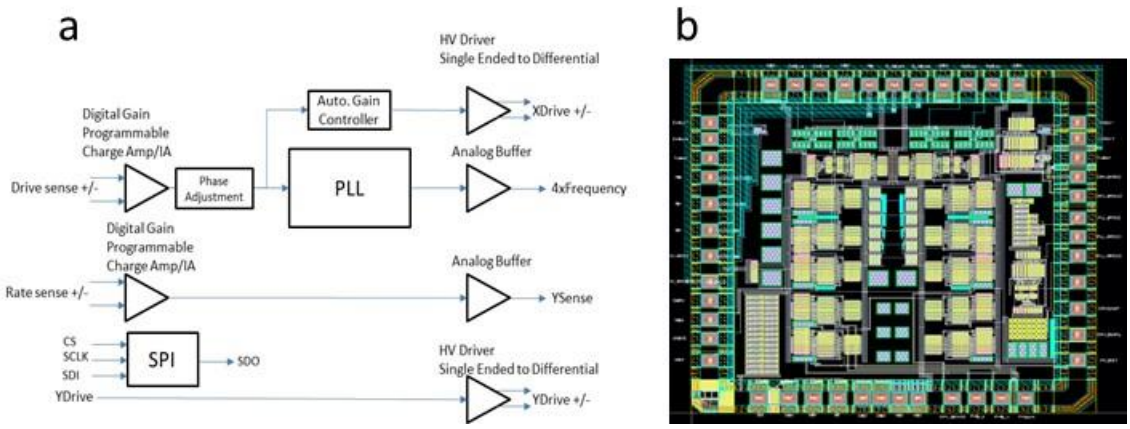

Figure 53 High Temperature ASIC block diagram (a) and layout (b)

The ASIC functionality and performance metrics were validated utilizing simulations across process and temperature ranges from 20ºC to 300°C. The process corners simulated include worst speed, worst power, lowest supply voltage, highest supply voltage, lowest temperature and highest temperature of operation. These corners

represent the range of device characteristics variations that are expected within the fabrication tolerances and operational conditions.

The simulation results covered both functionality of the design and the ability for the design to maintain performance across operational and process variations. The design was validated to comply with the design requirements across the full temperature range of interest. Programable tuning values were implemented for the gain and filter stages, to further mitigate risks, an external adjustment is provided for the tuning parameters and the overall circuit bias currents to provide extended parameter tuning capabilities beyond the programable range of values.

With the detailed design simulation complete, the risk mitigation approaches implemented, the completed ASIC layout verified against the design schematic, and the ASIC completed fabrication at XFAB.

ASIC Electronics component testing

ASIC test board description

To support the testing of the ASIC, and ASIC test board was designed and fabricated. The main functions of the ASIC test board were to enable stimulating the ASIC with signals into the sense channels (X and Y) to verify gain operation, applying gain settings of the sense channel, monitoring outputs of the sense channels, monitoring bias points of the internal ASIC, driving signals into the drive amplifiers and monitoring outputs, and providing monitoring test point of frequency generation from the ASIC. The test board were fabricated on high temperature PCB material as shown in Figure 54.

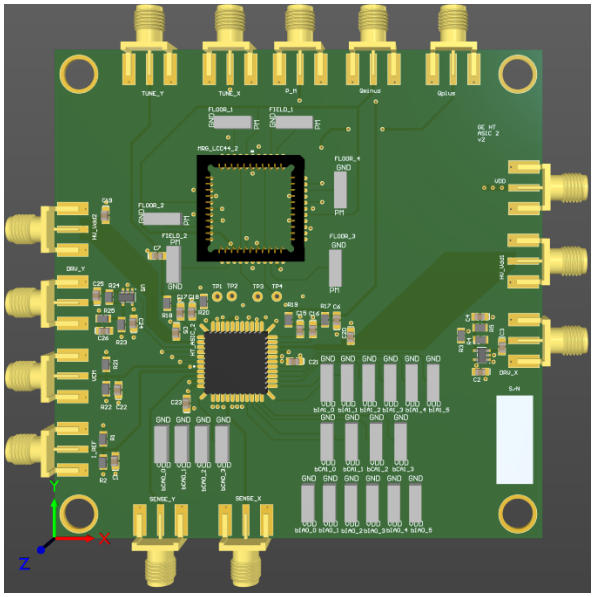

Figure 54 Test board for HT ASIC packaged in ceramic LCC48

ASIC packaging

The baseline packaging option for the ASIC test chips was in a ceramic LCC48 package, which enabled bond wiring out all signals of the ASIC, as shown in Figure 55. The ceramic LCC48 was chosen because it is capable of supporting 300°C operating temperature, its compact form factor and it is readily available commercially. The package overall dimensions of 12.7mm x 12.7mm x 3mm. The LCC48 is the primary packaging used in functional testing on the test boards.

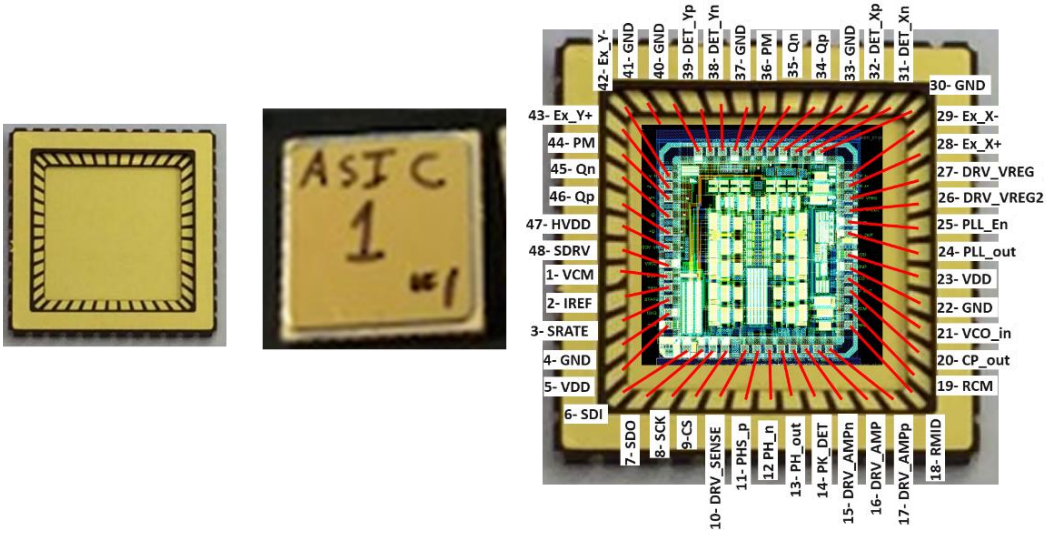

Figure 55 Ceramic LCC48 package (12.7mm x 12.7mm) and HT ASIC bonding diagram

The HT ASICs were also packaged in a second ceramic DIP28 package type as shown in Figure 56. This allowed tests to be conducted at 300°C using already available high temperature capable sockets maintained by GE in a >300°C capable temperature ovens. In order to connect the ASIC into the smaller pin count DIP28 several of the gain settings were hardwired together to reduce the number of inputs/Outputs (IOs) required for testing

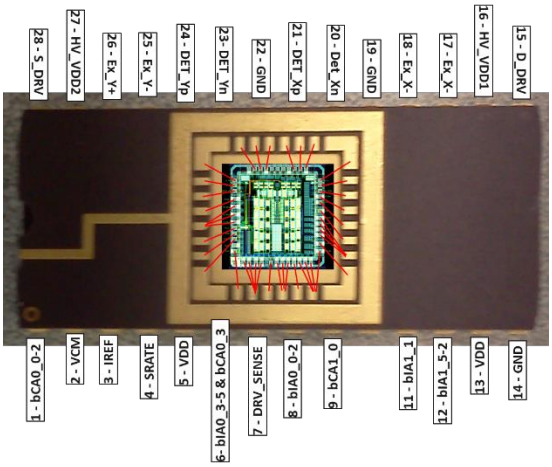

Figure 56 Ceramic DIP28 package (15.2mm x 35.5mm) and HT ASIC bonding diagram

Test results

Functional testing

Test of the sense channel gain, drive channel levels, and on chip frequency tracking was completed in the ceramic LCC48 package on the test boards. The sense gain operated as expected. Representative test results are summarized in Figure 57, Figure 58, Figure 59, and Figure 60. At the 1x AFE gain setting, the gain of the sense channel has a peak of -42.3dB, at the 2x AFE Gain setting, the peak gain increases by the expected 6dB to -36.3dB. For the 20x gain setting, the peak gain further increases by 20dB to -16.3dB and at the 40x gain setting, a further 6dB increase to -10.3dB is achieved. The gain setting results validate that the selectable gain follows the design intent and achieved the expected gain setting capabilities.

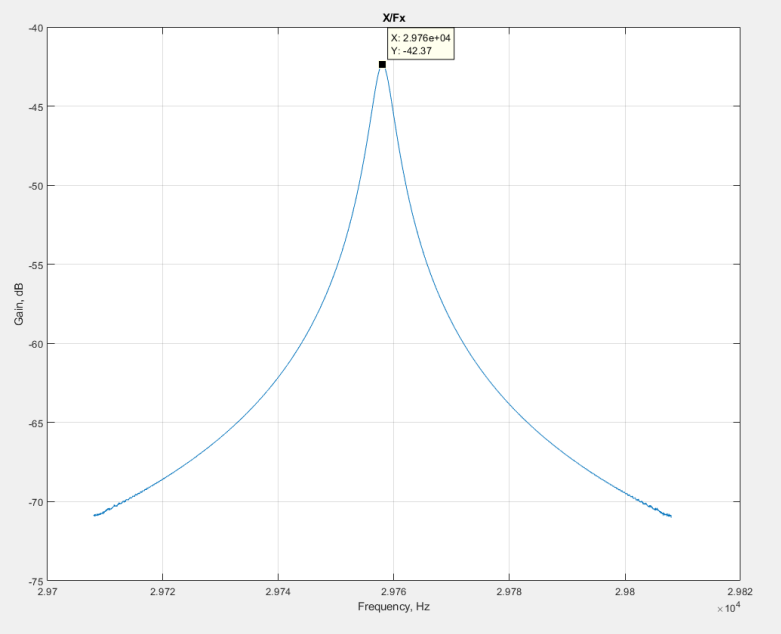

Figure 57 Test results of X sense channel gain ASIC/MRG test board with AFE gain set to 1x

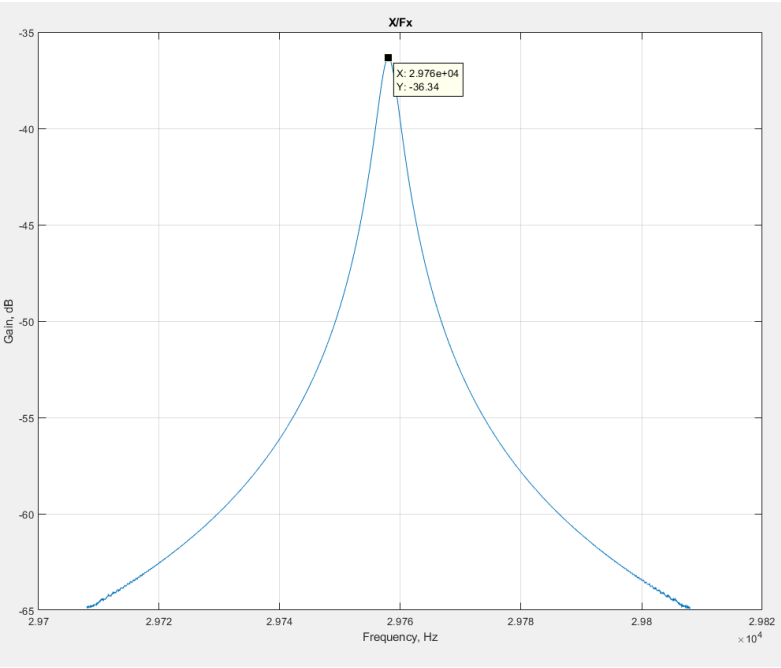

Figure 58 Test results of X sense channel gain ASIC/MRG test board with AFE gain set to 2x

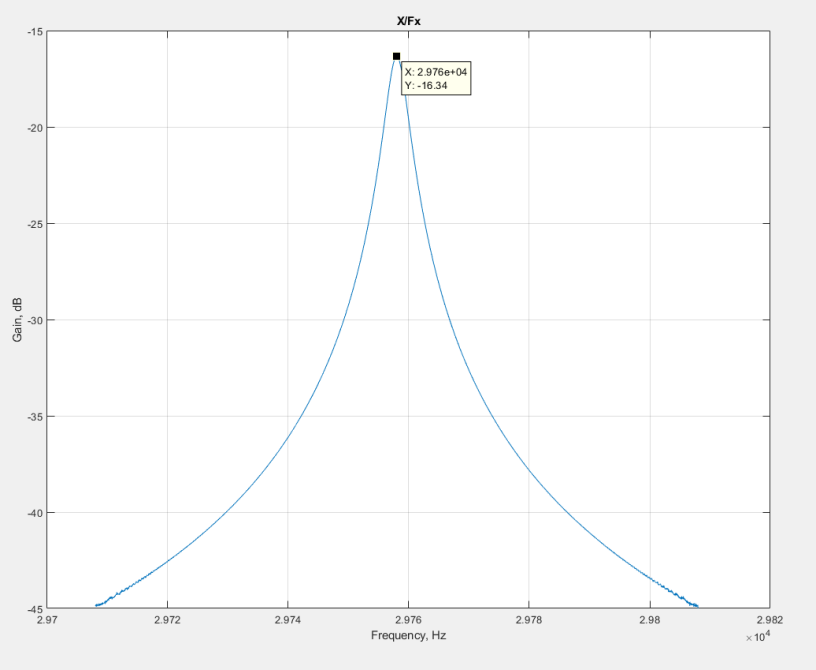

Figure 59 Test results of X sense channel gain ASIC/MRG test board with AFE gain set to 20x

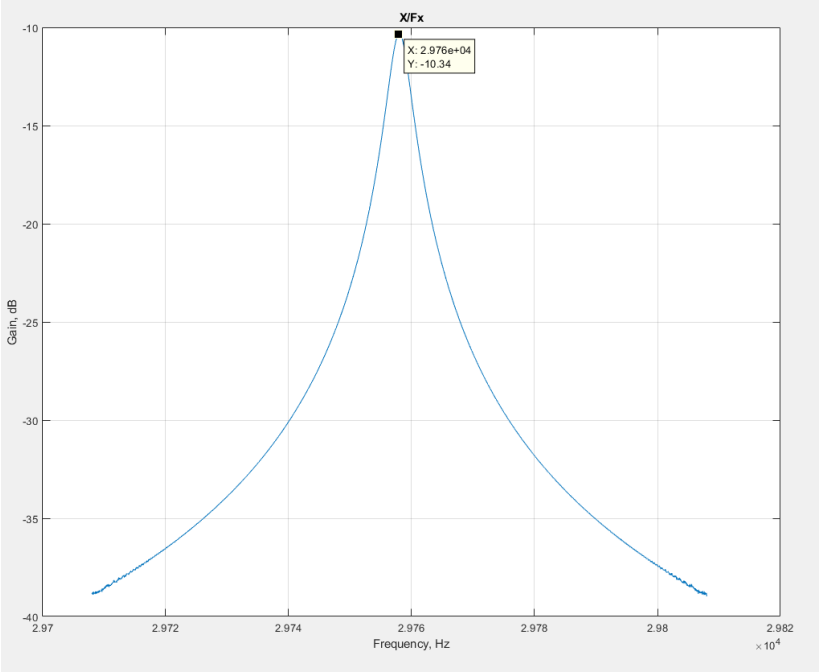

Figure 60 Test results of X sense channel gain ASIC/MRG test board with AFE gain set to 40x

The drive channel was tested from its minimum drive level 1Vpeak to double the required MRG maximum (6Vpeak) to 12Vpeak and operated, as shown in Figure 61

and Figure 62. The testing validates the ASIC's capability to achieve drive capability that covers the entire drive range of drive voltages from 1volt to 12 volt peak.

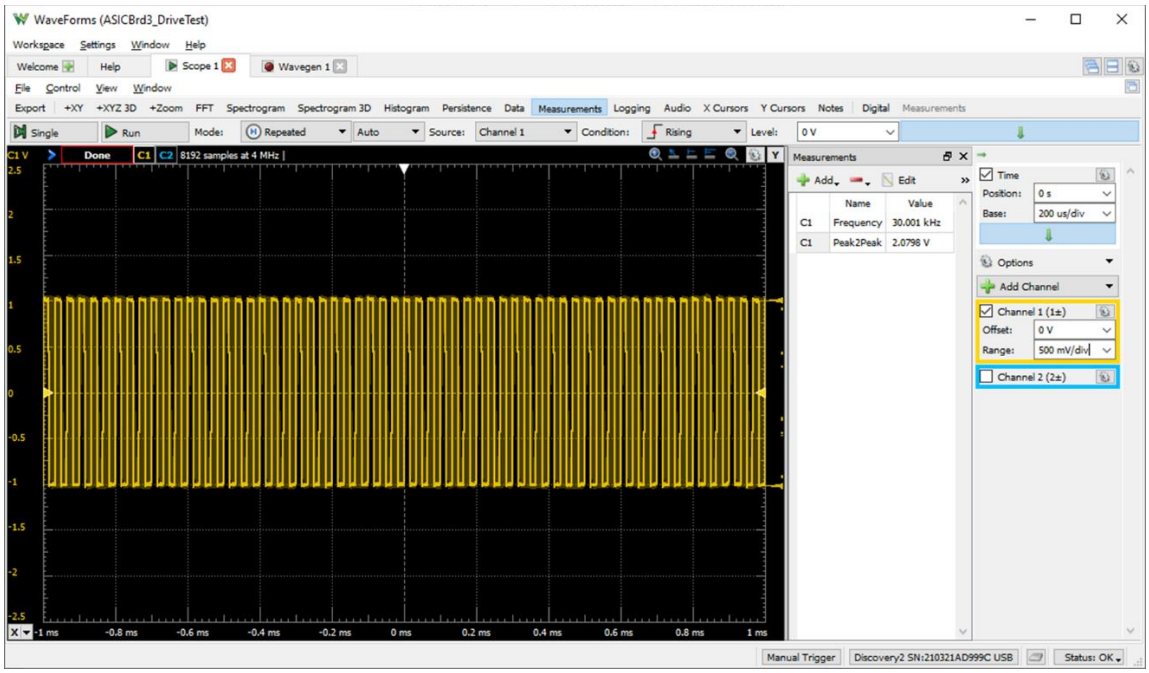

Figure 61 Test results of HT ASIC drive channel 1Vpeak minimum drive level

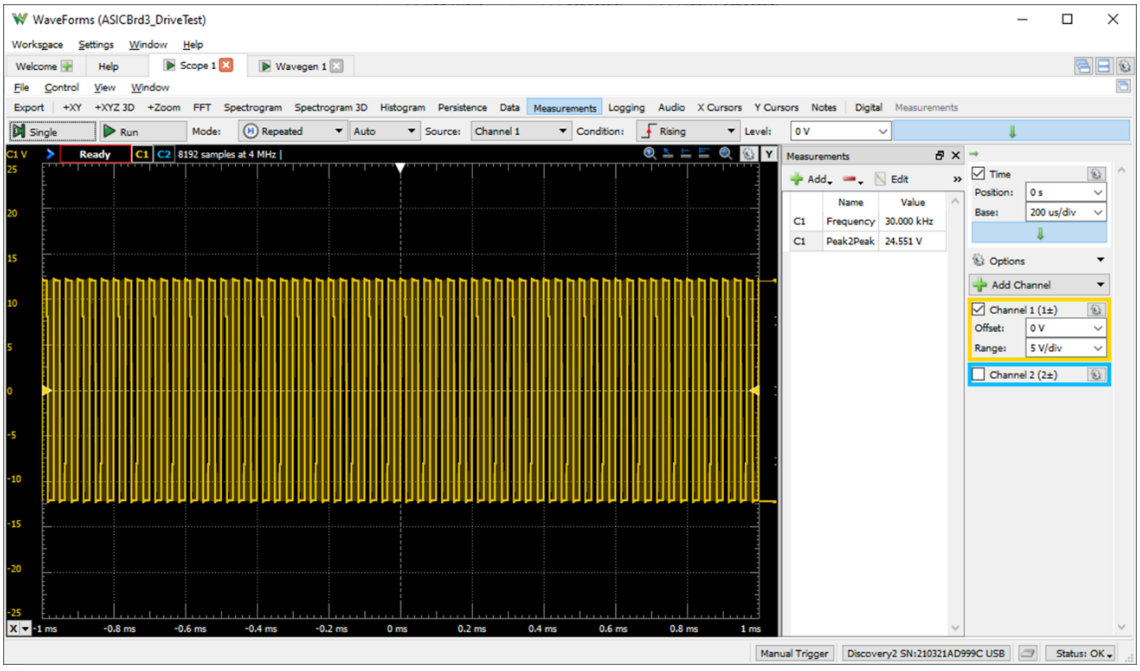

Figure 62 Test results of HT ASIC drive channel 12Vpeak maximum drive levels

Testing of the on-chip phased locked loop (PLL) frequency span was tested from ~20KHz – 60KHz, which provides a wide margin of coverage for the nominal MRG frequency of operation ~30KHz. Figure 63, Figure 64 and Figure *65* show the PLL test results and validate PLL operation at 20KHz, 30KHz and 60KHz, respectively. This validates the ASIC's capability to interface to MRGT devices with wide resonance frequency characteristics and covers the range of interest of 30KHz for the nominal MRGT resonance frequency.

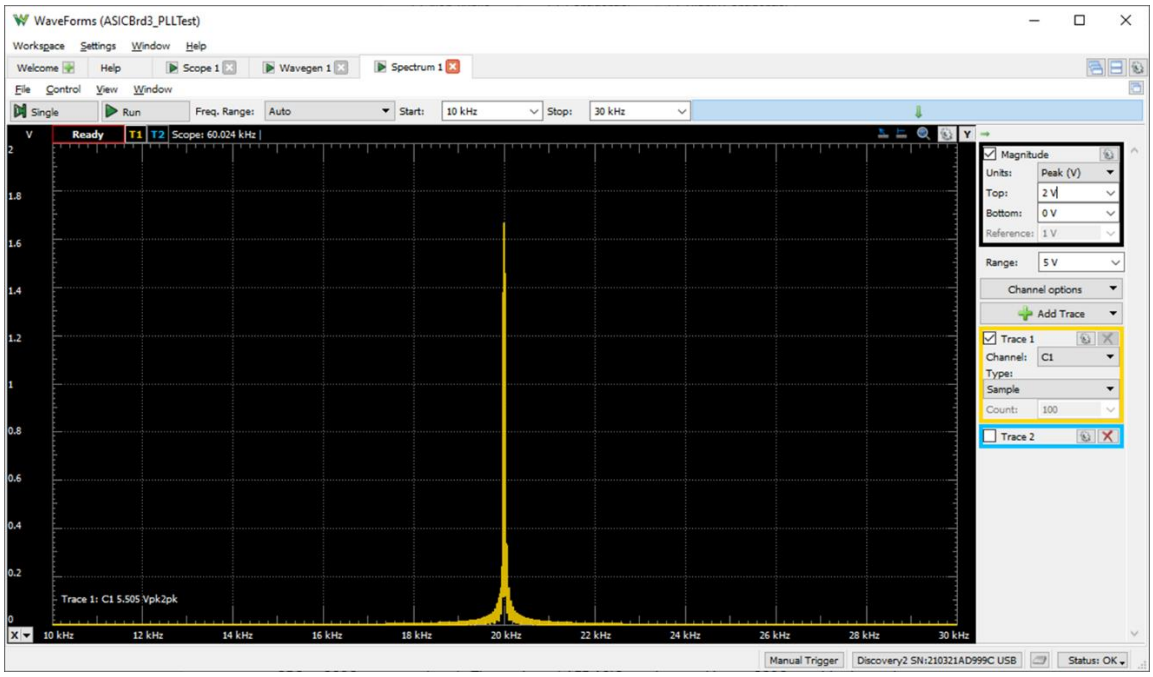

Figure 63 Test results of HT ASIC on chip on-chip phased locked loop frequency span testing at 20KHz

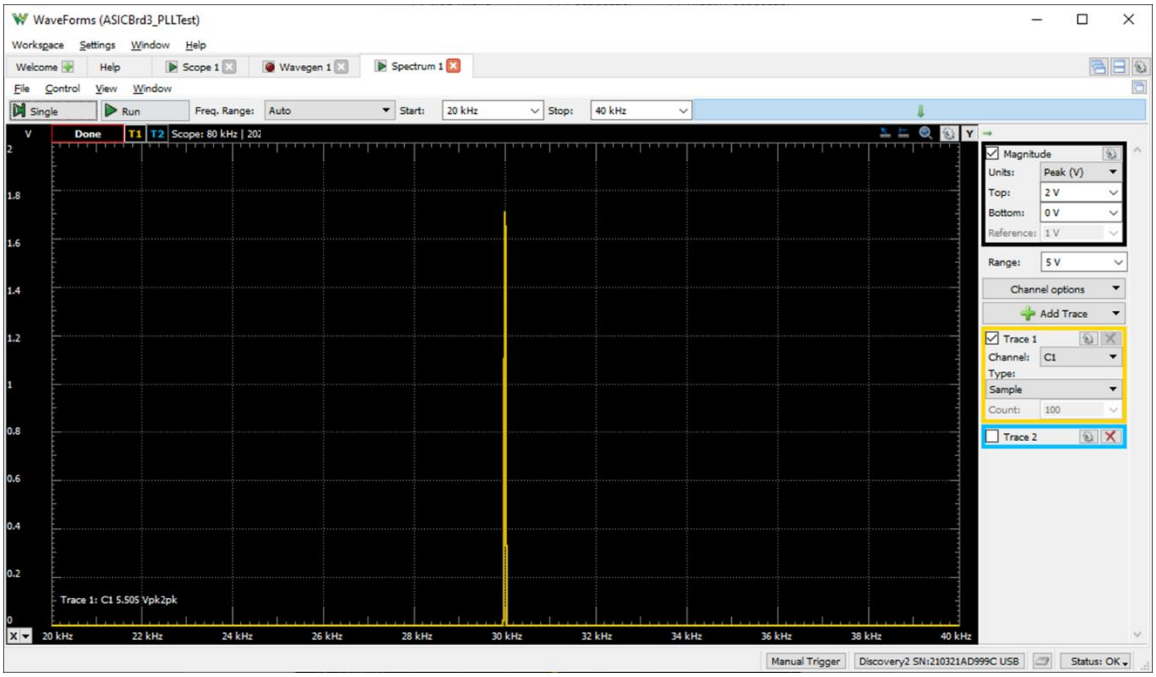

Figure 64 Test results of HT ASIC on chip on-chip phased locked loop frequency span testing at 30KHz

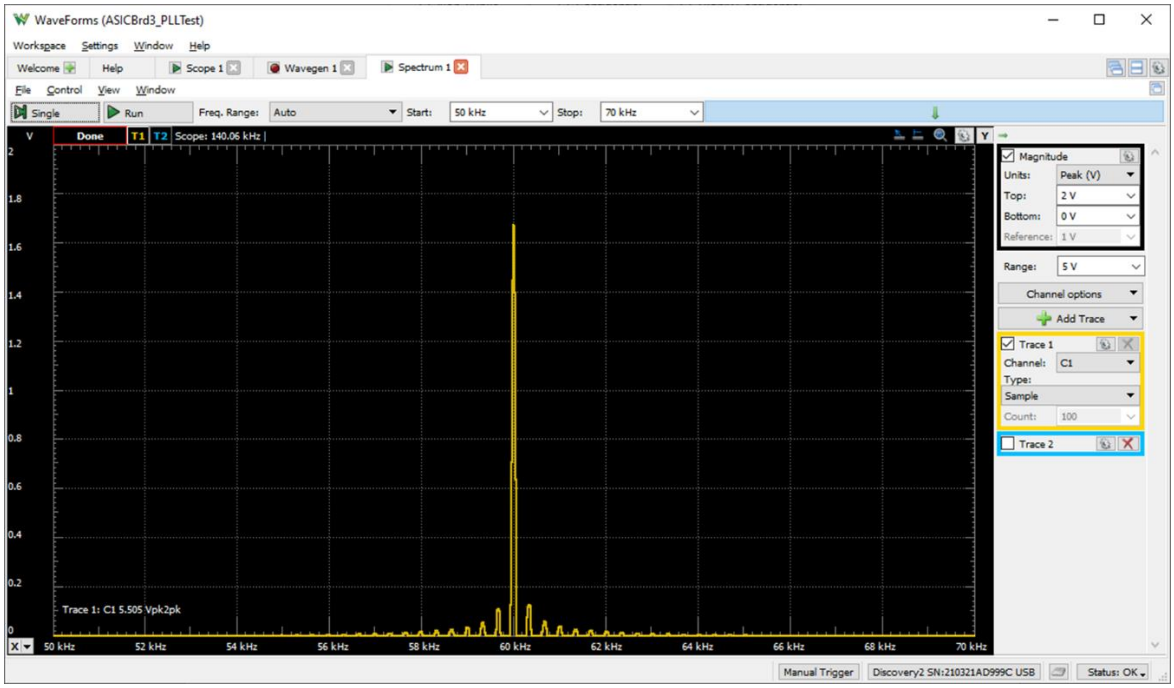

Figure 65 *Test results of HT ASIC on chip on-chip phased locked loop frequency span testing at 60KHz*

High temperature testing

Testing of the analog frontend (AFE) ASIC in a ceramic DIP package across temperature from 25°C to 300°C was completed. The packaged AFE ASIC was inserted into a 300°C capable thermal chamber into ceramic test socket with wiring that

provided the ability to control the ASIC AFE gain, drive signal through the AFE drivers, and monitor the output sense channel noise. The testing was accomplished through probes on the output channel into a datasampler and the noise power spectral density was calculated in MATLAB. The test setup is shown in Figure 66.

Figure 66 Test setup with 300°C chamber, probe connections to test system (outside chamber), and test equipment

There were some challenges in achieving low noise due to electromagnetic interference (EMI) leakage into the unshielded high temperature cabling. Coaxial shielded cabling was used to probe the sense signals during the noise test to reduce this effect, and the thermal controller was shut off during the noise test at each temperature point to reduce its high current EMI. Even with these precautions leakage from 60Hz wall power are seen in the data. Averaging of the data to determine the noise floor was accomplished to further mitigate its effect. Figure 67 shows the measured ASIC noise at room temperature and 300°C.

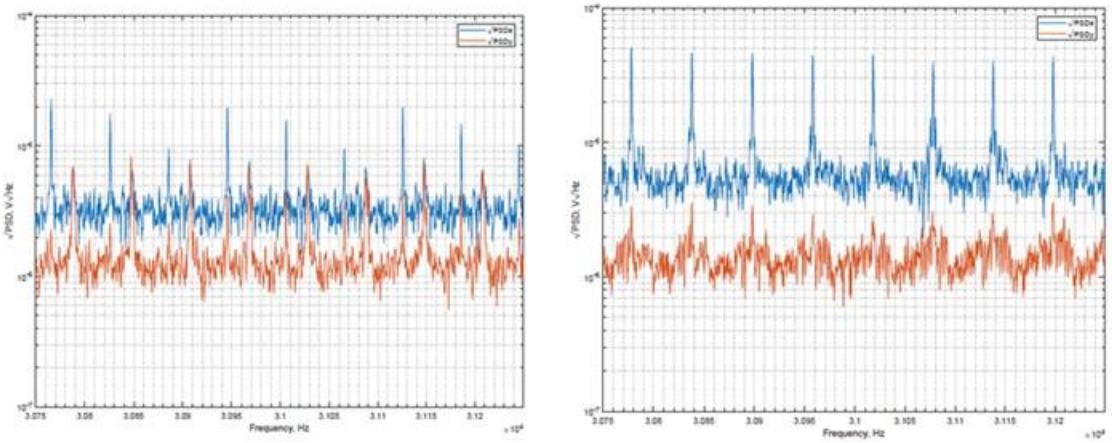

Figure 67 ASIC high gain X channel (blue), low gain Y channel (red) noise PSD at 25°C (left), 300°C (right)

The summary of data is shown in the following table of measured noise floor is show in Table 11.

Table 11 Noise floor measurements for high and log gain channels across temperature

Temperature	X Channel (Cfb=1pF/GIA=10X -High Gain)	Y Channel (Cfb=24pF/GIA=1X -Low Gain)
25°C	1.3uV/√Hz	2.8uV/√Hz
100°C	1.5uV/√Hz	3.1uV/√Hz
200°C	1.8uV/√Hz	4.3uV/√Hz
300°C	2.2uV/√Hz	5.2uV/√Hz

The gain settings were chosen as they are representative of the operating conditions for the MRG gyroscope with low gain being set on the ASIC for the drive channel, and the high gain being set on the gyroscope rate sense channel. Comparison to the simulated ASIC results were completed, and results are summarized at the room and 300°C in Table 12.

Table 12 ASIC noise measurement versus simulation comparison

Temperature	25°C	300°C
Simulation (High gain setting)	0.35uV/√Hz	2.7uV/√Hz
Measurement (High gain setting)	2.8uV/√Hz	5.2uV/√Hz

TIA high gain mitigation

The HT ASIC front end amplifier has all its components implemented on chip. It was found during testing that the very high resistance (~1Gohm at room temperature down to ~300Mohm at 300°C) of the on-chip feedback resistor caused the HT ASIC to be very sensitive to test board leakage. This exhibited as HT-ASIC outputs saturating, particularly at room temperature. To isolate this issue off-chip AC coupling capacitors were implemented that blocked potential leakage paths into the ASIC. Also, discrete electronics testing was demonstrated with ~10x lower resistance (100Mohm) that did not exhibit this susceptibility.

Further subsequent testing of the HT ASIC with the ceramic DIP28 in a socket and ceramic chip on board testing of the 1,000hr test confirmed that without leakage paths of a test board the ASIC operated correctly. In order to make the HT ASIC less susceptible to board leakage a metal change was fabricated in a second spin at XFAB to allow the user to set the feedback resistance with an off-chip resistor. To implement this, two of the extra ground pads in the ASIC were re-connected to the-necessary

internal point in the HT-ASIC frontend amplifier. This change was simulated and showed no impact to noise or gain performance at the MRGT frequency (~30KHz). The change also still enables use of the ceramic LCC48 packaging with a minimal 2 pin change, as shown in Figure 68 Metal change HT ASIC bonding diagram in ceramic LCC48.

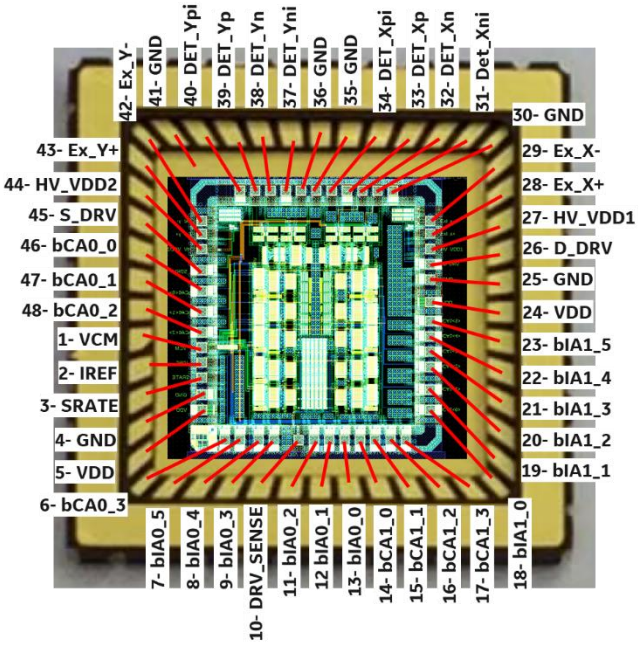

Figure 68 Metal change HT ASIC bonding diagram in ceramic LCC48

ASIC validation and comparison with simulation summary

The simulated performance versus measured performance for the HT ASIC overall matched quite well. The bias points measured were very close to the simulated results. The gain settings and measured sense channel gain showed correct operation and close correlation to simulation. The maximum operating voltage for the drive was demonstrated in measurement up to 12Vpeak, which is ~2x larger than required for maximum MRG displacement operation. The noise floor achieved in the high temperature test chamber of the ASIC was challenging due to the leakage of 60Hz and associated harmonics and other high current EMI into the high temperature cabling of the test setup. The absolute measured noise performance, at 300°C is ~2x larger than simulated. This performance is still below the Brownian thermal noise floor of the MRG. So its operation is well within the 10x margin that was predicted by analysis.

Integrated system development and testing

The developed MRGT and high temperature ASIC have been tested on a component level and shown to meet the design intent and requirements developed during the requirement development portion of the project. The second budget period of the project focused on the integration of the developed components and validating the functionality, performance, and lifetime capability of the integrated gyroscope system. The test approach and results are discussed in detail in the subsequent sections of this report.

Testing objectives and success criteria

Testing conducted during the project's second budget period targeted evaluation of two main aspects of the gyroscope system and its capabilities to function and perform at temperatures from room temperature to 300°C while achieving sufficiently long lifetime operation at high temperature to meet the needs of geothermal drilling campaigns. This evaluation is accomplished through functional and lifetime testing. The testing falls under three categories each with their associated test objectives and success criteria. The three testing categories are:

1. Functional capability demonstration
2. Performance capability evaluation
3. Lifetime capability assessment

Success criteria

The success criteria have been developed to define the target operational and survivability metrics that will be used to evaluate the MEMS gyroscope and electronics. Additionally, these metrics have been utilized to guide the test approach development to ensure that the testing possesses sufficient fidelity and lifetime capability in support of achieving the test objectives.

Functional capability demonstration

The functional capability demonstration testing aims to evaluate the combined functionality of the MEMS MRGT device along with the high temperature Silicon on Insulator (SOI) Application Specific Integrated Circuit (ASIC). Interface compatibility, excitation, control, and readout signal levels will be validated. A summary of the functional test parameters and success metrics is summarized in Table 13.

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Table 13: Functional test parameters and metrics

Test parameter	Success metric
Excitation frequency control	MRGT can be driven into resonance
Excitation amplitude capability	Drive level sufficient to achieve detectable sensed signals
Electronics receive chain functional	Able to detect received drive mode and sense mode signal
Functional operation	Sense output responsive to rotation rate
Temperature capability	Sense output responsive to rotation rate at temperature up to 300°C

Performance capability evaluation

The performance capability evaluation testing phase will assess the performance of the combined MEMS gyroscope and electronics across the temperature range from room temperature to 300°C. A summary of test parameters and success metrics for the performance capability evaluation is summarized in Table 14.

Table 14: Performance test parameters and metrics

Test parameter	Success metric
Quality factor	>10,000 at room temperature
	>3,000 at 300°C
Alan Deviation at 1 second	<2 degrees/hour at room temperature
	<10 degrees/hour at 300°C
Integration time	Bias instability <0.5 degree per hour across temperature

Lifetime capability

The lifetime capability assessment testing will evaluate the MEMS MRGT and ASIC capability to operate over extended periods of time at 300°C. The evaluation includes the capability of the packaging approach and material set choices to survive the extended time at temperature. Functional testing at intervals during the test will be utilized to track device responsivity to rotation rate over the duration of the high temperature testing. Any detected deterioration or failures will be analyzed and utilized in formulating improvement recommendations if any. A summary of test parameters and success metrics for the lifetime capability evaluation is summarized in Table 15.

Table 15: Lifetime test parameters and metrics

Test parameter	Success metric
Survivability	Die-attach maintains adhesion over test time
	Wirebonds maintain contact over test time
	Interconnects maintain connectivity over test time
Functionality	Responsivity to rotation rate is maintained over test time
	Device power consumption changes <10% over test time

Integrated gyroscope test platform description

To support the MRGT and ASIC integration testing over temperature, a custom 300°C capable ceramic substrate was designed and fabricated. The MRGT, ASIC, and passive components (resistors and capacitors) were then attached to the board with high temperature capable die attach. The MRGT and ASIC inputs and outputs (IOs) were electrically connected to the substrate using wirebonds. The ceramic substrate connects to a conventional temperature data collection interface board through an edge connector as seen in Figure 69.

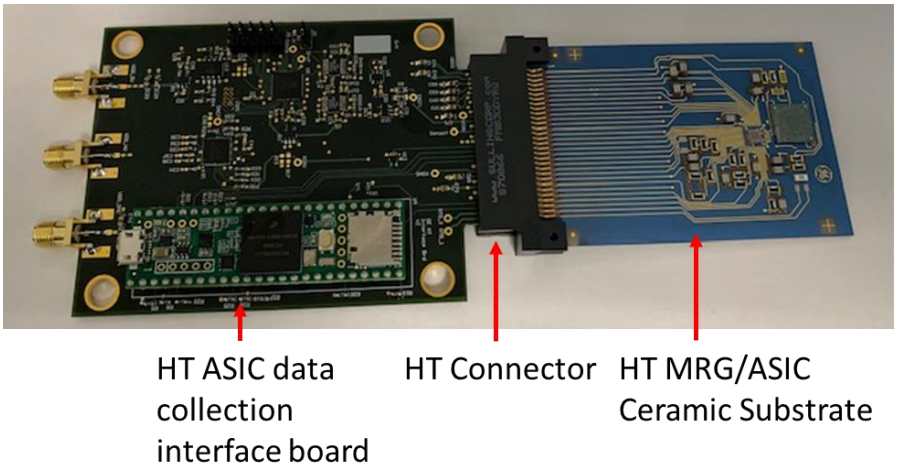


Figure 69 Test board configuration for integrated testing from room temperature to 300°C

Testing was conducted utilizing lab instrumentation and the combined MRGT/ASIC functionality was measured at room temperature. The test setup was then transferred to the hot plate and heated to 300°C and remeasured. Further details on the test

configuration and test boards utilized is provided in the subsequent subsections of this document.

Thermal gradient testing

The ceramic substrate was designed to enable localized heating in the vicinity of the MRGT, ASIC and passives under test to achieve 300°C test conditions, while providing a sufficient temperature gradient to achieve sufficient temperature drop at the board edge connector and the data collection interface board to maintain compatibility with the thermal capabilities of the edge connector and conventional data collection electronics utilized on the data collection interface board. Measurements were conducted on the hot plate to validate the thermal gradient as shown in Figure 70. The data shows that to achieve 300°C at the ceramic test board, a hot plate setpoint of 350°C is required. At that test condition, the edge of the ceramic board reaches a temperature of ~207°C.

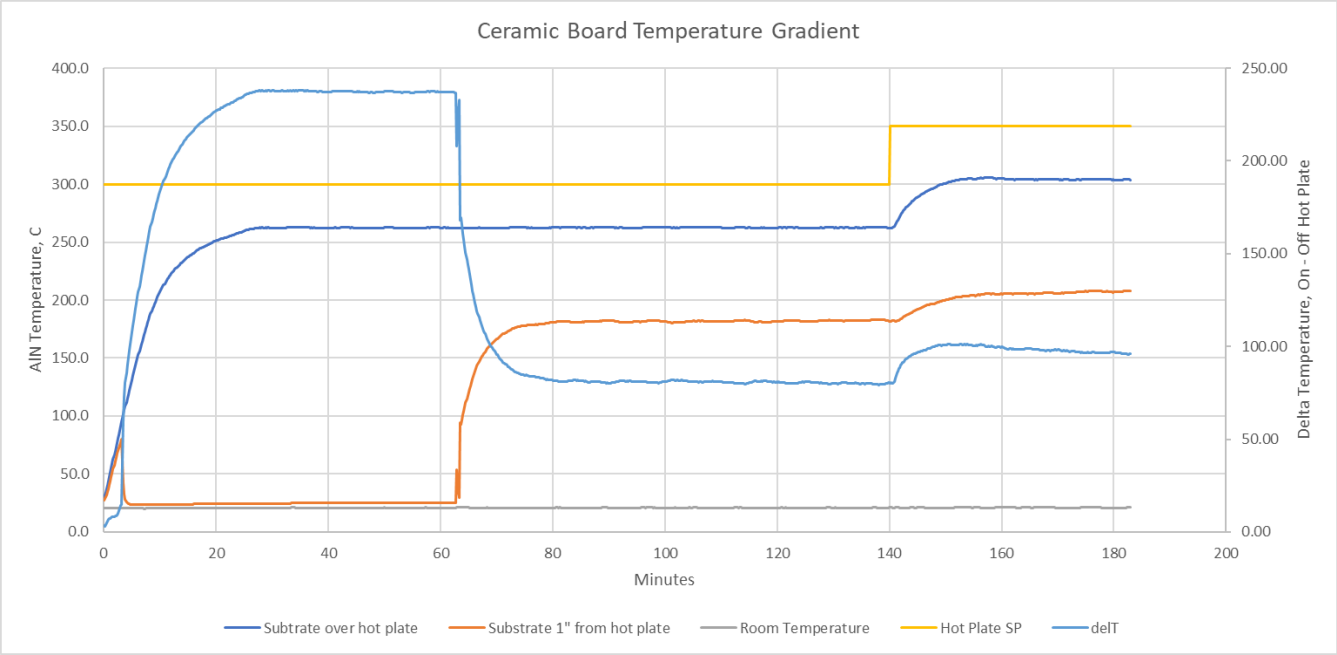


Figure 70 Temperature gradient test results

While the results achieved showed that a significant thermal gradient can be achieved, and that additional thermal drop at the edge connector is expected, it was determined that the temperature at the edge of the data collection interface board will likely exceed 170ºC in the duration of extended testing. The initial data collection and interface test board was designed and built utilizing conventional FR4 circuit board material, a revision was made and fabricated utilizing polyamide material to provide further thermal capability.

Additional thermal testing was conducted to evaluate the tests setup's capability to maintain temperature to multiple devices under test to support the long-term testing. A sample AlN board with Resistance Temperature Detector (RTD) and polyimide data collection interface board were connected using a Sullins FMB30DYRR 200°C card edge connector. Temperature was measured at the RTD, connector and AlN board where the end is 1" off the hot plate. Since this data is critical for the ability of the test setup to support 1,000 hours of testing, the test was run for an extended time to ensure that all components have reached steady state. Data was collected over a 16-hour period and is shown in Figure 71.

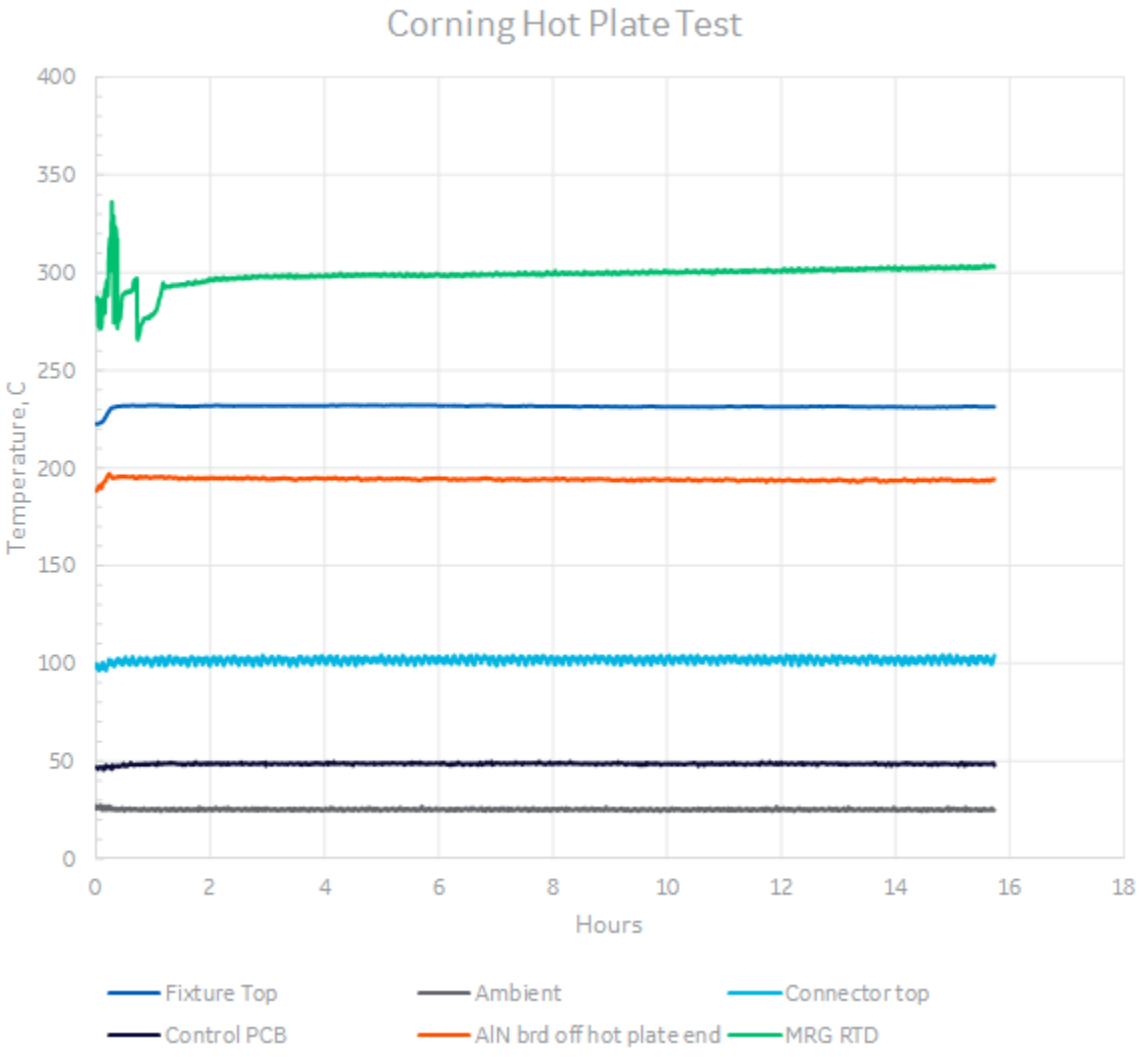


Figure 71 Component temperature testing on hotplate

The hot plate setpoint was adjusted so the MRG RTD reaches 300°C. At this temperature, the connector was at 100°C and the control board was at 50°C. Both well below their temperature capabilities.

To support testing multiple samples, the temperature distribution of the hotplate was first measured utilizing RTDs placed at different locations on the hotplate surface. The measured temperature distribution is shown in Figure 72. The measurement showed approximately 80°C drop between the center and the corner. To minimize the variation between the test samples, a placement approach was devised that placed the boards more symmetrically around the hotplate towards the center.

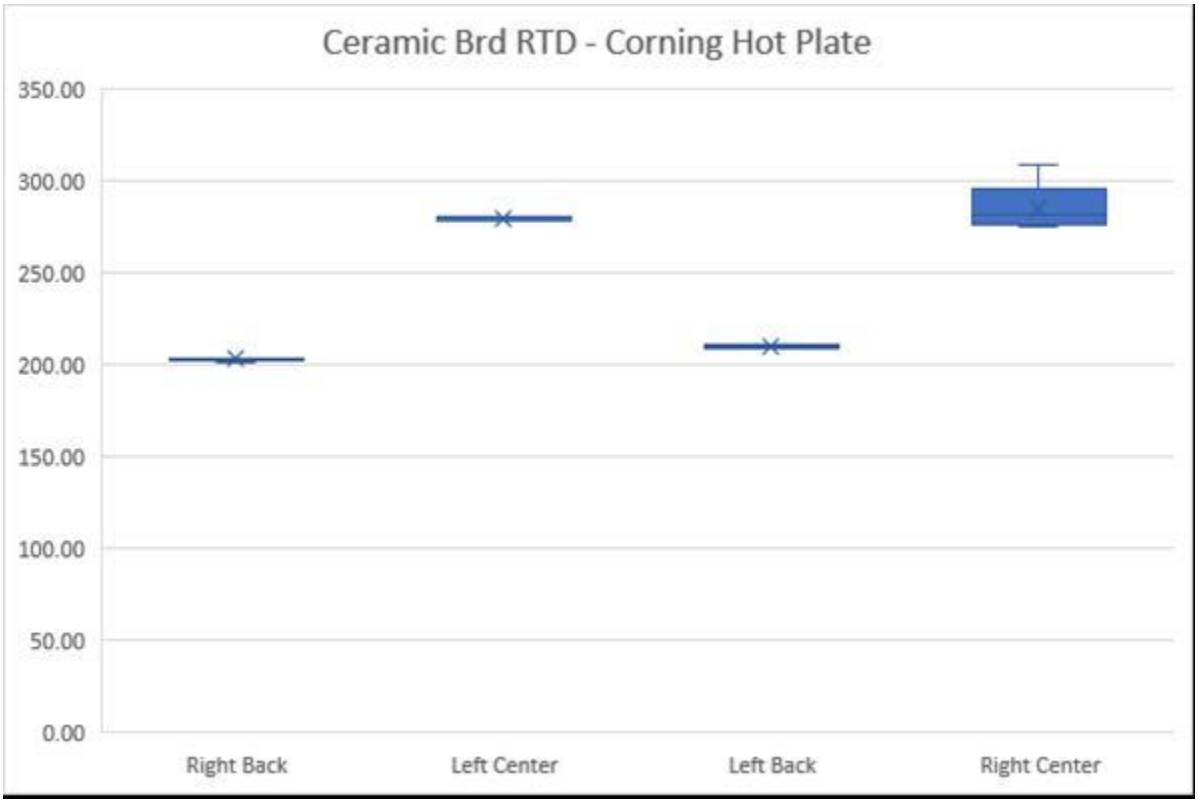


Figure 72 Hotplate temperature distribution in °C

Next, 4 ceramic boards were assembled onto the hotplate in the selected locations and instrumented with RTDs and the temperature spread was measured. Figure 73 shows that the temperature spread between the 4 samples was reduced to less than 50°C.

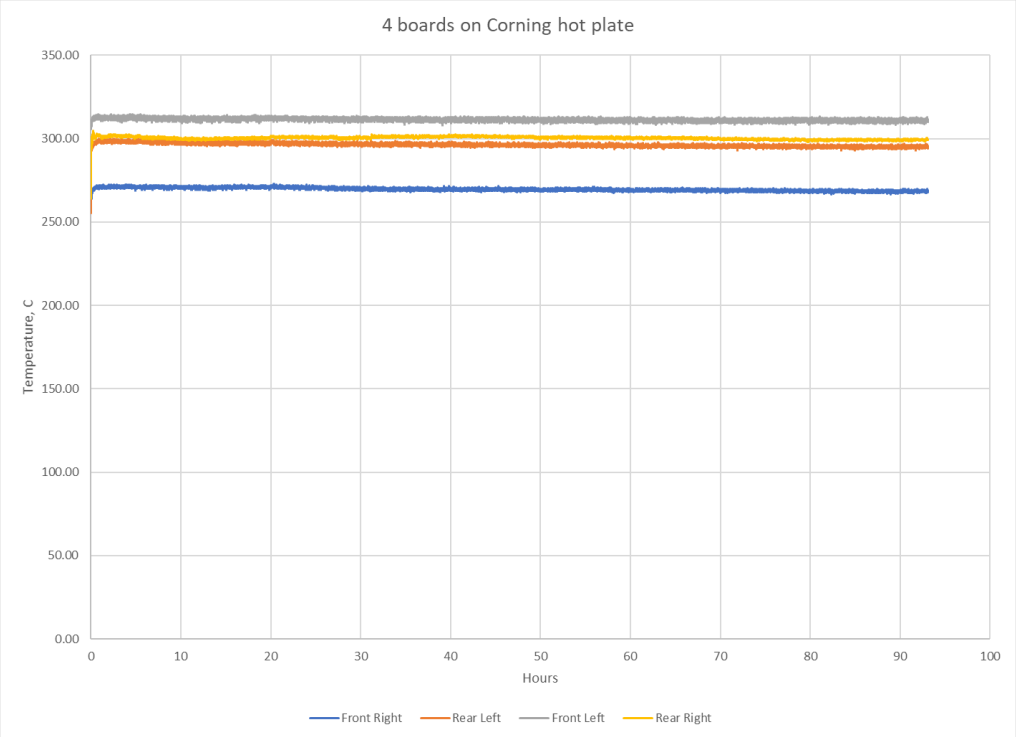


Figure 73 Temperature spread between 4 test samples

To further reduce the temperature spread between the test boards, a heat spreader was implemented which resulted in a reduction in the temperature variation between the four samples. Figure 74 shows that the heat spreader was able to reduce the temperature difference between samples to within approximately 16°C with all four samples maintaining temperatures of 300°C or higher, therefore meeting the long-term testing needs.

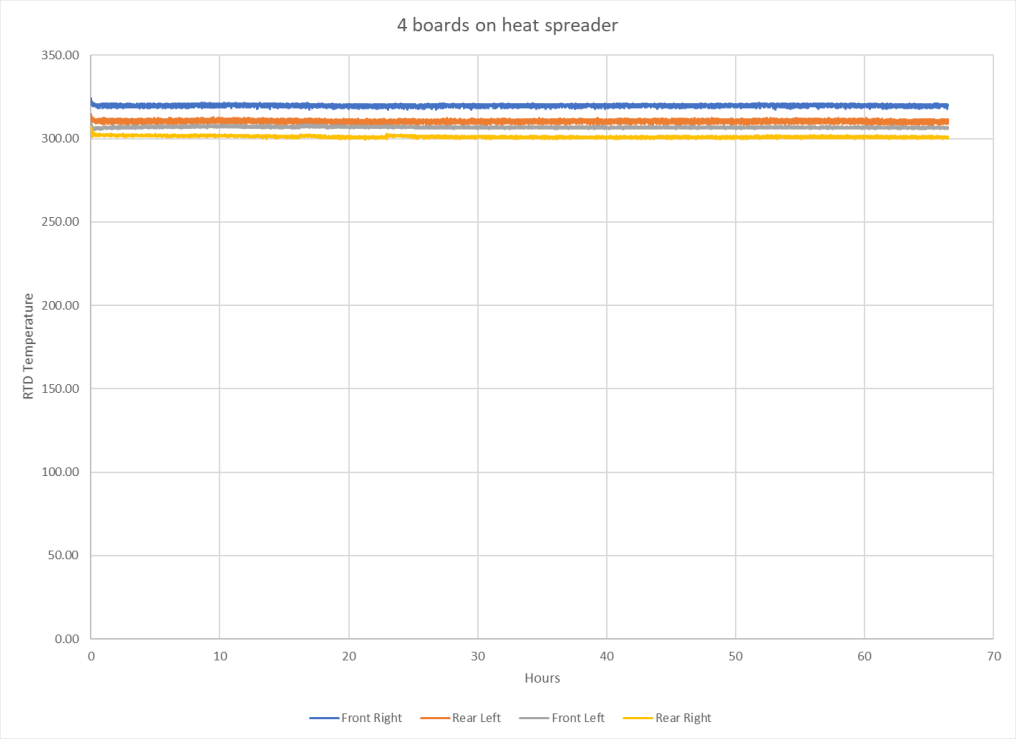


Figure 74 Reduced temperature spread with the addition of a heat spreader

High temperature ceramic test board

The HT test board is a ceramic substrate with high temperature conductor that provides the electrical interconnect between the MRGT, the ASIC and the other supporting passive components. The schematic of the ceramic board is shown in Figure 75.

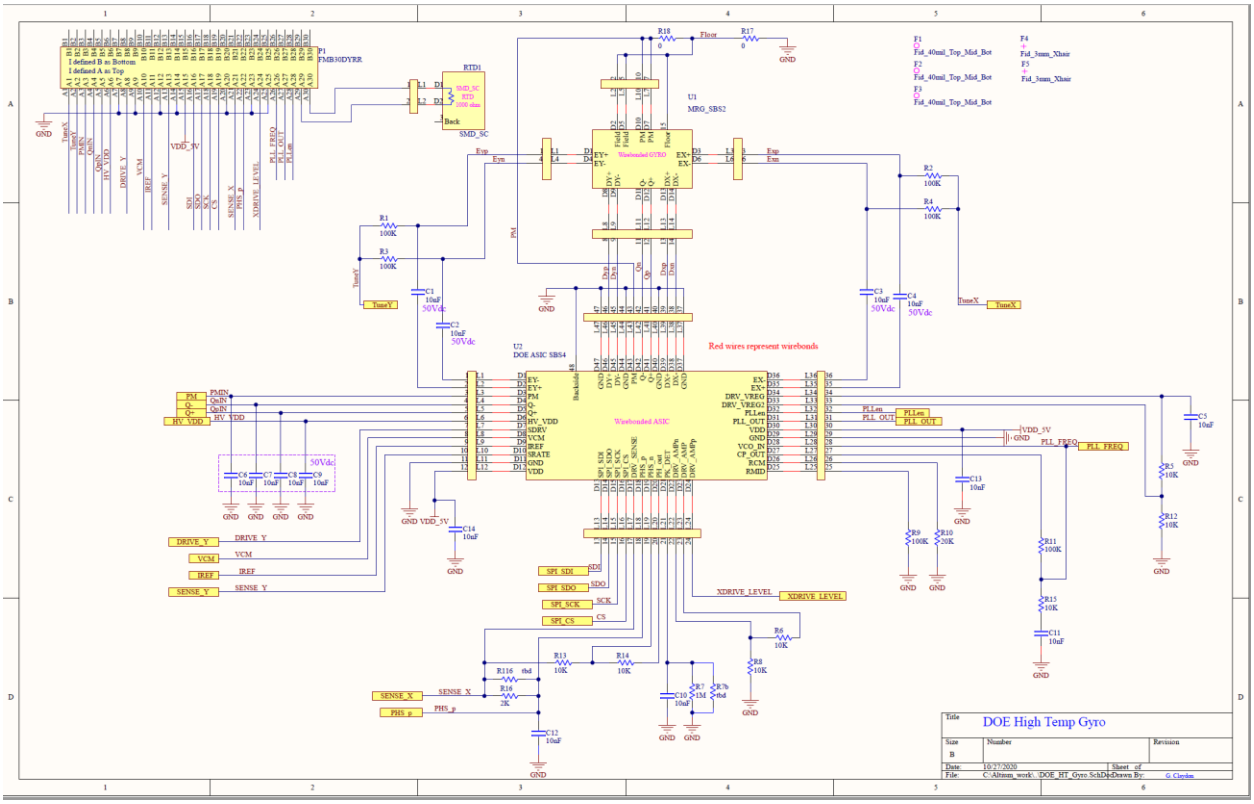


Figure 75 Ceramic board schematic

The schematic was converted into a layout utilizing design constraints imposed by the ceramic fabrication process such as minimum trace width and spacing. Prior to board fabrication, test coupons were fabricated to validate achievable capabilities of the process and materials used.

The board layout required two electrical interconnect layers, therefore a dielectric layer was utilized to achieve isolation between the interconnect layers. The board layout is shown in Figure 76. The first interconnect layer primarily contains the ground plane which provides the electrical reference potential for the MRGT and ASIC. The first layer also contains three electrical interconnects. The majority of the signal routing is accommodated on the second routing layer which also includes the pads for the passive components as well as the backside interconnect for the ASIC. Electrical connection points the ceramic board and the MRGT and ASIC are provided through wirebonds.

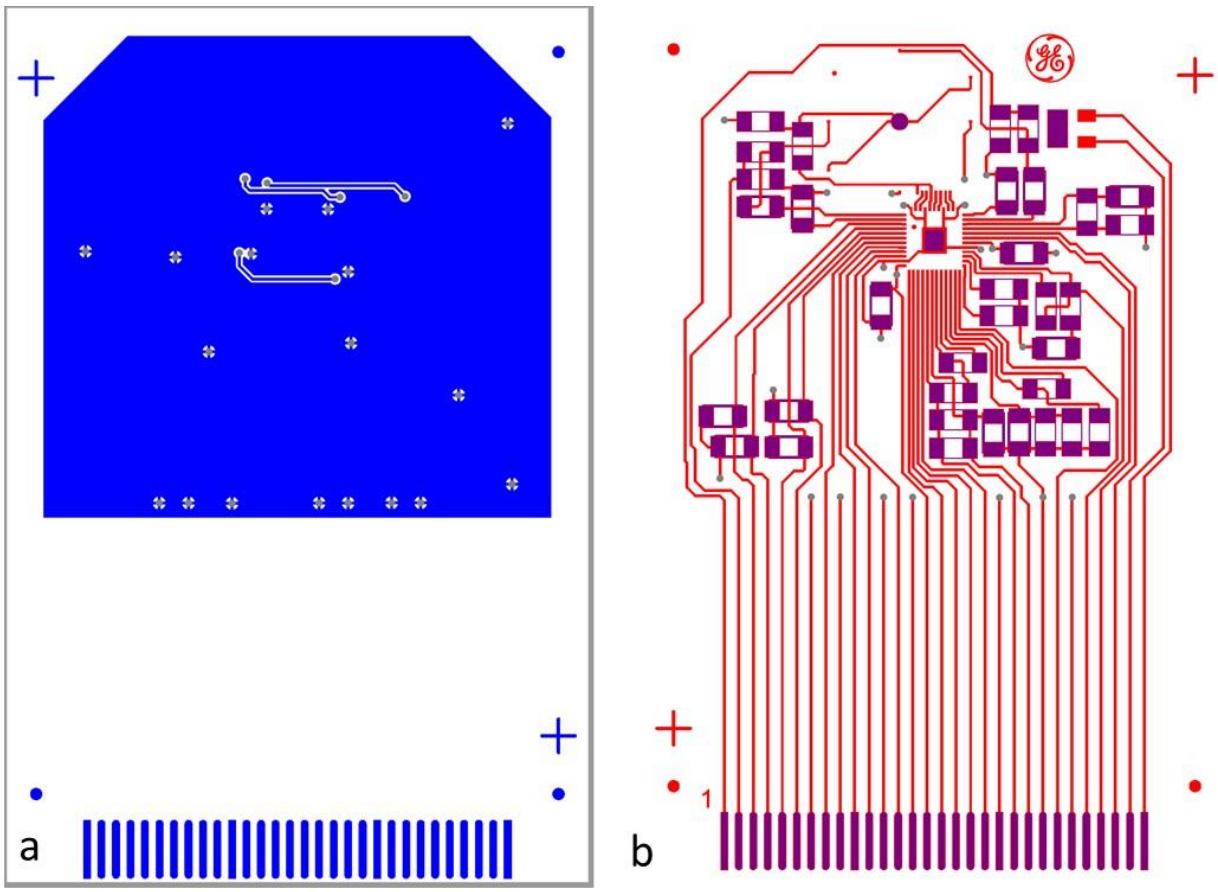


Figure 76 Ceramic board layout: (a) first interconnect layer layout. (b) second interconnect layer layout.

The wirebonding diagram was created to define the wirebond interconnection between the MRGT and the circuit board, the ASIC and the circuit board. The wirebonding diagram is shown in Figure 77. The ASIC and MRGT outlines are added for clarification. The wirebonds are shown connecting from pads on the MRGT and ASIC components to pads on the ceramic substrate to provide the electrical connectivity.

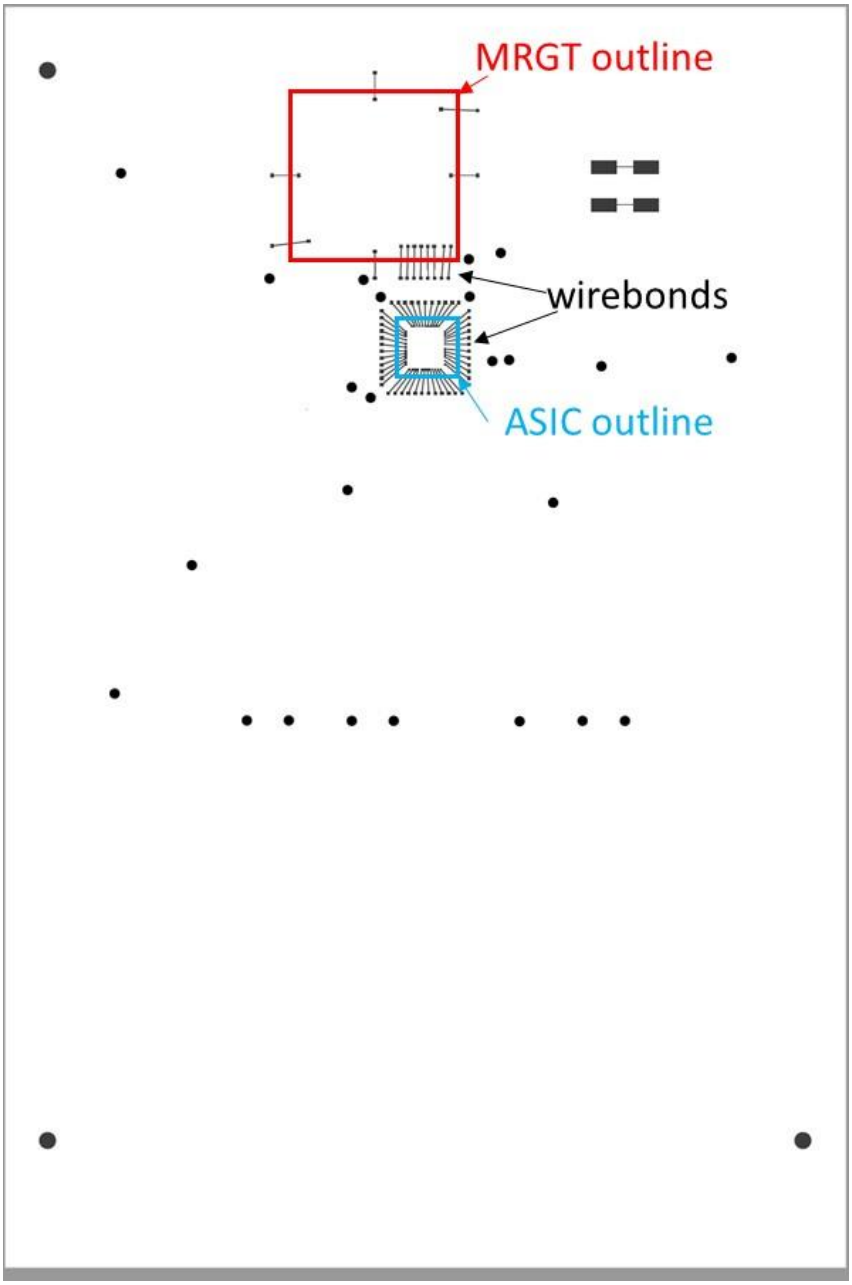


Figure 77 wirebonding diagram

Ceramic board fabrication assembly and test process

The high temperature test board was fabricated out of Aluminum Nitride (AlN) ceramic to enable extended test time at 300°C to support the lifetime testing. A detailed material and process selection was undertaken to achieve the desired reliability. To validate the material choices, several tests were conducted to assess the lifetime potential and identify any material or process weakness. Die attach screening was conducted by

varying the backside metallization stack composition and thickness on the MRGT die and utilizing the high temperature capable AuSn die attach to attach the dies onto a test coupon. The test coupons were metalized with the two variants of the thick film conductor material to be utilized in the fabrication of the electrical interconnect layers of the ceramic board. The coupon shown in Figure 78 was then aged at 300°C. After temperature aging, shear testing was conducted at 300°C to determine the adhesion strength with the various backside metal and thick film conductor materials.

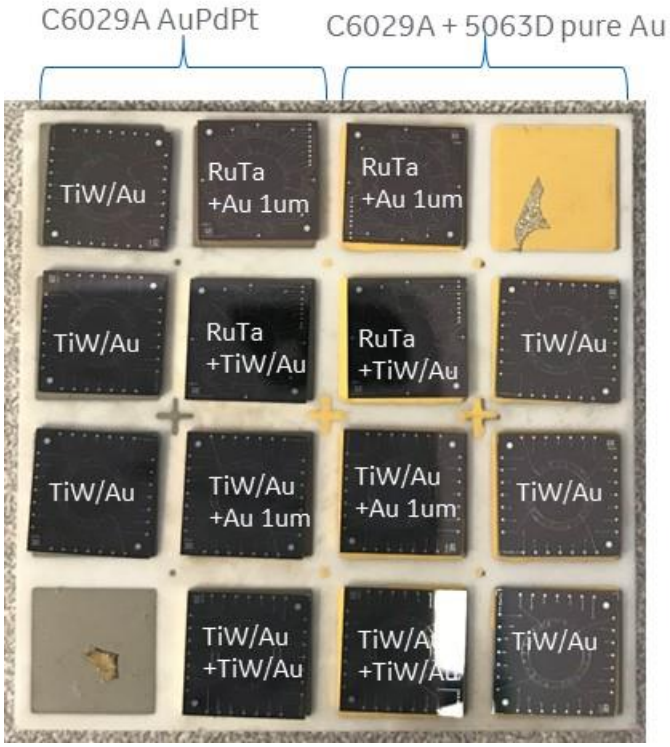


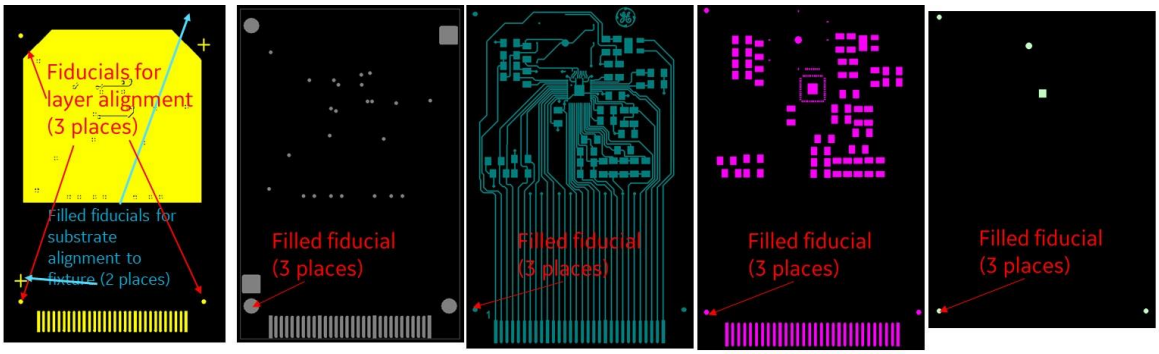
Figure 78 Die attach screening test coupon

Tanaka AuRoFuse Au sintering paste was used with TiW/Ru/Ta/Au backside metal for MRGT and ASIC die attach because its stable die shear strength at 300°C and low Youngs modulus (9.5 GPa vs 60 GPa for AuSn) to reduce the MRGT thermal strain.

Based on the tests conducted on the materials and processes, design rules and material choices were defined. An example of the design rules is that for the metal line and spacing required for each of the printed conductive material choices. A small line and space feature size is desired to accommodate routing densities, but a line width that is too narrow increases the probability of open circuits occurring, while line spacing that is too narrow increases the probability of adjacent lines shorting to each other. The

minimum line and space width for the C5730 gold thick film material utilized as the printed conductive material for the first metal layer was 6 mils, while the C6029A material utilized in the second interconnect layer (layer 3) was 8 mils.

The layer structure, material used and the alignment features utilized to align the various layers in the board are shown in Figure 79.



Layer1Groundandsignal: Print all yellow areas with C5730 Au conductor

Layer2Dielectric (negative) Print all non-grey areas inside grey rectangle outline with IP9242 dielectric. 2 layers printed and fired.

Layer3Signal: Print all cyan areas with C5730A Au conductor.

Layer4 WB and Solder: Print all purple areas with C6029A AuPdPt conductor.

Layer5 Pure Au pad: Print all green areas with DuPont 5063A Au.

Figure 79 Ceramic board layers and materials

Once the material selection was finalized, a substrate fabrication process was defined and the boards were built and tested per that process steps as shown in Figure 80.

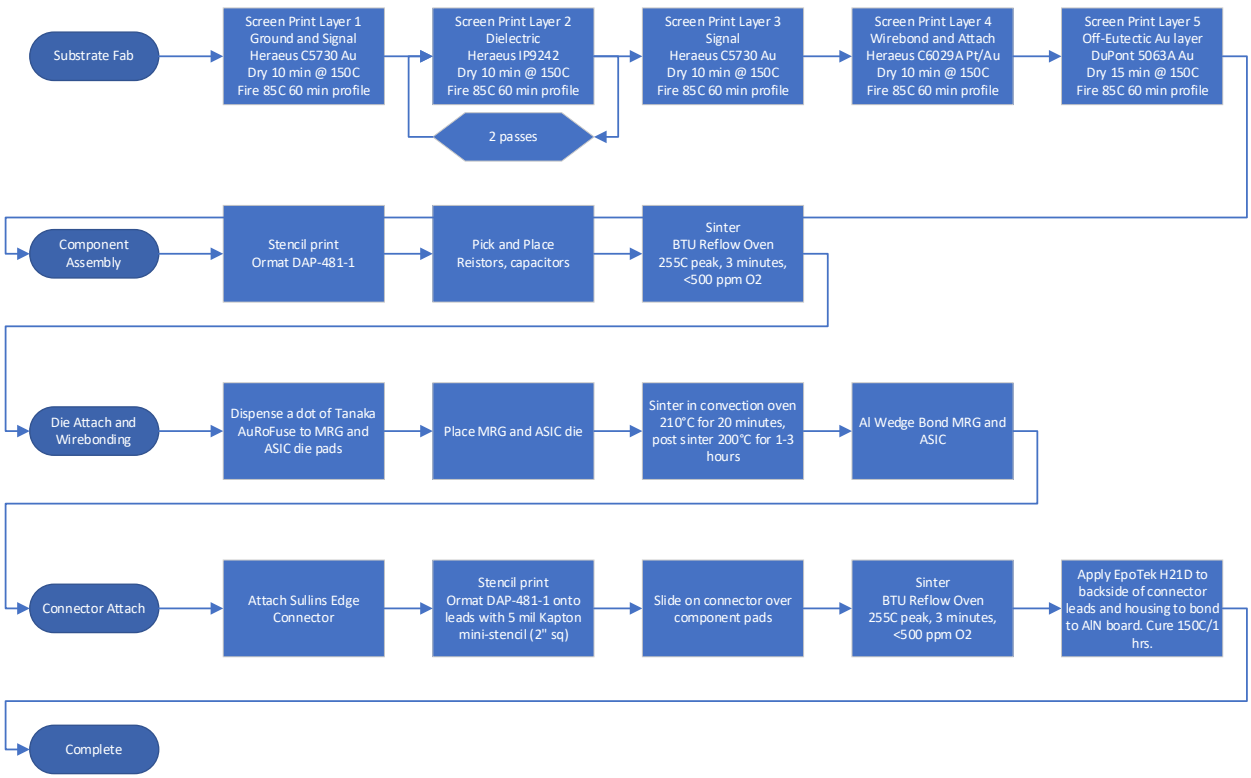


Figure 80 Ceramic board fabrication and test process flow

After board fabrication and assembly was completed, traces that are routed under components were inspected using Xray to ensure that no shorting has occurred. The Xray image shown in Figure 81 shows the two layers of interconnect metal and traces that have been routed under the passive components (resistors and capacitors) on the left portion of the image. Sufficient clearance between the traces and the component attach pads can be observed, indicating that no shorting has occurred.

Once the fabrication and assembly was complete, the boards were ready for functional testing.

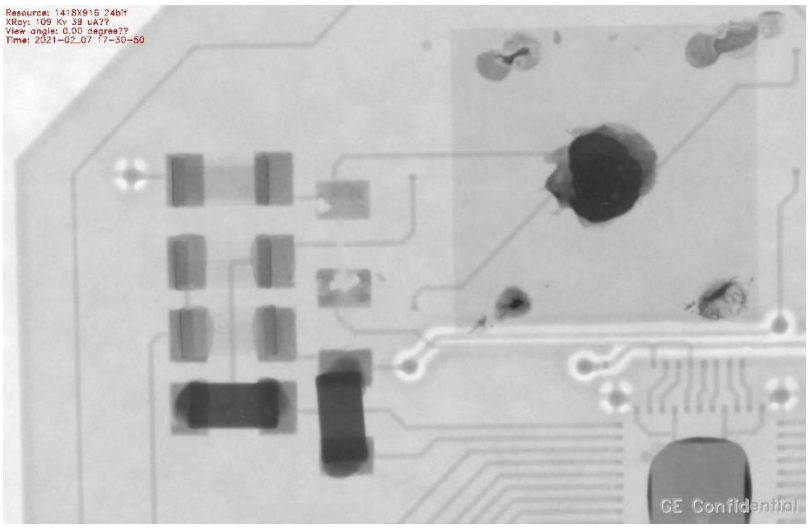


Figure 81 Xray inspection of completed high temperature boards

A picture of the completed high temperature ceramic test board is shown in Figure 82. The board includes the MRGT, ASIC and supporting passive components, and attaches to the data collection interface board through the board edge connector shown on the left-hand side of the board.

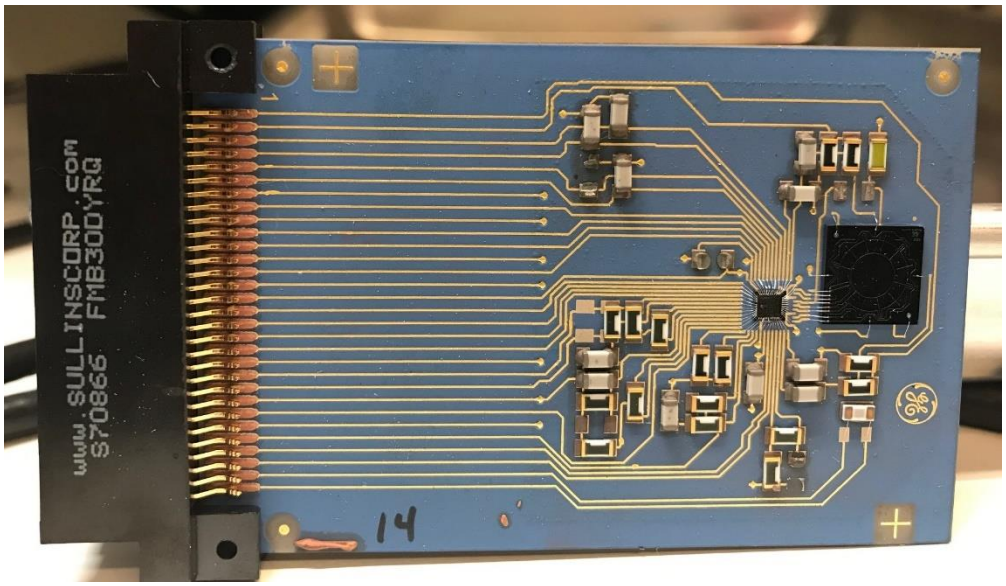


Figure 82 Assembled 300°C capable ceramic board

ASIC data collection interface board

The ASIC data collection interface board was designed to generate the power supply and control signals required to control and interrogate the combined MRGT and ASIC

integrated gyroscope system and collect and digitize the outputs for conveyance to the data collection PC. The interface board includes 40V DAC that provides the MRG with required high voltage electrostatic biasing, signal digital sampler for HT ASIC signal data collection, and a microcontroller with USB interface to data collection PC as shown in Figure 83.

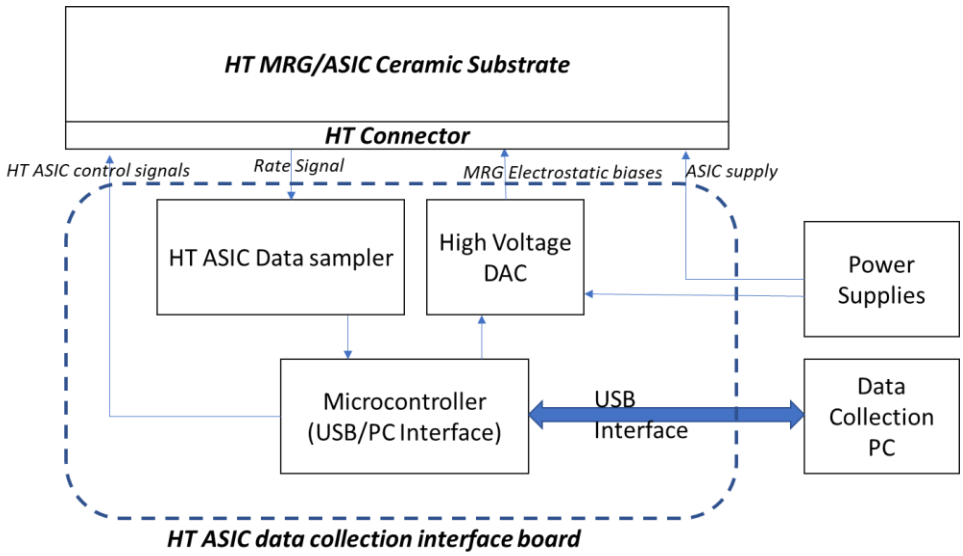


Figure 83 High Temperature ASIC data collection interface board functional block diagram

The data collection interface board schematic is shown in Figure 84.

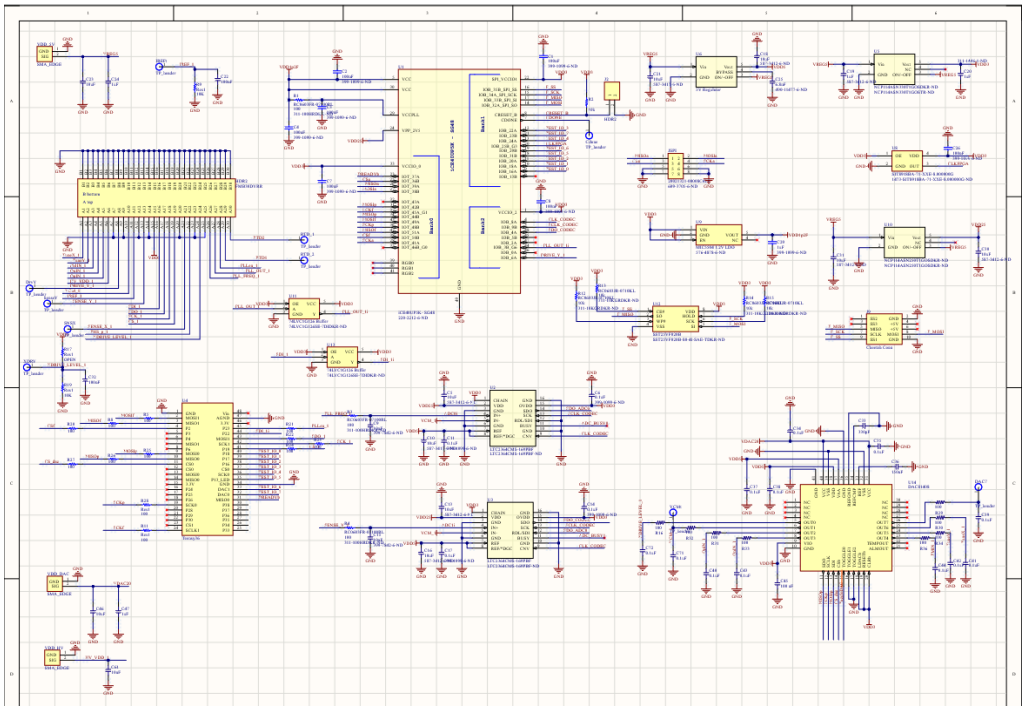


Figure 84: High Temperature ASIC data collection interface board schematic

The board layout is shown in Figure 85.

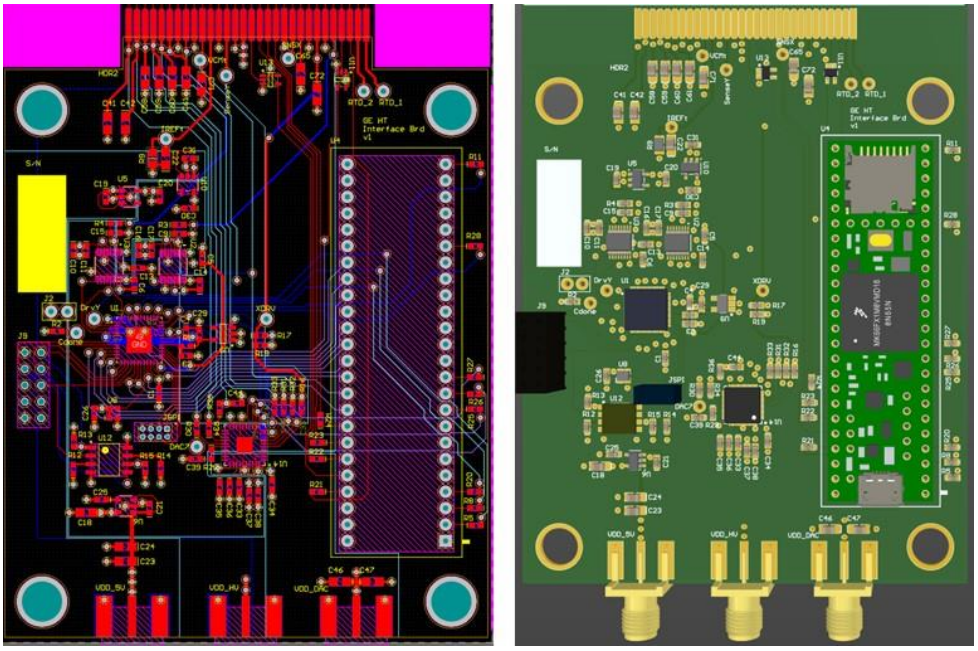


Figure 85 High Temperature ASIC data collection interface board layout (left) & populated board (right)

Heating and rotation capability

To support testing at 300°C, a hot plate is utilized to supply heat to the ceramic board. Due to thermal losses in the test setup, the ceramic substrate does not reach the hot plate setpoint temperature. A temperature sensor was utilized on the ceramic board, and the hotplate setpoint was adjusted until the ceramic board achieved the desired temperature.. The hotplate was placed on a rotation stage to facilitate testing the integrated MRGT+ASIC capability to detect rotation and measure key gyroscope parameters such as scale factor.

Support instrumentation

The complete test setup is shown in Figure 86. The hotplate on the rotation stage is shown on the bottom right of the image. Power supplies (top center of image) provide power to the MRGT/ASIC test board and the data collection interface board. A resistance measurement system, shown in the bottom left of the image, monitors the resistance of the onboard Resistance Temperature Detectors (RTD) to validate the test temperature.

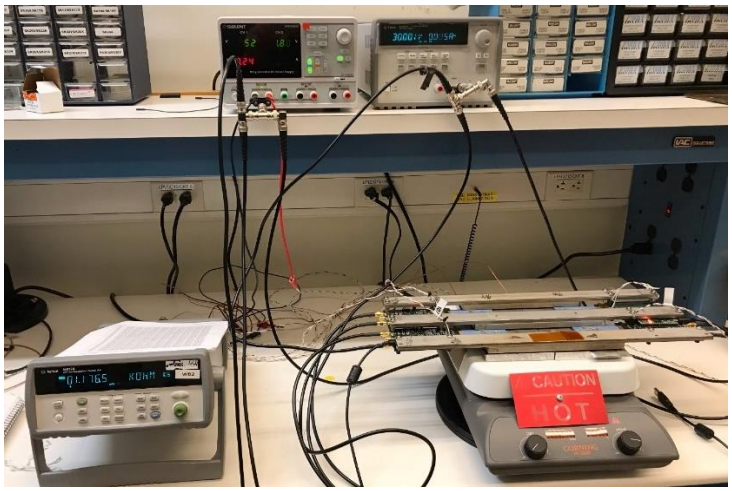


Figure 86 Integrated MRGT and ASIC test setup

Integrated system functional testing

Test description

The high temperature ASIC data collection interface board provides the following functionality –

- Connector for HT-ASIC circuit voltage 5V, and 30V bias voltage

- High voltage DAC biasing for electrostatic tuning (Proof Mass (PM), Quadrature +/- (Q+/-), and frequency tune (Tune X/Y))
- Necessary setup of the HT ASIC SPI register using onboard ARM processor with SPI interface
- Rate gyroscope data capture ADC
- USB interface to PC for data logging

The test setup consists of the 5V voltage supply, 30V bias voltage supply, temperature data logger that monitors the 300°C RTD temperature sensor on the MRG ceramic board, and the 3 devices under test (MRG Ceramic board + HT ASIC data collection interface board).

The testing was done on 3 DUTs: IB3-MRG1, IB2-MRG11, IB1-MRG12. The testing was done w/ drive-sense gain channel in a low gain configuration (CA setting: 16pF, IA setting: 1 V/V) to avoid saturation of the channel, and the rate-sense gain channel in a high gain configuration (CA setting: 1pF, IA setting: 4 V/V) to maximize scale factor and noise performance. These gain settings were programmed into the HT-ASIC using the following SPI 20-bit configuration (0xBEBB8) as shown in Table 16:

Table 16: ASIC gain settings

Bit	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	bCA1				bIA1						bCA0				bIA0					
	3	2	1	0	5	4	3	2	1	0	3	2	1	0	5	4	3	2	1	0
	1	0	1	1	1	1	1	0	1	0	1	1	1	0	1	1	1	0	0	0

The tests consisted of testing the following parameters:

MRG center frequency: Nominally 30KHz

MRG quality factor: >7000 at 25°C, ~2000-3000 at 300°C

MRG mechanical scale factor: 0.6~0.8 mV/degree-per-second at 25°C, 0.2~0.3 mV/degree-per-second at 300°C

An optimal value for the proof mass was found to be ~30V for the MRG operation enabled stable tuning of the quadrature and frequency trim, while providing maximum mechanical scale factor at 300°C operation. The drive level for the MRG was set at 5Vpp, which provides ~1um oscillation displacement. The sense channels were operated at a common mode voltage of 2.5V, which was ½ the HT-ASIC circuit 5V voltage to provide the largest operate rate range for the MRG.

Functional testing results

At 300°C each DUT was tested with a transfer across frequency around 30KHz with a starting electrostatic tuning at Proof mass VPM=30V, quadrature trim Q+/-=VPM=30V, and frequency tune TuneX/Y=0V. Figure 87, Figure 88, and Figure 89 show the results for the 3 DUTs (IB3-MRG1, IB2-MRG11, IB1-MRG12). The center frequency and quality factor were determined from these tests.

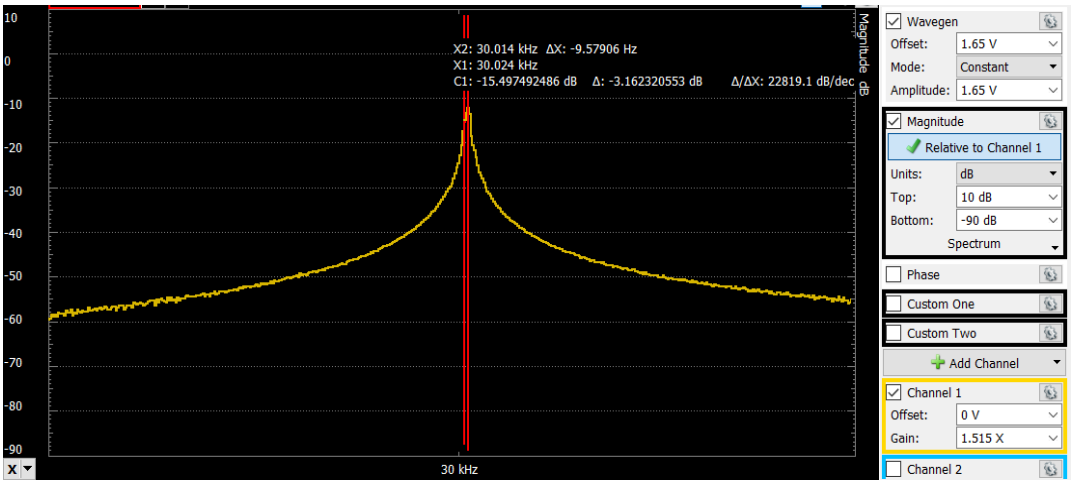


Figure 87 Interface Board 3-MRG1 transfer function

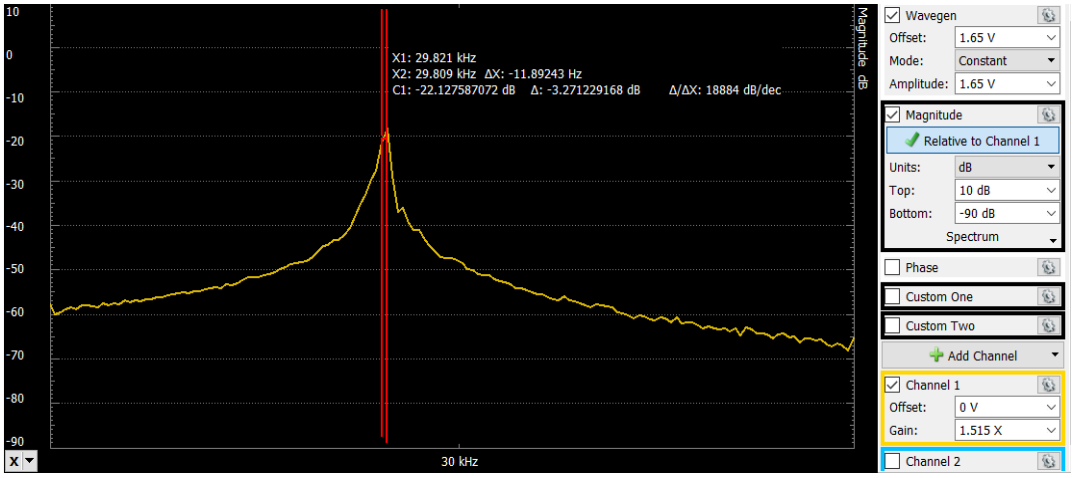


Figure 88 Interface Board 2-MRG11 transfer function

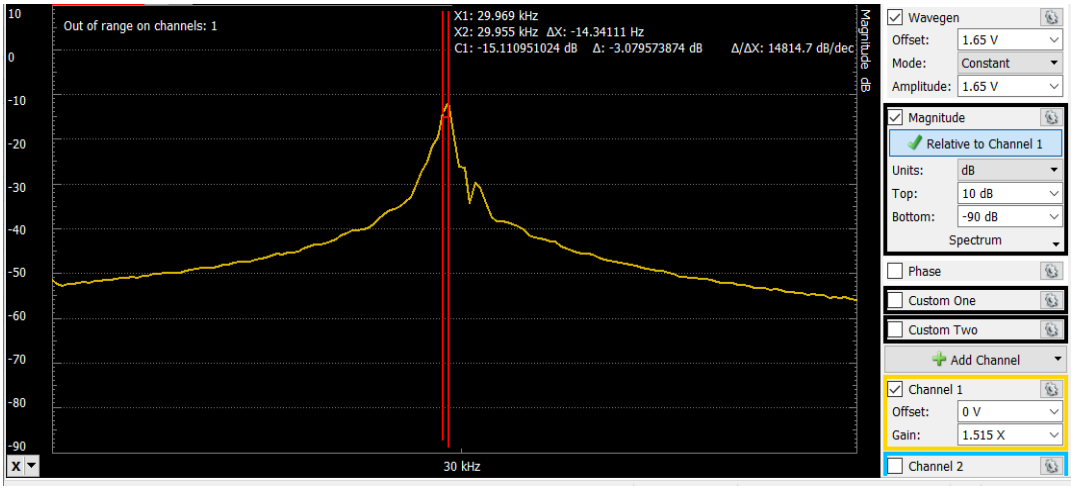


Figure 89 Interface Board 1-MRG12 transfer function

The quadrature trim voltages were then systematically adjusted to minimize the cross axis quadrature feedthrough into the sense-rate channel. In this case all 3 DUTs required adjustment of the Q+ trim. Minimizing the quadrature feedthrough improves rate noise performance and provides the maximum headroom for the rate range. The mechanical scale factor tests were completed by carefully manually turning the 300°C DUTs from 0˚ → 45˚ → 0˚ using the turn table under the heater platform as shown in

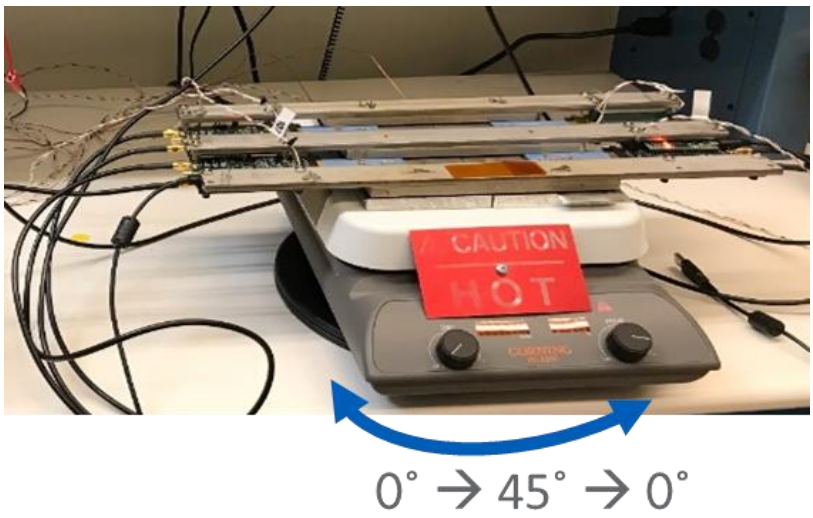


Figure 90.

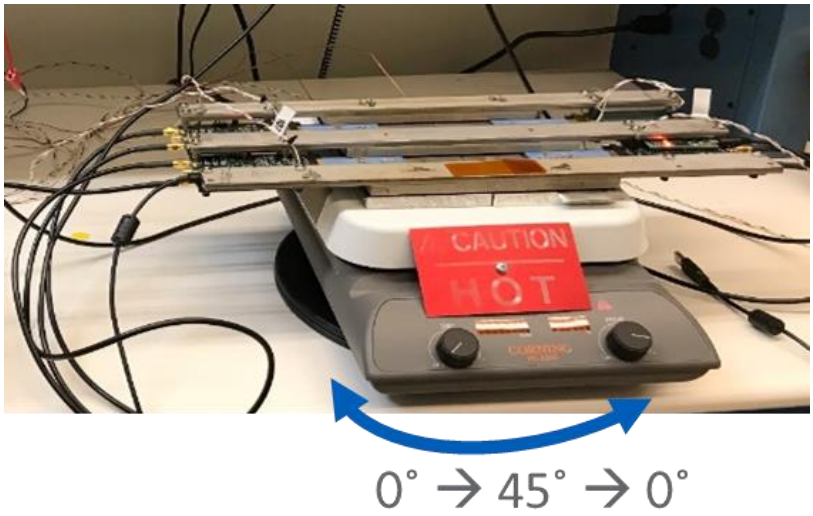


Figure 90 Mechanical scale factor test of DUTs

In order to maximize the scale factor the frequency trim voltage (TuneY) was then systematically adjusted such that the mechanical scale factor was maximized, indicating the MRG was operating in its highest gain mode matched condition. A summary of the test results and optimal operating points for the DUTs at ambient room temperature and 300°C are shown in Table 17 and Table 18.

Table 17: Summary of optimal operating points and test results for the DUTs operating at ambient

Int Brd	MRG Brd	SF (mV/dps)	Q factor	Fcenter (KHz)	XDrv (Vpp)	Vcm (V)	PM (V)	Qp (V)	TuneY (V)
3	1	0.6	7260	30.3	5	2.5	30	11	4.6
2	11	0.6	11600	30.097	5	2.5	30	9	5.1
1	12	0.8	8700	29.98	5	2.5	30	18	6.3

Table 18: Summary of optimal operating points and test results for the DUTs operating at 300°C

Int Brd	MRG Brd	SF (mV/dps)	Q factor	Fcenter (KHz)	XDrv (Vpp)	Vcm (V)	PM (V)	Q+ (V)	TuneY (V)
3	1	0.3	3134	30.24	5	2.5	30	12	7.7
2	11	0.3	2527	28.82	5	2.5	30	10	6.6
1	12	0.2	2089	29.96	5	2.5	30	19	10.2

The static rate noise performance of the DUTs at 300°C was then tested to determine Angular Random Walk (ARW) performance. Figure 91, Figure 92, and Figure 93 show the representative test results of the Allan Deviation for the 3 DUTs.

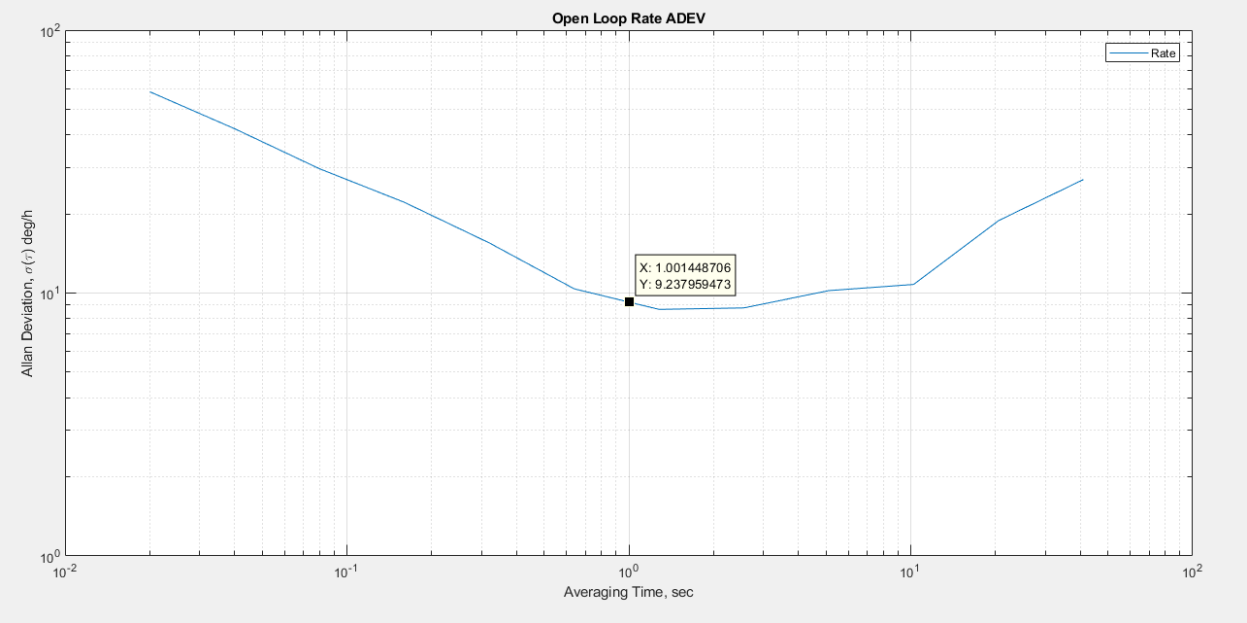


Figure 91 IB3-MRG1 Allan Deviation Test Result at 300°C

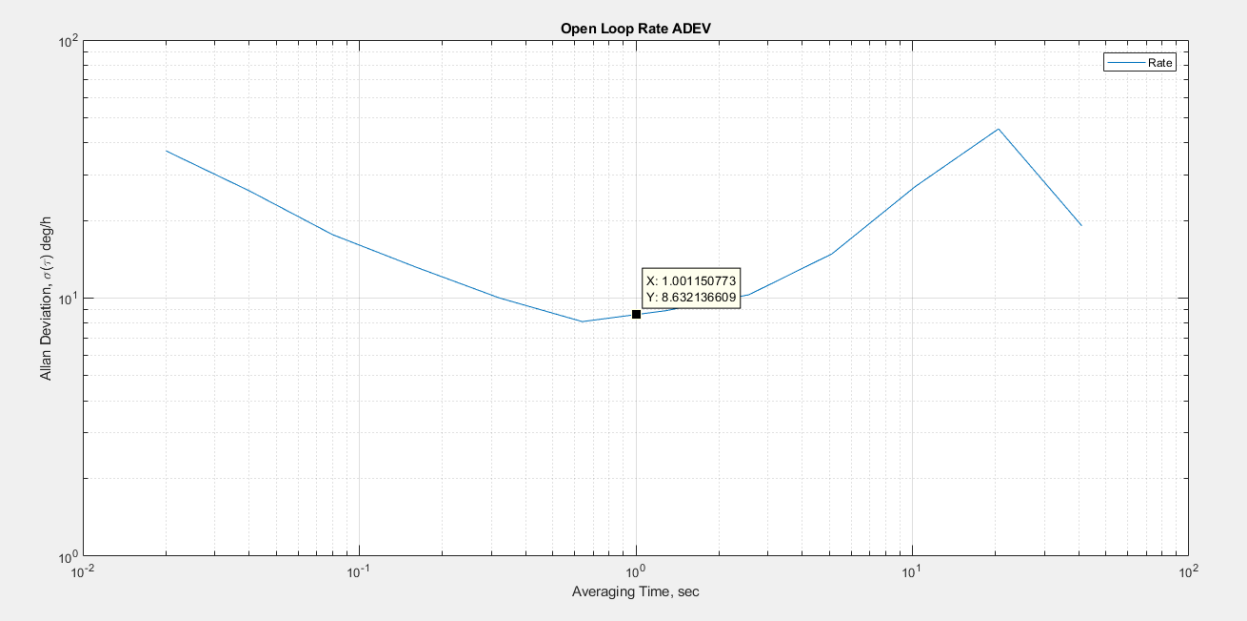


Figure 92 IB2-MRG11 Allan Deviation Test Result at 300°C

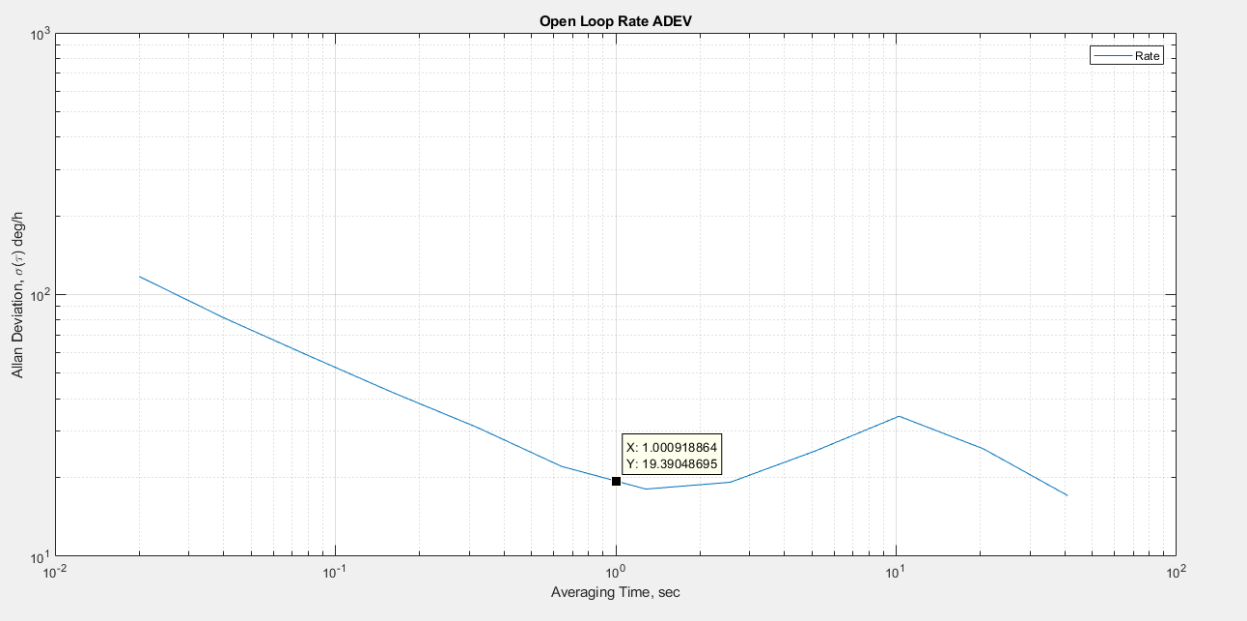


Figure 93 IB1-MRG12 Allan Deviation Test Result at 300°C

Test result discussion, performance assessment, gaps

The MRG-ASIC was fully functional from ambient to the intended 300°C operating temperature. From the Allan Deviation results the longer-term bias stability performance of the MRG-ASIC at 300°C is dominated by the thermal stability of the environment. If we extrapolate the bias curves from 1s integration to ~20-30s integration, then we expect we can achieve sub-1dph performance necessary to implement earth-rate gyrocompassing. We have developed thermal compensation scheme for the MRG that have been demonstrated at lower temperature ranges <125°C that can be applied to achieve sub-1dph performance at 300°C.

Long-term testing

The lifetime testing is intended to validate and demonstrate the lifetime capability of the integrated MRGT + ASIC + associated packaging at 300°C. The long-term testing comprises measuring key gyroscope system parameters at multiple points withing the 1,000-hour testing period. The parameters measured are the MRGT's resonance frequency and quality factor and the gyroscope system scale factor. Other parameters were also monitored to further validate the health of the overall system such as the current consumption and bias conditions.

The quality factor and resonance frequencies are direct indicators of the health of the MRGT. Any failure of the MRGT or loss of vacuum within the device can be detected

though these parameters. The measurement of the scale factor allows for testing of the full functionality of the MRGT and the ASIC. A successful scale factor measurement validates the following key functional elements:

1) The ASIC drive channel is driving the MRGT into resonance at the correct frequency and with sufficient amplitude
2) The MRGT's drive and sense modes are functional
3) The MRGT is responsive to rotation rate
4) The ASIC sense channel is functional and is able to amplify the sensed signal from the MRGT
5) The overall integration and packaging approach is functioning as intended.

Furthermore, while obtaining a response to rotation rate is indicative of a functioning system, the stability of the various test parameters provides an indication of whether any performance degradation is occurring over time. At the beginning of the test, two data sets were collected, one at room temperature and one at 300°C. The initial 300°C test point is utilized as baseline for comparison at subsequent intervals.

MRGT component reliability testing

Prior to the system level long-term testing, evaluation of the MRGT device capability to maintain performance after prolonged exposures to 300°C was conducted. The testing enables for a simple early indication of device weakness and is more readily extendible to long duration. The test can provide an indication of the long-term reliability of the packaging process and its ability to maintain vacuum, detect any device characteristics shifts caused by outgassing within the cavity or mechanical strain due to temperature. The testing comprised characterizing the noise and scale factor of an MRGT at room temperature at the beginning of the testing period, and then placing the MRGT in a 300°C. At approximately 1-week intervals, the device was pulled out of the oven, cooled to room temperature, and remeasured. At later portions of the testing, the testing period was extended to reduce test overhead. Test data was collected for approximately 2400 hours with no failures or noticeable shifts in MRGT characteristics. The MRGT scale factor is shown in Figure 94.

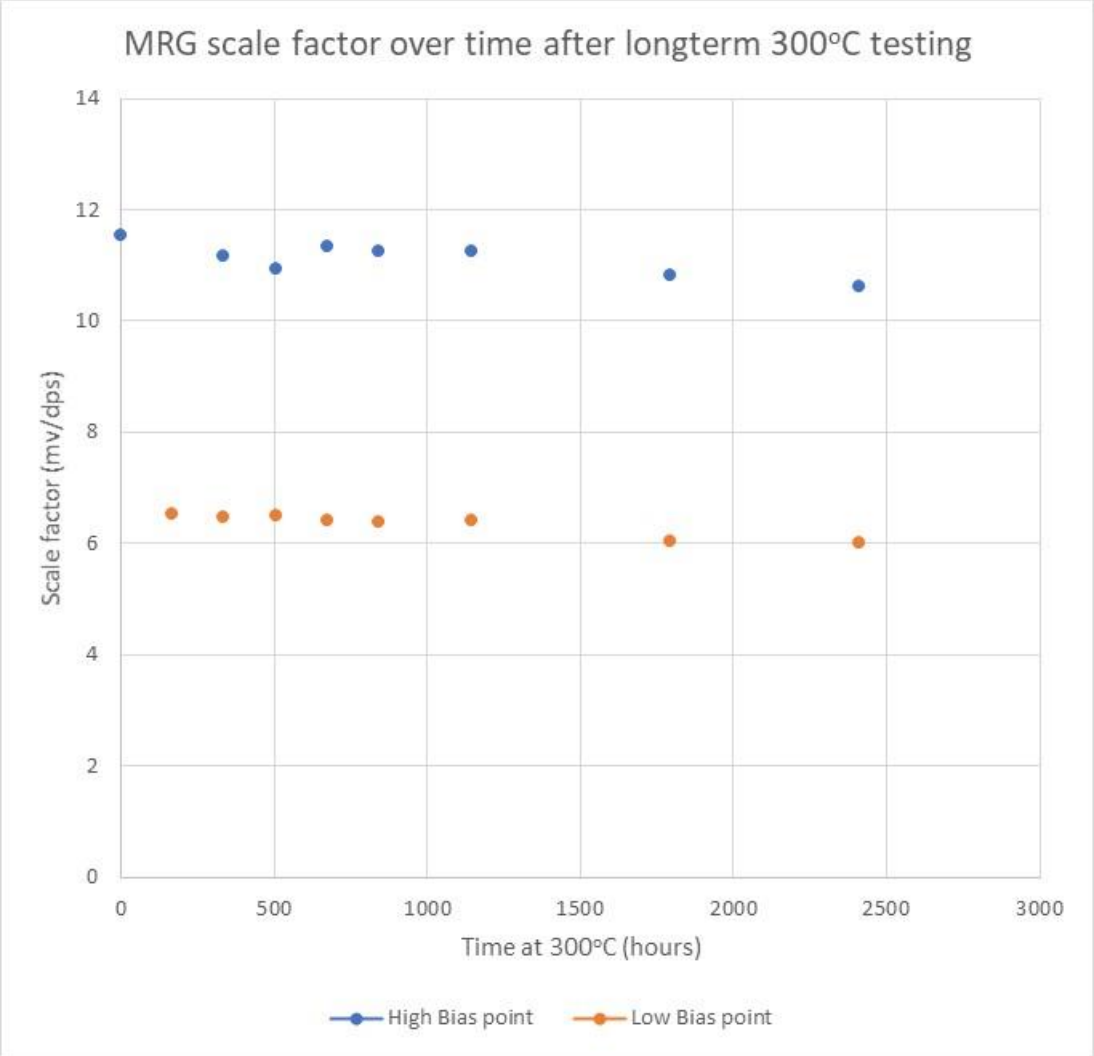


Figure 94 MRGT scale factor after 300°C high temperature storage testing

Table 19 summarizes the MRGT testing after high temperature storage testing. The MRGT device quality factor, scale factor and noise levels remain largely unchanged after 2,412 hours at 300°C. The test results validate the device design, and packaging materials choices to accommodate long-term survivability at 300°C and provides additional validation that the wafer bonding process can maintain vacuum within the device cavity over extended periods of time at temperature.

Table 19 MRGT measurement summary after 300°C storage testing

Interval	Time at 300C (hours)	Bias setting (sensitivity)	MRGT drive quality factor	MRGT sense quality factor	Adev @ 1 second (degrees.hour)	SF [mV/degree/sec]
0	0.0	High	15,954	15,899	0.75	11.54
1	168.0	Low	15,890	15,825	0.88	6.54
2	335.5	High	15,878	15,819	1.31	11.17
		Low	15,864	15,807	0.91	6.47
3	504.3	High	15,782	15,735	0.95	10.93
		Low	15,723	15,651	0.92	6.50
4	674.0	High	15,815	15,779	1.24	11.35
		val	15,755	15,680	0.92	6.41
5	843.0	High	15,709	15,600	1.10	11.25
		Low	16,345	16,279	1.03	6.37
6	1,147.0	High	15,799	15,716	0.99	11.25
		Low	15,738	15,655	1.17	6.42
7		High	15,344	15,291	0.92	10.83
	1,791.5	Low	15,282	15,221	1.88	6.05
8		High	14,095	14,045	0.89	10.62
	2,412.5	Low	14,008	13,967	0.89	6.02

The testing conducted on the MRGT validated the device capability to survive high temperature operation at extended periods of time. Prior work conducted at GE has validated the electronics Silicon-On-Insulator process capability to accommodate 10,000 hours+ of operation at temperatures of 350°C. The combination of MRGT testing and SOI electronics testing provided the baseline and risk reduction for the subsequent long-term reliability testing of the integrated gyroscope system comprising the MRGT, high temperature ASIC, packaging and supporting passive components.

Baseline data

The MRGT resonance frequency, quality factor and the system's scale factor were measured at the beginning of the test period at both room temperature and 300°C. The nominal room temperature and 300°C data is shown below:

MRGT center frequency: Nominally 30KHz

MRGT quality factor: >7000 at 25°C,
~2000-3000 at 300°C

MRGT mechanical scale factor: 0.6~0.8 mV/degree-per-second at 25°C,
0.2~0.3 mV/degree-per-second at 300°C

Interval testing

The long-term testing was conducted as interval testing where the test articles remained powered and at temperature throughout the test period, but at several intervals within the test time, the test setup was interrogated and subjected to rotation. At each of the intervals, the key parameters were measured and a test datapoint was collected.

Test results, stability over time

The following interval data was collected through the duration of the testing. At the first interval the baseline 300°C data (shown in Table 20) was collected and utilized as a comparison point for the subsequent tests. Since the three test articles were started at different points in time, the accumulated number of hours per board is different at the various interval points. Additionally, as new boards were added to the testing, the temperature was lowered for a duration of time to enable the integration of the new test articles. Any time that the heat source was brought to below 300°C was not counted towards the test time, thus providing for a worst-case lifetime assessment.

Table 21 summarizes the test data at the second test interval in which the three test boards had achieved 329, 685 and 780 operation test hours at 300°C with no detectable shift from the baseline performance. Table 22 shows the data from the third test interval at 521, 877 and 972 hours of operation with no deterioration.

Table 23 is data collected at the fourth test interval in which the boards has accumulated 1529, 1885 and 1980 hours respectively, at which point, it was observed that all three boards have ceased responding. It is unknown when in the time period between the third and the fourth interval the failure has occurred, therefore the last known good datapoint was taken as the test time achieved thus far. Since the last known good dataset was collected at the third test interval when the boards had achieved 521, 877 and 972 hours, this test point falls short of the goal of achieving 1,000 hours of life at 300°C.

Table 20 First interval (baseline) 300°C data at start of test for the three test articles

START TEST						
Test Date	Interface Board #	MRG/ASIC Substrate #	Test Temperature (C)	MRG Frequency (KHz)	Quality Factor	Scale Factor (mV/dps)
1/22/2021	1	12	300	29.9	2089	0.24
1/26/2021	2	11	300	28.8	2527	0.32
2/9/2021	3	1	300	30.3	3134	0.31

Table 21 Second interval test results at 300°C for the three test articles

Test time = 329, 685 and 780 hours for the three test boards						
Test Date	Interface Board #	MRG/ASIC Substrate #	Test Temperature (C)	MRG Frequency (KHz)	Quality Factor	Scale Factor (mV/dps)
2/24/2021	1	12	300	29.9	2034	0.28
2/24/2021	2	11	300	28.8	2612	0.31
2/24/2021	3	1	300	30.3	3024	0.34

Table 22 Third interval test results at 300°C for the three test articles

Test time = 521, 877 and 972 hours for the three test boards						
Test Date	Interface Board #	MRG/ASIC Substrate #	Test Temperature (C)	MRG Frequency (KHz)	Quality Factor	Scale Factor (mV/dps)
3/4/2021	1	12	300	29.9	2057	0.22
3/4/2021	2	11	300	28.8	2557	0.29
3/4/2021	3	1	300	30.3	3107	0.31

Table 23 Fourth interval test results at 300°C for the three test articles

Test time = 1529, 1885 and 1980 hours for the three test boards						
Test Date	Interface Board #	MRG/ASIC Substrate #	Test Temperature (C)	MRG Frequency (KHz)	Quality Factor	Scale Factor (mV/dps)
4/15/2021	1	12	300	-	-	-
4/15/2021	2	11	300	-	-	-
4/15/2021	3	1	300	-	-	-

Failure analysis

Investigation of the root cause of failure was kicked off. The integrated MRG and ASIC test boards contain several test points that can be probed to assess the electrical signals at various points along the signal path. Initial testing indicated that the ASIC drivers were not producing drive signal to excite the MRG. An area of investigation around a potential root cause was identified as the possible lifetime limitations of the high voltage capacitors used within that portion of the signal path. Failures in these capacitors can cause excess current to damage the drivers in the ASIC. And since no drive signal was measured, this was identified as a potential failure for further investigation.

Upon further inspection of the full test system, it was determined that the low temperature data collection interface test board used to drive the test had experienced a malfunction. The digital to analog converter (DAC) components on all three low temperature test boards were found to have malfunctioned. A possible root cause is a power surge during the test period. The DACs were replaced, and the testing resumed to determine the functional state of the test articles. It was determined that the ASIC driver outputs were still functional with no damage through the test duration achieved

thus far. Further testing indicated that the MRGT was still functional. In the process of testing the high temperature board, it was determined that the capacitor attach has begun losing adhesion to the test board, and that a reattach is advisable prior to retesting. The capacitor reattach was accomplished using a conductive adhesive

The capacitor utilized for the testing were specified to have gold termination to support the long-life testing. Gold terminated capacitors as well as Gold-Platinum terminated resistors have both been the subject of extensive reliability testing at GE. Due to a supplier issue, the capacitors that were sourced has tin termination instead. The tin terminated capacitor had the risk of poor adhesion which was partially mitigated through the use of a thicker layer of the sintering paste to improve the attach reliability. The thicker layer increased the risk for shorting to adjacent traces but was mitigated by the use of Xray inspection and electrical resistance measurement, as described in the Ceramic board fabrication assembly and test process section of this report, to ensure that no shorting has occurred during the attach process. After 1000 hours+ of testing at 300°C, poor adhesion was observed between the capacitors and the high temperature ceramic test board.

Post repair testing success and results

Once the low temperature DACs were replaced and the capacitors were reinforced with additional conductive adhesive, the testing indicated that all the high temperature components remained functional through the duration of the testing. The ASIC, MRGT, resistors and capacitors did not exhibit any functional or performance damage. The ceramic substrate, interconnect and dielectric layers also remained functional through the test time. The wirebonds, die attach, and resistor attach also remained robust and continued to function as anticipated. While the capacitor attach has shown loss of adhesion, this was consistent with the limitation of the tin termination on these components and its poor adhesion at extended time at temperature, but the capacitor components themselves continued to function as anticipated.

A gyroscope transfer function was collected as seen in Figure 95. The data showed the full system was still functional and maintained the same nominal operating parameters of the baseline system. This data was collected on test board number 3 which has achieved 1,529 hours of test time at 300°C, and therefore exceeded the target test time of 1,000 hours by more than 50%.

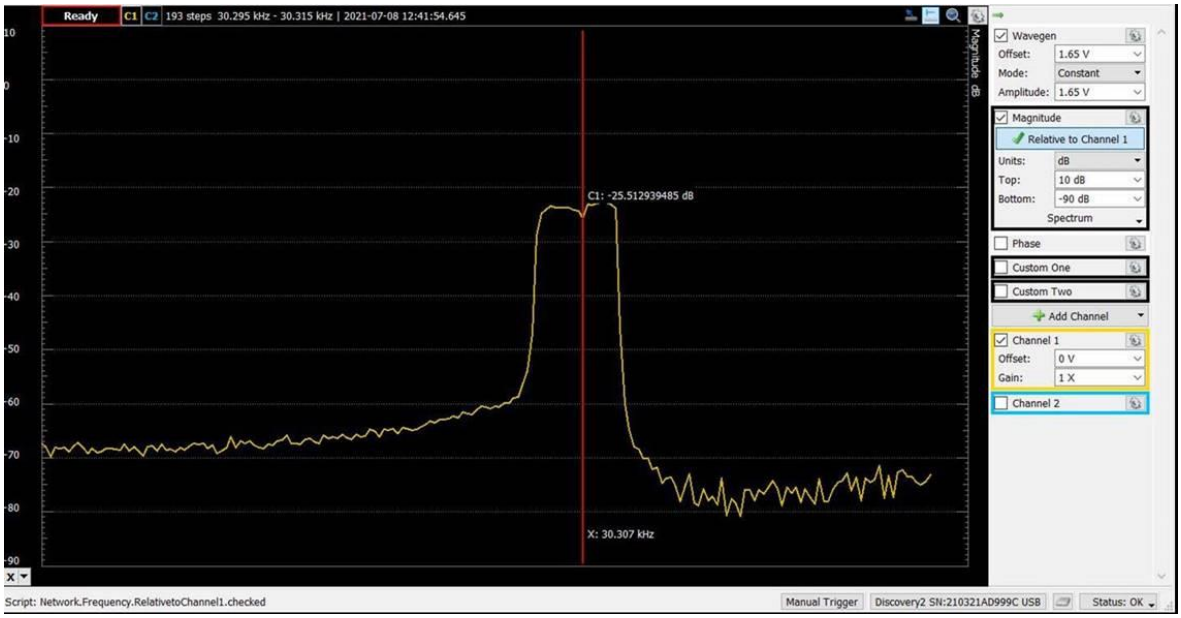


Figure 95 Post-repair transfer function

Integrated gyroscope test summary

The gyroscope system comprising the MRGT, the high temperature ASIC and associated packaging were tested for operation at 300°C over extended periods of time to validate long-term operation capability. Testing was conducted utilizing three test articles which were started at different times. A baseline dataset was collected at the beginning of the test and utilized as a comparison point to determine any functional or performance deterioration through the duration of the testing. While the test setup was powered and active through the duration of the test, the data collection was conducted in intervals. A failure associated with the test support components was detected at the fourth test interval indicating that a failure has occurred sometime after the last known interval in which the boards had achieved 521, 877 and 972 hours respectively, which was below the target lifetime of 1,000 hours. Failure analysis indicated a failed component in the low temperature test support equipment and uncovered a weakness in the capacitor attach. Once fixed, the testing indicated that the boards were functional with the high temperature components under test achieving a minimum of 1,529 hours of life at 300°C.

The testing validated that the integrated system can operate for extended periods of time at 300°C, therefore meeting or exceeding the temperature and lifetime capability needs of the geothermal drilling community. Since temperature is the main limiting

factor in the system's lifetime, even longer operating life can be expected at temperatures below 300°C.. The successful long-term testing has led to the advancement of the technology and to an increase in the technology readiness level (TRL) of the integrated gyroscope system to TRL 5+ having demonstrated components and parts of the system in a relevant environment.

Milestone List from SOPO and Progress Made Against Each

Table 24 Milestone Summary Table

Milestone Summary Table							
Recipient Name:	GE Global Research						
Project Title:	A MEMS Gyroscope for Reliable Long Duration Measurement While Drilling at 300°C						
Task #	**Task or Subtask (if applicable) Title**	**Milestone Type (Milestone or Go/No-Go Decision Point)**	**Milestone Number* (Go/No-Go Decision Point Number)**	**Milestone Description (Go/No-Go Decision Criteria)**	**Milestone Verification Process (What, How, Who, Where)**	**Anticipated Date (Months from Start of the Project)**	**Status**
1.1	Kick-Off meeting	Milestone	M1.1.1	Kickoff meeting with DOE	Conduct kickoff meeting with DOE	1	Completed Meeting conducted
2.1	2.1.2	Milestone	M2.1.1	State of the art benchmark publication	Publication benchmarking performance and gaps of existing MEMS gyroscopes at elevated temperatures	3	Completed Paper written and submitted to DOE. Material also included in Geothermal Resource Council annual meeting paper submission.
2.1	2.1.1	Milestone	M2.1.2	Performance requirements definition	Define performance requirements of gyroscope system	3	Completed. System requirements summarized in milestone M2.1.1

					including angular random walk, bias drift, electronics stability and noise requirements.		publication, electronics requirements summarized in milestone M2.4.1 report MRGT requirement summarized in milestone M2.3.1 report
2.2	2.2.3	Milestone	M2.2.1	MRGT characterization over temperature	Create a summary report of MRGT critical characteristics from room temperature to 300°C	6	Completed Summarized in report submitted to DOE
2.3	2.3.1	Milestone	M2.3.1	High temperature optimized MRGT design	MRGT device characteristics simulation results over temperature	6	Completed. Included in M2.3.1 report submitted to DOE
2.4	2.4.1	Milestone	M2.4.1	Electronics requirements flow down	Create electronics requirements document with critical performance parameters defined	6	Completed Summarized in report submitted to DOE
		Budget Period 1 Status Update 1	Status Update 1	Performance specifications and design requirements assessment.	WebEx meeting and presentation material on gyroscope and electronics performance specifications to meet orientation tool requirements	6	Completed. Meeting conducted
3.2	3.2.1	Milestone	M3.2.1	Electronics functional	Functional simulation results report.	8	Completed

				model complete			Summarized in report submitted to DOE
		Budget Period 1 Status Update 2	Status Update 2	Design feasibility assessment	WebEx meeting and presentation material on gyroscope and electronics gap analysis between the requirement flow-down and capability flow up	12	Completed. Meeting conducted
3.1	3.1.1	Milestone	M3.1.1	High temperature MRGT fabrication complete	At least 10 functional MRGT devices available for characterizatio n	12	Completed. 15+ devices tested to date.
3.2	3.2.2	Milestone	M3.2.2	Electronics design performance validated through circuit simulation	Report on circuit simulation results over design corners	13	Completed Summarized in report submitted to DOE
3.2	3.2.3	Milestone	M3.2.2	ASIC fabrication complete and ready for testing	At least 10 ASICs available for characterizatio n	16	Completed ASIC fabricated. 15+ parts packaged for component testing
3.2	2.2.5	Milestone	M3.2.4	Electronics component testing over temperature complete	Generate report on ASIC component performance at temperatures between 20°C and 300°C, and comparison with requirements	18	Completed ASIC tested and validated against its functional and performance requirements

3.1	3.1.3	Milestone	M3.1.2	MRGT component testing over temperature complete	Generate report on MRGT component performance at temperatures between 20°C and 300°C, and comparison with requirements	18	Completed MRGT component characterized over temperature and performance validated against requirements.
3.3	3.3.2	Milestone	M3.3.1	Gyroscope system functionality and reliability test plan defined	Generate test plan document including performance metrics and success criteria	18	Completed Plan devised and implemented for test and characterization of integrated gyroscope system over temperature and time
		Go/No-Go Decision Point	go/no-go #1	Component design performance established	Prepare gap analysis report detailing component performance capabilities and the system requirements	18	Performance entitlement established in analysis and validated by measurement results. See significant findings section in this report
4.1	4.1.2	Milestone	M4.1.1	Complete functional testing of integrated gyroscope system	Prepare a test report with integrated ASIC and MRGT performance over temperature	21	Completed. Measured integrated system performance from room temperature to 300°C and validated system capability
		Budget Period 2 Status Update	Status Update 3	System testing update	WebEx meeting and presentation material on integrated	21	Completed. Meeting conducted

					gyroscope system testing over temperature.		
4.1	4.1.3	Milestone	M4.1.2	Complete long-term testing	Prepare a test report on long term survivability of integrated gyroscope system at temperature	24	Completed. Demonstrated 1,500+ hours of operating life at 300°C of the integrated gyroscope system

Summary of key project task outcomes

A summary of the key project accomplishments in each of the development areas is summarized below.

MRGT design:

- ✓ Developed MRGT design to meet performance requirements and operating temperature capability.
- ✓ Validated key design choices with simulation and analysis.
- ✓ Designed device tuning feature to support sensing performance enhancement
- ✓ Developed device design compatible with fabrication process capabilities.

MRGT Fabrication:

- ✓ Wafer bonding process developed, WLP package implemented, survivability validated to 600°C
- ✓ Improved wafer yield and further improved device uniformity across wafer
- ✓ Micro-needle mitigation process developed and tested
- ✓ Fabricated MRGT parts to support the project's component and integration testing needs

MRGT Component Test:

- ✓ Developed multiple levels of test capability support component development, characterization and validations
- ✓ Developed vacuum chamber test capability to characterize unpackaged first generation MRGT devices
- ✓ Completed wafer level characterization of MRGT devices
- ✓ Completed MRGT functional testing from room temperature to 300°C
- ✓ Validated MRGT performance against requirements

Electronics and Controls:

- ✓ Performed requirements flow down to electronics requirements.

- ✓ Completed electronics architecture definition.
- ✓ Developed board-level room temperature electronics to validate the electronics design and requirements.
- ✓ Utilized the board-level electronics to develop the MRGT control and tuning functions
- ✓ Completed the ASIC block level and detailed transistor level detailed design and layout
- ✓ Validated the ASIC functionality in simulation across temperature and process corners.
- ✓ Fabricated high temperature capable SOI ASIC
- ✓ Developed packaging and testing capability to characterize the ASIC over temperature
- ✓ Completed ASIC component test and validation from room temperature to 300°C
- ✓ Demonstrated ASIC performance against requirements

Packaging:

- ✓ Vacuum packaging approach designed and validated
- ✓ High temperature capable device packaging approach developed and utilized in MRGT characterization testing at 300°C
- ✓ Ceramic substrate approach for MRGT and ASIC integration defined
- ✓ Defined design rules, material and process selection for high temperature ceramic board

System Integration and testing:

- ✓ Developed high temperature test platform to support characterization and long-term testing of integrated gyroscope system
- ✓ Designed and fabricated high temperature, high reliability substrate for integrated MRGT and ASIC testing to support extended duration testing at 300°C
- ✓ Completed functional testing of integrated MRGT and ASIC from room temperature to 300°C
- ✓ Validated functionality and performance of integrated gyroscope comprising high temperature MRGT, ASIC and associated packaging
- ✓ Completed long term testing of integrated MRGT and ASIC
- ✓ Validated greater than 1,000 operating hours at 300°C

Other project outputs:

Submitted Reports

In addition to the required quarterly reports, the following topical technical reports have been submitted to DOE as part of the project execution.

Table 25 Project output reports

Report file name	Milestone addressed	Description and key findings
State of the art benchmark M2.1.1	M2.1.1	Topical report/Publication covering: 1. benchmarking performance and gaps of existing MEMS gyroscopes at elevated temperatures. Identified ~200ºC gap between COTS parts and 300°C operation goal 2. Wellpath and Azimuth uncertainty requirements flow-down. Identified bias uncertainty requirements of under X º/h to meet < 1 degree azimuth uncertainty requirement
Topical report on MRGT temperature test data - rev1	M2.2.1	Topical report covering: 1. Characterization of first generation MRGT devices over temperature and established functionality at 300°C 2. Validation of device performance models
Topical report on MRGT design and fabrication - rev1	M2.3.1	Topical report covering: 1. MRGT design optimization for high temperature operation 2. Fabrication plan, capability and risk assessment to support the high temperature optimized MRGT design
Topical report on electronics requirements - rev1	M2.4.1	Topical report covering: 1. Analytical model for MRGT and electronics operation and noise performance 2. Electronics and ASIC interface requirements 3. Electronics architecture definition 4. Analysis of electronics capability to meet key performance requirements
Topical report on functional simulation results_rev1	M3.2.1	Topical report covering 1. Board level validation of functional electronics circuit 2. Control system design refinements to improve performance 3. Noise characterization results to 200ºC and extrapolation to 300°C 4. Circuit simulation results
Topical report on circuit simulation	M3.2.2	Topical report covering:

results over corners_rev1		1. Circuit simulation results over design corners and temperature 2. ASIC testability and risk mitigation approach 3. ASIC readiness for fabrication
Topical report on gyroscope system test plan-rev1	M3.3.1	Topical report covering: 1. Integrated MRGT and ASIC test approach and test plan 2. Test success criteria for performance and lifetime testing
Topical report on MRGT component performance-rev1	M3.1.2	Topical report covering: 1. MRGT characterization results over temperature 2. MRGT performance and capability validation
Topical report on ASIC test results over temperature_rev1.pdf	M3.2.3	Topical report covering: 1. ASIC functional characterization 2. ASIC performance testing over temperature
Topical report on Integrated MRG ASIC performance over temperature rev 1.pdf	M4.1.1	Topical report covering: 1. Integration and packaging to support 300°C operation 2. Integration testing of ASIC and MRG 3. Functional and performance of the integrated ASIC and MRG at 300°C
Topical report on long-term survivability of integrated gyroscope system at temperature_rev1	M4.1.2	Topical report covering: 1. Long-term testing capable high temperature test system design 2. Long-term (>1,000 hours) functional and survivability testing approach and results of integrated system at 300°C

Publications, Abstracts and Presentations

- ✓ Abstract and paper has been submitted to ION PLANS conference, and has been accepted and awarded best-in-track paper award:

  Lin, D., MacDonald, R., Calbaza, D., Scherer, B., Johnson, T., Toepfer, T., and Andarawis, E., “Sub-Degree-Per-Hour MEMS Gyroscope for Measurement While Drilling at 300ºC”. Accepted for publication at IEEE/ION PLANS (2020).

  OSTI E-link ID 1634024

- ✓ An abstract and paper has been submitted to the Geothermal Resources Council annual meeting

Scherer, B., Lin, D., Macdonald, R., Calbaza, D., and Andarawis, E. “A MEMS gyroscope for Reliable Long-Duration Measurement While Drilling at 300ºC”
OSTI E-link ID 1840695

- ✓ Paper to: The 8th IEEE International Symposium on Inertial Sensors & Systems

  D. Lin et al., "Polaris - A Low Cost MEMS Fabrication Platform for Navigation-Grade Inertial Sensors," 2021 IEEE International Symposium on Inertial Sensors and Systems (INERTIAL), 2021, pp. 1-4, doi: 10.1109/INERTIAL51137.2021.9430465.
  OSTI E-link ID 1840691

- ✓ Conference presentation at 2021 National Space & Missile Materials Symposium (NSMMS) & the Commercial and Government Responsive Access to Space Technology Exchange (CRASTE)

  Popp, J., Andarawis, E., and Lin, D. “Extreme Temperature, High Reliability Navigation Sensors and Electronics for Low SWaP-C Operation”
  OSTI E-link ID 1840684

Summary and Conclusions

During the project period of performance, the team has advanced the state of the art in MEMS multi-ring gyroscopes and Silicon-on-Insulator electronics to demonstrate a high temperature capable gyroscope system capable of extended operation at 300°C. The project achieved all its technical goals and advanced the technology readiness level of the development. A number of publications were generated further supporting the goal of advancing the geothermal community awareness and engagement.

Fabrication innovations of the MRGT during the project period of performance further advanced the manufacturing readiness level of the device and achieved yield and reproducibility advancements that further increase the viability and adoption potential of the technology.

References

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(3) B. Kim, R. Candler, M. Hopcroft, M. Agarwal, W. Park, T. W. Kenny, Frequency stability of wafer-scale film encapsulated silicon based MEMS resonators, Sensors and Actuators A ,136, pp125–131,(2007).