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U.S. DEPARTMENT OF ENERGY

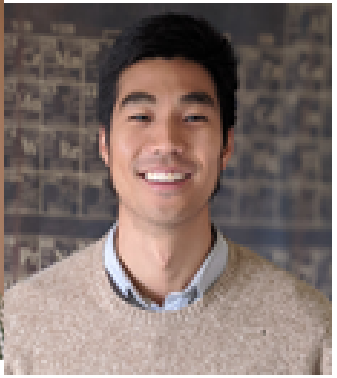
Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

Manufacturing an Extremely Energy Efficient Transistor for Decarbonization

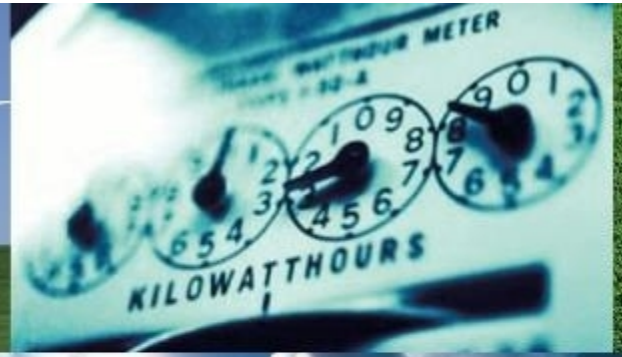
Tina Marie Kaarsberg, PhD

Technology Manager, Advanced Manufacturing Office (AMO) energy.gov/eere/amo/

Shashank Misra, Sandia National Laboratories, Kenta Shimizu, Energetic



“Presented at the 2021 Summer Study on Energy Efficiency in Industry”



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EERE's Advanced Manufacturing Office (AMO)

U.S. DEPARTMENT OF ENERGY

Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

Advanced Manufacturing Office

BUDGET

$396M

FY21

WHAT WE DO

Partner with industry, academia, states, and National Laboratories **to increase energy and material efficiency in manufacturing,** driving energy productivity, economic growth, and industrial decarbonization.

STAFF

~70

Feds, contractors, and fellows

GOLDEN, CO AND DOE HEADQUARTERS

R&D Projects

FY21 = $218M

R&D Consortia

FY21 = $133M

Technical Partnerships

FY21 = $45M

Administration Climate Goals & DOE Priorities

BIDEN ADMINISTRATION CLIMATE GOALS

A carbon pollution-free power sector by 2035

50% cut in carbon emissions by 2030

Make basic science breakthroughs

Turn that science into deployable technologies

Fund deployment of clean energy technologies

- **CREATE GOOD-PAYING JOBS**
  associated with the fast-growing global market for products that reduce carbon emissions
- **COMMIT TO RACIAL JUSTICE**
  and target disadvantaged communities for new clean energy investments, jobs, and businesses
- **ENCOURAGE ROBUST COLLABORATION**
  across the federal government, the fifty states, and the private sector

Manufacturing Overview & AMO Industrial Decarbonization Goal

AMO works to **increase energy and material efficiency in manufacturing,** driving energy productivity, economic growth, and decarbonization

MANUFACTURING

- Uses roughly 25% of the nation's primary energy
- Accounts for one quarter of the U.S.'s greenhouse gas emissions
- Represents nearly 80% of energy use in energy-intensive sectors
- Generates 12% of the U.S. GDP and nearly 11 million jobs
- Incurs >$150 billion in energy costs annually

KEY AMO GOALS

1. Improve the **productivity, competitiveness, energy efficiency, and security** of U.S. manufacturing
2. Reduce the **life cycle energy and resource impacts** of manufactured goods
3. Leverage diverse **domestic energy resources and materials** in U.S. manufacturing, while strengthening environmental stewardship
4. Transition **DOE-supported innovative technologies** and practices into U.S. manufacturing capabilities
5. Strengthen the **U.S. manufacturing workforce**
6. Accelerate emerging and transformative

greenhouse gas

Transistors and Circuits, and Chips—Oh My!

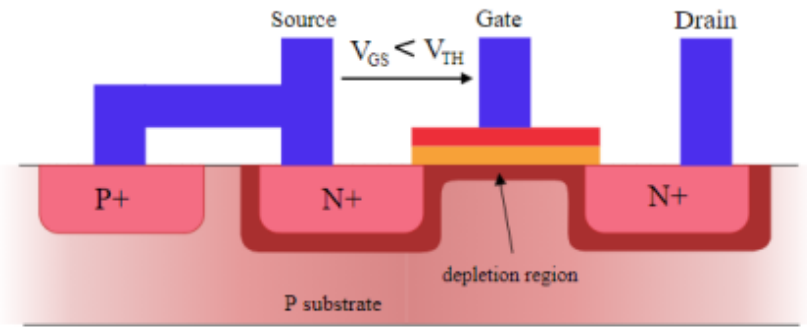
Transistors

Moore's Law

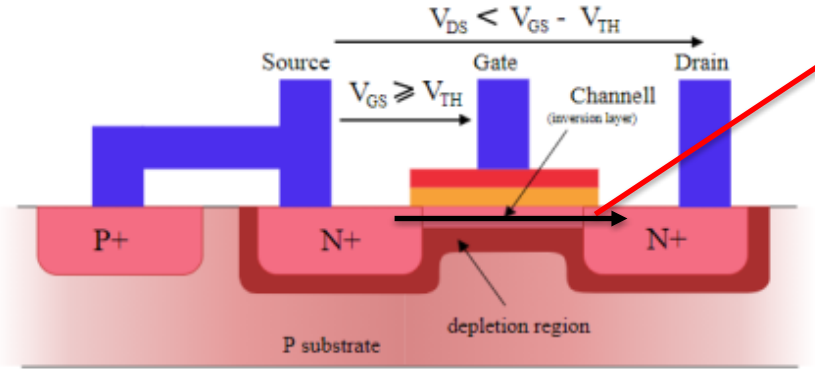
Beyond Moore's Law

Transistors in Microelectronics and Computing

- An input voltage on the “gate” of a transistor—made of semiconducting silicon—results in a large current on the “drain” side of the transistor by providing a conducting path for electrons (in an n-type device) or holes (in a p-type device) between source and drain contacts.
- A transistor is a switch where the higher “on” voltage represents a 1 and the lower “off” voltage represents a “0” in binary computing.
- The transistor is the fundamental building block of computing.



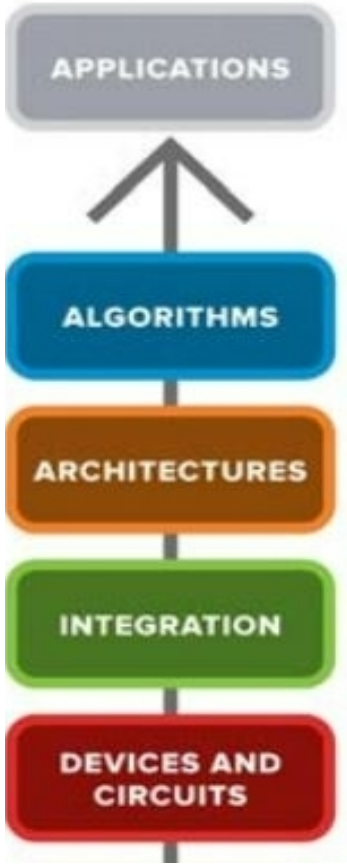
Off-State: “0”, no current flow



Flow of electrons through conducting channel

On-State: “1”, current flow

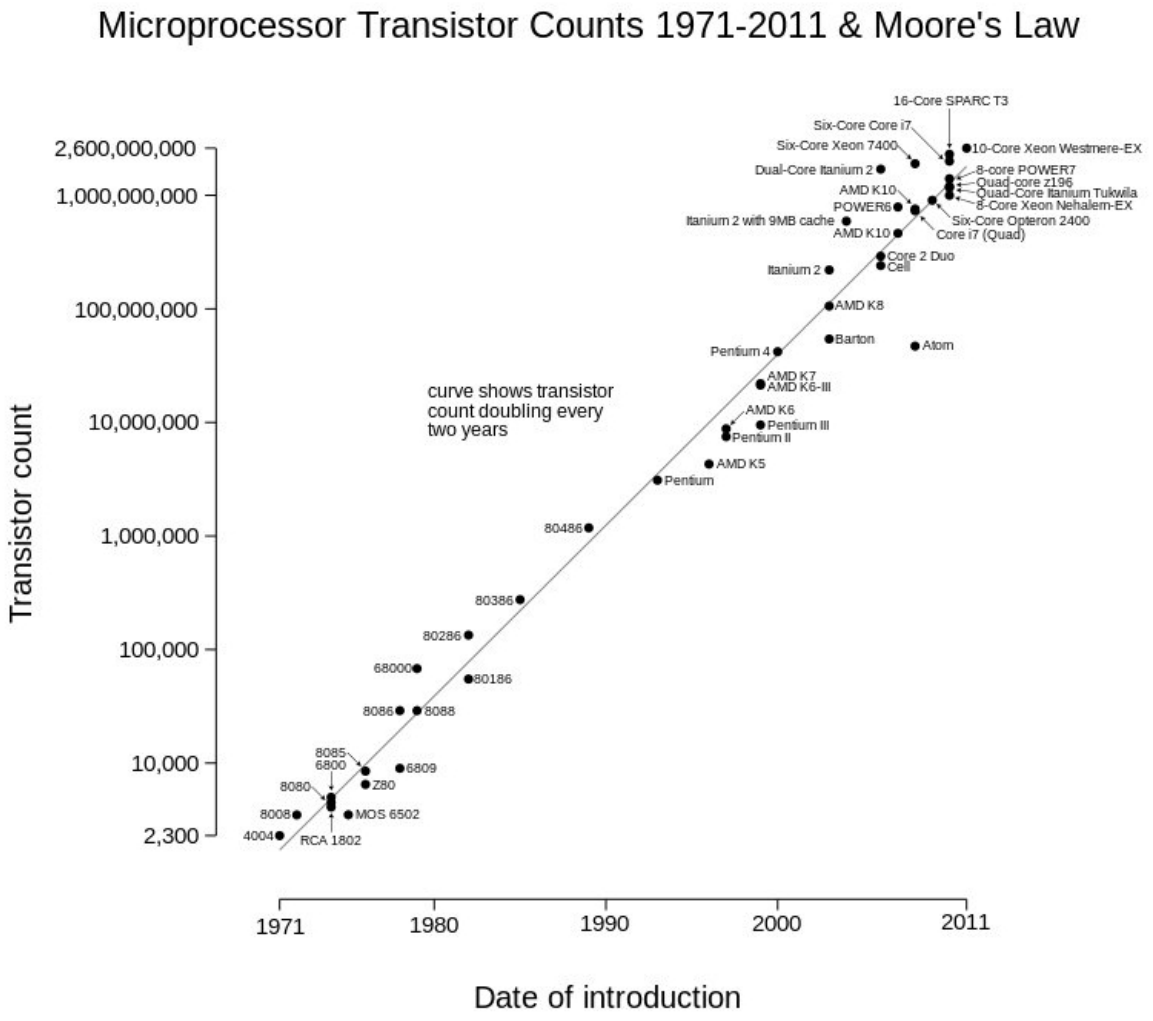
Source: Wikipedia



Transistors are Foundational

Moore's Law

- Over the years, semiconductor manufacturers set and met ambitious goals to decrease transistor size because the smaller the transistor is, the shorter the distance between source and drain and the lower the input voltage need to be.
- A smaller transistor automatically uses less power and switches faster.
- Gordon Moore observed that transistor density was doubling roughly 18 months – this became known as Moore's Law

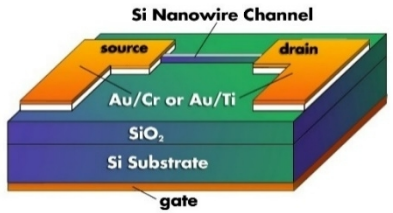


Source: ACM

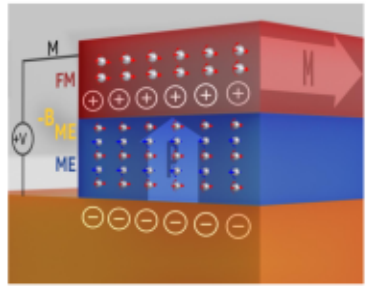
Microelectronics Efficiency Beyond Moore's Law

- However, in the past decade, Moore's Law and the efficiency gains from it have begun to slow
- Making transistors themselves more energy efficient in ways *other than* shrinking them is critical to improve the energy efficiency of general-purpose computing, which will continue to be heavily used.
- For example, graphic processing units have been used to provide enormous gains in efficiency over generalized central processing units for neural networks in certain tasks
- Five candidate "beyond Moore" technologies are listed to the right

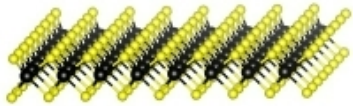
Candidate Technologies



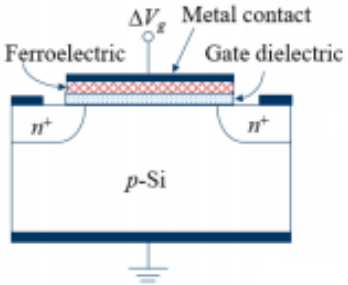
1D material systems
(nanowires, CNTs)



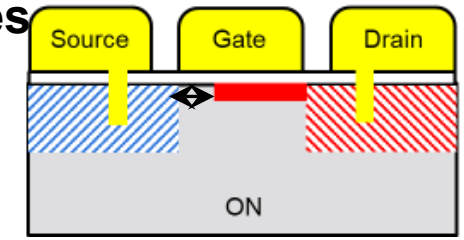
Magneto-electric spin orbit devices



2D material systems
(graphene, transition metal dichalcogenides)



Ferroelectric devices



Tunnel FETs

Microelectronics-Decarbonization Connection

SMART Manufacturing/ Electrification Connection

Minimizing Looming Energy Use Explosion from Semiconductors

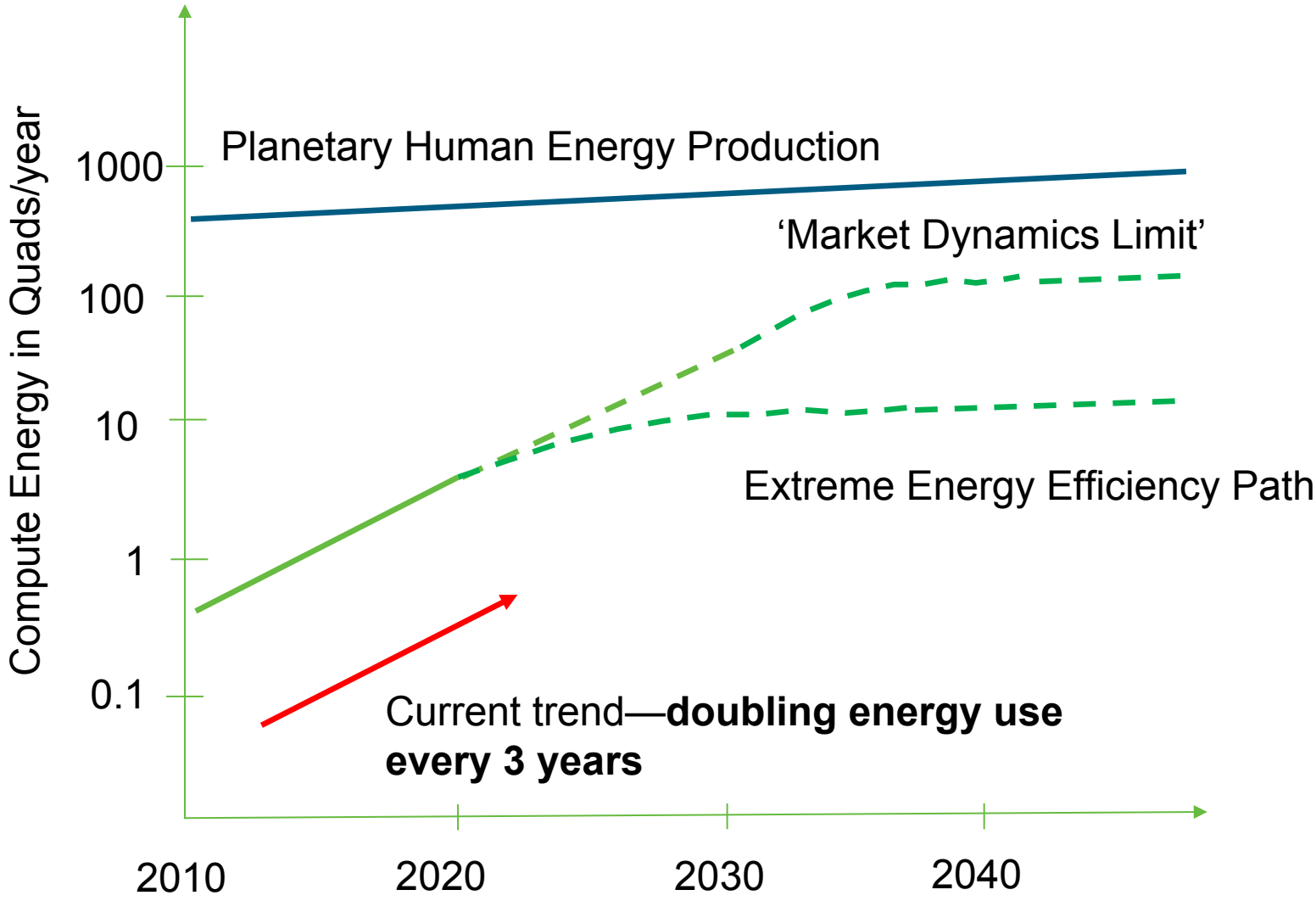
Extreme Energy Efficiency

SMART Manufacturing/ Electrification Connection

- Industrial sector is a challenging sector hard to decarbonize through electrification
- Semiconductors are key to the electrification of major sectors
  - Improvements in integrated sensor systems, powered by microelectronics, make processes and sensor systems more energy efficient and lower barriers to ubiquitous wireless sensors with edge computing for improved performance.
- Semiconductor innovation is needed in order to fully realize the potential of ICT including Industry 4.0, 5G+

Minimize Semiconductor Energy Crisis w/Extreme Energy Efficiency

- Current trends would lead to market dynamics plateau at ~20% of planet energy—not so great for climate either
- Market dynamics limit implies job losses and other negative economic impacts
- Extreme energy efficiency is based on expanding and accelerating innovation



Source: SRC Jan 2021

Extreme Energy Efficiency needed by 2030

"Extreme energy efficiency technologies" ≡ technologies that use (>10x) less energy*

Energy Efficiency can lead to 50% cut in U.S. GHG emissions (Nadel and Ungar, 2019;)

Extreme Energy Efficiency can cut emissions 50% *in a decade* (Kaarsberg, Hopson, and Clay, 2004)

*than traditional technology.

Extremely Energy Efficient Microelectronics Technology: Tunnel Field Effect Transistor

Water Bucket Analogy

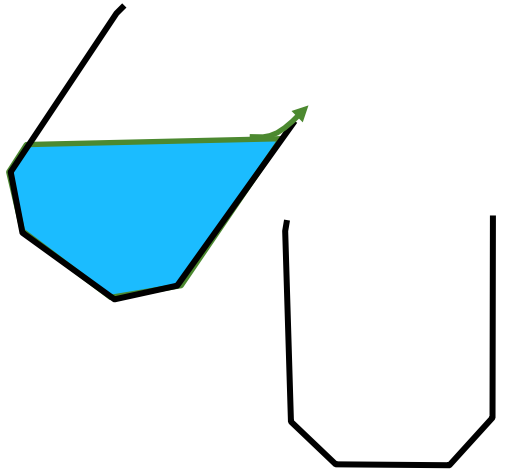
Current-Voltage Relationship

Limitations from Manufacturing

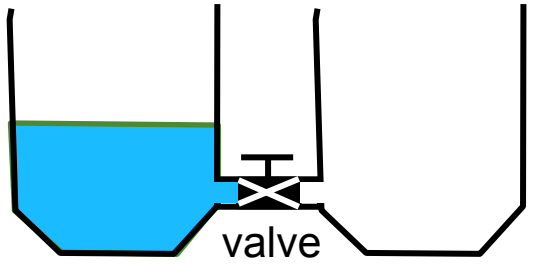
Water Bucket Analogy for MOSFET & TFET

Water transfer analogy for switching

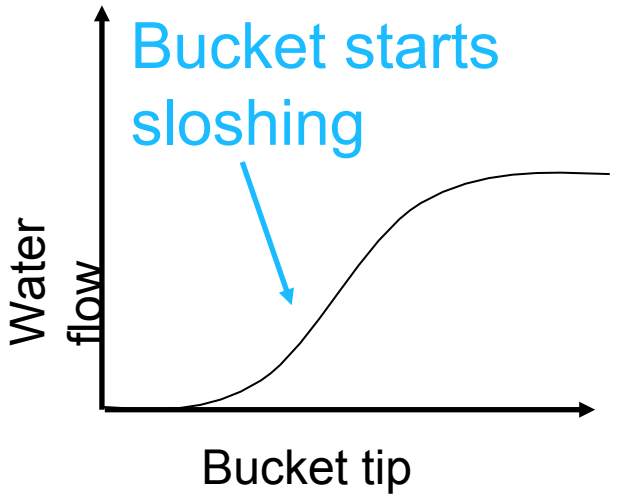
MOSFET – state of the art

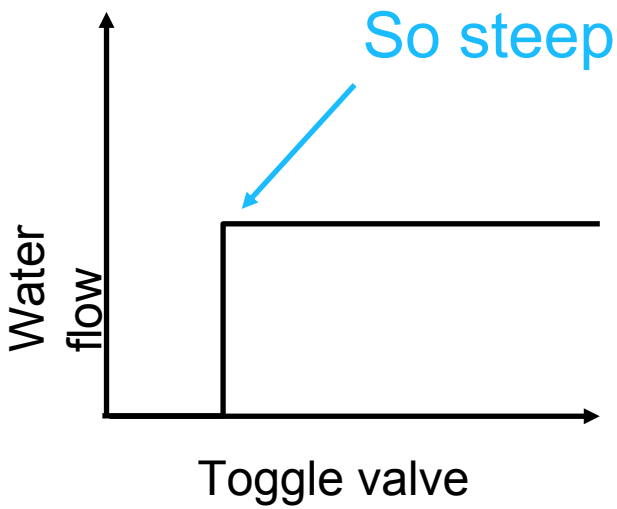


TFET – next generation?



Horizontal axis = how much energy you put in

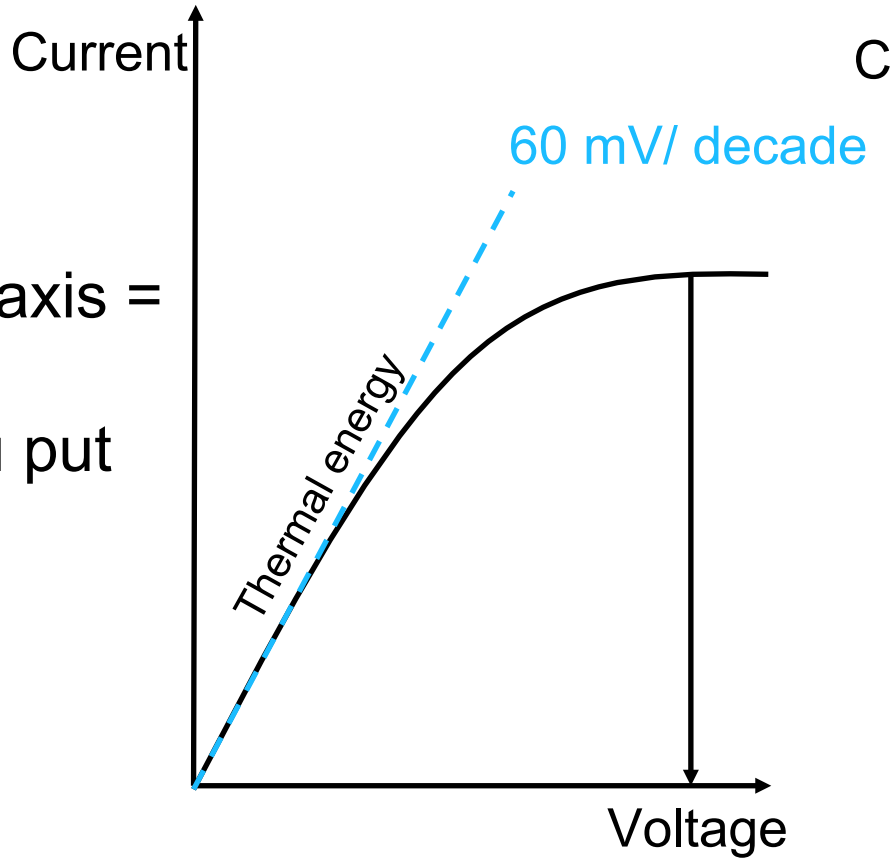




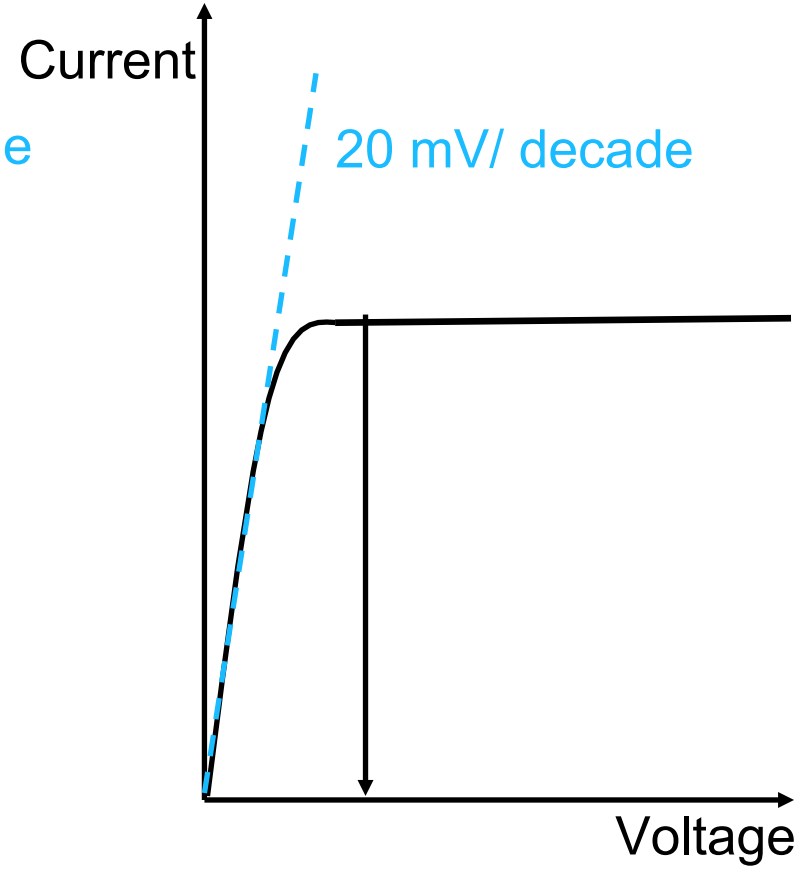
Vertical axis = how much work you get out!

What makes for an efficient transistor?

MOSFET – state of the art



TFET – next generation?



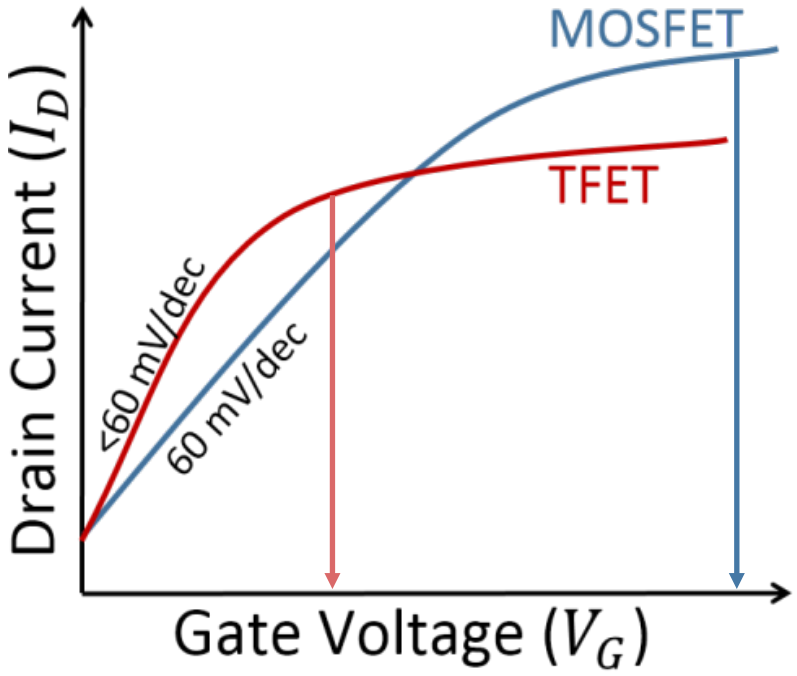
Horizontal axis = how much energy you put in

Vertical axis = how much work you get out!

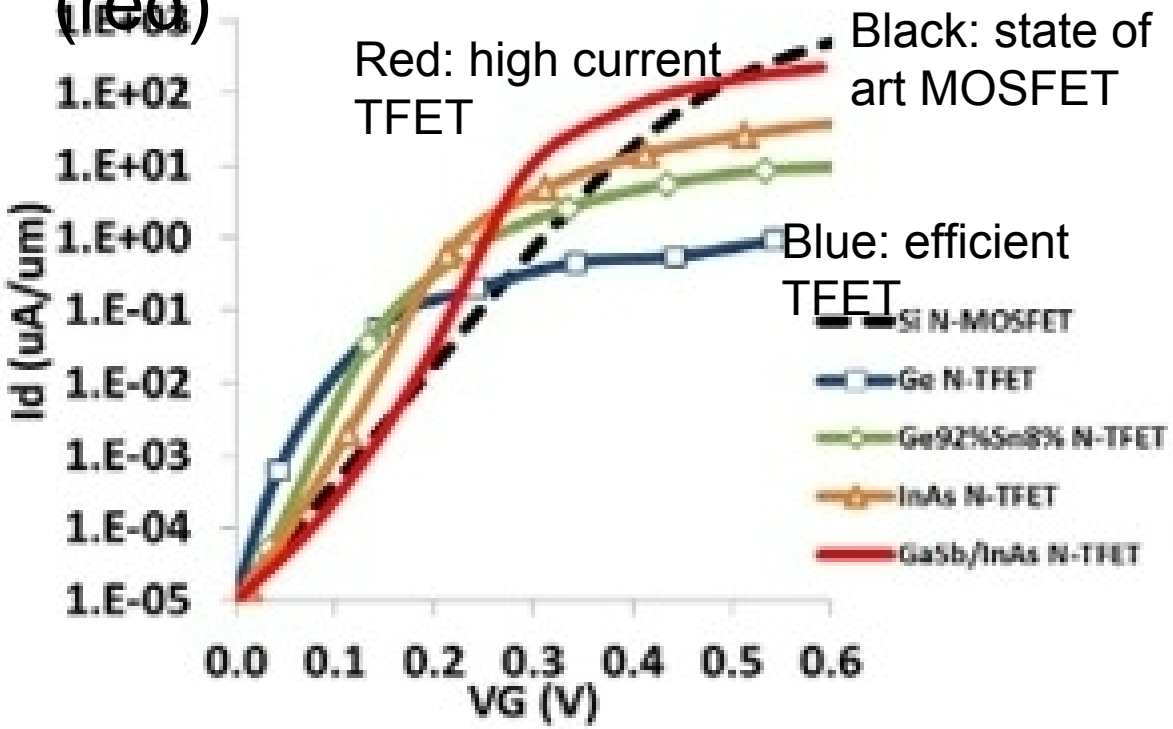
Efficiency is related to the subthreshold slope:
less mV / decade = more efficient!

TFETs have not reached their potential in practice

10x improvement in energy efficiency predicted



In practice, efficient TFETs can't do much work (blue) and TFETs that do a lot of work aren't efficient (red)



Manufacturing to Overcome TFET Barriers

1. To increase current by changing geometry

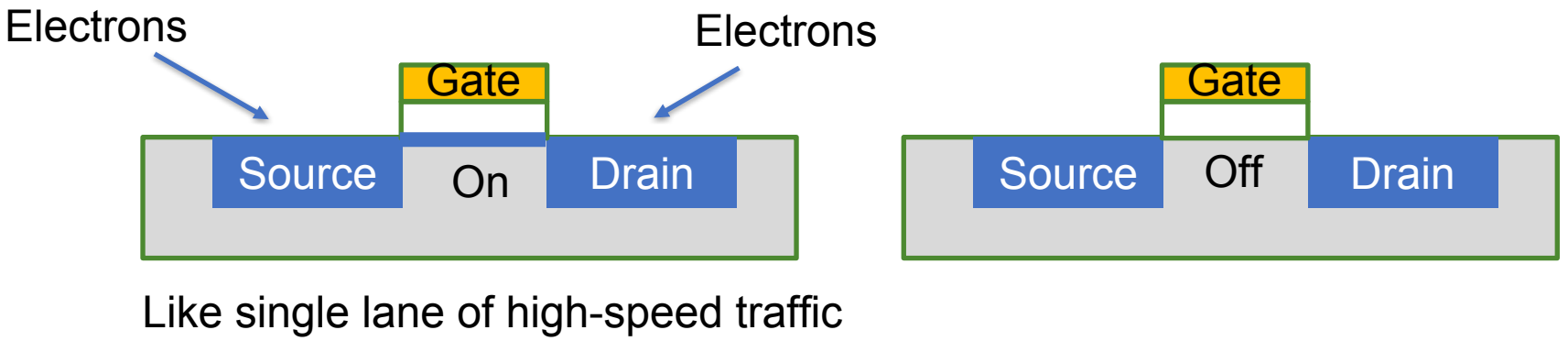
Vertical TFET Architecture

2.To lower voltage, steepen slope:

Atomically Precise Advanced Manufacturing

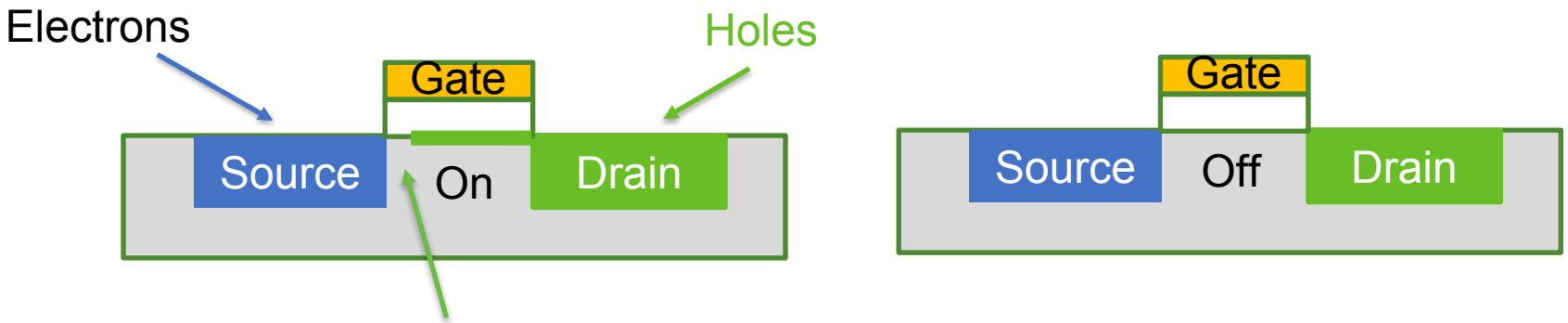
Origin of the barrier limiting TFET current

MOSFET



Like single lane of high-speed traffic

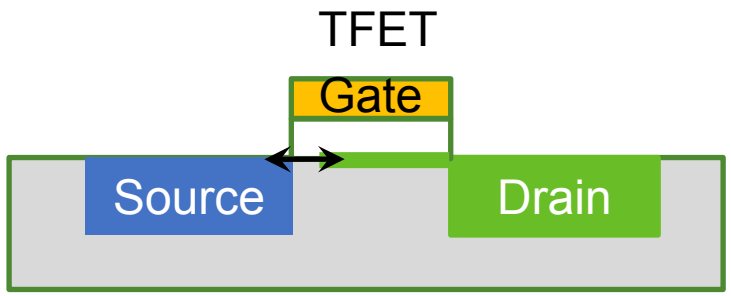
TFET



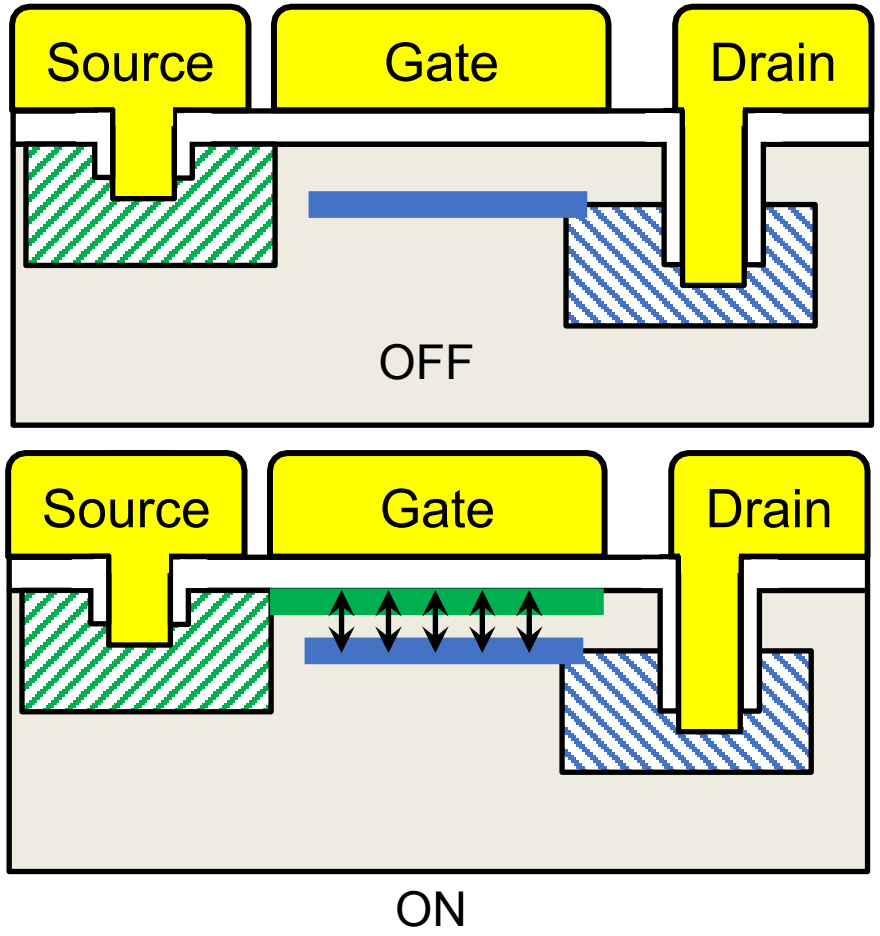
Like a single lane of traffic with a speed bump

(1) Current: Intrinsic speed bump associated with tunneling

Overcoming Barrier 1: Vertical TFET

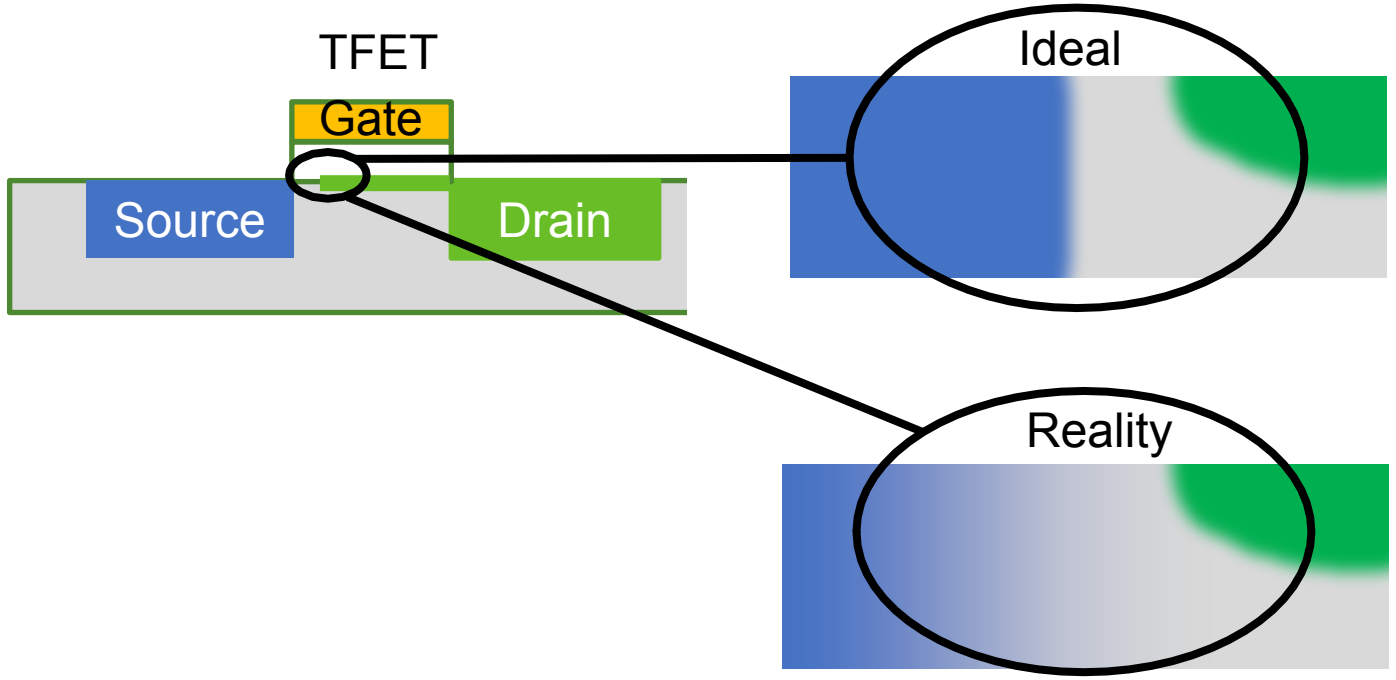


(1) Solution: Vertical geometry creates many parallel channels

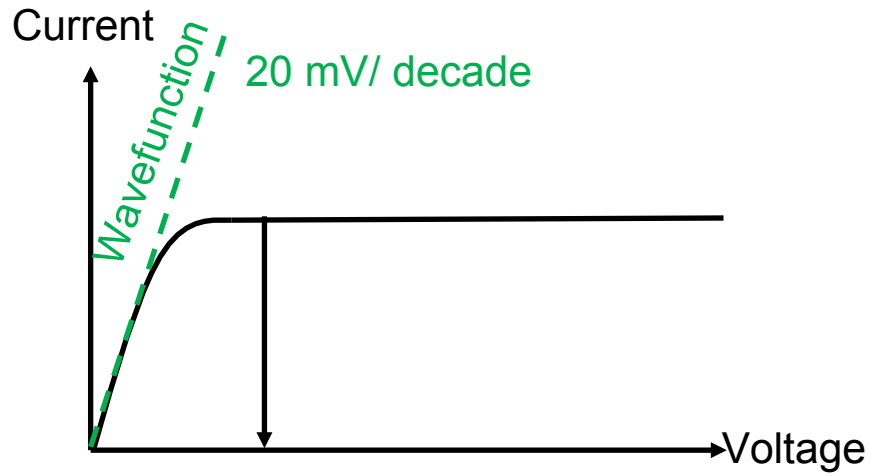


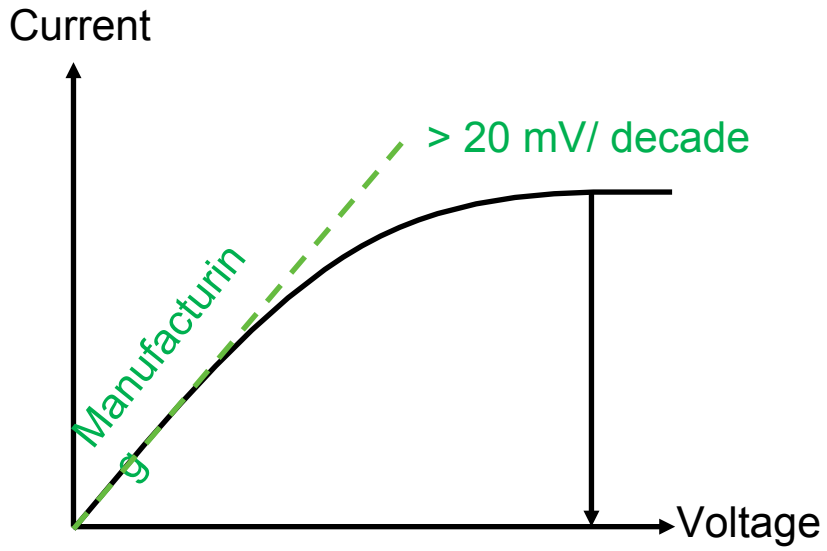
Many lanes of traffic, each with a speed bump

Origin of the barrier limiting TFET voltage



High temperature → diffusion

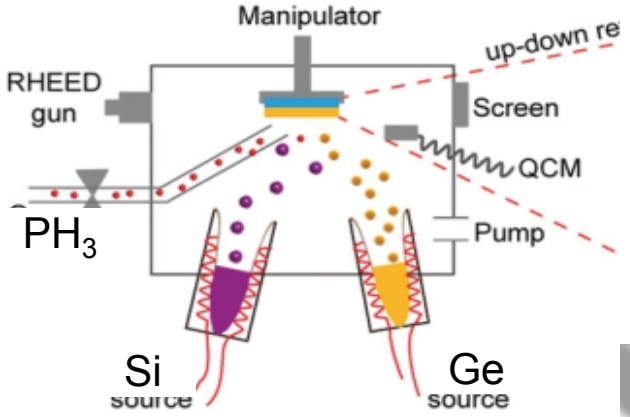


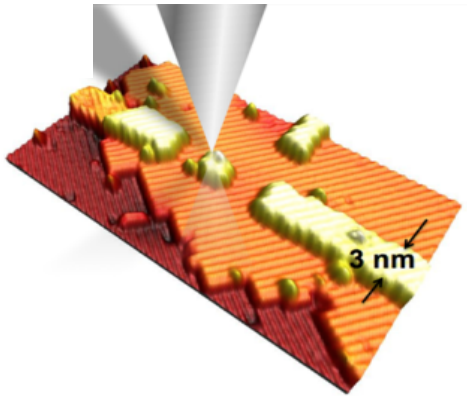


(2) Voltage: manufacturing limitation with abruptness of doping profile

Overcoming Barrier 2: Atomic precision advanced manufacturing

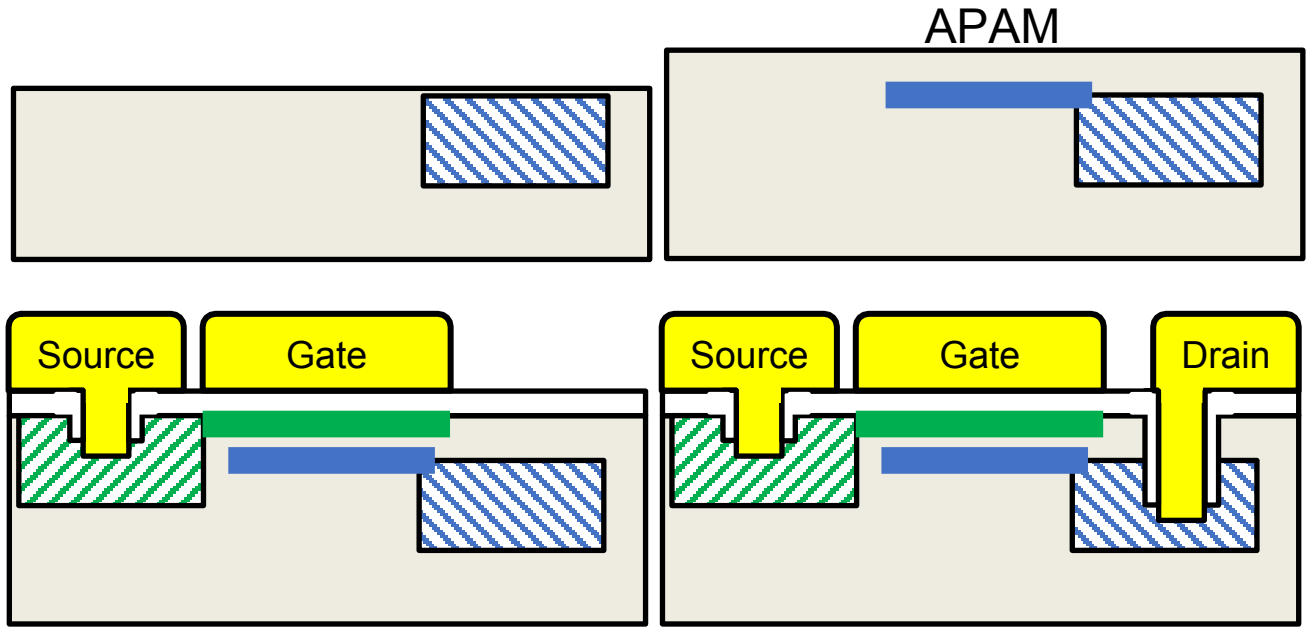
Leverage chemistry to replace high temperature





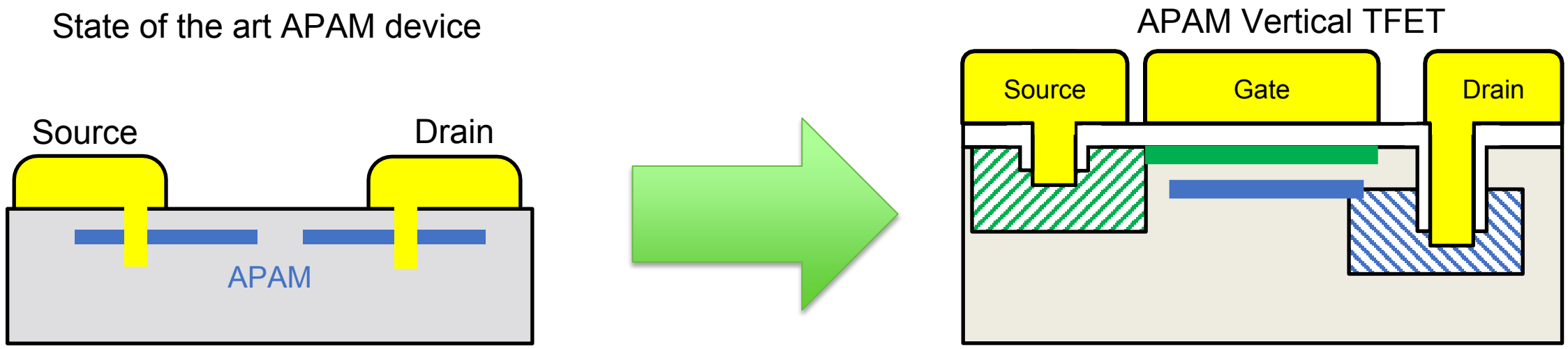
(2) Solution: atomic precision advanced manufacturing (APAM)

TFET process flow



All subsequent steps must be low temperature

FY 21 AMO project: Big energy efficient transistors (BEETS)

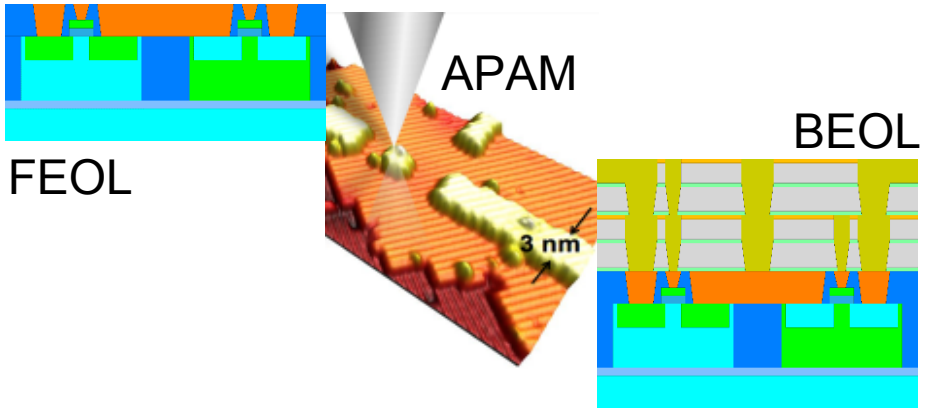


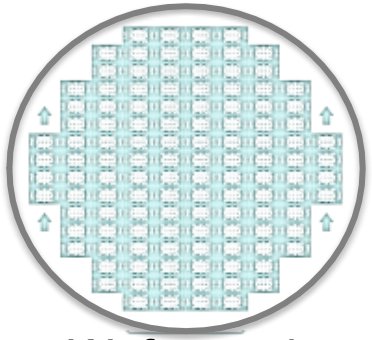
BEETS: can be implemented in legacy and leading technologies

- Discover device components
- Combine new components into transistor
- Establish modeling framework to project performance

Path to manufacturing – contact resistance

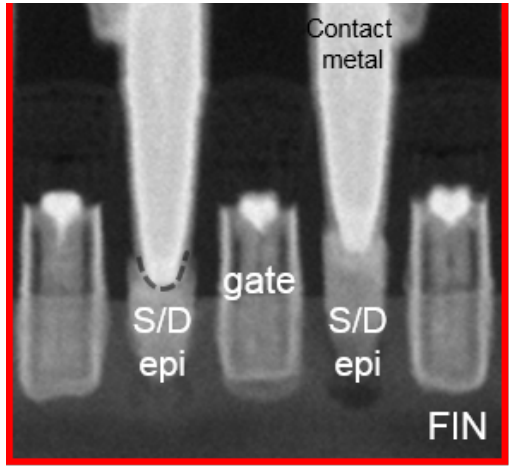
Sandia: proof-of-principle insertion into semiconductor manufacturing





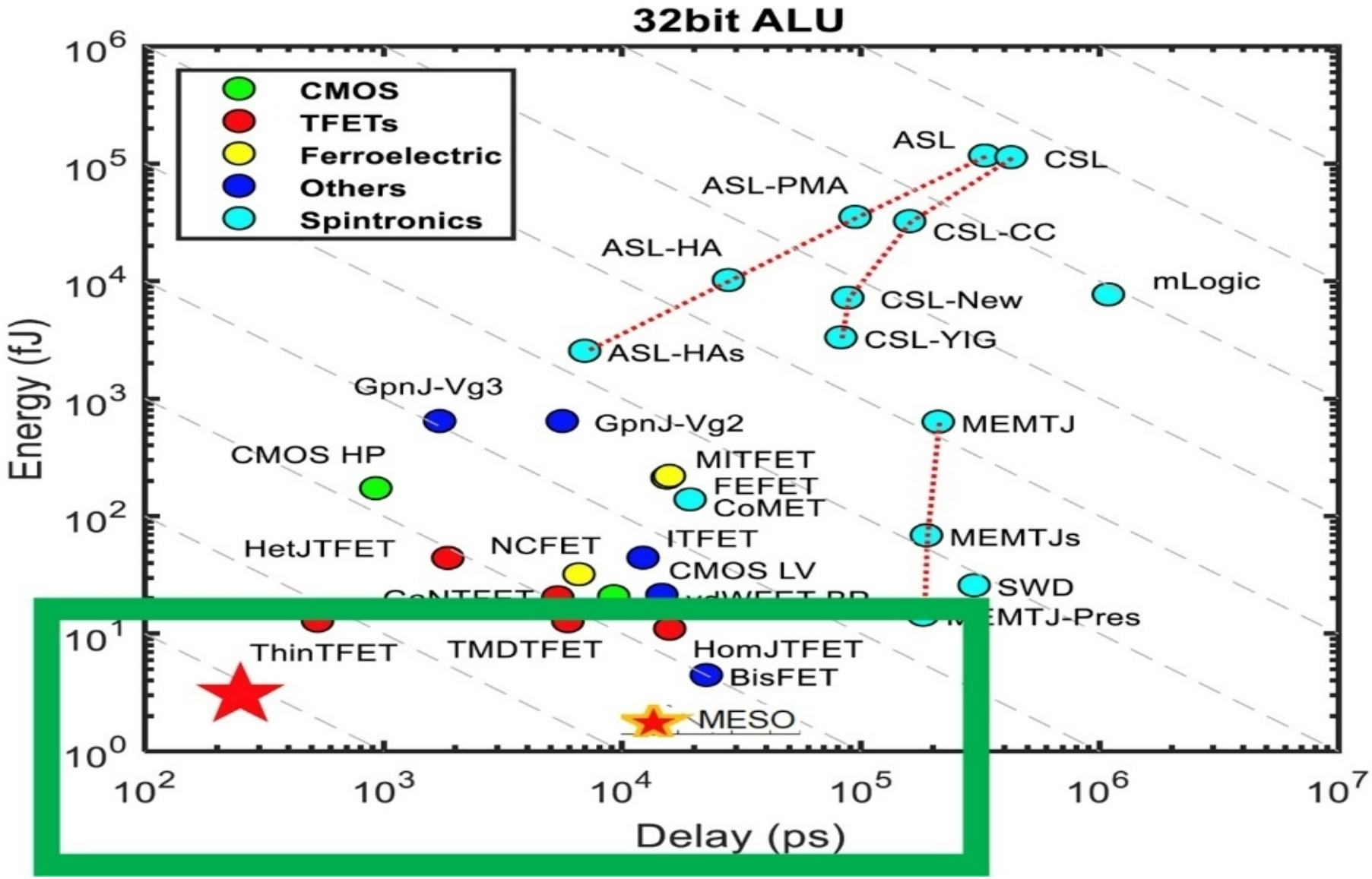
Wafer-scale lithography

Sandia is engaged with a tool maker on near-term application for APAM: contact resistance



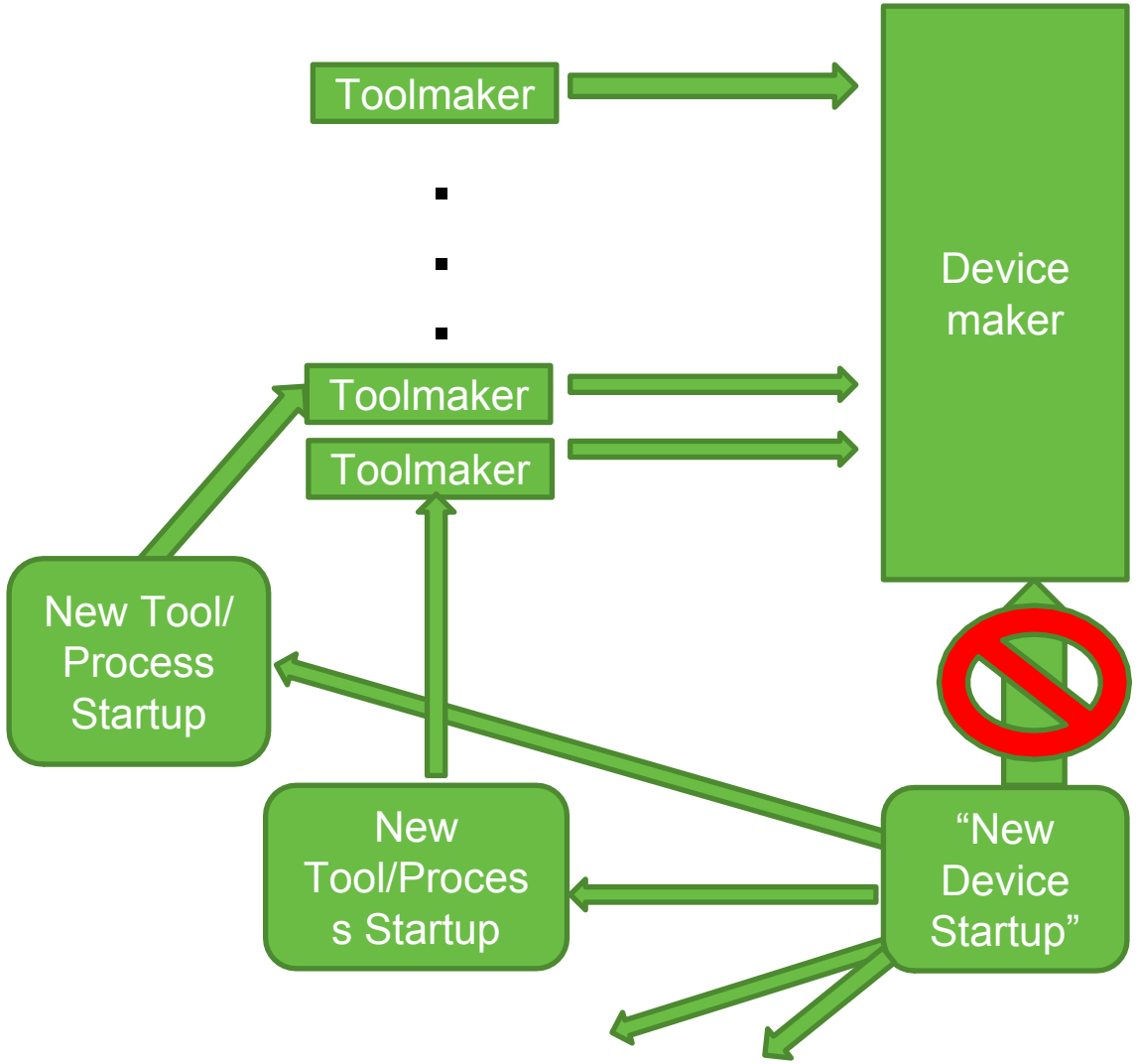
Same tool needed for near-term applications may be leveraged for manufacturing TFET in the future

Other Extremely Energy Efficient Transistors



Technology Transition Pathways

- **Early Applications of APAM technology unlikely to be entire Transistor**
- **Start with commercializing APAM subprocesses with Tool Makers**
  - Lower tech, less complex applications (e.g. Advanced Packaging)
  - Solve urgent problem for Toolmakers (e.g. interconnection bottlenecks)
- **As more Tool Makers develop confidence in subprocesses, chances to commercialize entire new device increase.**



Thank you for your attention

For additional information and to subscribe for updates:

energy.gov/eere/amo/

EXTRA AFTER THIS

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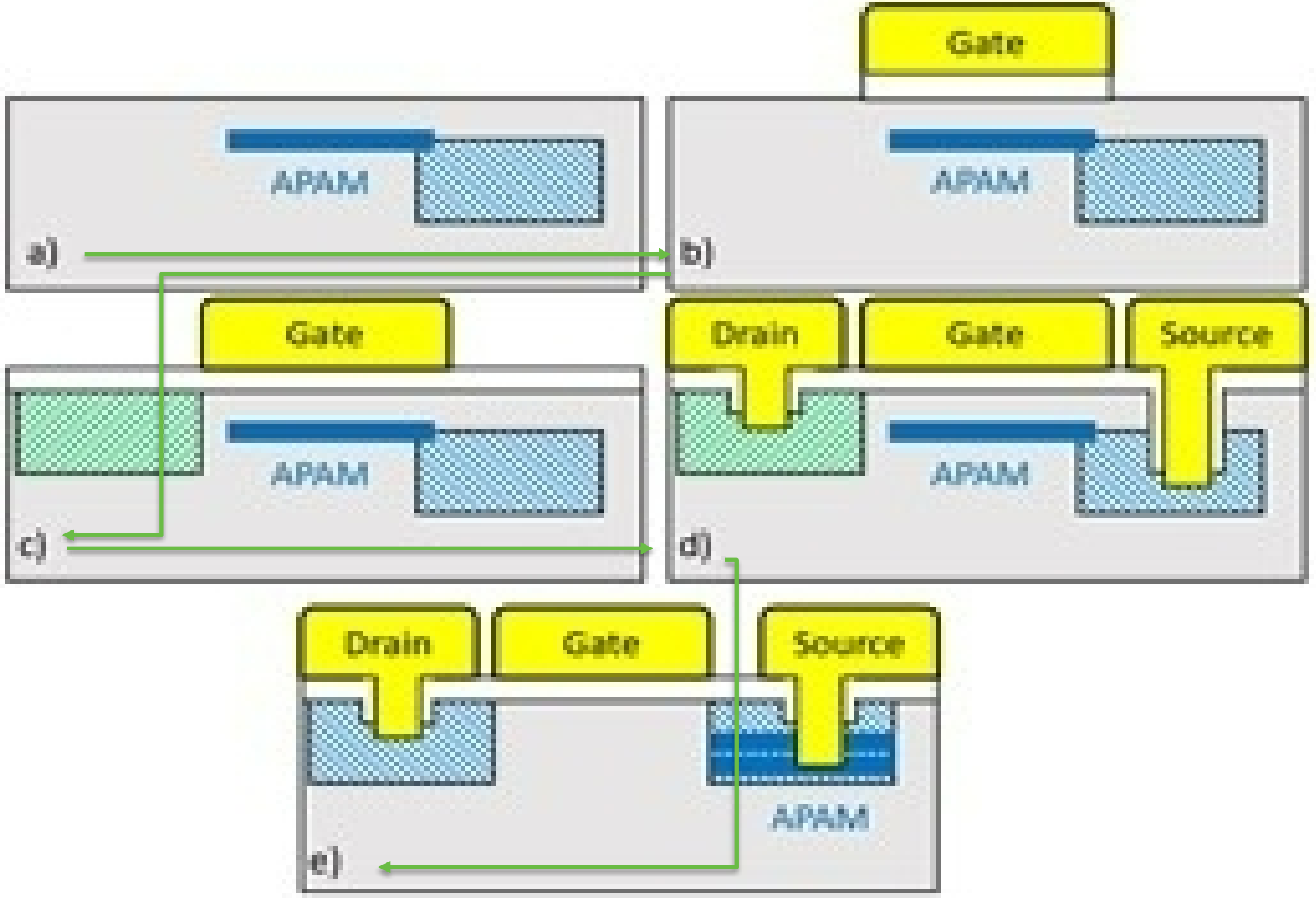
APAM TFET Manufacturing Process Flow

a) ion implant to form source contact+ HDL to make buried APAM electrode.
b) high-κ dielectric/metal gate deposited
c) surface hole silicide formed for drain
d) independent contacts for drain + source made to buried APAM layer.
e) Alternate: APAM in source contact to reduce metal-semiconductor contract resistance.



Relevant Workshop April 20-21, 2021

Sandia National Laboratories'

Hosted by Dr. Shashank Misra, PI of Sandia's FAIR DEAL Grand Challenge

Sandia Atomic Precision Workshop Summary

- ***microelectronic devices***
  - Sandia did research on TFET aging and showed APAM is more stable than the metal part of the vertical TFET exemplar
  - UC Berkeley emphasized the need to use self-limited processing to gain control over variations at small scales.
  - Purdue discussed devices based on metal chalcogenide ALD films and nanowires, and how new electronic properties emerge with quantization.
  - Notre Dame discussed interdependence of advanced technologies in microelectronics, and need for vertically-integrated teams of researchers.
  - UPenn speaker discussed the lifecycle of a successful 10-year technology transition for a GeTe RF switch while he was at DARPA.
- ***near-atomic fabrication***
  - Focus was on scaling down near-atomic processes (e.g. ALD, ALE)
  - Intel emphasized the problems with shrinking features includes edge placement error, and nonuniformity in thickness & film integrity
  - NCSU noted that ALD/ALE have inherent randomness/defects --some originating from each cycle not really leading to an atomic layer.
  - IBM noted atomic layer etching needs to accommodate a wide range of process needs – e.g. materials.
  - T.U. Ilmenau speaker noted most characterization averages over area, but combining, e.g., scanned probe with SEM confers spatial resolution.
  - Self limited bottom up approaches are the future. Top down has a ton of entropy that must be conquered
- ***in-operando characterization at the atomic limit***
  - In APM it's a lot easier to make a device than characterize it.
  - Synchrotron light sources average over an area, but offer multimodal characterization, +use of lenses has opened < 10 nm spatial resolution.
  - ORNL emphasized opportunities from putting physics-based modeling in the loop for transmission electron microscopy (TEM.)
  - NIST emphasized opportunity in being able to characterize something in operando while processing it.
  - Speaker from Utah, who does biophysics, emphasized the need to use AI/ML to sense and react for real-time characterization.
  - Discussions on looking at devices in operation, and pump-probe approaches.

AMO Semiconductor R&D for Energy Efficiency Series

Workshop 1: Integrated Sensor Systems
January 25-26, 2021

Examined opportunities to improve sensor systems for manufacturing applications

- Discussion sessions focused on:
  - Needs of different supply chain stages
  - Sensing platforms & materials
  - Energy sources & power conditioning
  - Digital and analog circuits & communications
  - Monolithic & hybrid sensor system integration

Workshop 2: Ultra-Precise Control for Ultra-Efficient Devices
April 21-23, 2021

Discussed semiconductor devices and atomically precise manufacturing processes that can enable >1,000x improvements in operational energy efficiency

- Discussion sessions focused on:
  - Ultra-efficient semiconductor devices
  - Ultra-precise manufacturing processes
  - Ultra precise manufacturing tools and metrology

Workshop 3: Analog & Neuromorphic Hardware
August 11-13, 2021

Will cover analog and neuromorphic computing approaches and devices that can enable efficiency and speed improvements in areas of sensing, communication, and ML.

- Discussion sessions will focus on:
  - Needs and impacts on system developers
  - Analog computing for sensor data
  - Analog computing for communications
  - Neuromorphic Devices