SAND2017-7491PE

Copper Electrodeposition in Mesoscale Through-Silicon-Vias

Unique 3D Integration Applications for SOI Substrates

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Presentation Outline

Unique Application

- Ion Trap Basics
- Wire Bond Issues
- TSVs in Ion Traps
- Cu TSV ECD Electrical Connection & Isolation

Conformal Copper TSV Filling

- Wetting Issues
- ECD Basics
- Fill Profile Requirements
- Chemical Analysis
- CEAC Mechanism Scalability

Bottom-Up Filling Technique

- Fundamentals
- Parameter Modification Optimization
- Ion Trap TSV Application
- Plating Approach
- Transition to MSA

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RF (or Paul) Ion Trap Basics

- A potential well is formed via an oscillating RF electromagnetic field to control ion(s)
- The traps discussed here are operated under cryogenic conditions (3-4 K and ultra-high-vacuum)
- Optical access is required, for cooling lasers to drop the ions into their respective ground states

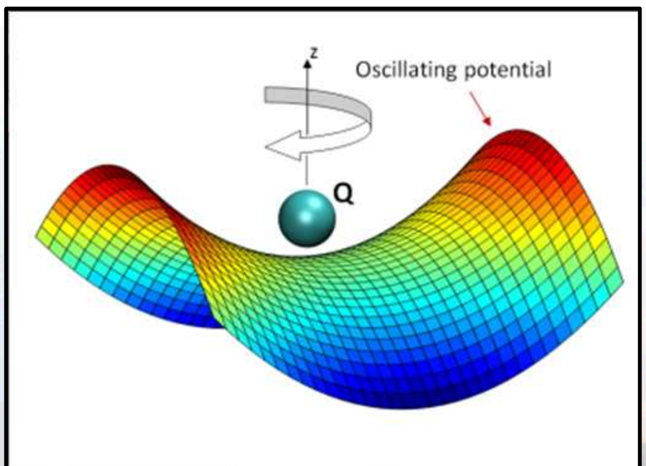
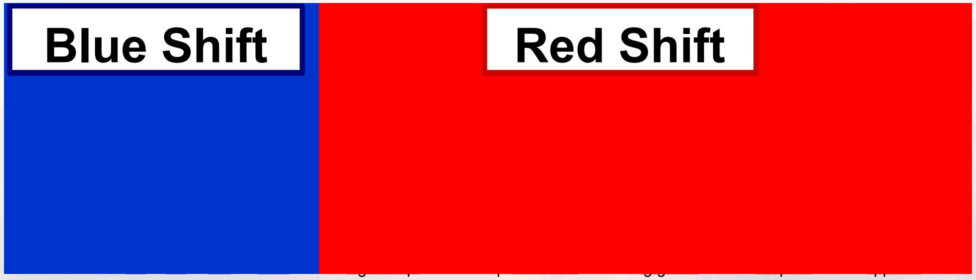


Image Retrieved From: http://www.kurzweilai.net/nanopores-may-lead-to-fast-low-cost-dna-sequencing-device

Doppler Effect



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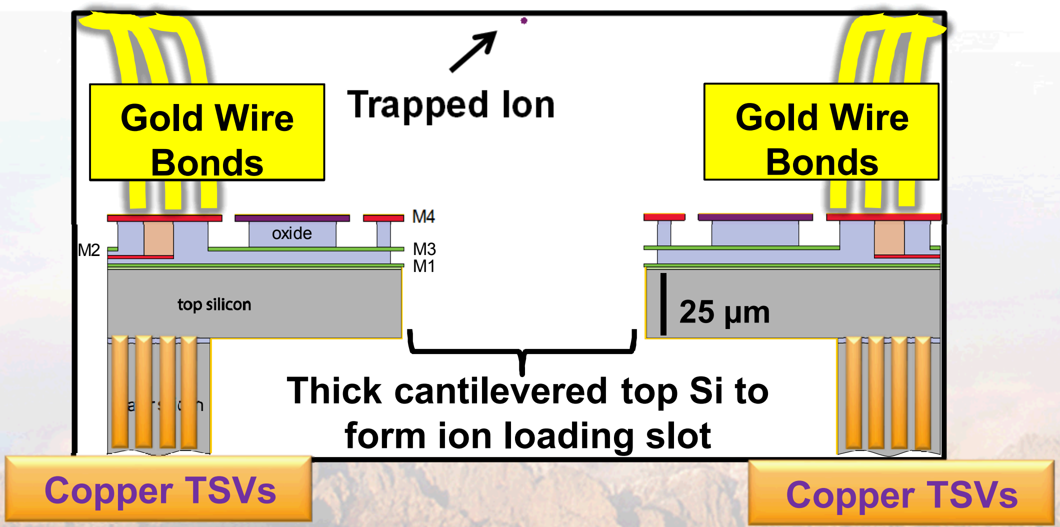
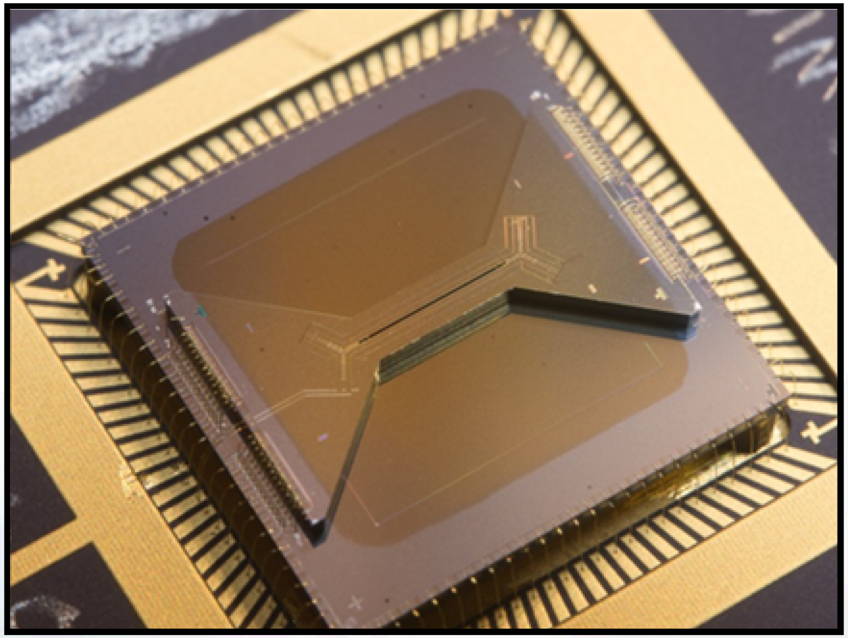
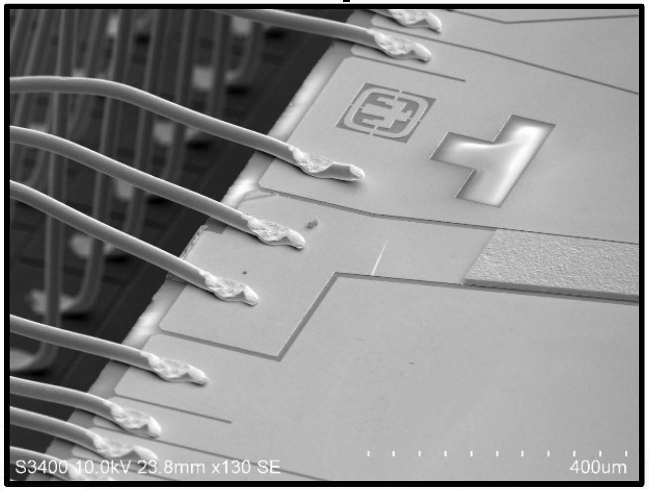


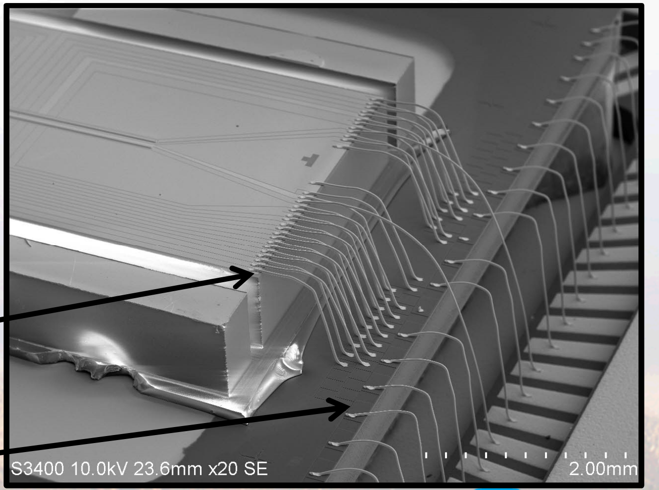
Wire Bonded Paul Trap Examples

"Bowtie" Surface Ion Trap



Two-Level Wire Bond Examples





Gold Wire Bonds to Interposer

Interposer to Ceramic Pin Grid Array Wire Bonds

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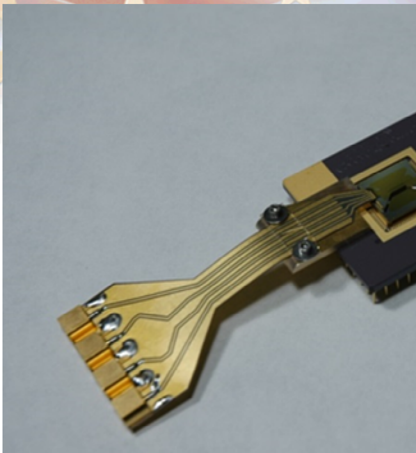
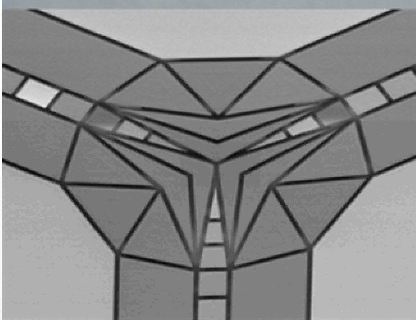
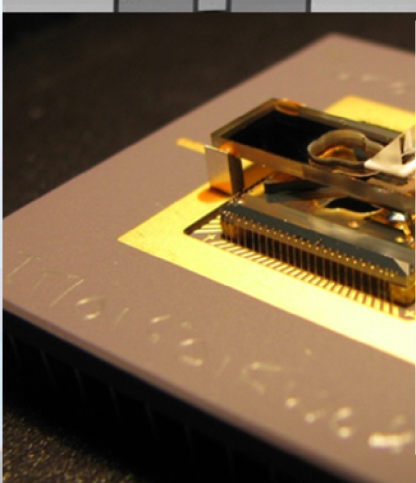
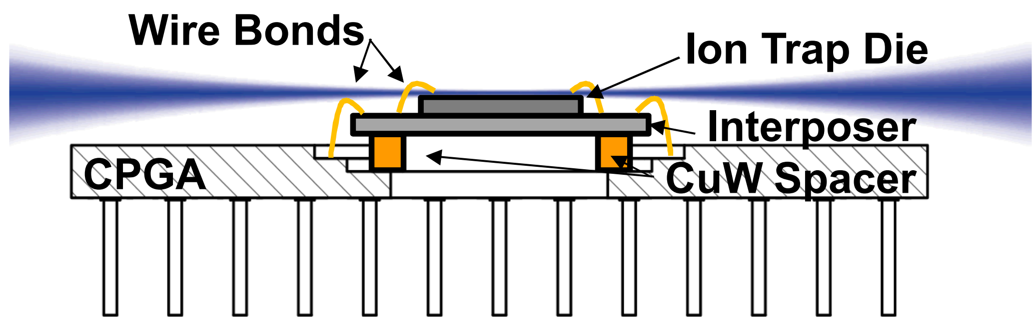
Ion Traps as a Quantum Information Platform

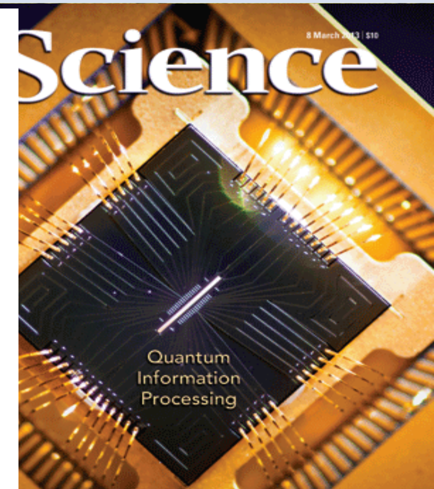


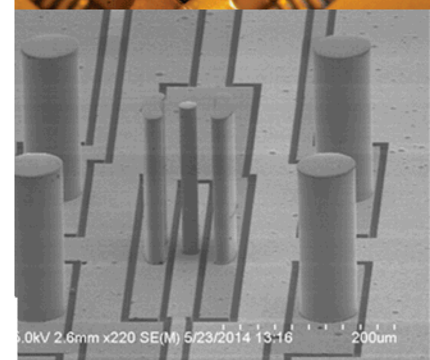


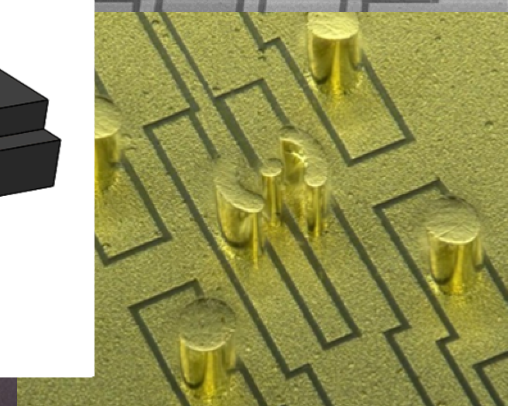




70 µm ion height

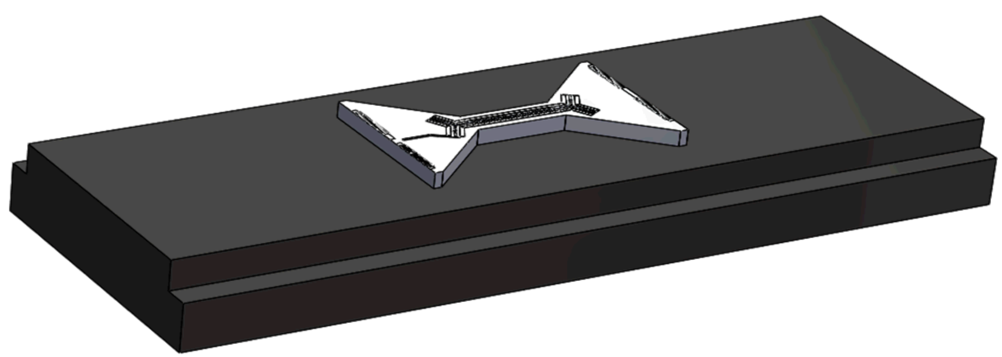


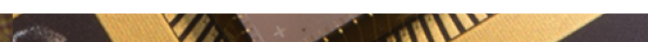




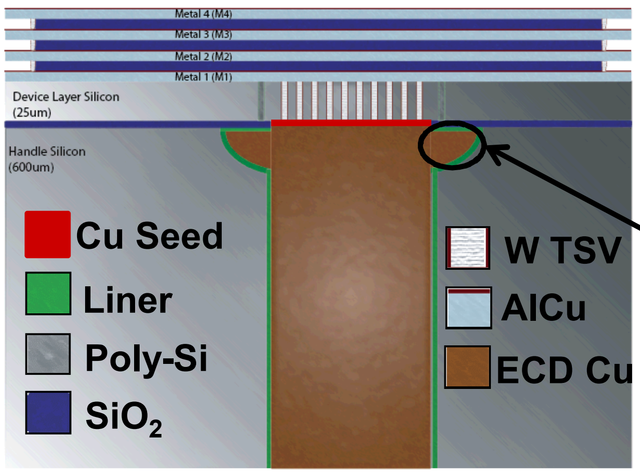
TSVs for Ion Traps

- Improve Optical Access
- Increase I/O per area
- Reduced electrical parasitics for RF and microwave signals
- Improved thermal sinking for cryogenic operation





Hybrid W Via First, Cu Via Last Approach for SOI Substrates



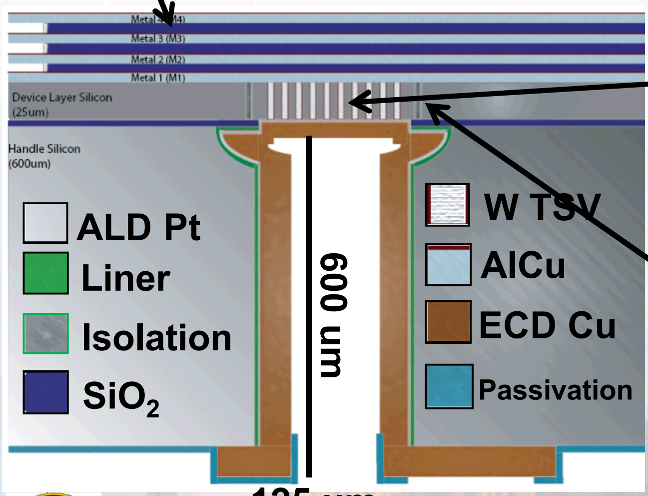
1st Approach: Through mask via fill: plating from evaporated seed metal only at the bottom of the via

- Cu seed metal directional evaporation to contact W implanted vias
- Plating is initiated from Cu seed

A void free fill of the notch will be difficult to achieve

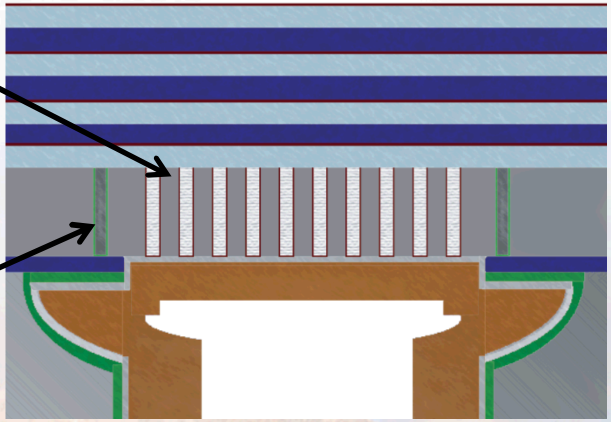
2nd Approach: Conformal via fill: plating from a ALD Pt film, filling the via from the outside in.

Multi-layer routing

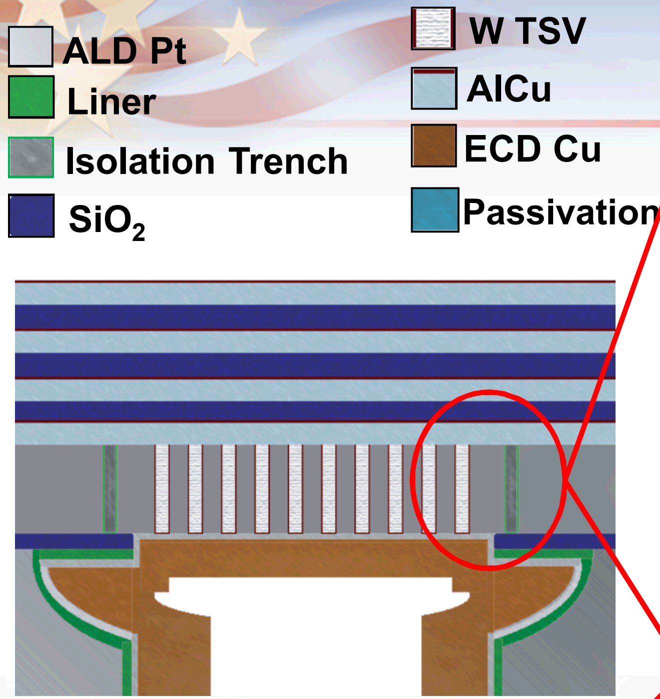


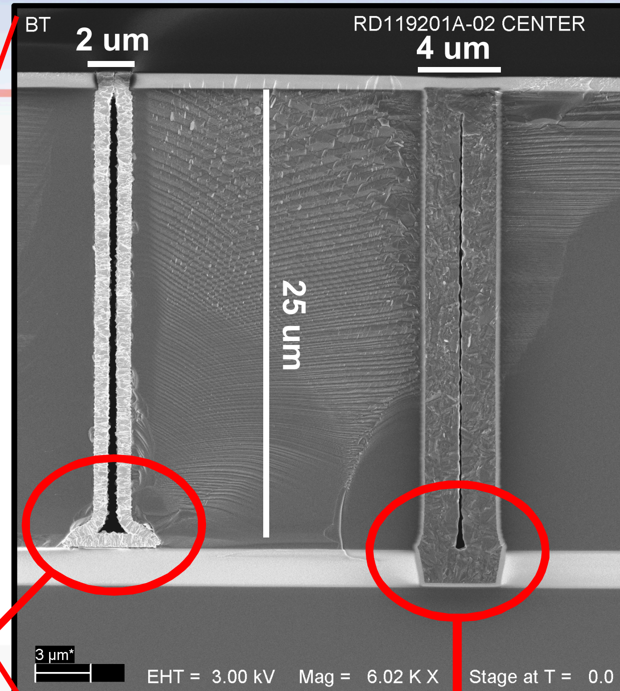
W vias to connect Cu TSV through BOX and top Si layer

Isolation trench to electrically isolate the vias from the device Si layer

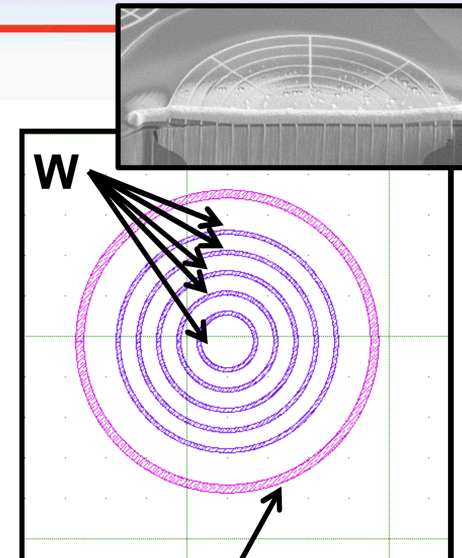


Tungsten Vias and Electrical Isolation



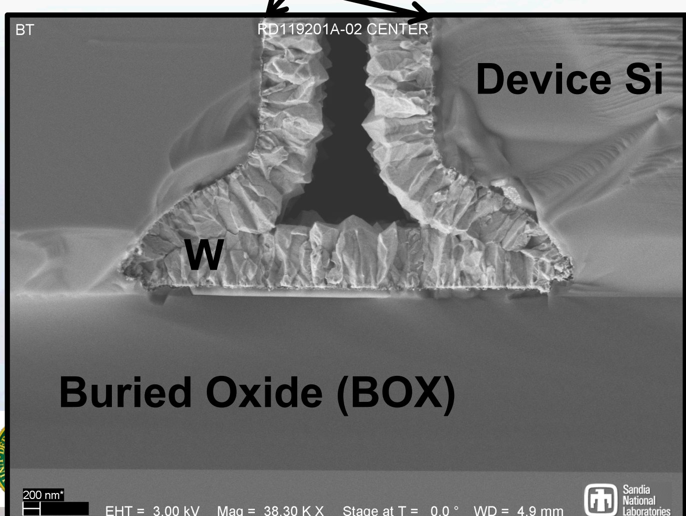


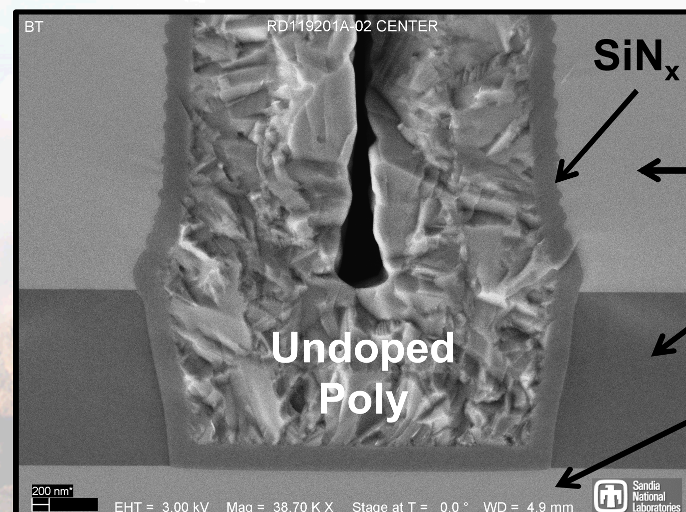
Top Si Layout



Isolation Trench

Degenerately doped Poly Si





Device Si

BOX

Handle Si

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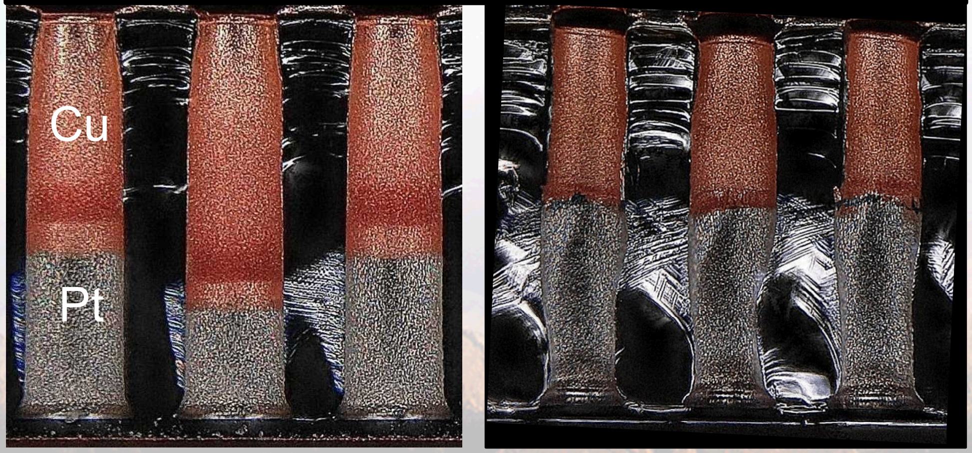
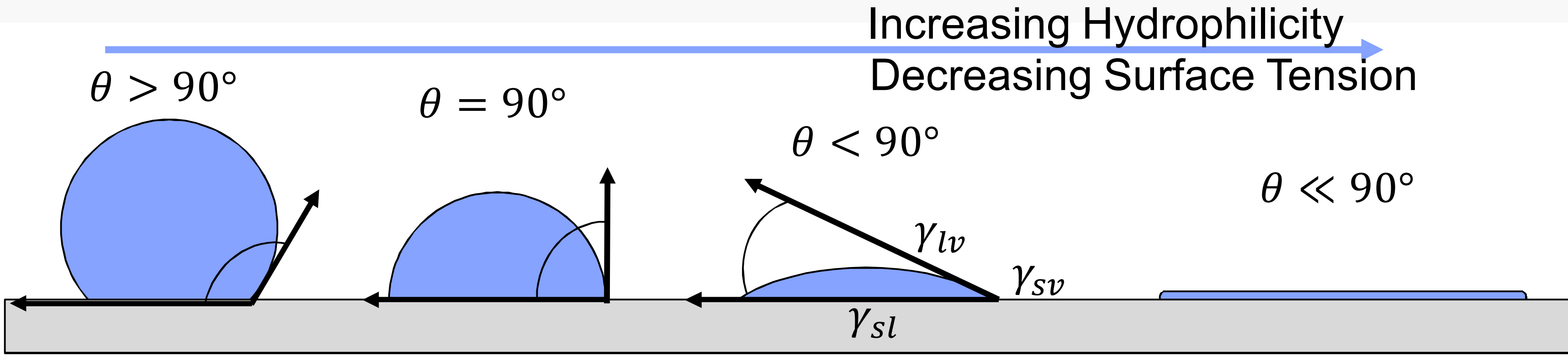
TSV Wetting Issue

- ALD Pt should also be completely hydrophilic, but carbonaceous contamination can yield a hydrophobic surface[2,3]
- Potential solutions for achieving full via wetting:
  a) Improve substrate hydrophilicity through surface preparation (or cleaning) techniques
  b) Pre-wet the vias with some fluid under vacuum or and/or positive pressure and submerge in chemistry

Cleaved Samples with Insufficient Wetting



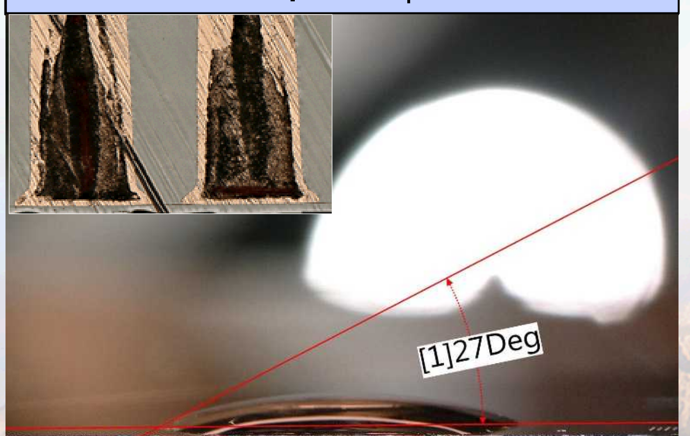
Platinum Substrate Wetting[2,3]



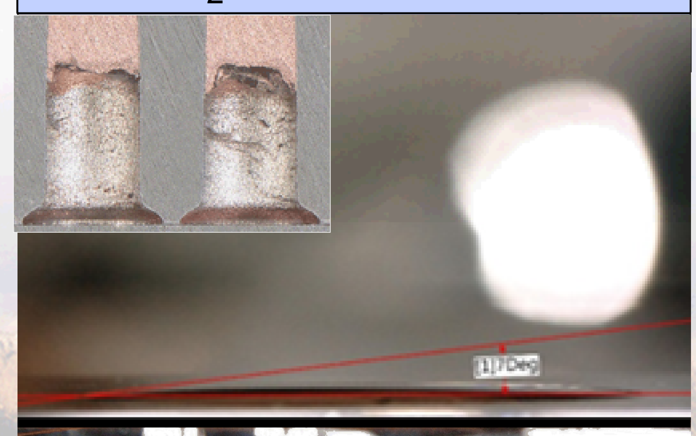
$\gamma_{lv} cos\theta = \gamma_{sv} - \gamma_{sl}$

$\gamma_{lv}, \gamma_{sv}, \gamma_{sl}$ = liquid-vapor, solid-vapor, solid-liquid interfacial tensions

Room Temp NH_4OH Clean



O_2 Plasma Clean



[2]Zhang, Junhong, et al. "Wetting process of copper filling in through silicon vias." *Applied Surface Science* 359 (2015): 736-741.
[3]Yuan, Yuehua, and T. Randall Lee. "Contact angle and wetting properties." *Surface science techniques*. Springer Berlin Heidelberg, 2013. 3-34.

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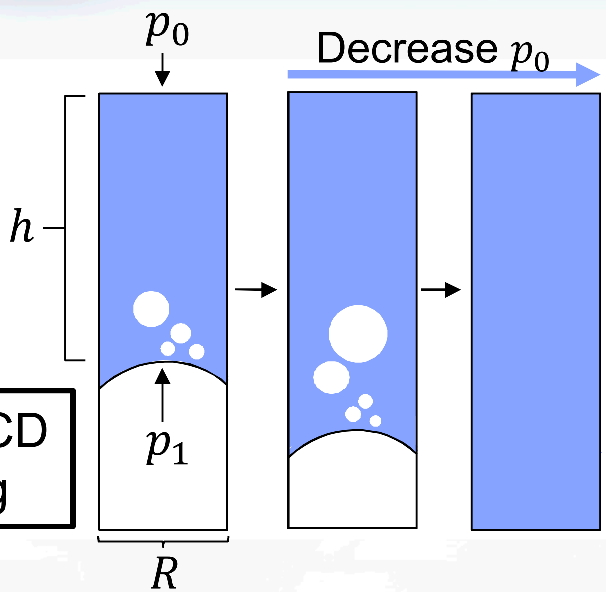
Further Research into TSV Wetting[2]



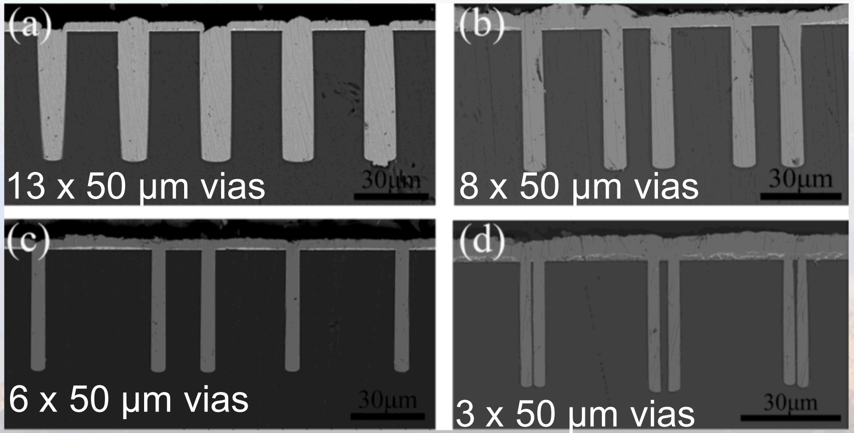
Pre-ECD wetting

$$P_1 = P_0 + \rho g h + \sigma\left[\frac{1}{R} + \frac{1}{R}\right]$$

σ = Surface Tension (Determined using contact angle measurement)

So, $\boldsymbol{P_1 > P_0 + \sigma\left[\frac{1}{R} + \frac{1}{R}\right]}$ **for full wetting to occur (this can be accomplished by decreasing external pressure or fluid temperature)[4]**

After Pre-Wet in DI Water at 0°C, 17.3 torr[2]



After Pre-Wet in EtOH at 22°C, 10^{-3} torr

[2]Zhang, Junhong, et al. "Wetting process of copper filling in through silicon vias." *Applied Surface Science* 359 (2015): 736-741.

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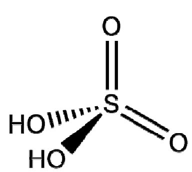
Copper Electrodeposition Basics

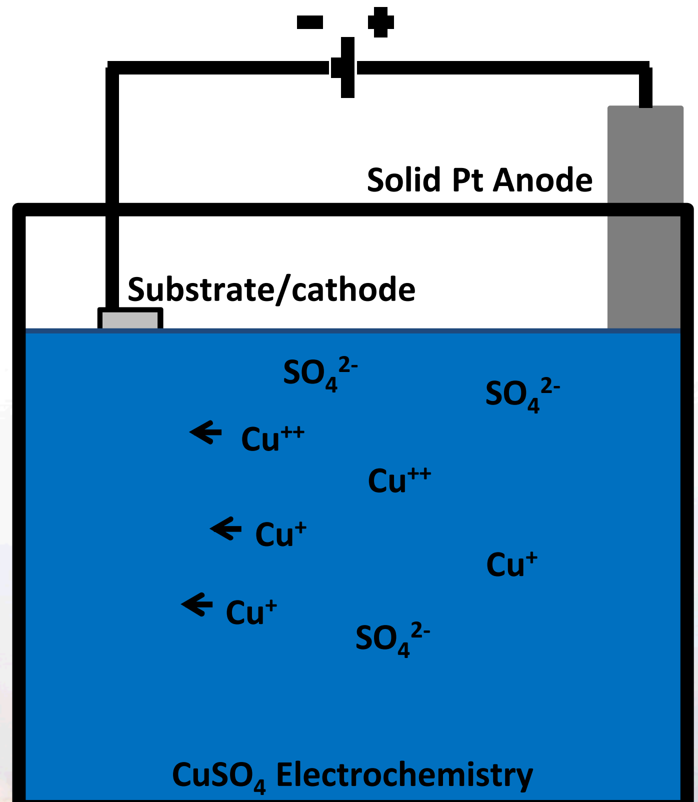
Additive-free Acid Sulfate Copper Electrolyte			
Constituent	**Form**	**Concentration**	**Purpose**
Copper Sulfate Pentahydrate	Solid (salt)	1-1.3 mol/L	Metal ion source
Sulfuric Acid Or Methane Sulfonic Acid (MSA)	Liquid	0.25-1 mol/L	Cu reduction & bath stability aid
Sodium Chloride Or Hydrochloric Acid	Liquid	50-100 mg/L	Complexing agent for additives

Copper Sulfate Pentahydrate



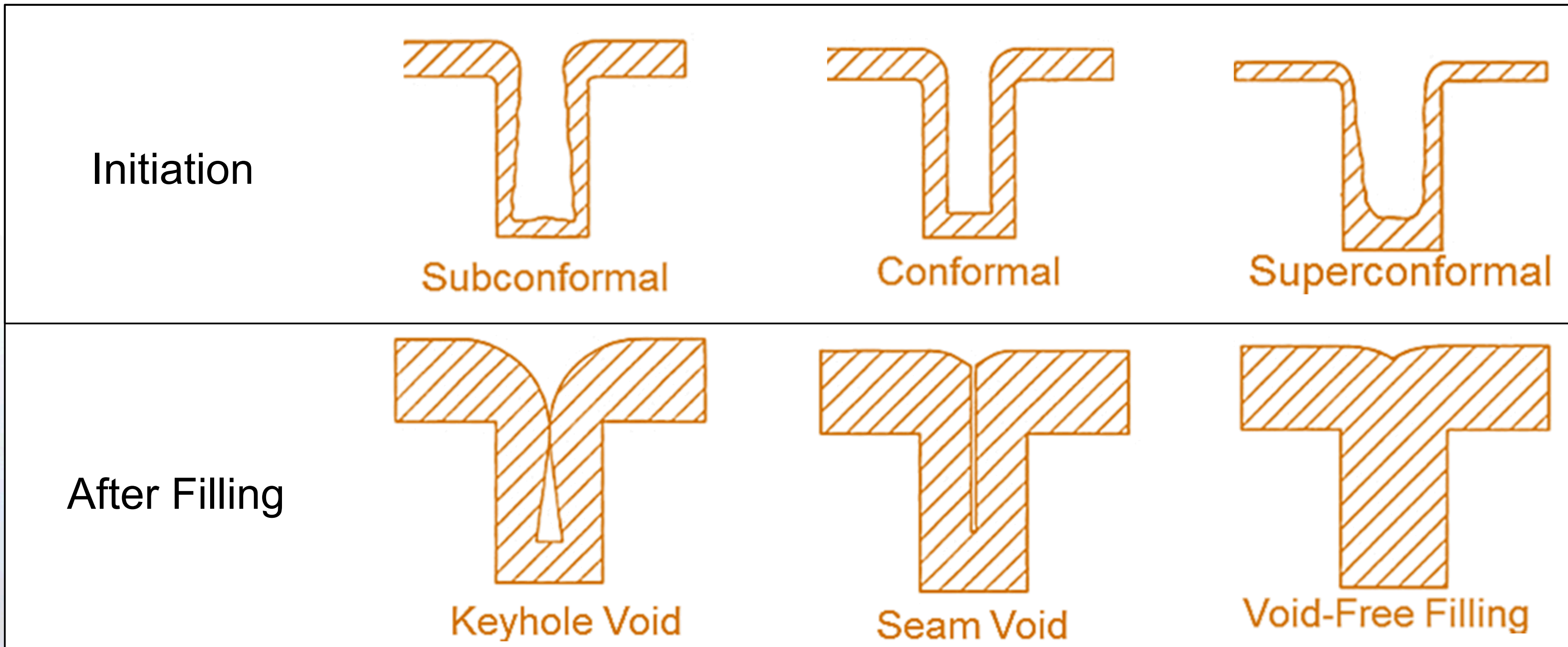
H_2SO_4 or MSA

- Prevents Cu from reacting with oxygen
- Allows for an energetically favorable Cu reduction
- Improves film quality
- Improves bath stability



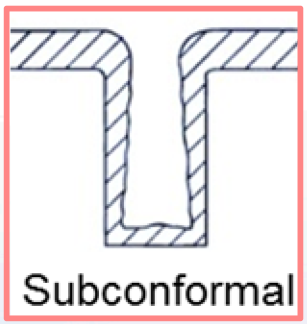
Growth Front Importance in TSVs

- Any void formation is problematic for these features due to the environment they operate at (ultra high vacuum, low temperature)
- Voids can also trap wet chemistry, leading to device degradation over time

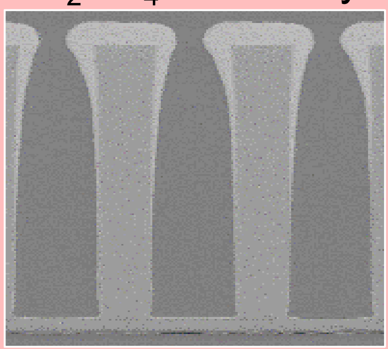


Copper Concentration Analysis

- Methanesulfonic acid (MSA) and sulfuric acid (H_2SO_4) electrolytes have been widely researched for TSV filling[4,5].
- Higher solubility of Cu in MSA as compared to H_2SO_4 suggests that MSA is the optimal electrolyte for the purpose of filling these TSVs.



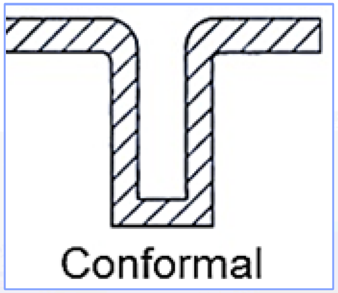
Proprietary (Low Cu)
H_2SO_4 Chemistry



60 g/L Cu

MSA Electrolyte

80 g/L Cu



- More Cu ions available in each via decreases mass transport limited depletion of Cu, leading to increased plating conformality.

[4]Cho, Sung Ki, Myung Jun Kim, and Jae Jeong Kim. "MSA as a supporting electrolyte in copper electroplating for filling of damascene trenches and through silicon vias." *Electrochemical and Solid-State Letters* 14.5 (2011): D52-D56.
[5]Moffat, T. P., and D. Josell. "Extreme bottom-up superfilling of through-silicon-vias by damascene processing: suppressor disruption, positive feedback and turing patterns." *Journal of The Electrochemical Society* 159.4 (2012): D208-D216.
[6]Sun, Jian-Jun, et al. "High-aspect-ratio copper via filling used for three-dimensional chip stacking." *Journal of The Electrochemical Society* 150.6 (2003): G355-G358.

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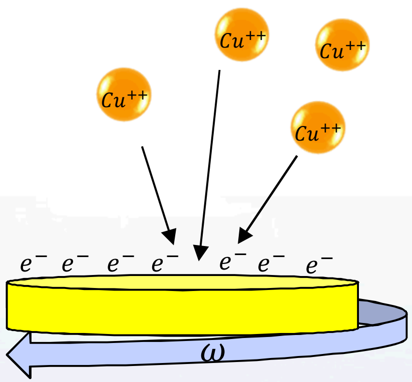
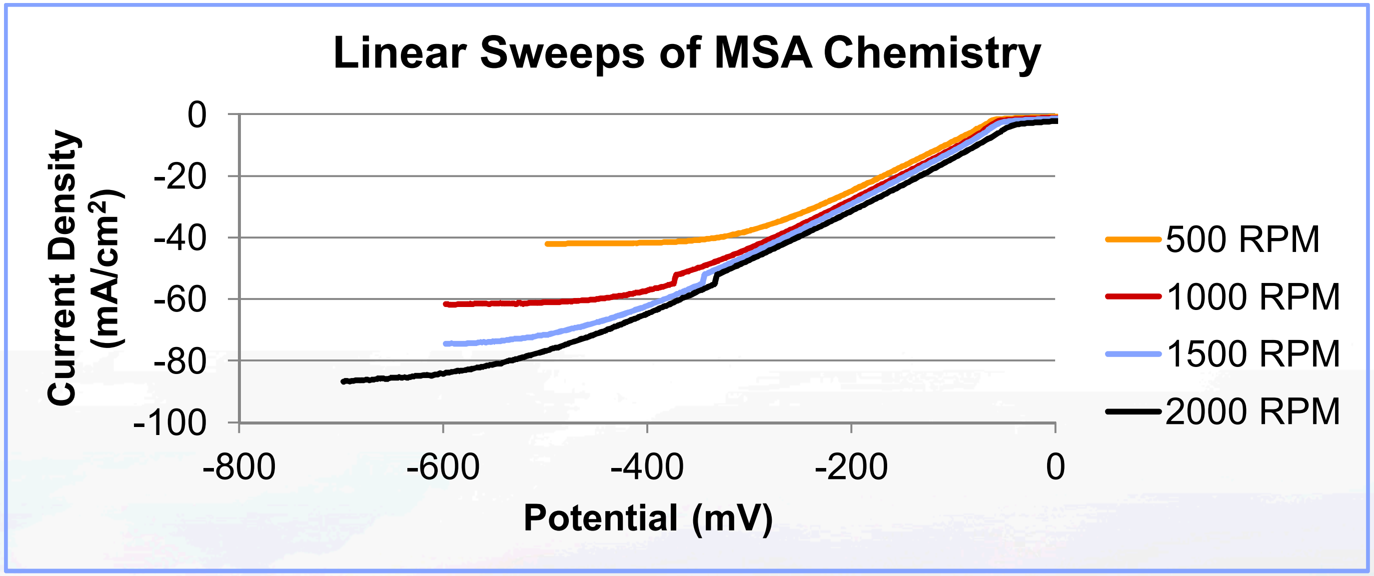
Plating Parameter/Diffusion Coefficient Study

- A linear voltammetric study was performed using a gold (Au) rotating disk electrode (RDE) to determine the diffusion coefficient of Cu ions in the MSA electrolyte.

Rotating Disk Electrode (RDE)



Diffusion Layer Thickness $(\delta_f) \propto \omega^{-1/2}$



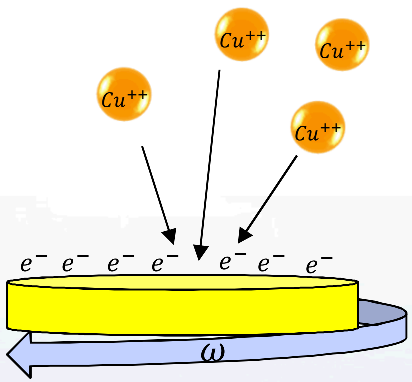
$$I_L = 0.62nFAD^{\frac{2}{3}}\omega^{\frac{1}{2}}\nu^{\frac{-1}{6}}C$$

Experimentally Determined D_{Cu}	Roha, D. Et. Al. Provided D_{Cu}[13]	Chuan Seng Tan, K.-N. C. Provided D_{Cu}[14]
985 µm²/sec	**800 µm²/sec**	**1000 µm²/sec**

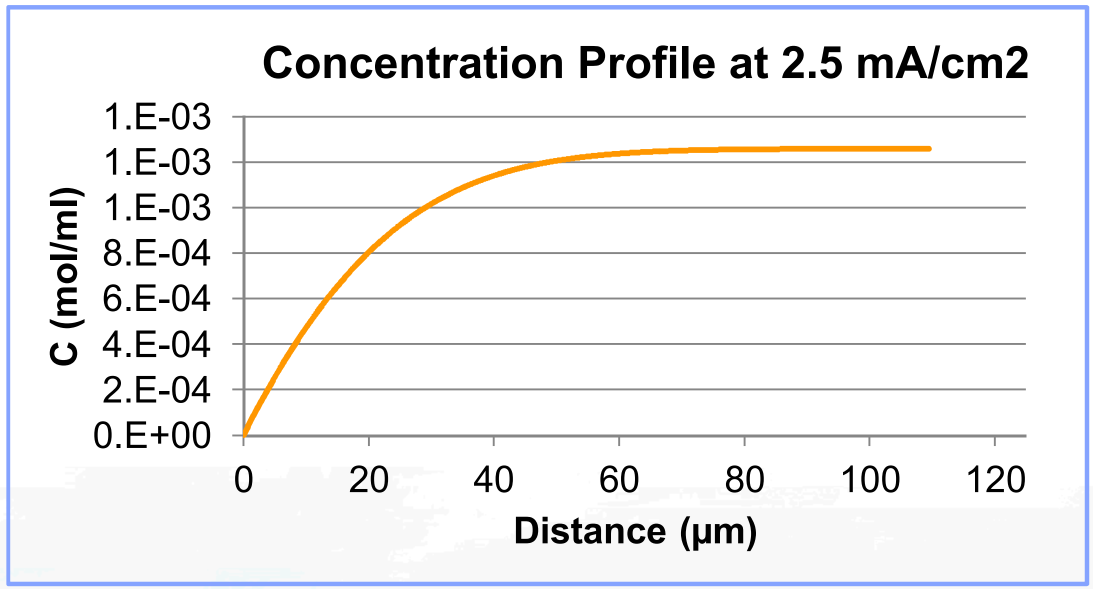
7. Alvanos, T., et al., *A Novel Methodology for Wafer-Specific Feed-Forward Management of Backside Silicon Removal by Wafer Grinding for Optimized Through Silicon Via Reveal.* 2014 Ieee 64th Electronic Components and Technology Conference (Ectc), 2014: p. 452-458.
8. Huang, B.K., et al., *Integration Challenges of TSV Backside Via Reveal Process.* 2013 Ieee 63rd Electronic Components and Technology Conference (Ectc), 2013: p. 915-917.

Plating Parameter/Diffusion Coefficient Study

Rotating Disk Electrode (RDE)



Diffusion Layer Thickness (δ_f) $\propto \omega^{-1/2}$



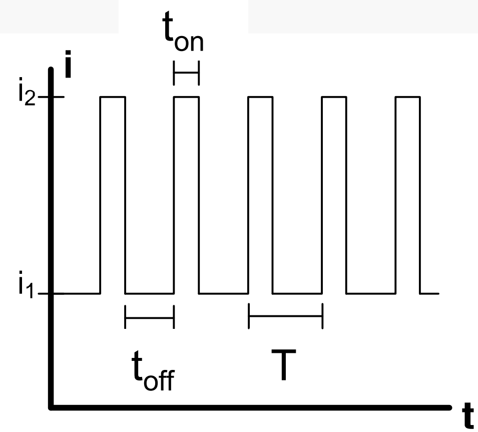
$$C(x,t) = C^* - \frac{i}{nFAD}\left\{2\left(\frac{Dt}{\pi}\right)^{\frac{1}{2}} exp\left(-\frac{x^2}{4Dt}\right) - x\, erfc\left[\frac{x}{2(Dt)^{\frac{1}{2}}}\right]\right\}$$

Cu Diffusion Time for Replenishment in TSV Bottom = 1.6 sec
Applied Potential on Time for Cu Depletion = 0.105 sec

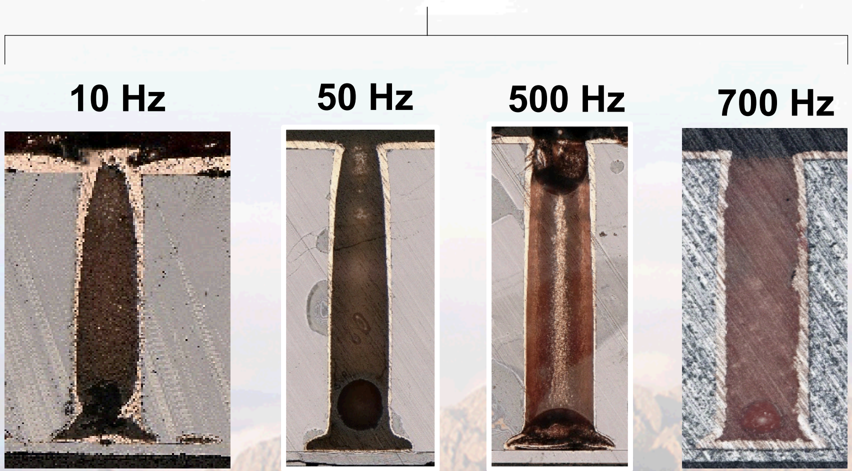
$$\frac{\boldsymbol{On\ Time}}{\boldsymbol{Off\ Time}} = \frac{\mathbf{105}}{\mathbf{1600}} = \mathbf{6.6\%}\ \boldsymbol{Duty\ Cycle}$$

Frequency/Duty Cycle Optimization

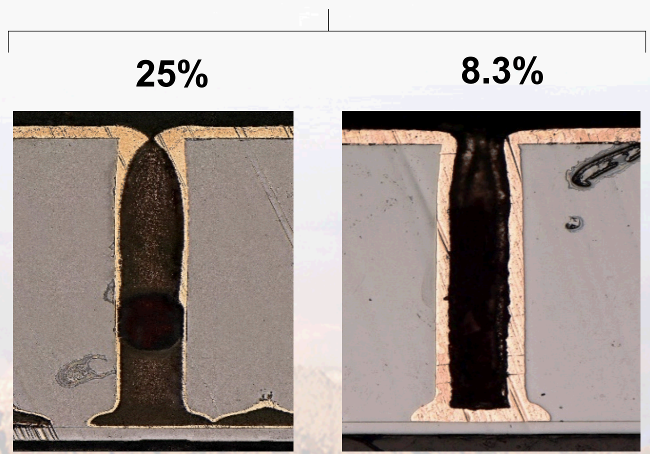
- Pulse plating can mitigate copper depletion issues down the features as “off” time allows for Cu replenishment
- Using pulse plating will require a longer fill time



Frequency Comparison at 50% Duty Cycle



Duty Cycle Comparison at 700 Hz



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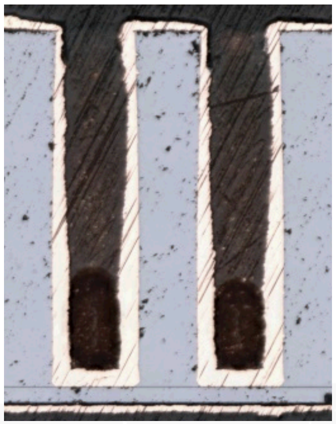
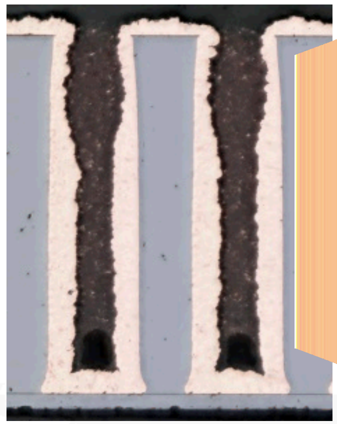
Further Process Optimization

Current Density Comparison

5 mA/cm^2

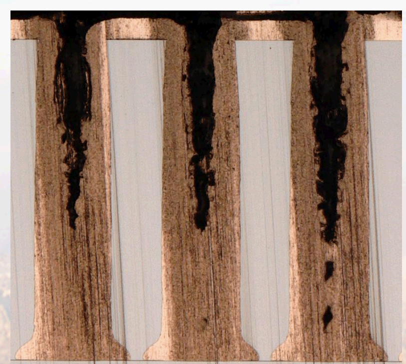


2.5 mA/cm^2



Large grains lead to void formation

Seam/Keyhole voids



Void formation ultimately occurs even after optimizing conditions:

High Cu concentration, 2.5 mA/cm^2, 700 Hz, 8.3% Duty Cycle

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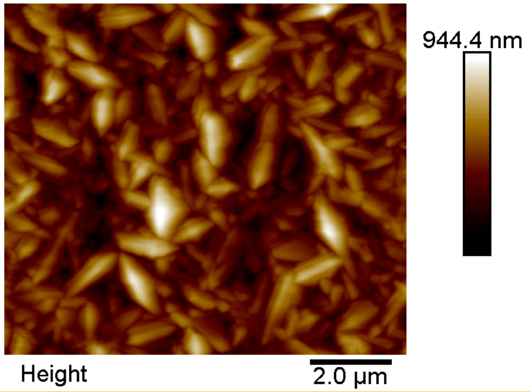
Effect of Additives on Planar Substrates

Optical and Atomic Force Microscopy

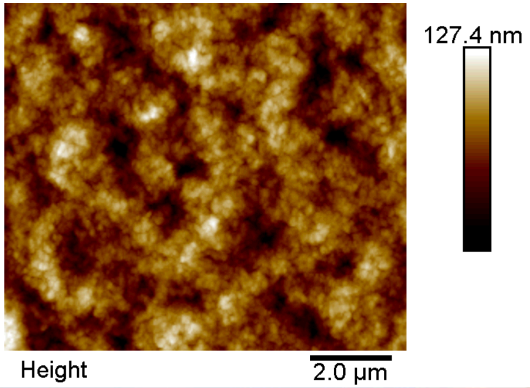
No Additives

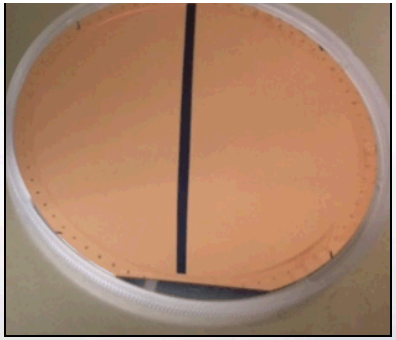


RMS Roughness
134 nm

Uniformity (Center to Edge)
8% - 100%

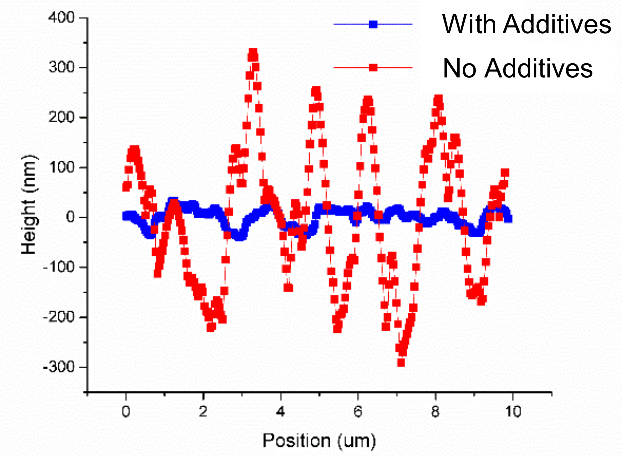
With Cu Additives – Leveler, Accelerator, & Suppressor





RMS Roughness
18 nm

Uniformity (Center to Edge)
< 5%



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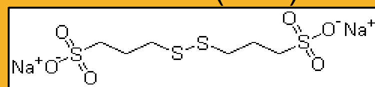
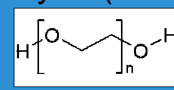
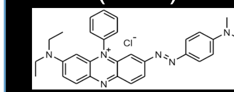
Feature Filling Profiles and Additives

Common Additives to Achieve Void-Free Fill Profile

Accelerator bis-(sodium sulfopropyl)-disulfide (SPS)	Suppressor Polyethylene Glycol (PEG)	Leveler Janus Green B (JGB)	HCl Or NaCl
			

- Accelerator – Surfactant molecule that adsorbs on the surface and, by coverage increase with area loss, preferentially increases plating rate in concave regions
- Suppressor - Large chain polymer (1k-20k mW) whose gradient of concentration yields an associated gradient in deposition rate (slower higher in via)
- Leveler - Disables accelerator to reduce overburden thickness; grain refiner
- Chloride – Competitively complexes with suppressor and accelerator species at electrode surface; required for suppressor function

[7] Moffat, Thomas P., et al. "Superconformal film growth: Mechanism and quantification." *IBM Journal of Research and Development* 49.1 (2005): 19-36.

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Curvature Enhanced Adsorbate Coverage[7,8,9]

- More strongly adsorbed molecules (accelerator) agglomerate on concave surfaces during Cu growth by[7,8]:

$$\frac{d\theta}{dt} = k_{ads}(1-\theta_{SPS})C_{SPS} - k_{inc}\theta^{q} + \boxed{\nu\kappa\theta_{SPS}}$$

Where,

$k_{ads} \equiv SPS\ Adsorption\ Rate\ Const.$

$\theta_{SPS} \equiv SPS\ Surface\ Coverage$

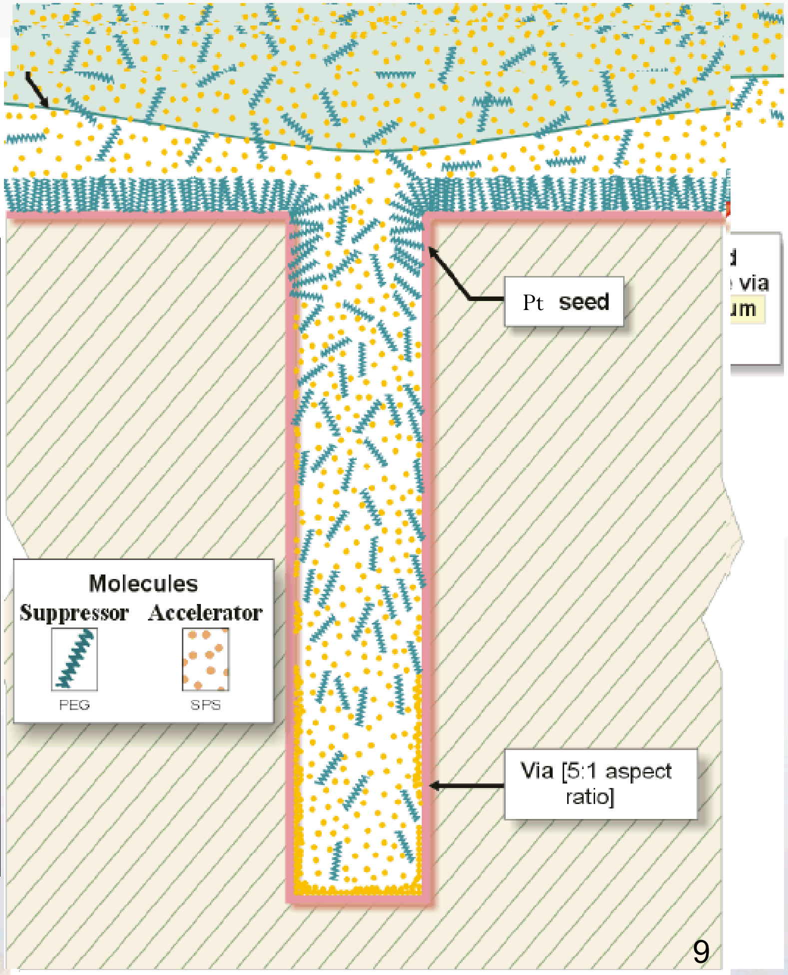
$C_{SPS} \equiv SPS\ Concentration$

$k_{inc} \equiv SPS\ Incorporation\ Rate\ Const.$

$q \equiv Reaction\ Order$

$\nu \equiv Interface\ Velocity$

$\kappa \equiv Local\ Curvature$



[7] Moffat, Thomas P., et al. "Superconformal film growth: Mechanism and quantification." *IBM Journal of Research and Development* 49.1 (2005): 19-36.
[8] Moffat, T. P., et al. "Curvature enhanced adsorbate coverage model for electrodeposition." *Journal of The Electrochemical Society* 153.2 (2006): C127-C132.
[9] Keigler, A., et al. “Sematech 3D Equipment Challenges: 300mm Copper Plating.” *NEXX Systems (2008).*

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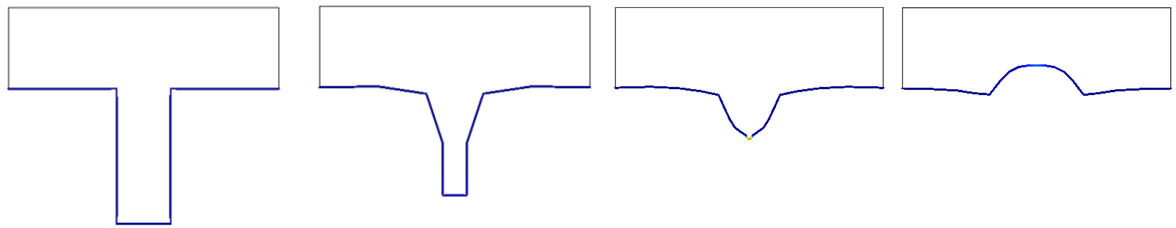
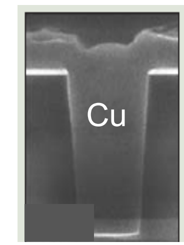
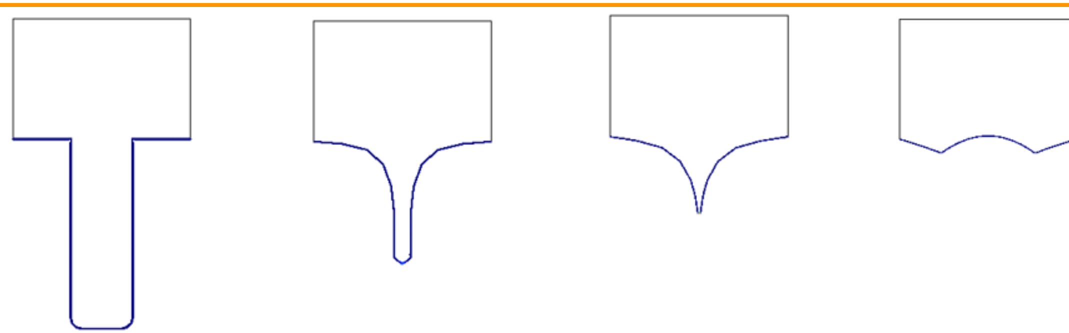
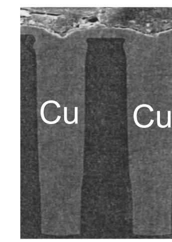
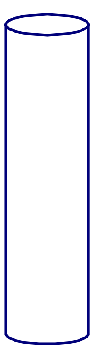
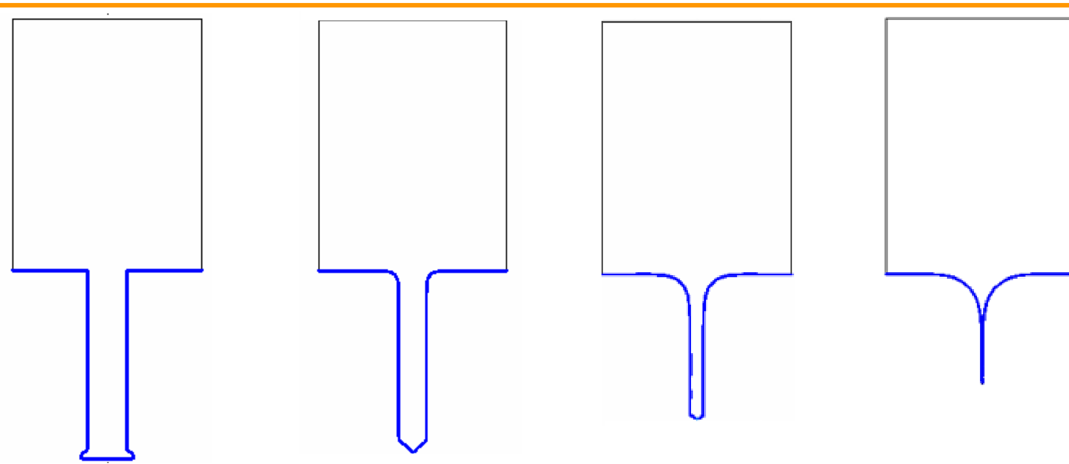
CEAC Mechanism Scaling

COMSOL Modeling

Scale		Modeled Growth Front Tracking (t_1, t_2, t_3, t_{fill})	Experimental Results[6,7]
.	0.5 x 3.25 µm TSV		
	10 x 70 µm TSV		
	Ion Trap 125 x 600 µm TSV		

[7] Moffat, Thomas P., et al. "Superconformal film growth: Mechanism and quantification." *IBM Journal of Research and Development* 49.1 (2005): 19-36.

Presentation Outline

Unique Application	Conformal Copper TSV Filling	Bottom-Up Filling Technique
• Ion Trap Basics • Wire Bond Issues • TSVs in Ion Traps • Cu TSV ECD Electrical Connection & Isolation	• ECD Basics • Wetting Issues • Fill Profile Requirements • Chemical Analysis • CEAC Mechanism Scalability	• Fundamentals • Parameter Modification Optimization • Ion Trap TSV Application • Plating Approach • Transition to MSA

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Alternative Approach to TSV Filling

S-Shaped Negative Differential Resistance (S-NDR) Approach[10]

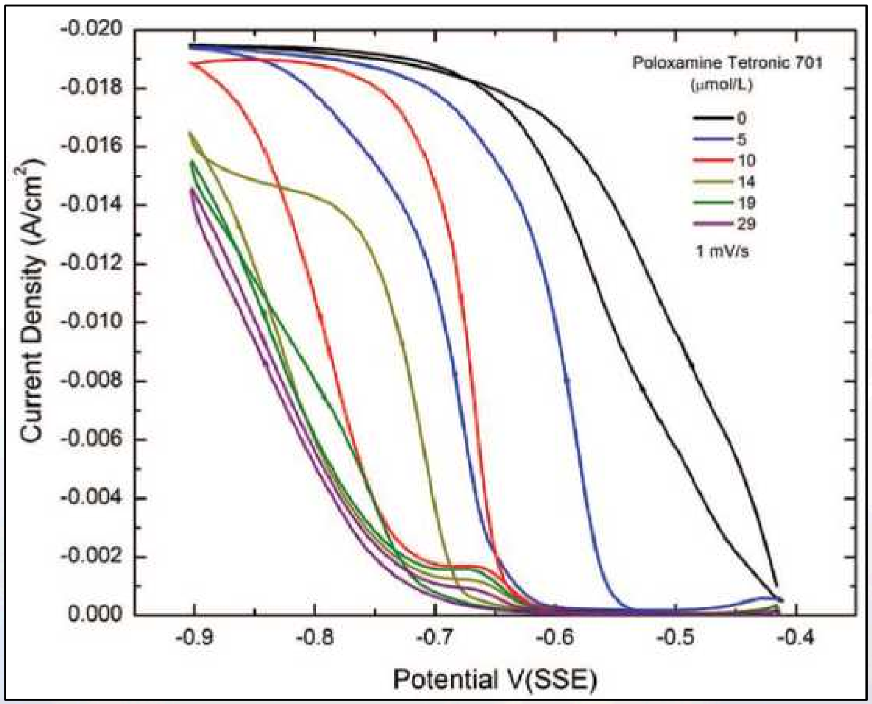
- Single suppressor additive system
- Bottom-up growth mode even with conformal seed metal

Seeded TSV

[10] Moffat, T. P., and D. Josell. "Extreme bottom-up superfilling of through-silicon-vias by damascene processing: suppressor disruption, positive feedback and turing patterns." *Journal of The Electrochemical Society* 159.4 (2012): D208-D216.

S-NDR Research[10]

- Hysteresis represents breakdown of suppressor blocking layer
- This hysteresis causes 'Turing Patterns' on planar electrodes



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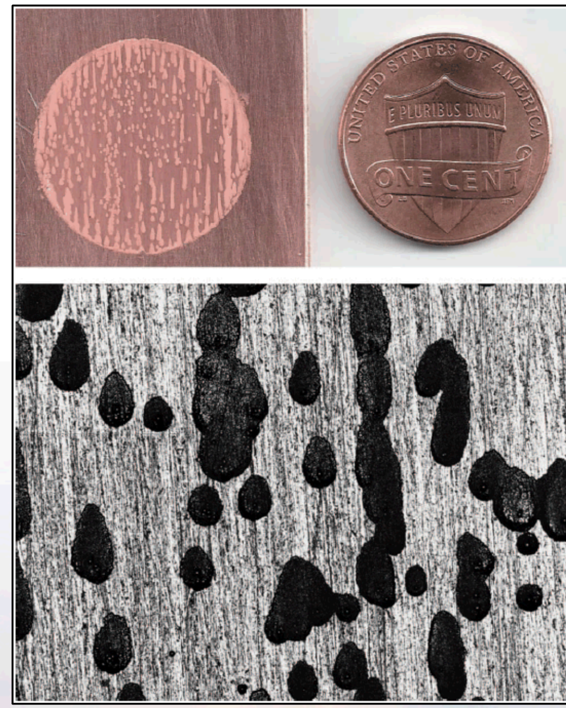

[10] Moffat, T. P., and D. Josell. "Extreme bottom-up superfilling of through-silicon-vias by damascene processing: suppressor disruption, positive feedback and turing patterns." *Journal of The Electrochemical Society* 159.4 (2012): D208-D216.

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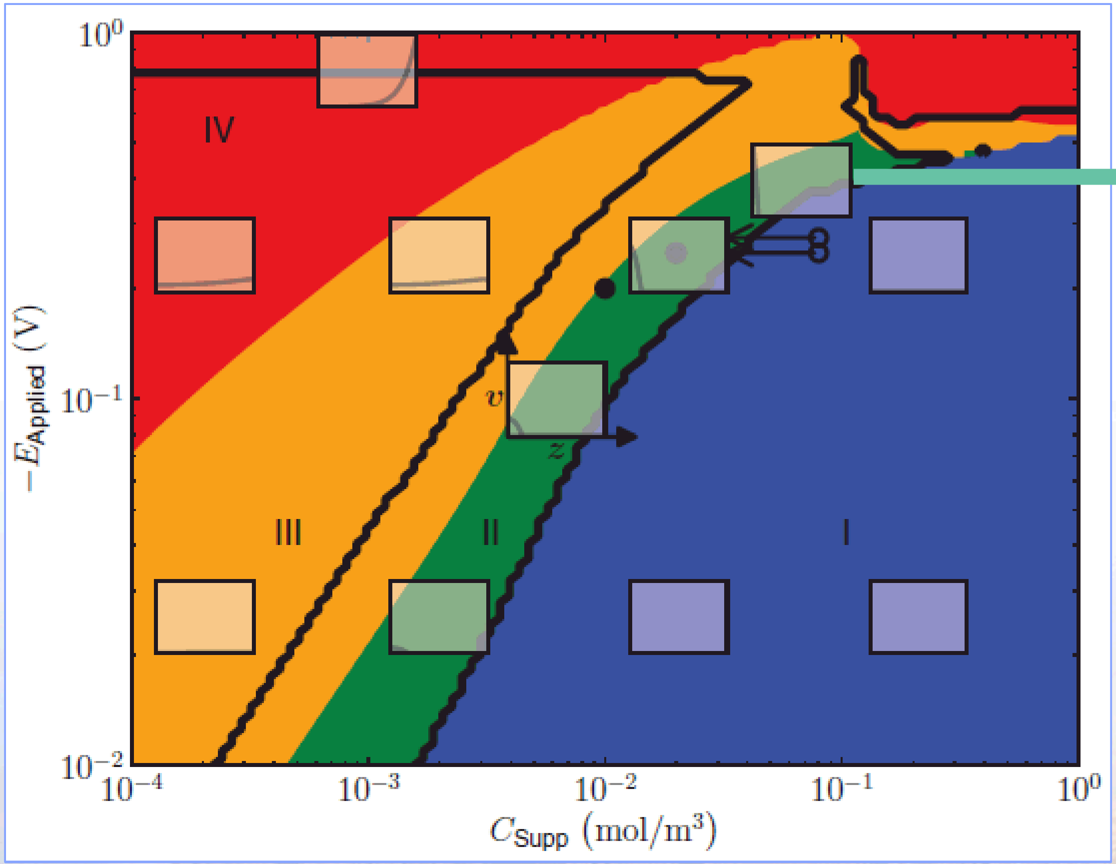
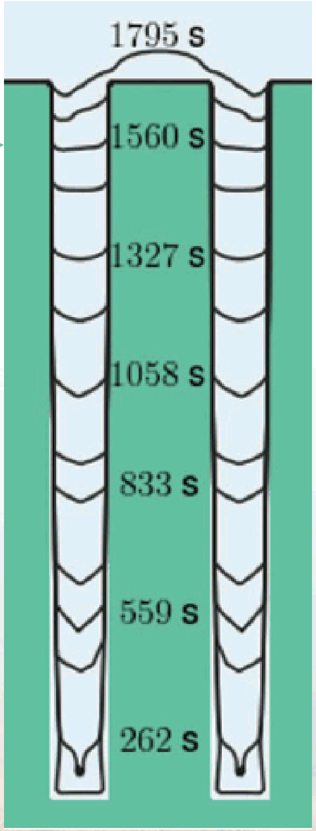
S-NDR Technique Fundamentals[11,12]

- **Suppressor concentration and applied potential are two key parameters**



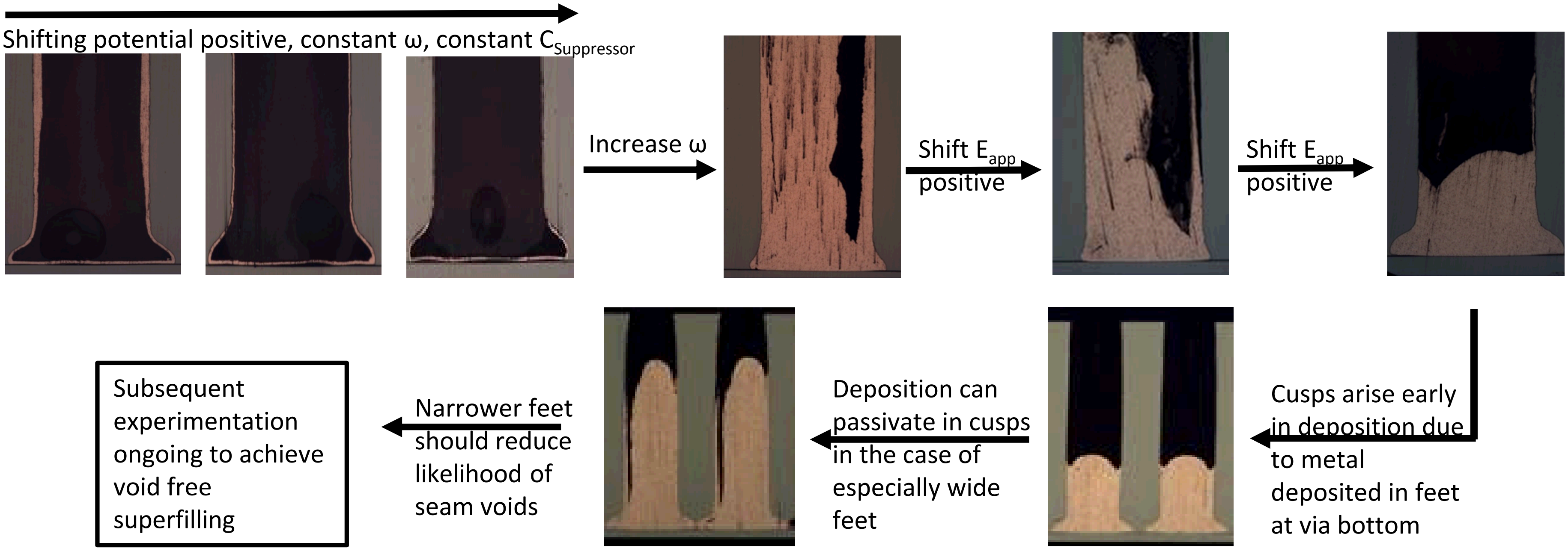
$C_{Supp} = 0.06 \frac{mol}{m^3}$,
$E_{App} = -0.45\ V$



[11] Josell, D., D. Wheeler, and T. P. Moffat. "Modeling extreme bottom-up filling of through silicon vias." *Journal of The Electrochemical Society* 159.10 (2012): D570-D576.
[12] Wheeler, D., T. P. Moffat, and D. Josell. "Spatial-temporal modeling of extreme bottom-up filling of through-silicon-vias." *Journal of The Electrochemical Society* 160.12 (2013): D3260-D3265.

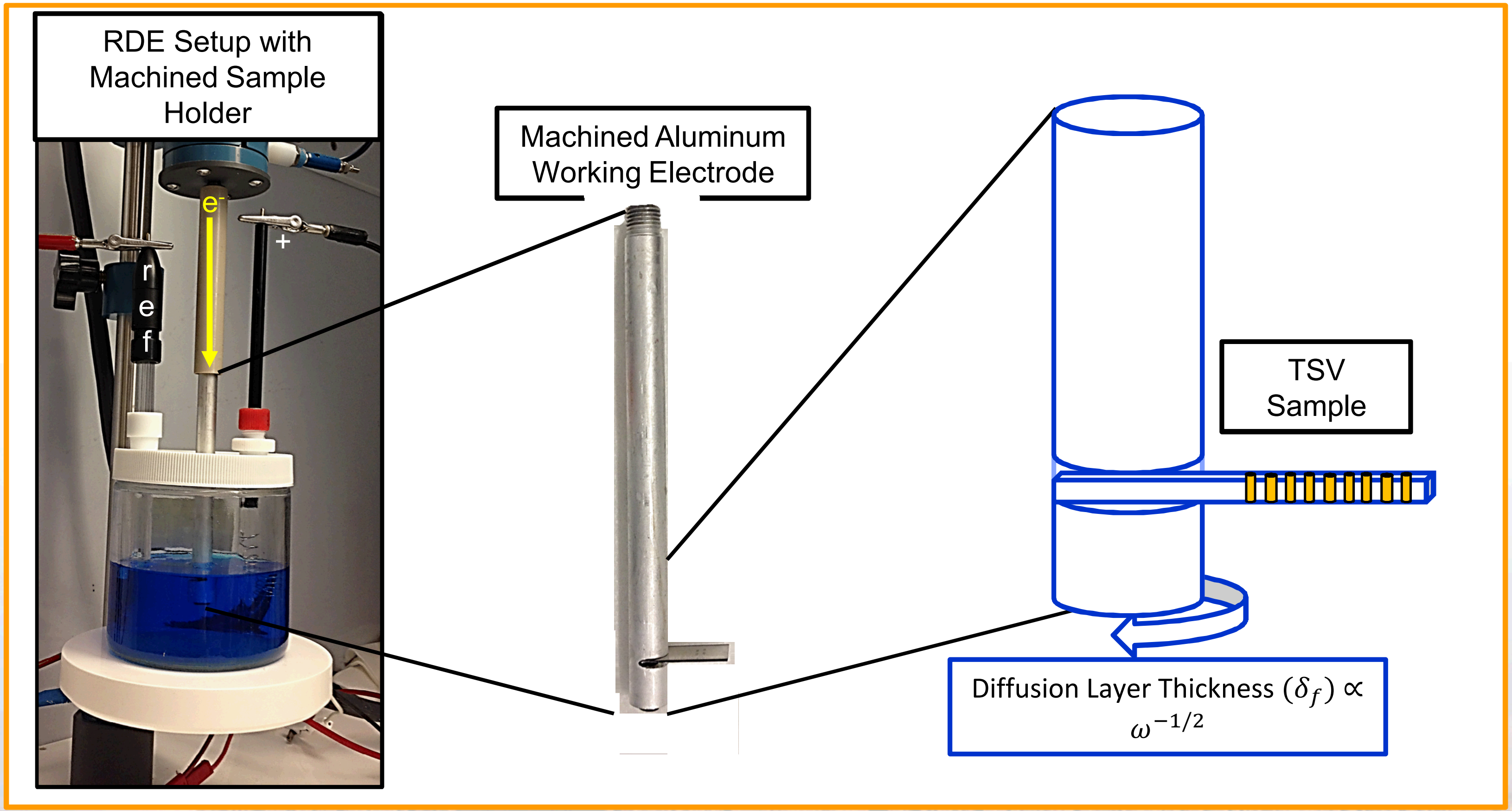
S-NDR Approach on Ion Trap TSVs

Three key variables manipulated: Applied potential, electrolyte fluid flow, and suppressor concentration

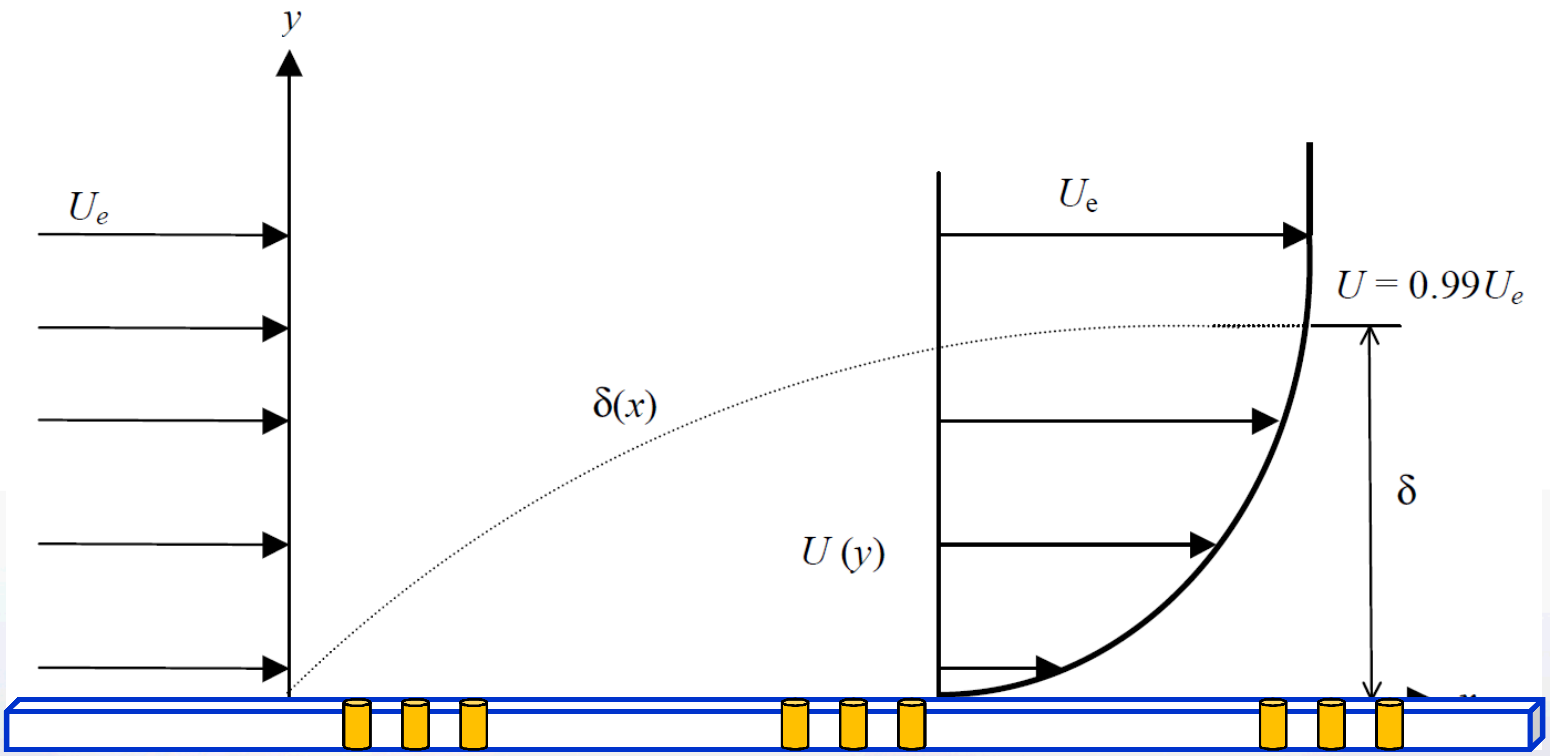


$$\text{Diffusion Layer Thickness} \propto \omega^{-1/2} = \delta_f = 1.61\,(D_f)^{1/3}\nu^{1/6}\omega^{-1/2}$$

S-NDR Plating Setup



Boundary Layer Thickness Above Rotating Planar Substrate



Fluid Velocity (u)

$$u = 2\pi r \omega_{cyc}$$

*Boundary Layer Thickness (**δ**)*

$$\delta = \sqrt{\frac{\nu x}{u}}$$

$$\delta_{avg} = \frac{1}{x}\sqrt{\frac{\nu}{u}}\int_0^x \sqrt{x}dx$$

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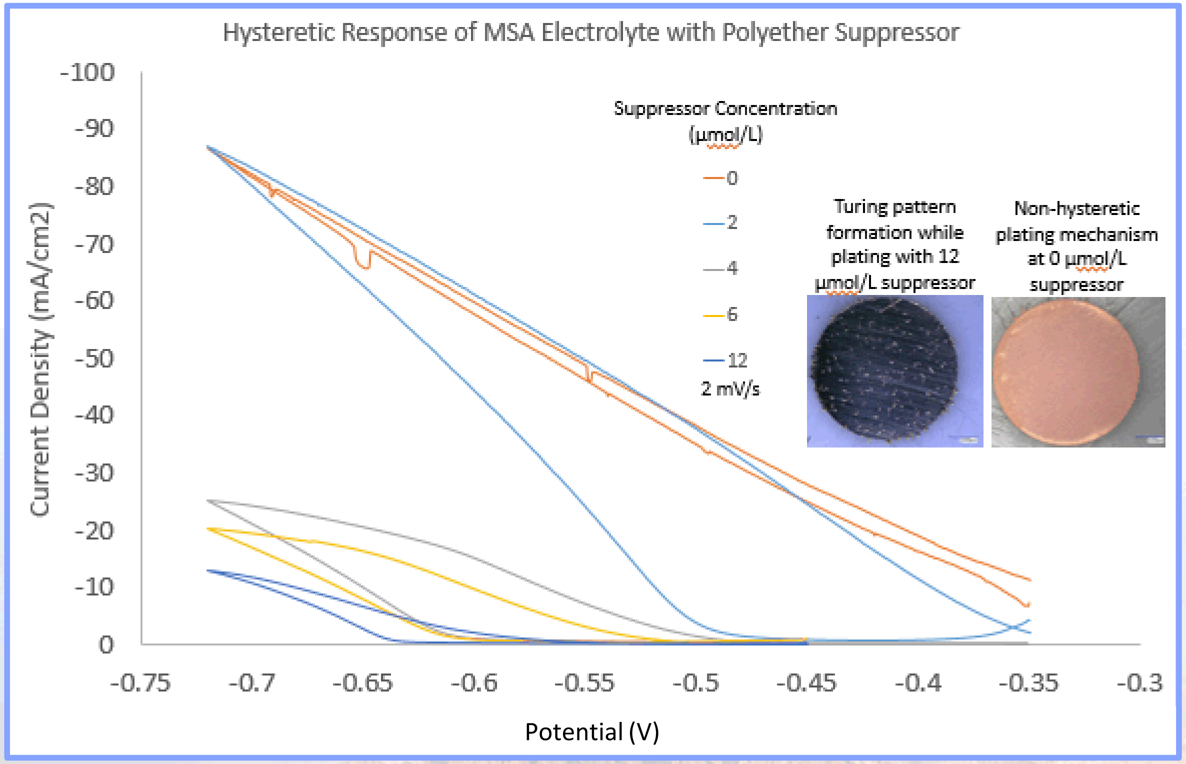
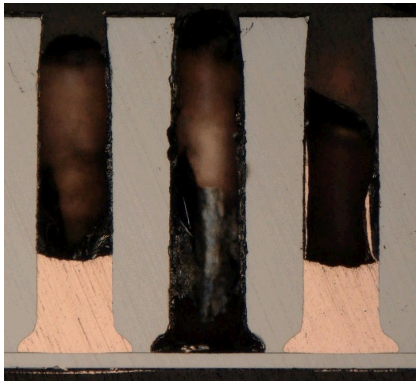
S-NDR Results with MSA Electrolyte

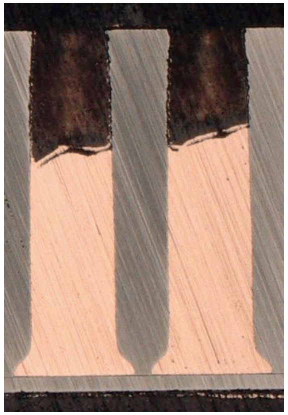
- S-NDR mechanism can likely be applied to high Cu, MSA electrolyte to increase plating rate



R8, -0.6 V (SSE), 2 hr, 400 rpm



R11, -0.6 V (SSE), 4.5 hr, 400 rpm



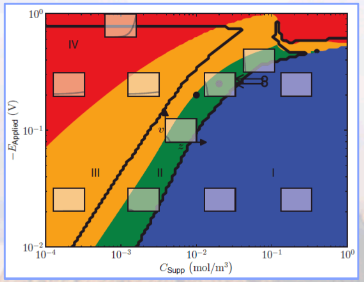
Summary

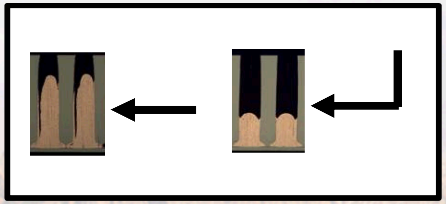
Established:

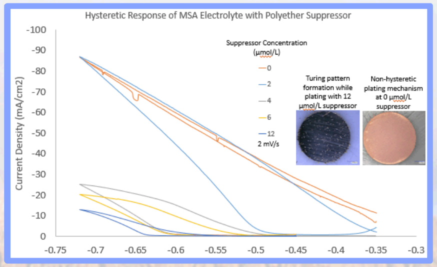
- TSV wetting procedure
- MSA as electrolyte for sufficient conformal jacketing
- Traditional additive system deficiencies

Future Work:

- Examine alternative TSV wetting procedures
- Continue replicating S-NDR approach with H_2SO_4 electrolyte
- Develop S-NDR process with MSA electrolyte







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