Ultrathin ferroic HfO_2–ZrO_2 superlattice gate stack for advanced transistors

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With the scaling of lateral dimensions in advanced transistors, an increased gate capacitance is desirable both to retain the control of the gate electrode over the channel and to reduce the operating voltage[1]. This led to a fundamental change in the gate stack in 2008, the incorporation of high-dielectric-constant HfO_2 (ref. [2]), which remains the material of choice to date. Here we report HfO_2–ZrO_2 superlattice heterostructures as a gate stack, stabilized with mixed ferroelectric–antiferroelectric order, directly integrated onto Si transistors, and scaled down to approximately 20 ångströms, the same gate oxide thickness required for high-performance transistors. The overall equivalent oxide thickness in metal–oxide–semiconductor capacitors is equivalent to an effective SiO_2 thickness of approximately 6.5 ångströms. Such a low effective oxide thickness and the resulting large capacitance cannot be achieved in conventional HfO_2-based high-dielectric-constant gate stacks without scavenging the interfacial SiO_2, which has adverse effects on the electron transport and gate leakage current[3]. Accordingly, our gate stacks, which do not require such scavenging, provide substantially lower leakage current and no mobility degradation. This work demonstrates that ultrathin ferroic HfO_2–ZrO_2 multilayers, stabilized with competing ferroelectric–antiferroelectric order in the two-nanometre-thickness regime, provide a path towards advanced gate oxide stacks in electronic devices beyond conventional HfO_2-based high-dielectric-constant materials.

With the two-dimensional scaling of silicon field-effect transistors reaching fundamental limits[1], new functional improvements to transistors[4], as well as novel computing paradigms and vertical device integration at the architecture level[5], are currently under intense investigation[1,4,6]. Gate oxides have a critical role in this endeavour as a common performance booster for all transistor devices based on a wide range of materials, including silicon[2], new high-performance channel materials[7,8], and even materials suitable for three-dimensional integrated transistors[9,10]. Indeed, the gate oxide transition from SiO_2 to high-κ dielectrics is considered a paradigm shift in computing technology (κ, dielectric constant). In this context, ferroelectric (FE) oxides offer new functionalities[11] that are considered promising for energy-efficient electronics[4,9]. The advent of atomic layer deposition (ALD)-grown doped-HfO_2 FE films[12] has overcome much of the material compatibility issues that plague traditional perovskite-based FE materials[2]. In addition, ferroic order persists down to a thickness of 1 nm in this system[13–15], fostering integration into the most aggressively scaled devices in which the state-of-the-art high-κ oxide thickness is less than 2 nm.

In an advanced silicon transistor, the gate oxide is a combination of two distinct layers. The first is an interfacial SiO_2 formed with a

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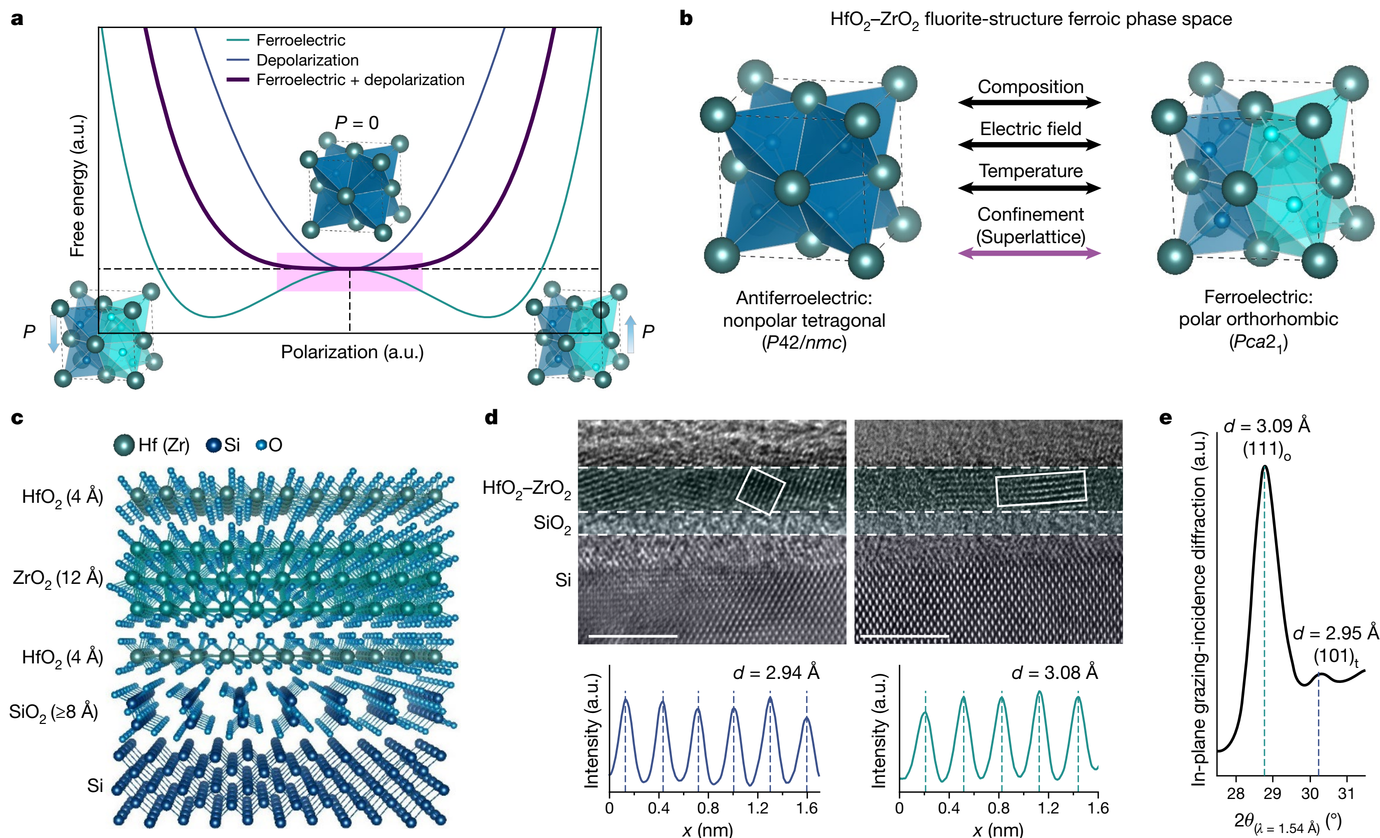

Fig. 1 | Atomic-scale design of negative capacitance in ultrathin HfO_2–ZrO_2. **a**, Energy landscape flattening. An FE double-well energy landscape is flattened by the depolarization field energies originating from electrostatic and elastic inhomogeneities present in the laterally arranged polar–nonpolar (orthorhombic FE–tetragonal AFE) thin-film system. The energy landscape flattening increases the permittivity of the overall system, as susceptibility is proportional to the inverse landscape curvature; such flattening is analogous to negative capacitance stabilization[29,30,49]. The stable energy minimum of the composite free-energy landscape, corresponding to the negative curvature (that is, negative capacitance) regime of the ferroelectric energy landscape, is highlighted in pink. **b**, Engineering ferroic phase competition in the HfO_2–ZrO_2 fluorite-structure system. Beyond the conventionally studied tuning parameters—composition, electric field, temperature[32,38]—here we introduce dimensional confinement via superlattice layering to tailor ferroic phase competition at the atomic scale. **c**, Schematic of the HZH fluorite-structure multilayer on Si; the heterostructures maintain distinct layers (that is, not solid-solution alloys) based on EELS, XRR and depth-resolved XPS (Extended Data Fig. 1). The role of the layering on the underlying ferroic order and capacitance is studied by electrical measurements as a function of HfO_2–ZrO_2 stacking structure and annealing temperature (Extended Data Figs. 4 and 5, respectively). **d**, High-resolution TEM images of the atomic-scale HZH trilayer (top) and extracted d-lattice spacings (bottom, determined from the solid white box regions) corresponding to the fluorite-structure AFE tetragonal ($P4_2/nmc$, left) and FE orthorhombic ($Pca2_1$, right) phases, respectively. The layer delineations are approximate, as the HfO_2–ZrO_2 and SiO_2 interlayer thicknesses are more rigorously determined by XRR and TEM analysis (Extended Data Figs. 1 and 6, respectively). Note that imaging the crystallinity of the HfO_2–ZrO_2 layers requires mistilt with respect to the Si lattice (Methods). Scale bars, 5 nm. **e**, Synchrotron in-plane grazing-incidence diffraction demonstrating the presence of both the AFE T-phase $(101)_t$ and FE O-phase $(111)_o$ reflections, the d-lattice spacings of which are consistent with those extracted from TEM. Detailed indexing for structural identification is provided by wide-angle synchrotron diffraction (Extended Data Fig. 2a). a.u., arbitrary units.

self-limiting process, resulting in approximately 8.0–8.5-Å thickness[16]. The next is the high-κ (HK) dielectric HfO_2 layer that is typically approximately 2 nm in thickness. Higher capacitance of this series combination is desirable to suppress short channel effects. The capacitance is conventionally represented by equivalent oxide thickness, $EOT = t_{SiO_2} + t_{HK}/(\varepsilon_{HK}/\varepsilon_{SiO_2})$, where lower EOT represents higher capacitance. Therefore, the EOT minimum value is limited by the interfacial SiO_2 thickness. Typically, with HfO_2 as the high-κ layer, the EOT is approximately 9.5 Å. To go below this value[17,18], the semiconductor industry has implemented sophisticated scavenging techniques[16,18,19] to reduce the SiO_2 thickness after the full gate stack has been deposited. Although this technique is effective in scaling EOT, the thinner SiO_2 results in undesirable leakage[20], mobility degradation[2,16] and reliability issues.

In this work, we present an ultrathin HfO_2–ZrO_2 superlattice gate stack that exploits mixed ferroelectric–antiferroelectric (FE–AFE) order (Fig. 1a, b), stabilized down to 2-nm thickness—the same high-κ oxide thickness used in advanced transistors. When integrated on silicon, the gate stack shows an overall EOT of 6.5 Å, even though both transmission electron microscopy (TEM) and electrical characterization reveal an 8.0–8.5 Å interfacial SiO_2 thickness, as is typically expected from a chemically grown interfacial layer without scavenging. No scavenging of the interfacial SiO_2 results in substantially lower leakage current for the same EOT compared to benchmarks established by major semiconductor industries[3]. In addition, no mobility degradation is observed as EOT is scaled with these HfO_2–ZrO_2 ferroic gate stacks. Therefore, ultrathin HfO_2–ZrO_2 gate stacks exploiting ferroic order offer a promising pathway towards advanced energy-efficient transistors.

Ultrathin FE–AFE HfO_2–ZrO_2 superlattices

Thin films of HfO_2–ZrO_2 are grown using ALD, in which the nanolaminate periodicity is dictated by the sequence of Hf:Zr (4:12) ALD cycles before the Hf–Zr superstructure is repeated various times (Fig. 1c,

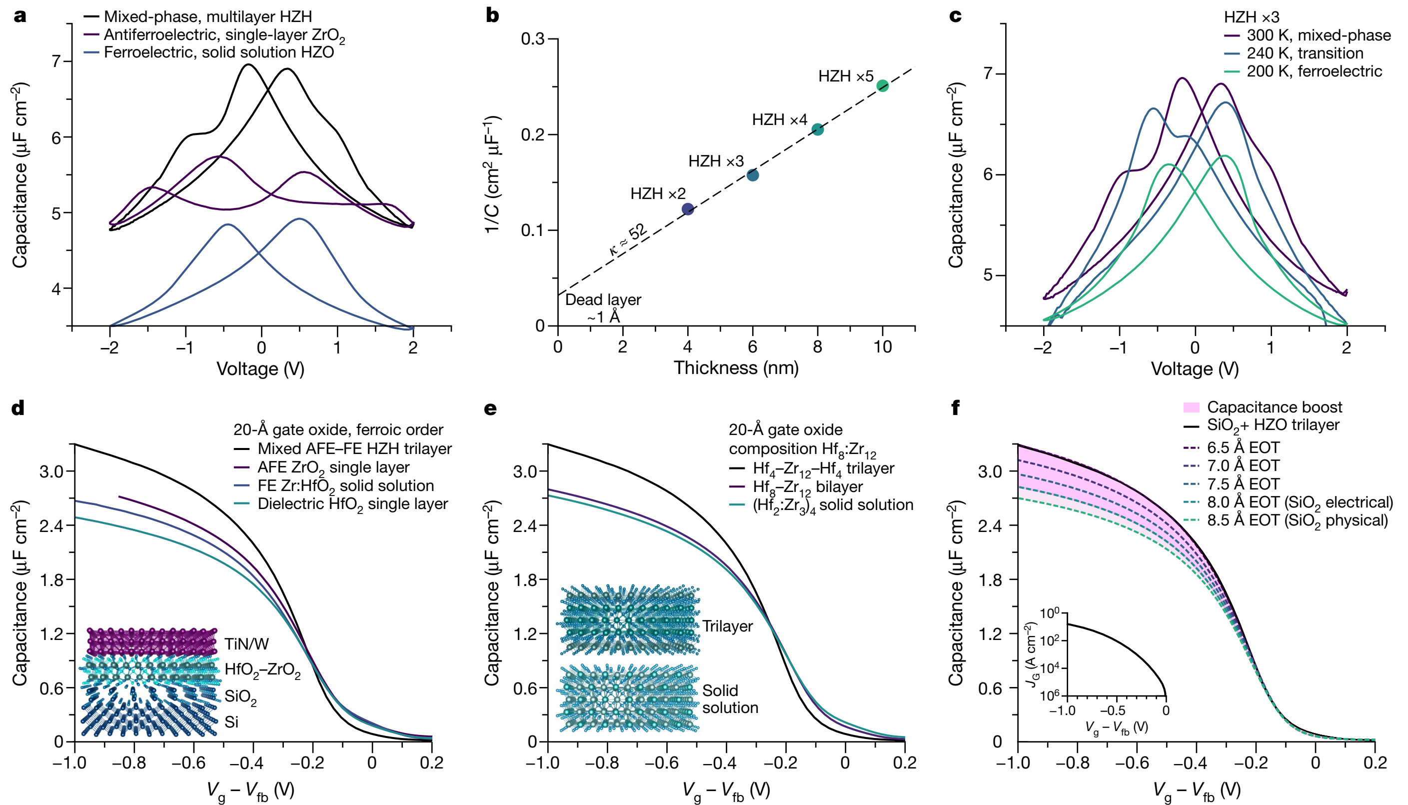

Fig. 2 | Enhanced capacitance in ultrathin HfO_2–ZrO_2 mixed-ferroic heterostructures. a, Metal–insulator–metal (MIM) C–V hysteresis loops for a mixed FE–AFE HZH multilayer demonstrating higher capacitance compared against its AFE (ZrO_2) and FE (Zr:HfO_2) counterparts of the same thickness. **b**, Inverse capacitance versus thickness for MIM HZH multilayers up to five superlattice repeats (10 nm); the extracted permittivity of 52 is large for HfO_2-based oxides. **c**, MIM C–V hysteresis loops for HZH multilayers of the same periodicity demonstrating an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room temperature. The proximity to the temperature-dependent phase transition (Extended Data Fig. 3) suggests that the HZH heterostructure lies near its maximum electric susceptibility position, ideal for negative capacitance stabilization[30,49]. **d**, MOS accumulation C–V of HZH trilayer compared to AFE ZrO_2, FE Zr:HfO_2 and dielectric HfO_2, all of the same thickness (20 Å), indicating that mixed-ferroic behaviour is optimal for enhancing capacitance. **e**, Accumulation C–V of the HZH trilayer compared to bilayer and solid-solution films of the same thickness (ALD cycles) and composition (Hf:Zr cycles), demonstrating that the capacitance enhancement is not simply driven by Hf:Zr composition[32,38], but instead the atomic-scale stacking (Extended Data Figs. 4 and 5). Inset, schematic multilayer versus solid solution (Hf and Zr cations vertically separated versus intermixed). **f**, Accumulation C–V for a 2-nm HZH grown on sub-nm SiO_2 fit EOT simulations. Inset, gate leakage of the same stack. 2-nm HZH on SiO_2 demonstrates lower EOT than the thickness of SiO_2 interlayer alone, carefully extracted via physical (8.5 Å) and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence of capacitance enhancement via negative capacitance. Furthermore, these 2-nm ferroic gate stacks demonstrate amplified charge from pulsed I–V measurements relative to the SiO_2 interlayer (Extended Data Fig. 7), marking, to our knowledge, the thinnest demonstration of charge and/or capacitance enhancement (Extended Data Fig. 7).

Methods). After top metal deposition, the entire gate stack undergoes a low-temperature post-metal anneal (200 °C, 60 s, N_2), which does not interfere with the HfO_2–ZrO_2 multilayer structure: various characterization techniques—synchrotron X-ray reflectivity (XRR), layer-resolved electron energy loss spectroscopy (EELS) and angle-resolved X-ray photoelectric spectroscopy (XPS)—confirm the expected Hf 4 Å–Zr 12 Å periodicity (Extended Data Fig. 1). The underlying mixed ferroic order in these HfO_2–ZrO_2 heterostructures is structurally established by high-resolution TEM (Fig. 1d and Extended Data Fig. 2e, f) and in-plane grazing-incidence diffraction (Fig. 1e and Extended Data Fig. 2a). Both techniques indicate the presence of the tetragonal ($P4_2/nmc$, T phase) and orthorhombic ($Pca2_1$, O phase) phases, which correspond to AFE and FE order in fluorite-structure films, respectively. Furthermore, local TEM imaging indicates the FE (orthorhombic) and AFE (tetragonal) phases are laterally intertwined (Fig. 1d and Extended Data Fig. 2e, f). Synchrotron X-ray spectroscopy and optical spectroscopy further confirm the presence of inversion symmetry breaking in the 2-nm HfO_2–ZrO_2–HfO_2 (HZH) multilayer (Extended Data Fig. 2c, d).

We note here that the original Kittel view of an 'antipolar' crystal structure[21] does not apply to the nonpolar tetragonal lattice attributed to fluorite-structure antiferroelectricity. Instead, the field-induced tetragonal-to-orthorhombic (nonpolar-to-polar) phase interconversion as the origin of antiferroelectricity has been examined in both ZrO_2[22,23] and HfO_2[22,24]. Therefore, at low electric fields, the mixed FE–AFE behaviour is analogous to an FE–dielectric (polar–nonpolar) heterostructure, which can impart depolarization fields on the FE layer[25]. The laterally intertwined nonpolar–polar phases present in the ultrathin HZH heterostructure are conducive to flattening the FE energy landscape through the aforementioned depolarization fields[26–28] (Fig. 1a). Furthermore, heterogeneous elastic energies in structurally inhomogeneous systems have been shown to destabilize long-range polarization, suppress polarization, and thereby flatten energy landscapes[28].

Additionally, the polarization in the ultrathin HZH multilayer exhibit an in-plane component. 2D reciprocal space maps indicate a strong out-of-plane (111) texture (Extended Data Fig. 2b), which is consistent with TEM images demonstrating vertically stacked planes of 111-interplanar lattice spacing (Extended Data Fig. 2f). Therefore, considering that the polarization is directed along a principal lattice direction for the $Pca2_1$ orthorhombic structure, the highly oriented out-of-plane (111) texture indicates an in-plane projected polarization.

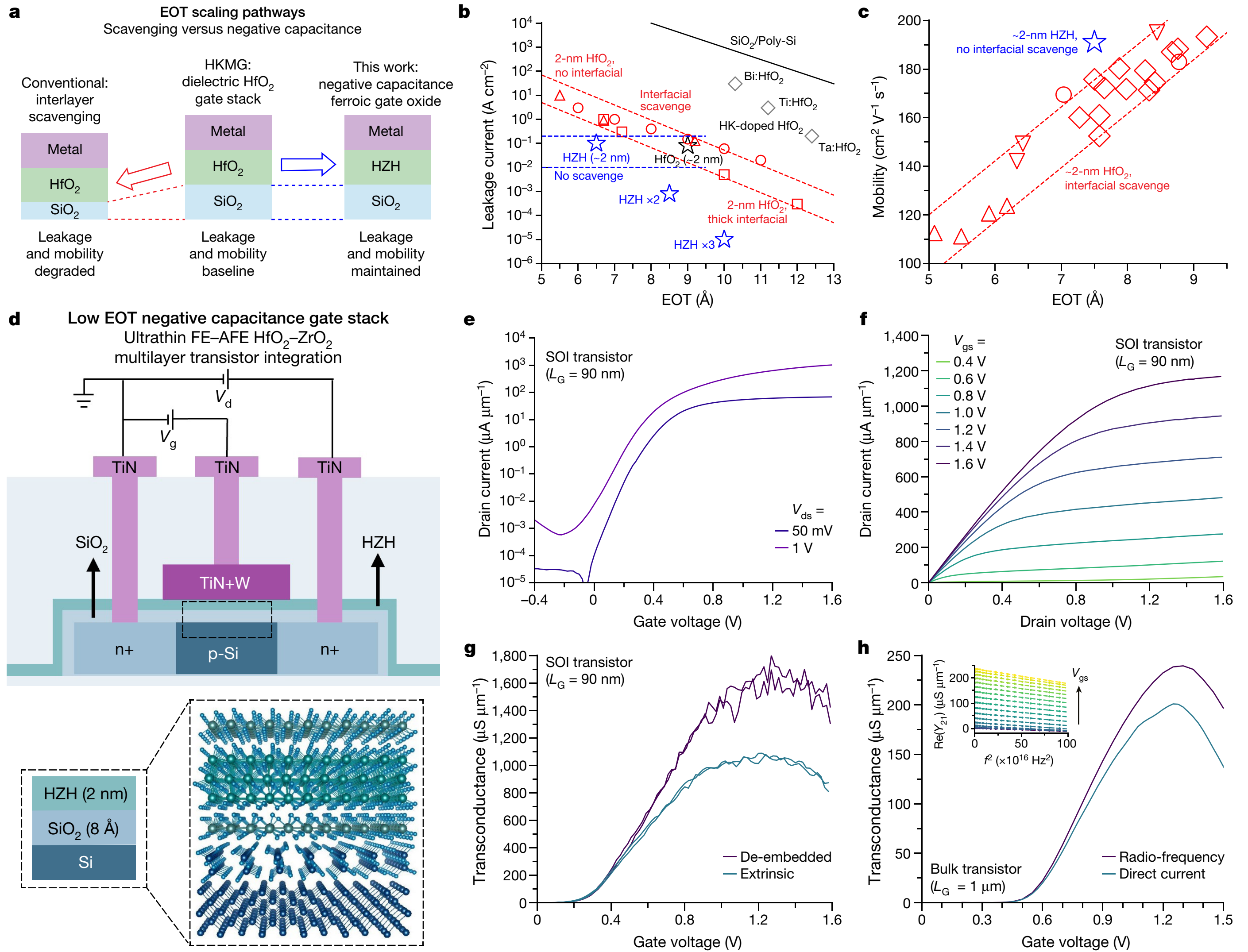

Fig. 3 | Device performance benefits from using ultrathin mixed-ferroic HfO_2–ZrO_2 gate stacks. a, EOT scaling pathways: conventional interlayer scavenging implementing standard high-*κ* dielectric HfO_2 reduces the EOT by thinning the SiO_2 interlayer (red), leading to leakage and mobility degradation[3]; integrating a ferroic negative capacitance oxide that exhibits a capacitance enhancement effect on SiO_2 (blue) lowers the EOT without reducing the thickness of the SiO_2 interlayer. **b**, Leakage–EOT scaling of the HZH multilayer gate stacks (blue) benchmarked against reported high-*κ* metal gate (HKMG) literature[3], including interlayer-scavenged 2-nm HfO_2 (red), high-*κ* doped HfO_2 (grey), and SiO_2/poly-Si (black). The leakage is the lowest reported for a 6.5-Å EOT MOS capacitor on silicon[3], and similar to the standard higher-EOT 2-nm HfO_2 high-*κ* dielectric (black), owing to maintaining the same SiO_2 thickness. **c**, Raw mobility versus EOT for long-channel transistors integrating the 2-nm HZH (blue) versus industry-reported long-channel transistors integrating standard 2-nm HfO_2 (red)[42], reported at 10^{13} cm^{-2} charge density. The raw mobility for HZH sits above the industry-reported trend line[42], owing to scaling EOT without requiring scavenging. Mobility results are also benchmarked against other industrial HKMG reports[3] (Extended Data Fig. 8d). **d**, Schematic transistor device layout, which integrates the 2-nm HZH gate stack. **e**–**g**, d.c. *I*–*V* transfer characteristics (I_d–V_{gs}; **e**), d.c. output characteristics (I_d–V_{ds}; **f**), and d.c. transconductance (g_m–V_{gs}; **g**) for short-channel (L_G = 90 nm) SOI transistors. V_{gs}, gate-to-source voltage; V_{ds}, drain-to-source voltage. Notably, the maximum on-current and g_m at V_{ds} = 1 V exceeds 1 mA μm^{-1} and 1 mS μm^{-1}, respectively. **h**, Transconductance versus gate voltage for long-channel bulk transistors (L_G = 1 μm) via d.c. (derivative of I_d–V_{gs}) and radio-frequency ($Re(Y_{21})$) measurements at V_{ds} = 1 V. Inset, de-embedded $Re(Y_{21})$ (open circles) as a function of squared frequency at different d.c. bias points (V_{gs} ranging from 0.2–1.2 V in 0.05 V steps) extrapolated to the zero-frequency limit (dotted lines) to extract the radio-frequency g_m (Extended Data Fig. 9).

The in-plane polarization introduces additional depolarization field, owing to the electrostatic coupling with the nonpolar AFE phases in the lateral direction. Notably, exploiting inhomogeneity to induce depolarization fields and enhance susceptibility has been demonstrated for perovskites exhibiting heterogeneous polar–nonpolar regions[28]. Following the same underlying mechanisms, our work demonstrates that it is possible to stabilize a mixed nonpolar–polar phase competition in 2-nm-thick binary oxide films and enhance its permittivity. We also note that flattening of the energy landscape via depolarization fields is the same underlying principle of the negative capacitance effect[11,29], in which depolarization fields stabilize the FE locally at a higher energy state compared to the ground state of an isolated, homogeneous FE, leading to negative-curvature energy landscapes[30,31].

To confirm the higher susceptibility in the mixed AFE–FE system directly, we have performed capacitance–voltage (*C*–*V*) hysteresis loops in metal–insulator–metal capacitor structures on thicker films with the same superlattice periodicity (Fig. 2a). Besides features indicative of mixed FE–AFE order, the total capacitance for the superlattice is larger than both conventional AFE ZrO_2 and FE Zr:HfO_2 of the same thickness (Fig. 2a), demonstrating enhanced susceptibility. To quantify the permittivity, capacitance measurements were performed across the superlattice thickness series. These measurements yield an extracted

permittivity of approximately 52 (Fig. 2b, Methods), which is larger than both the FE orthorhombic Zr:HfO_2 and AFE tetragonal ZrO_2 values[32].

To further understand the ferroic evolution in these HZH superlattices, we performed low-temperature measurements where enhanced FE phase stabilization is expected. Indeed, temperature-dependent *C*–*V* loops for thicker HZH demonstrate an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room temperature (approximately 240 K, Fig. 2c), consistent with temperature-dependent X-ray spectroscopy indicating transition from mixed tetragonal–orthorhombic phase to predominately orthorhombic structure at similar temperatures (Extended Data Fig. 3c). That the capacitance decreases upon cooling as the system moves away from the highly susceptible mixed ferroic phase is consistent with previous work on negative capacitance in FE–dielectric systems[29], which establishes the energy landscape link between enhanced capacitance and susceptibility near phase transitions. Notably, the intertwined FE–AFE phases within the superlattice and the resulting enhancement in susceptibility from the competition of FE and AFE phases are analogous to negative stiffness composites of ferroelastics within a metal matrix[33,34], that is, the mechanical analogue to negative capacitance.

Ultrathin FE–AFE HfO_2–ZrO_2 MOS capacitors

Next, the superlattices were grown on Si substrates in metal–oxide–semiconductor (MOS) capacitor structures. A self-limiting chemical oxide SiO_2 was grown first, resulting in approximately 8.0–8.5-Å thickness[3], following the standard practice in advanced Si devices (Methods). Subsequently, a 20-cycle-thick multilayer was grown with ALD following the same stacking as before, that is, Hf:Zr:Hf 4:12:4. Accumulation *C*–*V* curves of the superlattice stack show considerably larger capacitance in comparison to other conventional stacks—dielectric HfO_2, AFE ZrO_2, FE Zr:HfO_2—of the same 20-Å thickness (Fig. 2d). Furthermore, the Hf:Zr:Hf 4:12:4 trilayer demonstrates enhanced capacitance compared to a bilayer (Hf:Zr 8:12) and solid solution (Hf:Zr $[2:3]_4$) of the same thickness and Hf:Zr composition (Fig. 2e).

Notably, the composition in our films is close to where several previous reports have postulated a possible morphotropic phase boundary (MPB) in thicker HfO_2–ZrO_2 solid-solution films[35]. We note that MPB systems follow strict symmetry requirements[36], which have not been established for the HfO_2–ZrO_2 system. In our ultrathin HZH multilayers, the negative free-energy curvature of the polar FE O phase compensates the positive curvature of the nonpolar AFE T phase (Fig. 1a), leading to a flattened energy landscape. Similarly, energy landscape flattening is postulated as the thermodynamic origin of enhanced piezoelectric response in canonical perovskite ferroelectrics[36], in which multiple crystal symmetries are nearly degenerate across a composition phase boundary (MPB). However, a critical distinction is that here the overall energy landscape flattening, and corresponding increase in capacitance, is determined by the stacking of the atomic-scale HfO_2–ZrO_2 layers, and not the volume fraction of the constituent elements[37]: solid solution of the same Hf:Zr composition does not provide the same high capacitance (Fig. 2e). Furthermore, compared to HfO_2–ZrO_2 solid solutions across a range of typically reported Zr-rich 'MPB-like' compositions[35], the HZH multilayer demonstrates larger capacitance (Extended Data Fig. 4). This indicates that the enhanced capacitance in HZH films is not simply driven by doping[32,38], but can instead be tuned by the configuration of the multilayer structure (Extended Data Figs. 4, 5). In the ultrathin regime, surface energies become a more dominant consideration for determining polymorphic phase stability[22]; accordingly, the importance of stacking is amplified.

To quantify the observed capacitance, we have performed EOT simulations of MOS capacitors using the industry-standard Synopsys simulation platform (Methods). The Hf:Zr:Hf 4:12:4 trilayer stacks vary between 6.5–7.0-Å EOT (Fig. 2f), consistent over many measured capacitors. Notably, this EOT is smaller than the expected thickness of the interfacial SiO_2 layer (8.0–8.5 Å), as mentioned. To investigate further, high-resolution TEM of the gate stacks (Extended Data Fig. 6) illustrates that the SiO_2 thickness is indeed approximately 8.5 Å. To supplement this physical characterization, we next implemented electrical characterization of the interfacial layer via inverse capacitance versus thickness analysis of conventional dielectric HfO_2 and Al_2O_3 thickness series grown on the same SiO_2 (Methods, Extended Data Fig. 6). All thermal processing is kept the same as the HfO_2–ZrO_2 superlattice gate stack. The extracted HfO_2 and Al_2O_3 permittivities—19 and 9, respectively—are consistent with the typical dielectric phases of these two materials. Therefore, one can reliably extract the SiO_2 layer thickness, yielding 8 Å (Extended Data Fig. 6), consistent with the high-resolution TEM results and values established by the semiconductor industry[3].

Moreover, the consistent interlayer thickness extracted from both material systems indicates that neither Hf nor Al encroaches into the interfacial SiO_2, which would reduce its thickness and/or increase its permittivity. This is expected considering that the gate oxides are processed at much lower temperature than that needed for silicate formation[39] and works reporting an increased SiO_2 interlayer permittivity[40]. Furthermore, XRR, EELS and XPS data indicate that for both the undoped control HfO_2 gate stack and the superlattice gate stack, the HfO_2 layer sits right on top of SiO_2, leading to the same interface in both cases (Extended Data Fig. 1). Therefore, considering the interfacial layer thickness as 8 Å, the HZH multilayer gate stack demonstrates an overall EOT approximately 1.5 Å lower than the constituent SiO_2 thickness. We note that, for simplicity, we have used an EOT to quantify the capacitance of the superlattice stack; however, for a rigorous description, one should solve for the non-linearities that are expected to emerge from the ferroic nature of the gate oxide[41].

To supplement the *C*–*V* evidence of capacitance enhancement, pulsed current–voltage (*I*–*V*) measurements of MOS capacitors integrating the approximately 2-nm HZH gate stack—which can quantify the amount of charge as a function of voltage[26] (Methods, Extended Data Fig. 7)—demonstrate larger stored charge than if just interfacial SiO_2 was sitting on top of Si. This provides further electrical evidence of charge enhancement in the ultrathin mixed-ferroic gate stack (Extended Data Fig. 7e). Furthermore, from these measurements, the extracted polarization–electric field relationship for just the HZH multilayer (Extended Data Fig. 7f) exhibits a regime of negative slope, which mathematically corresponds to negative capacitance stabilization[26].

Ultrathin FE–AFE HfO_2–ZrO_2 device results

The practical implication of this capacitance enhancement can be clearly seen in Fig. 3b, which shows leakage current versus EOT behaviour. The leakage current is measured at $V_g - V_{fb} = -1$ V, where V_{fb} is the flatband voltage of the semiconductor and V_g is the gate voltage. All other data points on this plot are taken from reported industrial gate stacks[3]. The leakage current for the Hf:Zr:Hf 4:12:4 stack is substantially lower at the same EOT. Note that below 9 Å, the other gate stacks need sophisticated scavenging techniques to reduce the thickness of the interfacial SiO_2 (ref. [3]). On the other hand, the ferroic gate stack can achieve approximately 6.5 Å without any scavenging, resulting in the lower leakage current (Fig. 3b).

Furthermore, the scavenging of the interfacial SiO_2 leads to a loss of mobility of approximately 20 $cm^2 V^{-1} s^{-1}$ per every Å of scavenged SiO_2, owing to an increase in remote phonon scattering[3,16]. To examine how the mobility evolves with EOT, we compared transistors implementing the lower-EOT HZH gate stack compared to higher-EOT conventional HfO_2 gate stack, both of the same physical thickness (Methods). Notably, the mobility remains essentially the same for both stacks, demonstrating that there is no fundamental change in electron transport as a result of the mixed-ferroic multilayer gate stack compared to the standard high-κ dielectric gate stack (Extended Data Fig. 8d). Furthermore, this work demonstrates no penalty in mobility below 9 Å EOT, the point where

conventional high-κ gate stacks display the mobility degradation due to scavenging that is necessary for lowering EOT (Fig. 3c, Extended Data Fig. 8d). Indeed, raw mobility extracted from long-channel transistors integrating the 2-nm HZH mixed-ferroic heterostructure gate stack exceed that of industry-reported long-channel transistors integrating standard 2-nm HfO_2 high-κ dielectric gate stacks[42] at the same EOT (Fig. 3c).

To examine how the capacitance enhancement in the 2-nm HZH gate stack behaves at high frequency, radio-frequency measurements were performed on the same long-channel (gate length $L_G = 1\ \mu m$) devices (Methods, Extended Data Fig. 9) to extract device parameters up to approximately 800 MHz for our devices (close to the cut-off frequency). Of particular interest is the transconductance (g_m), which is proportional to the product of capacitance and electron velocity (mobility). From Y-parameter measurements one can find alternating current (a.c.) transconductance as $\mathrm{Re}(Y_{21}) = g_m + af^2$, where f is the frequency (Methods). This yields an a.c. transconductance as a function of applied gate voltage (V_g). Plotting this dependence, together with direct current (d.c.) transconductance ($\partial I_d/\partial V_g$ from d.c. I_d–V_g; Fig. 3h), illustrates that the d.c. and a.c. transconductance are similar, with a.c. transconductance roughly 15% larger at the peak value. This slightly larger a.c. transconductance may result from the fact that certain interface traps, which affect the d.c. behaviour, cannot respond at frequencies larger than 100 MHz, leading to better gate control. More importantly, these radio-frequency results show that the observed capacitance enhancement is not limited to the low-frequency regime[43,44].

Next, shorter-channel ($L_G = 90$ nm) devices, fabricated on a silicon-on-insulator (SOI) transistor with 18-nm SOI thickness, were examined. The transfer and output characteristic of a typical transistor are shown in Fig. 3e, f. Note that the threshold voltage of this device is 0.55 V, which is consistent with the work function of W used as the gate metal. Because of this, the transistors have been driven up to 1.6-V gate voltage so that an overdrive voltage ($V_{ov} = V_g - V_T$) of approximately 1 V can be applied (V_T, threshold voltage). It is found that at a drain voltage (V_d) and V_{ov} of 1 V, the drain current exceeds 1 mA μm^{-1}. Additionally, the measured extrinsic transconductance of approximately 1.1 mS μm^{-1} (Fig. 3g) corresponds to an intrinsic transconductance of approximately 1.75 mS μm^{-1} (Methods, Extended Data Fig. 10). The transconductance is substantially larger than conventional 90-nm transistors. In addition, it is larger than control devices with a HfO_2 gate stack of the same physical thickness, demonstrating the dual benefits of the HZH mixed-ferroic gate stack: low EOT without adversely affecting the electron transport.

Finally, to probe the interface quality, especially trap-induced effects[45] relevant for MOS field-effect transistor (MOSFET) reliability—a very crucial aspect for commercial application—we performed positive-bias temperature instability measurements on nFET transistors (Extended Data Fig. 8e–h). The results demonstrate very similar behaviour for both the HZH and control HfO_2 stacks of the same physical thickness, and similar to those reported in literature for high-κ HfO_2 stacks[46]. This is not unexpected; reliability characteristics are predominantly determined by the interfacial oxide and its high-κ interface[46]; here both stacks have the same un-scavenged SiO_2 interlayer (Extended Data Fig. 1). Furthermore, stress measurements on capacitors demonstrate negligible V_{fb} shift and non-existent capacitance degradation with increased stress time (Extended Data Fig. 8i, j).

Discussion

Capacitance enhancement via negative capacitance has been demonstrated for FE–dielectric superlattices in many single-crystalline perovskite-structure systems[30,31,47,48]. This work demonstrates that the same enhancement is possible in HfO_2–ZrO_2 fluorite-structure superlattices on Si, which exhibit mixed FE–AFE (polar–nonpolar) order in films as thin as just approximately 2 nm. The ability to go down to such thickness and still stabilize competing ferroic order, conducive for negative-capacitance-mediated capacitance enhancement, is very important for advanced electronic devices, because dimensional scaling requires ultrathin gate stacks. Furthermore, this work establishes the critical role of atomic-layer stacking—as opposed to conventional doping techniques[32,38]—in controlling the ferroic phase space and permittivity of fluorite-structure oxides down to ultrathin limits, leveraging its unique size effects[13–15] and rich AFE–FE polymorphs[22,23]. When this mixed phase HfO_2–ZrO_2 multilayer is integrated on Si, the gate stack exhibits a capacitance enhancement, lowering the EOT below a threshold that traditionally required careful scavenging of interfacial SiO_2, which would otherwise degrade mobility[3]. Additionally, the low EOT is achieved at over an order of magnitude lower leakage current. Therefore, harnessing atomic-scale layering in ultrathin HfO_2–ZrO_2 ferroic gate oxides presents a promising materials design platform for future Si transistors beyond the conventional high-κ dielectrics that have spurred semiconductor industry scaling over the past two decades.

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Methods

Gate stack

Gate oxide. Thin films of HfO_2–ZrO_2 were grown by atomic layer deposition (ALD) in a Fiji Ultratech/Cambridge Nanotech tool (UC Berkeley) at 270 °C in which tetrakis (ethylmethylamino) hafnium and tetrakis (ethylmethylamino) zirconium precursors are heated to 75 °C and water vapour is used as the oxidant. For metal–FE–insulator–semiconductor (MFIS) capacitor structures, sub-nm chemically grown SiO_2 on lightly doped Si (10^{15} cm^{-3}) was prepared by the standard clean (SC-1) solution (5:1:1 H_2O:H_2O_2:NH_4OH at 80 °C for 10 min) after the Si wafer was cleaned in Piranha (120 °C for 10 min) to remove organics and HF (50:1 H_2O:HF at room temperature for 30 s) to remove any native oxide. Subsequently, HZH multilayers are deposited at 270 °C by ALD. After ALD deposition, post-deposition annealing (PDA) was performed at 175 °C (20 min, forming gas N_2/H_2 background) to help cure the SiO_2–oxide interface. For confirmation and reproducibility, HZH multilayers of the same ALD cycling were also deposited at MIT Lincoln Laboratory (MIT LL); after ALD deposition, PDA was performed at 250 °C (1 min, N_2 background).

Gate metal. For UC Berkeley capacitors, the first layer of the gate metal, TiN, is deposited by ALD (250 °C, 20 cycles, 15 Å) in N_2 and H_2 plasma. Subsequently, W is deposited by sputtering (room temperature, 60 nm). For MIT LL capacitors, the gate metal, TiN, is deposited by PVD (room temperature).

Annealing. The entire gate stack undergoes a low-temperature post-metal anneal (200 °C, 1 min, N_2) to cure interface defects. This low temperature does not interfere with the HZH multilayer structure, as confirmed by various characterization techniques (Extended Data Fig. 1), and maintains the mixed-ferroic behaviour, as high-temperature annealing would induce purely FE behaviour (Extended Data Fig. 5). X-ray diffraction and TEM confirm the presence of crystalline ultrathin films despite the low deposition temperature, afforded by the low crystallization temperature of ZrO_2[50]. In fact, non-post-annealed ALD-grown ZrO_2 has previously demonstrated crystallization into the FE orthorhombic phase on Si[51].

Device fabrication

MOS and MIM capacitors, bare structures. For MOS capacitor structures, after gate stack deposition, top electrodes are defined by photolithography and dry etching. For bare structures (structural studies), the top metal is removed by chemical etching to expose the gate oxide surface. For metal–insulator–metal (MIM) capacitors, W is deposited by sputtering (room temperature, 30 nm) on a lightly doped Si substrate as the bottom metal electrode. After ferroic film deposition by ALD, 60 nm of W is deposited by sputtering. The top electrodes are then again defined by photolithography and dry etching.

Bulk transistors. The n-type bulk transistors were fabricated by a non-self-aligned gate-last process on bulk silicon wafers (10^{17} cm^{-3}) with local oxidation of silicon (LOCOS) as device isolation technique. First, 10 nm of SiO_2 thermal oxide and 30 nm of low-pressure chemical vapour deposition (LPCVD) Si_3N_4 were grown on the Si substrates. After the active region was defined by photolithography and Si_3N_4/SiO_2 etching, dry oxidation was performed to form the LOCOS isolation. Next, the source/drain regions were defined by photolithography and ion implantation with an ion dose of 3×10^{15} ions per cm^2. The dopants were then activated by a rapid thermal anneal (RTA) at 900 °C for 7 min in N_2 ambient. The gate stacks with the sub-nm chemically grown SiO_2, 2-nm HZH heterostructure, and 100 nm of sputtered W gate was then deposited. After the gate fingers (from 500 nm to 50 μm) were patterned by photolithography and etched by inductively coupled plasma (ICP) metal etching, the 400-nm-thick interlayer dielectric (ILD) SiO_2 was deposited using plasma-enhanced CVD (PECVD). Last, after the contact hole opening, the Ti/TiN contact metal was deposited by sputtering, defined by photolithography, and then etched by ICP metal etching.

Short-channel SOI transistors. The n-type short-channel transistors were fabricated by a non-self-aligned gate-last process on SOI substrates with a gate length (L_G) down to 90 nm. First, the device layer was thinned down to 20 nm and the active regions were defined by photolithography with expose regions etched slightly into the buried oxide. The hydrogen silsequioxane (HSQ) negative resist were written by e-beam lithography as a hard mask for the ion implantation with a dose of 5×10^{15} ions per cm^2. The dopant activation was conducted in an RTA at 900 °C for 15 s in N_2 ambient. The gate stacks with the sub-nm chemically grown SiO_2, 2-nm HZH heterostructure, 1.5 nm of PEALD TiN, and 100 nm of sputtered W were sequentially deposited. The gate region (250 nm) was then patterned by photolithography. Similar to the back-end process for the bulk transistors, 400 nm of ILD and sputtered Ti/TiN contact metal were deposited and defined by photolithography and ICP etching.

Microscopy

Transmission electron microscopy. Electron microscopy was performed at the National Center for Electron Microscopy (NCEM) facility of the Molecular Foundry at Lawrence Berkeley National Laboratory (LBNL). The high-resolution bright field TEM images of HZH thin films were performed by FEI ThemIS 60-300 microscope with image aberration corrector operated at 300 kV (Fig. 1d, Extended Data Fig. 2e, f). To prepare cross-sectional TEM samples of HZH thin films, mechanical polishing was employed by using an Allied High Tech Multiprep at a 0.5° wedge to thin down the total thickness of samples down to 10 μm. Later, Ar ion milling of the Gatan Precision Ion Milling System was used to make an electron-transparent sample, starting from 4 keV down to 200 eV as final cleaning energy. For high-resolution imaging, in order to capture the crystallinity of the HZH layers, the zone axis alignment required varying degrees of mistilt with respect to the Si lattice, explaining the slightly obscured Si atomic columns (Fig. 1d, Extended Data Fig. 2e, f).

The local interplanar *d*-spacing in the ultrathin HZH films (Extended Data Fig. 2e, f) was measured by DigitalMicrograph software using its line profile plus integration width analysis. For the 2-nm HZH multilayer film, the extracted interplanar lattice spacings were averaged over multiple lattice periodicities and confirmed across various local regions of the film (Extended Data Fig. 2e, f). The SiO_2 interlayer thickness from low-magnification wide field-of-view (FOV) imaging was determined by the same method (Extended Data Fig. 6a). In particular, the intensity line scan from the wide FOV image (Extended Data Fig. 6a) is obtained from averaging across the entire FOV specified by the teal-coloured box (~150 nm). Next, the inflection points of the intensity peak were used as the criteria to set the boundaries of the SiO_2 interlayer (Extended Data Fig. 6a). This methodology was also utilized to determine the boundaries of the HZH layers from the EELS spectrum (Extended Data Fig. 1c). Regarding the wide FOV cross-sectional TEM (Extended Data Fig. 6a), both the low atomic weight and lack of crystallinity of the SiO_2 layer contribute to its weak scattering (bright colour), which aids in the visual delineation of the layer boundaries and the thickness extraction from the corresponding averaged intensity line scan.

Optical microscopy. Second harmonic generation (SHG) measurements (Extended Data Fig. 2d) were performed with a Ti:sapphire femtosecond laser (Tsunami, Spectra Physics, $\lambda \approx 800$ nm, frequency ≈ 80 MHz). The linearly polarized femtosecond laser beam was focused through 50× objective lens (numerical aperture (NA) ≈ 0.42) which results in a focal spot size of 2 μm. The generated SHG signal was collected through the same objective lens and separated from the fundamental beam by the harmonic separator. After passing through the optical bandpass filter, the SHG signals were registered to the photon multiplier tube (PMT) without a polarizer. The fundamental beam

was mechanically chopped, and the signal collected by the PMT was filtered by a lock-in amplifier to reduce the background noise. For SHG spatial mapping, a two-axis piezo stage was used and the coordinate was synchronized with the PMT signal. The SHG intensity was obtained by averaging the mapping signals across a 100 μm × 100 μm sample area.

X-ray characterization

X-ray reflectivity. Synchrotron X-ray reflectivity (XRR)—performed at Sector 33-BM-C beamline of the Advanced Photon Source, Argonne National Laboratory and at Beamline 2-1 of the Stanford Synchrotron Radiation Lightsource, SLAC National Accelerator Laboratory—confirmed the thickness of HZH heterostructures (Extended Data Fig. 1b). The overall thickness of the HZH heterostructures is consistent with the growth rate (~1 Å per cycle) of ALD-grown $Zr:HfO_2$ as demonstrated in our previous work[13]. Furthermore, the presence of irregularly spaced fringes in the thicker HZH heterostructures suggests the presence of well separated HZH layers, that is, not a solid solution. This is confirmed by XRR fitting (Extended Data Fig. 1b) performed with the python package GenX[52] which considers factors such as density, roughness, and thickness.

In-plane grazing-incidence diffraction. Synchrotron in-plane grazing-incidence diffraction (GID) (Fig. 1e and Extended Data Fig. 2a) was performed at Sector 33-ID-D beamline of the Advanced Photon Source, Argonne National Laboratory. A Pilatus-II 100K area detector mounted on the del-arm was used to collect diffraction signal with a grazing-incidence geometry. The region of interest on the detector was set such that the ring-like signal was fully integrated. In-plane GID was collected by sweeping the in-plane angle ν (8–50°) with a fixed out-of-plane grazing angle δ (δ = 0.9°); the corrected Bragg angle (2θ) over which the data are plotted and indexed is determined from the relationship $\cos(2\theta) = \cos(\nu)\cos(\delta)$ set by the geometry of the diffractometer. The X-ray source was fixed at 16 keV (λ = 0.775 Å). In-plane diffraction yields more diffraction peaks with better defined width, probably owing to the preferred orientation and disc-shape domains in the film. Therefore, in-plane GID enables clear indexing to the FE orthorhombic ($Pca2_1$) and AFE tetragonal ($P4_2/nmc$) fluorite structure in the ultrathin HZH films, as the presence of many reflections from the in-plane GID spectra (Fig. 1e, Extended Data Fig. 2a) enables clear distinction from other nonpolar fluorite-structure polymorphs. Such diffraction spectra would be otherwise prohibited in typical out-of-plane geometry owing to the lack of vertical diffraction planes and the large linewidth inherent to ultrathin films.

Two-dimensional diffraction. Two-dimensional reciprocal space maps (Extended Data Fig. 2b) were measured at Beamline 11-3 of the Stanford Synchrotron Radiation Lightsource, SLAC National Accelerator Laboratory. Rayonix MX225 CCD area detector collected diffraction flux in grazing-incidence (<0.20°) geometry; the X-ray source (50 μm vertical × 150 μm horizontal beam size) was fixed at 12.7 keV. The sample–detector work distance was set to 80 mm to enable detection of a wide region of reciprocal space (Q range 0.2 to 5 Å^{-1}) at the expense of reciprocal space resolution, set by the pixel size. The two-dimensional diffraction scans—in which a wide portion of the entire reciprocal space was collected simultaneously, rather than at discrete regions in Q_x–Q_y space—were averaged over data collection time and for repeated scans. These measurement features, in tandem with the high X-ray flux afforded by the synchrotron source, enabled sufficient diffraction signal detection and contrast in films just 2 nm in thickness. Data analysis was performed Nika, an Igor Pro package for correction, calibration and reduction of two-dimensional areal maps into one-dimensional data[53]. Two-dimensional reciprocal space maps on bare HZH heterostructures confirm the presence of crystalline ultrathin films despite the low deposition temperature, afforded by the low crystallization temperature of ZrO_2 on Si[50].

Ferroic phase identification from diffraction. For fluorite-structure thin films, the main phases to consider are the dielectric monoclinic ($P2_1/c$), AFE tetragonal ($P4_2/nmc$), and FE orthorhombic ($Pca2_1$) phases. Various diffraction reflections from the wide-angle in-plane GID spectra enable indexing to the orthorhombic $Pca2_1$ phase. Lattice parameters (a, b, c)—determined via Bragg's law from the d_{200} family of reflections—are self-consistently checked against the (111) lattice spacing ($\frac{1}{d_{111}^2} = \frac{1}{a^2} + \frac{1}{b^2} + \frac{1}{c^2}$) as well as other higher-order reflections present in the in-plane diffraction spectra (Extended Data Fig. 2a). For example, the lattice parameters extracted from the {200} reflections were a = 5.36 Å, b = 5.23 Å, c = 5.47 Å. This corresponds to a d_{211} lattice spacing of 2.209 Å, which agrees well with the lattice spacing (2.205 Å) obtained from Bragg's law based on the reflection position.

The monoclinic phase was ruled out owing to a lack of two {111} peaks in the diffraction spectra and the $(111)_o$ and $(101)_t$ reflections being substantially offset from its expected peak position in the monoclinic phase. With regards to the indexing of tetragonal $(101)_t$ peak (Extended Data Fig. 2a), it is always reported that the tetragonal $(101)_t$ reflection has a smaller d spacing[54] in thicker HfO_2-based films[55], and is therefore expected to be present at a higher angle compared to the orthorhombic $(111)_o$ reflection, which is the case in the indexed diffraction spectra (Extended Data Fig. 2a), based on the result that the self-consistent indexing methodology outlined above provides.

In terms of extracting the phase fraction of the tetragonal and orthorhombic phases, although Rietveld refinement has been applied to grazing-incidence X-ray diffraction of thick (10 nm) $Zr:HfO_2$[56] to determine the orthorhombic phase fraction, that methodology cannot be applied in the ultrathin regime, as the films are highly oriented, as opposed to fully polycrystalline (Extended Data Fig. 2b), which is a requirement to apply Rietveld refinement.

Regarding strain effects: strain-induced ferroelectricity in antiferroelectrics is a key consideration; strain-induced ferroelectricity has been predicted in ZrO_2[23], which is indeed what we observe in certain lateral regions of our film. From the cross-sectional TEM (Fig. 1d, Extended Data Fig. 2e, f), the presence of both the FE orthorhombic $Pca2_1$ phase grains and AFE $P4_2/nmc$ tetragonal phase grains can be locally identified to persist throughout the entire HZH thickness. Considering that the 2-nm HZH heterostructure has distinct layers (evidenced by XRR, EELS and XPS characterization in Extended Data Fig. 1), that means the middle ZrO_2 layer has local regions where it is stabilized in the FE orthorhombic phase, and other local regions where it is stabilized in the AFE tetragonal phase.

Regarding structural indicators of such strain effects, again we look to the measured d_{111} (O phase) and d_{101} (T phase) lattice spacings for the ~2-nm HZH film—structural markers for distortion and strain in this fluorite-structure system[13]. Note that truly stress-free values cannot be obtained because bulk ferroelectricity is not stabilized in this material system, so we compare against DFT values[22] for HfO_2, ZrO_2 and $Zr:HfO_2$ (HZO)[22], which closely match experimental values for thicker HfO_2–ZrO_2 ferroic films[57].

In particular, the FE O-phase d_{111}-spacing for HZH (3.09 Å) is larger than typical values for thick FE HZO films (2.95 Å)[22], demonstrating that the individual HfO_2 and ZrO_2 layers in the HZH multilayer are in fact strained, that is, have increased rhombic distortion. This is consistent with the ultrathin enhanced lattice distortions trend observed in previous ALD-grown highly oriented orthorhombic FE HZO films[13], as well as epitaxial orthorhombic FE HZO films[58]. On the other hand, we observe that the d spacing for the tetragonal (101) reflection (2.95 Å) is nearly the same as is expected for prototypical AFE T-phase ZrO_2 (2.94 Å)[22]. This is expected: when the tetragonal phase is strained, it transitions to the lower-symmetry orthorhombic phase as opposed to remaining in the tetragonal phase, as it does not have the same tolerance of the FE O phase to maintain its symmetry when strained. Consequently, the larger d spacing is always attributed to the FE O phase[57], as confirmed

by self-consistent indexing to higher-order reflections (Extended Data Fig. 2a). These diffraction-based *d* spacings are confirmed by cross-sectional TEM (Extended Data Fig. 2e, f). Furthermore, the presence of the ZrO_2 layer developing ferroelectricity is supported by the presence of orbital polarization at the Zr L edge from synchrotron X-ray linear dichroism (Extended Data Fig. 2c).

X-ray absorption spectroscopy. Hard and soft synchrotron X-ray spectroscopy (Extended Data Fig. 2c) was measured at beamline 4-ID-D of the Advanced Photon Source, Argonne National Laboratory and Beamline 4.0.2. of the Advanced Light Source, Lawrence Berkeley National Laboratory, respectively. Spectroscopy measurements were taken at the oxygen K edge (520–550 eV), zirconium $M_{3,2}$ edge (325–355 eV), hafnium M_3 edge (2,090–2,150 eV), and zirconium $L_{3,2}$ edge (2,200–2,350 eV). X-rays were incident at 20° off grazing. XAS (XLD) was obtained from the average (difference) of horizontal and vertical linearly polarized X-rays. To eliminate systematic artefacts in the signal that drift with time, spectra measured at ALS were captured with the order of polarization rotation reversed (that is, horizontal, vertical, vertical and horizontal) in successive scans, in which an elliptically polarizing undulator tuned the polarization and photon energy of the synchrotron X-ray source[59]. Spectra measured at ALS were recorded under total electron yield (TEY) mode[59] from room temperature down to 100 K. Spectra measured at APS were recorded under various modes: total electron yield (TEY), fluorescence yield (FY) and reflectivity (REF).

Ferroic phase identification from spectroscopy. X-ray spectroscopy provides various signatures to distinguish the competing FE orthorhombic ($Pca2_1$) and AFE tetragonal ($P4_2/nmc$) phase. Simulated XAS spectra at the oxygen K edge (Extended Data Fig. 3d) for ZrO_2 in the various fluorite-structure polymorphs (orthorhombic $Pca2_1$ and tetragonal $P4_2/nmc$) were computed through the Materials Project[60] open-source database for XAS spectra[61]. The T-phase ($P4_2/nmc$) non-polar distortion (D_{4h}, 4-fold prismatic symmetry) from regular tetrahedral (T_d, full tetrahedral symmetry) fluorite-structure symmetry does not split the degenerate *e*-bands ($d_{x^2-y^2}$, $d_{3z^2-r^2}$), as confirmed by experiment[62] and the aforementioned XAS simulations[13]. Meanwhile, the O-phase ($Pca2_1$) polar rhombic pyramidal distortion (C_{2v}, 2-fold pyramidal symmetry) does split the *e*-manifold based on crystal field symmetry, providing a spectroscopic means to distinguish the T and O phases. The additional spectroscopic feature present between the main *e* and t_2 absorption features due to orthorhombic symmetry-lowering distortion is illustrated by its crystal field diagram (Extended Data Fig. 3b). This provides a spectroscopic fingerprint for phase identification beyond diffraction which can often be ambiguous owing to the nearly identical T-phase and O-phase lattice parameters. For the 2-nm HZH trilayer, the experimental O K edge XAS spectra demonstrates tetrahedral and rhombic splitting features closely matching the polar O phase ($Pca2_1$) emerge slightly below room temperature, indicative of the mixed tetragonal–orthorhombic to orthorhombic phase transition upon cooling. This temperature-dependent tetragonal–orthorhombic structural evolution is expected for fluorite-structure thin films[63] and is consistent with temperature-dependent capacitance measurements (Extended Data Fig. 3f). Further XAS phase identification details are provided in previous work on ultrathin Zr:HfO_2 films[13].

X-ray photoelectron spectroscopy. Angle-resolved photoelectron spectroscopy (ARPES) was performed using a Phi Versaprobe III at the Stanford Nano Shared Facilities (Extended Data Fig. 1d). A monochromatic aluminium source was used to give a photon energy of 1,486.6 eV. Data were fitted and analysed using CasaXPS. Angle-dependent XPS at various incident grazing angles enabled depth-resolved composition analysis to help confirm the HZH multilayer structure.

Dielectric measurements

MOS capacitance. Capacitance–voltage (*C*–*V*) measurements were performed using a commercial Semiconductor Device Analyzer (Agilent B1500) with a multi-frequency capacitance measuring unit (MF-CMU). 19-µm W tips (DCP-HTR 154-001, FormFactor) made electrical contact within a commercial probe station (Cascade Microtech); voltage was applied to the W top electrode and the lightly doped Si bottom electrode was grounded. To eliminate contributions from series and parasitic resistances, frequency-dependent *C*–*V* measurements were performed. In particular, *C*–*V* data were analysed at two frequencies (100–500 kHz regime) to allow for the extraction of accurate frequency-independent *C*–*V* via a three-element circuit model consisting of the capacitor and the parasitic series and parallel resistors[64]. The frequency-independent capacitance is given by

$$C = \frac{f_1^2 C_1(1 + D_1^2) - f_2^2 C_2(1 + D_2^2)}{f_1^2 - f_2^2},$$

where C_i and D_i refer to the measured capacitance in parallel mode (C_p–R_p) and dissipation values at frequencies f_i. The dissipation factor is given by $D = -\cot\theta$, where θ is the phase. To maximize the accuracy of this method, it is important the dissipation factors are small ($\ll 1$) at the frequencies chosen; therefore, high frequencies were selected.

Permittivity extraction. The permittivity of Al_2O_3 and HfO_2 dielectric layers was extracted from thickness-dependent MOS *C*–*V* measurements on lightly doped p-substrates (Extended Data Fig. 6). In the accumulation region of the MOS *C*–*V* measurements, the MOS capacitor can be modelled as three capacitors (Al_2O_3 or HfO_2 dielectric layer, SiO_2 interlayer, and Si space charge layer) in series using the following equation

$$\frac{1}{C} = \frac{1}{\epsilon_0 \epsilon_{HK}} t_{HK} + \frac{1}{\epsilon_0 \epsilon_{SiO_2}} \left[t_{SiO_2}^{phys} + \frac{t_{CL} \epsilon_{SiO_2}}{\epsilon_{Si}} \right],$$

where t_{HK} is the thickness of the high-κ (Al_2O_3 or HfO_2) layer, $t_{SiO_2}^{phys}$ is the physical SiO_2 thickness, and t_{CL} is the charge-layer thickness in silicon. The physical SiO_2 thickness is constant across all the thickness series (Al_2O_3 and HfO_2 single layers). Additionally, the capacitance values were extracted at various values of fixed charge ($Q = 0$ to $-3\ \mu C\ cm^{-2}$) which ensures that the charge-layer thickness is constant across all thicknesses and in the accumulation region. Therefore, the inverse capacitance at a fixed charge as a function of film thickness should result in a line and the permittivity can be extracted from the slope. This yielded extracted permittivities of 9 and 19 for the Al_2O_3 and HfO_2 thickness series, respectively, as expected for these systems. Note that for the HfO_2 thickness series, thicknesses of 6 nm and higher were used to ensure HfO_2 stabilizes in the dielectric monoclinic phase ($\kappa \approx 18$)[22]. Similarly, the permittivity of the HZH heterostructures was extracted from thickness-dependent MIM *C*–*V* measurements (Fig. 2b). The inverse capacitance is a linear function of the film thickness, and the permittivity can be extracted from the slope.

Electrical interlayer thickness extraction. The thickness of the SiO_2 interlayer was determined not only by TEM (Extended Data Fig. 6a), but also electrically via *C*–*V* measurements of both dielectric HfO_2 and Al_2O_3 thickness series on SiO_2-buffered Si (Extended Data Fig. 6f). The inverse capacitance at a fixed charge as a function of dielectric thickness should result in a line and the capacitance-equivalent thickness (CET) of the SiO_2 interlayer and Si charge layer can be extracted from the *y* intercept. By extracting the CET at different charge values, the *Q*–*V* relation of the SiO_2 interlayer and Si charge layer can be calculated through the following equation

$$V - V_{fb} = \int_0^Q \frac{t_{SiO_2}^{phys} + \frac{t_{CL}\epsilon_{SiO_2}}{\epsilon_{Si}}}{\epsilon_0 \epsilon_{SiO_2}} dQ,$$

where V_{fb} is the flatband voltage (Extended Data Fig. 6b, d). To confirm this methodology, another method for determining the Q–V relation of the SiO_2 interlayer and Si charge layer was extracted from the Q–V relations of both the dielectric HfO_2 and Al_2O_3 thickness series. At a fixed charge, the corresponding voltage values of each thickness were fitted to a line and the y intercept corresponds to the voltage value for the SiO_2 interlayer and Si charge layer Q–V relation (Extended Data Fig. 6c, e). As expected, both methods lead to the same extracted Q–V relation (Extended Data Fig. 6c, e), corresponding to 8 Å EOT (Extended Data Fig. 6f)—close to the SiO_2 physical thickness of 8.5 Å obtained via TEM (Extended Data Fig. 6a)—based on technology computer-aided design simulation (TCAD) Q–V relations of different SiO_2 thicknesses on lightly doped Si.

Hysteretic *C*–*V* measurements. Capacitance–voltage (C–V) measurements on MIM capacitors were performed using a commercial semiconductor device analyser (Agilent B1500) with a multi-frequency capacitance measuring unit. 19-µm W tips (DCP-HTR 154-001, FormFactor) made electrical contact within a commercial probe station (Cascade Microtech); voltage was applied to the W top electrode, and the W bottom electrode was grounded.

Electrical characterization

Benchmarking to HKMG literature. In Fig. 3b, the leakage-equivalent oxide thickness (J_G–EOT) scaling of the negative capacitance multilayer gate stack benchmarked against reported HKMG literature includes references taken from interlayer-scavenged 2-nm HfO_2[16,19,65] (red), high-κ doped HfO_2[19] (grey), and SiO_2/poly-Si[3] (black). In Fig. 3c, the raw mobility of long-channel transistors integrating the negative capacitance multilayer gate stack (blue) is benchmarked against industry-reported long-channel transistors integrating standard 2-nm HfO_2 high-κ dielectric gate stacks (red) of various EOT[42]. In Extended Data Fig. 8d, the normalized mobility versus EOT scaling of the negative capacitance multilayer gate stack benchmarked against reported HKMG literature includes references taken from interlayer-scavenged 2-nm HfO_2[16,19,42] (red) and hybrid silicate-scavenged interlayer[16] (magenta). In Extended Data Fig. 8d, inset, the SiO_2 interlayer thickness versus EOT scaling scatter plot considers the 7.0-Å EOT HZH trilayer to HKMG references which use interlayer scavenging to reduce EOT[16,19,65,66].

Transistor transfer and output characteristics. Transistor I_d–V_g and I_d–V_d characterization of short-channel and long-channel transistors were performed using a commercial semiconductor device analyser (Agilent B1500). 19-µm W tips (DCP-HTR 154-001, FormFactor) made electrical contact within a commercial probe station (Cascade Microtech); voltage was applied to the gate and drain contacts, whereas the source and Si substrate were grounded.

Mobility extraction. The low-field transistor mobility for SOI transistors integrating ~2-nm HZH ferroic multilayers and standard high-κ HfO_2 gate stacks of the same physical thickness (Fig. 3c, Extended Data Fig. 8c) is calculated on the basis of the channel resistance (R_{ch}) and inversion sheet charge density (Q_{inv}), which are extracted respectively from transfer characteristics (I_d–V_{gs}, Extended Data Fig. 8b; V_{gs}, gate-to-source voltage) and from the intrinsic gate capacitance–voltage (C_{gg} versus $V_{gs} - V_{fb}$, Extended Data Fig. 8a) measurements. Given the device aspect ratio of channel length (L) and channel width (W), we have

$$R_{ch}(V_{gs}) = \frac{L}{W} \times \frac{1}{\mu_{eff}(V_{gs}) Q_{inv}(V_{gs})}.$$

First, the channel resistance is extracted at 50-mV drain-to-source bias (V_{ds}) by subtracting the parasitic resistance (R_p) from the measured drain-to-source resistance (R_{ds}).

$$R_{ds}(V_{gs}) = \frac{V_{ds}}{I_d(V_{gs})} = R_{ch}(V_{gs}) + R_p,$$

where R_p is ascribed to the resistance of the source and the drain contacts and the n+ extension regions that are extrinsic to the channel region. When the overdrive voltage ($V_{ov} = V_{gs} - V_T$, where V_T is the threshold voltage) is sufficiently large, R_{ch} is known to be inversely proportional to V_{ov}. Therefore, R_p can be extracted using a linear extrapolation of the $R_{ds} - 1/V_{ov}$ relationship, which is derived from the I_d–V_{gs} (Extended Data Fig. 8b) from which V_T can be characterized with the max-g_m method. Second, the C_{gg} versus $V_{gs} - V_{fb}$ (Extended Data Fig. 8a) is integrated and normalized to the channel area to estimate the inversion charge.

$$Q_{inv}(V_{gs}) \approx \int_{-\infty}^{V_{gs}} \frac{C_{gg}(\upsilon_{gs})}{A} d\upsilon_{gs}.$$

Finally, we combine the above characterizations to obtain the effective mobility (Fig. 3c and Extended Data Fig. 8c).

Transconductance extraction from d.c. measurements. The measured transconductance ($g_m = \partial I_d/\partial V_{gs}$) and the output conductance ($g_{ds} = \partial I_d/\partial V_{ds}$) are affected by the series resistance on the source (R_s) and the drain sides (R_d), as they reduce the voltage drops on the channel region,

$$V_{gs,i} = V_{gs} - I_d R_s,$$

$$V_{ds,i} = V_{ds} - I_d(R_s + R_d),$$

where $V_{gs,i}$ and $V_{ds,i}$ are the gate-to-source and the drain-to-source voltages intrinsic to the channel, respectively. $R_s \approx R_d \approx R_p/2$ because the transistor is symmetric. R_p can be extracted from the $R_{ds} - 1/V_{ov}$ relationships as discussed in Methods section 'Mobility extraction'. Besides, devices with different gate length (L_G) series are fabricated on silicon-on-insulator (SOI) wafers, which enables another extraction method with R_{sd}–L_G relations. At low V_d and a given V_{ov}, Q_{inv} and μ_{eff} are unchanged across different L_G if short-channel effects are not considerable, making R_{ch} proportional to the channel length. Such condition is confirmed by the consistency of V_T across measured L_G (Extended Data Fig. 10a). Therefore, the L_G offset as well as the R_p can be found at the intersection of the linear relations of R_{sd}–L_G with different V_{ov} (Extended Data Fig. 10c). The two R_p extraction methods yield consistent results.

The following equation is solved to extract the intrinsic $g_{m,i} = \partial I_d/\partial V_{gs,i}$ and $g_{ds,i} = \partial I_d/\partial V_{ds,i}$ without the degradation due to R_s and R_d.

$$\begin{pmatrix} 1 - g_m R_s & -g_m(R_s + R_d) \\ -g_{ds} R_s & 1 - g_{ds}(R_s + R_d) \end{pmatrix} \begin{pmatrix} g_{m,i} \\ g_{ds,i} \end{pmatrix} = \begin{pmatrix} g_m \\ g_{ds} \end{pmatrix},$$

where g_m and g_{ds} are measured, and $R_s \approx R_d \approx R_p/2$ from the above-discussed characterizations. Using this methodology, the intrinsic $g_{m,i}$ and intrinsic $g_{ds,i}$ are extracted (Fig. 3g and Extended Data Fig. 10d, e).

Transconductance extraction from radio-frequency measurements. Scattering parameters (S parameters) for $L_G = 1$ µm bulk transistors (henceforth referred to as the device under test, DUT) at various d.c. biases as well as open and short structures (Extended Data Fig. 9a) are measured using a Keysight E8361C network analyser in conjunction with a Keysight 4155C semiconductor parameter analyser. The devices were measured using low-contact-resistance Infinity Series probes. To calibrate the measurement setup, a

line-reflect-reflect-match (LRRM) calibration was performed with a Cascade Microtech Impedance Standard. Following calibration, S parameters were measured for each of the DUT, open and short structures. These measured S parameters were converted to admittance parameters (Y parameters), Y_{DUT}, Y_{open} and Y_{short}. To remove the effects of parasitic shunt pad capacitance and series pad resistance and inductance of the DUT, the following de-embedding process was followed. First, to decouple the effect of shunt parasitic capacitances, the Y parameters of the open structure (Y_{open}) are subtracted from the Y parameters of the DUT and short structure, and then are converted to impedance parameters (Z parameters):

$$Z_1 = (Y_{DUT} - Y_{open})^{-1},$$

$$Z_2 = (Y_{short} - Y_{open})^{-1}.$$

Next, to decouple the effect of series pad resistance and inductance of DUT, Z_2 is subtracted from Z_1 and the resulting difference is converted back to admittance parameters, Y_{corr}:

$$Y_{corr} = (Z_1 - Z_2)^{-1}.$$

Y_{corr} represents the de-embedded admittance parameters of the DUT. This de-embedding procedure is schematically represented in Extended Data Fig. 9a.

To extract the transconductance (g_m) from the de-embedded admittance parameters, a small-signal model of the transistor was assumed (Extended Data Fig. 9b). Under this small-signal model, the Y parameters can be written in terms of model parameters and frequency (assuming $R_s = R_d = 0$, $C_{gg} = C_{gs} + C_{gd}$, and $4\pi^2 C_{gg}^2 R_g^2 f^2 \ll 1$)

$$\begin{aligned}
Y_{11} &= 4\pi^2 C_{gg}^2 R_g f^2 + j2\pi f C_{gg},\\
Y_{12} &= -4\pi^2 C_{gd} C_{gg} R_g f^2 - j2\pi f C_{gd},\\
Y_{21} &= g_m - 4\pi^2 C_{gd} C_{gg} R_g f^2 + j2\pi f (C_{gd} + g_m R_g C_{gg}),\\
Y_{22} &= g_{ds} + 4\pi^2 C_{gd} R_g \left(C_{gd} + C_{gg} g_m R_g\right) f^2\\
&\quad + j2\pi f (C_{ds} + C_{gd} + C_{gd} g_m R_g).
\end{aligned}$$

The transconductance (g_m) can therefore be extracted at a fixed d.c. bias via the following relation (Fig. 3h, Extended Data Fig. 9c).

$$g_m = \mathrm{Re}(Y_{21})|_{f^2=0}.$$

Reliability. Positive-bias temperature instability (PBTI) measurements were performed on bulk nMOSFET devices integrating the ~2-nm mixed-ferroic HZH and conventional high-κ dielectric HfO_2 gate stacks at 85 °C at electric fields up to 9 MV cm^{-1} (Extended Data Fig. 8f, g). A measure–stress–measure (MSM) voltage scheme (Extended Data Fig. 8e) was used to apply the PBTI bias, where the drain current was measured with a minimized delay time (600 µs) at V_{ds} = 50 mV to minimize the recovery effect[67]. The measured drain current was then converted to a ΔV_T shift by comparing it to the drain current measured on the virgin device. Additionally, the time exponent, n, was extracted by noting that[67] $\Delta V_T = At^n$. The extracted time exponent, n, was found to similar to those reported in literature for high-κ HfO_2 stacks[67], which is expected considering the reliability characteristics are predominantly determined by the interfacial oxide and interfacial-high-κ interface[46]; both stacks with different EOT have HfO_2 sitting on the same SiO_2 interfacial (Extended Data Fig. 1). Furthermore, the d.c. lifetime[67]—the stress time needed to induce a 50-mV ΔV_T shift—was extracted as a function of electric field from the PBTI measurements for the HZH and HfO_2 gate stacks. Both HZH and HfO_2 show comparable rates of degradation as a function of field (Extended Data Fig. 8h), which is expected for the aforementioned reasons related to the consistent SiO_2 interfacial.

Additionally, the extracted time exponent for HZH (n = 0.14, Extended Data Fig. 8f) is closer to the ideal value[67] of n = 0.16 compared to HfO_2 (n = 0.10, Extended Data Fig. 8g), indicating that there are initially a smaller number of interface traps for HZH. When field stress is applied, trap generation accelerates until the number of traps reaches a certain threshold beyond which it eventually saturates. As a result, the relative degradation is larger for HZH at smaller fields, although the absolute degradation is always slightly smaller than HfO_2. This can also be seen directly from the extracted d.c. lifetimes (Extended Data Fig. 8h) as the d.c. lifetime is slightly better for HZH at intermediate field stresses before it becomes similar to HfO_2 at high field stresses. We again note that extracted n values are similar to what has been reported in literature for HfO_2-based high-κ metal gate stacks[67].

Stress measurements were also performed on lightly doped p-type MOS capacitors with the ~2-nm mixed-ferroic HZH and conventional high-κ dielectric HfO_2 gate stacks at room temperature (Extended Data Fig. 8i, j) at $V_g - V_{fb}$ = −1 V. The stresses were applied again with a MSM voltage scheme, where the accumulation C–V was measured in between bias application at 500 kHz. The stress-induced effect was found to be minimal (Extended Data Fig. 8i, j) and no EOT degradation was observed after 10^3 s of stress at $V_g - V_{fb}$ = −1 V (Extended Data Fig. 8i, j).

Charge boost measurements. Pulsed charge–voltage measurements (Extended Data Fig. 7) were conducted on p-Si/SiO_2 /HZH (2 nm)/TiN/W capacitor structures to extract the energy landscape of the ferroic HZH heterostructure, following the measurement scheme detailed in previous works[26,68–70]. The capacitor structures were connected to an Agilent 81150A pulse function arbitrary noise generator and the current and voltage was measured through an InfiniiVision DSOX3024A oscilloscope with 50-Ω and 1-MΩ input impedances, respectively. Short voltage pulses (500 ns) with increasing amplitudes were applied to the capacitor (Extended Dat a Fig. 7c). From the integration of the measured disch arging current, a charge versus voltage relationship was extracted (Extended Data Fig. 7d). The voltage was calculated by $\max(V - IR)$, where V is the applied voltage pulse, I is the measured current, and R is a combination of the oscilloscope resistance (50 Ω) and parasitic resistances associated with the set-up and lightly doped substrate (220 Ω). Fast voltage pulses were applied in order to minimize charge injection into the FE–dielectric interface, which could mask the observation of the negative capacitance regime[26,69]. Additionally, short voltage pulses help prevent electrical breakdown of the SiO_2 layer. The Q–V relation of the series capacitance of the SiO_2 interlayer and Si charge layer was determined via thickness-dependent C–V measurements of Al_2O_3 and HfO_2 (Extended Data Fig. 6, Methods section 'Electrical interlayer thickness extraction'), which corresponded to 8-Å SiO_2 on lightly doped Si. The charge boost was calculated by integrating the difference between the Q–V relations of the 2-nm HZH heterostructure and the series combination of the SiO_2 interlayer and the Si charge layer (Extended Data Fig. 7e).

To determine the polarization–electric field (P–E_F) relation of just the 2-nm HZH heterostructure (Extended Data Fig. 7f), the electric field across the ferroic HZH heterostructure was calculated by subtracting the voltage across the series capacitance of the SiO_2 interlayer and Si charge layer (V_d) at a fixed charge value,

$$E_F = \frac{1}{t}(V - V_d),$$

where t is the thickness of the HZH heterostructure.

Modelling

Energy landscape considerations. One can write the total free energy (F) of the system as:

$$F=\int_V (f_{\text{bulk}}+f_{\text{elas}}+f_{\text{elec}}+f_{\text{grad}})\,\mathrm{d}V,$$

where V is the volume, f_{bulk} is the bulk free energy (Landau), f_{elas} is the elastic energy density, f_{elec} is the electrostatic energy density, and f_{grad} is the gradient energy density.

For the laterally arranged mixed FE–AFE phase present in our material, all of the above terms are important, especially the gradient terms, which are by default present owing to the mixed polar–nonpolar (FE–AFE) phase distribution. Additionally, heterogeneous elastic energies in structurally inhomogeneous systems—such as our mixed orthorhombic–tetragonal (FE–AFE) system—have been shown to destabilize long-range polarization, leading to suppressed polarization and a flattened energy landscape[28,71]. Furthermore, considering that the polarization in our films has an in-plane component (as described in the text), this leads to an additional depolarization field on the FE grains, similar to an FE–dielectric heterostructure (albeit in the in-plane direction). At low electric fields, the mixed FE–AFE behaviour is analogous to an FE–dielectric (polar–nonpolar) heterostructure—owing to the nonpolar parent structure of fluorite-structure antiferroelectricity—which has been shown to impart depolarization fields on the FE layer[25,72]. The laterally intertwined nonpolar–polar phases present in the ultrathin HZH heterostructure are conducive to flattening the FE energy landscape through the aforementioned depolarization fields[26–28] (Fig. 1a).

Overall, the above contributions all lead to a suppression of the bulk polarization via depolarization fields. As it has been shown[26–28], the depolarization field essentially flattens the bulk energy landscape for the FE ($E_{\text{d}} \propto -P$, hence $\mathbf{E}\cdot\mathbf{P}>0$) and leads to a permittivity enhancement ($\varepsilon \propto (\partial^2F/\partial D^2)^{-1}$). Depolarization field-induced flattening of the energy landscape is also the underlying physics of the negative capacitance effect[26,27,29,30,49].

Technology computer-aided design simulations. The measured C–V curves are calibrated to Sentuarus technology computer-aided design simulations (TCAD) device simulator which solves the electrostatics, electron and hole transport, and the quantum confinement effect self-consistently[73]. MOS capacitors with 10^{15} cm^{-3} p-type substrate doping and planar SOI MOSFETs are simulated with finite-element methods. The EOT and the metal work function (φ_{m}) are the only two parameters that are fit to the MOS capacitor measurement results, yet the slope of the accumulation capacitance can be successfully captured by the model (Fig. 2f, Extended Data Fig. 6). Similarly, the intrinsic C_{gg} versus $V_{\text{gs}}-V_{\text{fb}}$ extracted from SOI transistors can be successfully model by the TCAD model with appropriate EOT and φ_{m} (Extended Data Fig. 8a).

Atomic-scale HZH mixed-ferroic heterostructure

Thickness limits and atomic-scale heterostructures. Recent perspectives on HfO_2-based ferroelectricity for device applications[9,74–77] posed the technological challenges stemming from thickness limit concerns of HfO_2-based ferroelectricity, and thereby, negative capacitance. The use of short-period superlattices, that is, nanolaminates, is common in the high-κ field to enhance permittivity[78–82]; in particular, rutile-structure TiO_2 is often paired with fluorite-structure HfO_2 and/or ZrO_2 in dynamic random-access memory (DRAM) capacitors[83]. Recently, fluorite-structure nanolaminates were used to tune the FE behaviour of HZH films[84–86]. However, all of these works have studied nanolaminates with thick periodicity, going as thin as 10 ALD cycles (~1.1 nm) per superlattice sublayer[84]. In this work, we scale down to a much thinner thickness limit while still maintaining physical separation of the individual layers (Extended Data Fig. 1). The reasoning behind using a short-period superlattice structure to scale down the ferroic behaviour of HZH rather than simply thinning down a solid solution stems from the notorious thickness-dependent FE behaviour in Zr:HfO_2 at fixed composition[38,57,63]. Here, the use of nanolaminated structures can help provide thickness-independent scaling of ferroic order, as has been previously demonstrated to overcome the upper thickness limit of HfO_2-based ferroelectricity[86]. The persistence of high capacitance for these 2-nm films is notable considering that other high-κ dielectric systems suffer from considerable permittivity degradation in the thin film (sub-10 nm) regime, particularly TiO_2- and $SrTiO_3$-based oxides[83,87]. Sustaining the mixed ferroic order underlying negative capacitance to the 2-nm regime is extremely relevant for advanced technology nodes[88] which budget only ~2 nm for the oxide layer.

Iso-structural polycrystalline multilayer. Previous attempts to heterostructure FE Zr:HfO_2 with dielectric Al_2O_3[26,69,70] failed to demonstrate capacitance enhancement, which was attributed to the fixed charges at the FE–dielectric interface. These charges can screen the FE polarization, pushing the stable point of the energy well to one the minimum points, and thereby preventing stabilization of negative capacitance regime via depolarization fields from the dielectric. Here, the use of iso-structural HZH to serve as both the nonpolar (AFE) and polar (FE) layers and leveraging the high (low) onset crystallization temperature of HfO_2 (ZrO_2) on Si[50], enables interfaces with diminished defects, allowing for the polar layer to experience the depolarization fields and stabilize in the 'forbidden' negative capacitance regime. Regarding the polycrystalline nature of the ultrathin multilayers, it has been experimentally[48] and theoretically[89] established that negative capacitance can be stabilized in the presence of FE domains, as recently reviewed[76].

Data availability

The experimental data contained in the manuscript are available for download at https://doi.org/10.5281/zenodo.5797030.

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Author contributions S.S.C. and S.S. designed the research. S.S.C. performed design, synthesis, and optimization of the superlattice oxide heterostructure and its ferroic characterization. N.S. and C.-H.H. performed capacitor fabrication. C.-H.H. helped optimize annealing treatments. N.S. and S.S.C. performed capacitor measurements and analysis. L.-C.W. fabricated the transistors and performed d.c. characterization. D.W.K. and J.B. developed the initial processes for transistor fabrication. Y.-H.L. performed simulations including EOT estimation, series resistance determination and mobility and transconductance analysis. M.S.J., J.G. and W.L. contributed to radio-frequency electrical measurements and analysis. N.S. performed MOSCAP stress measurements. W.C. and N.S. performed MOSFET reliability measurements under the guidance of S.D., S.M. and S.S. M.M., R.R., C.S., D.P., G.P., M.C. and B.T. contributed to capacitor fabrication and characterization at MIT LL. S.-L.H. performed TEM. S.S.C. and S.-L.H. performed TEM analysis. Y.R. performed second-harmonic generation. S.K.V. performed X-ray photoelectron spectroscopy. S.S.C. and C.-H.H. performed synchrotron soft X-ray spectroscopy at ALS. S.S.C., V.A.S. and J.W.F. performed synchrotron X-ray spectroscopy at APS. S.S.C., C.-H.H., V.A.S. and Z.Z. performed synchrotron in-plane diffraction at APS. S.S.C. and N.S. performed synchrotron X-ray reflectivity and 2D diffraction at SSRL. S.S.C. and S.S. co-wrote the original manuscript; S.S.C., N.S. and S.S. revised the manuscript. S.S. supervised the research. All authors contributed to discussions and manuscript preparations.

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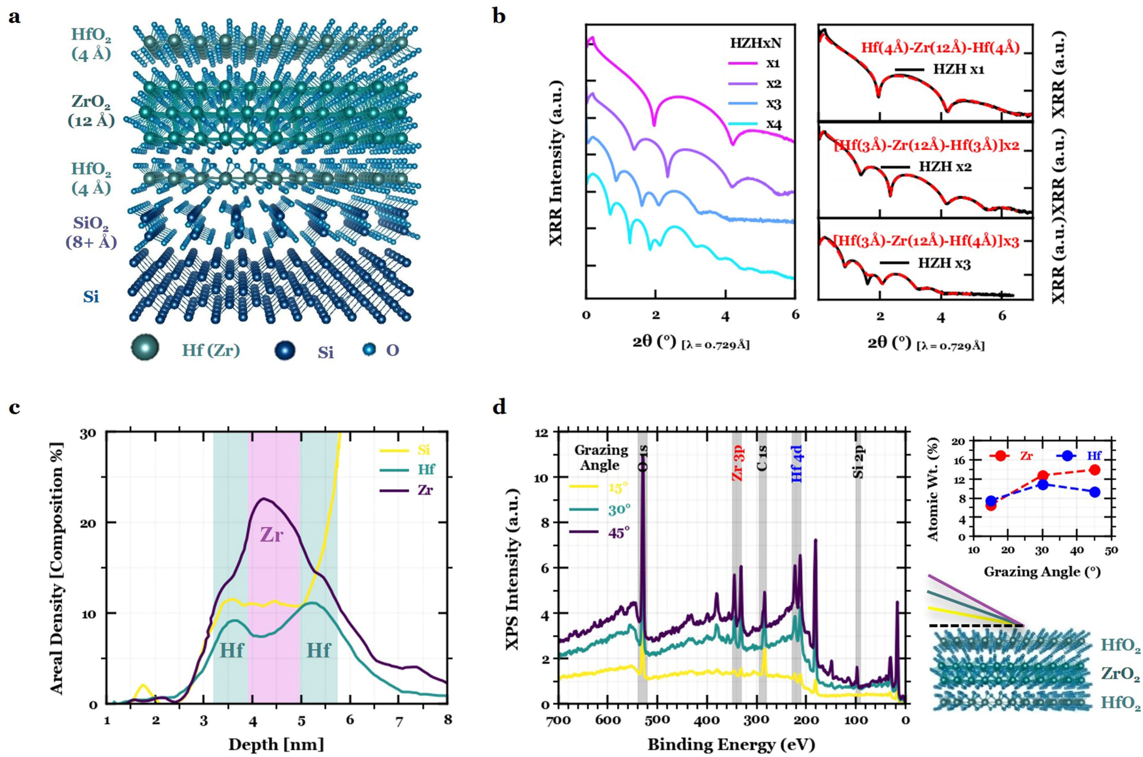
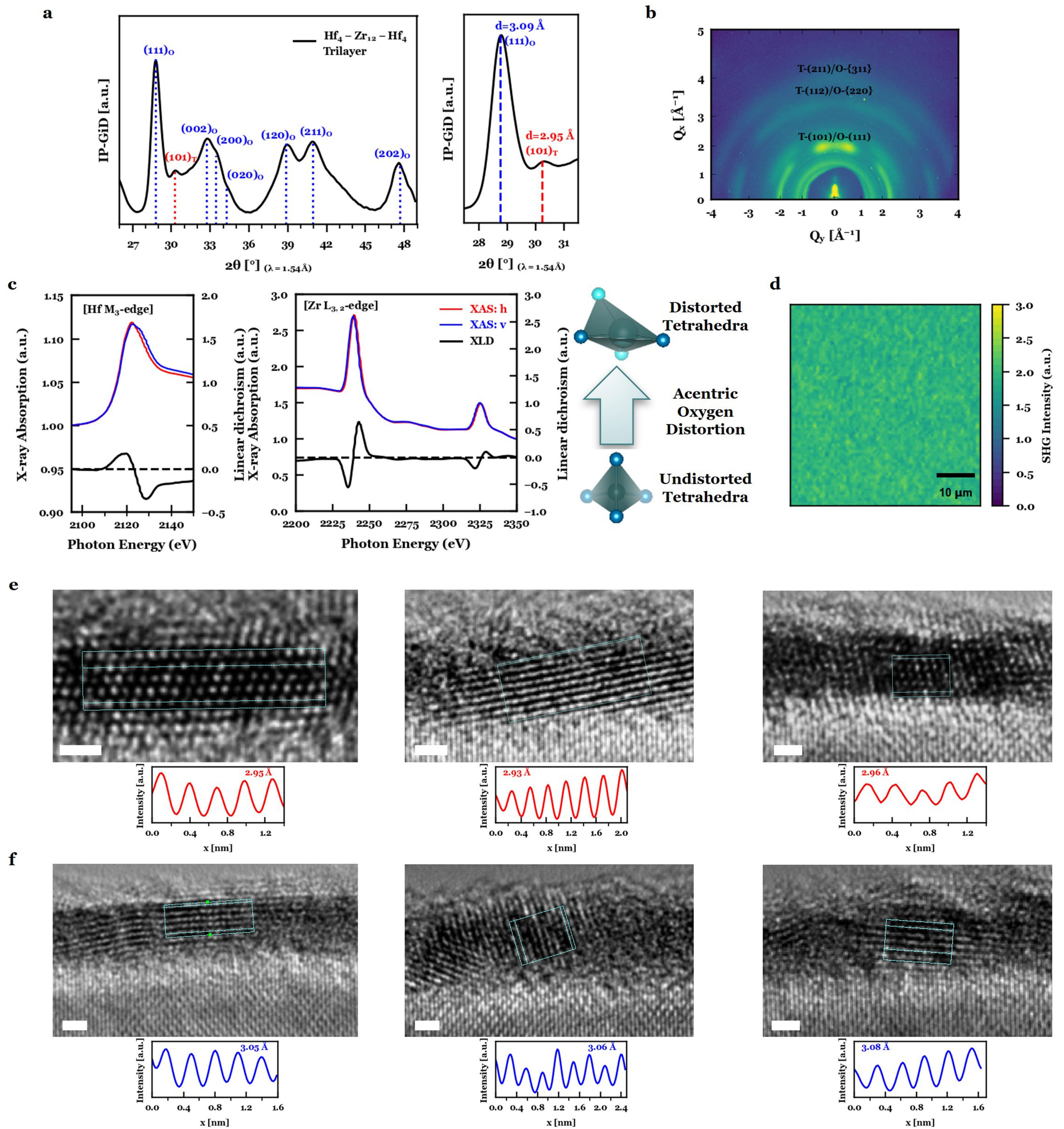
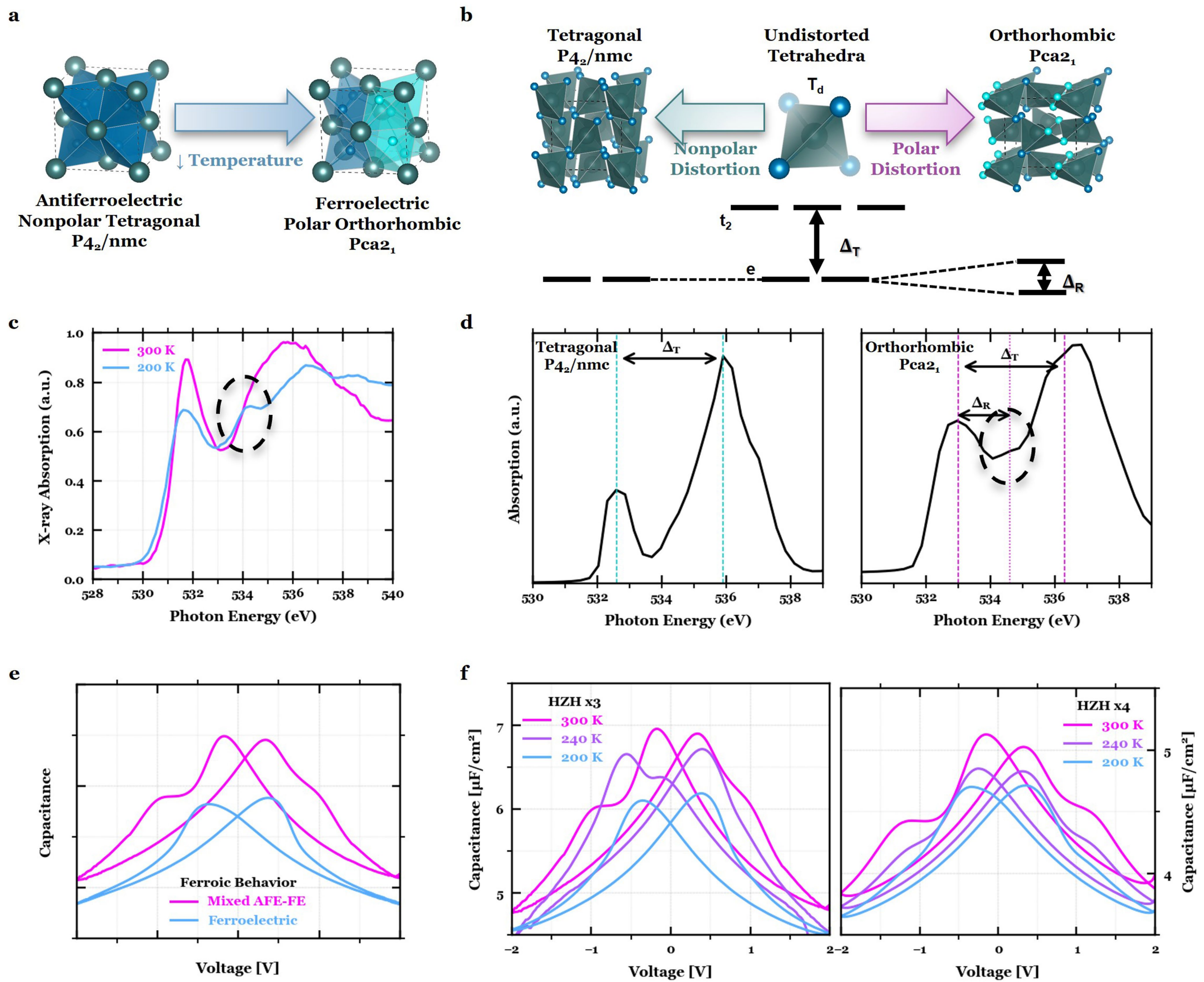


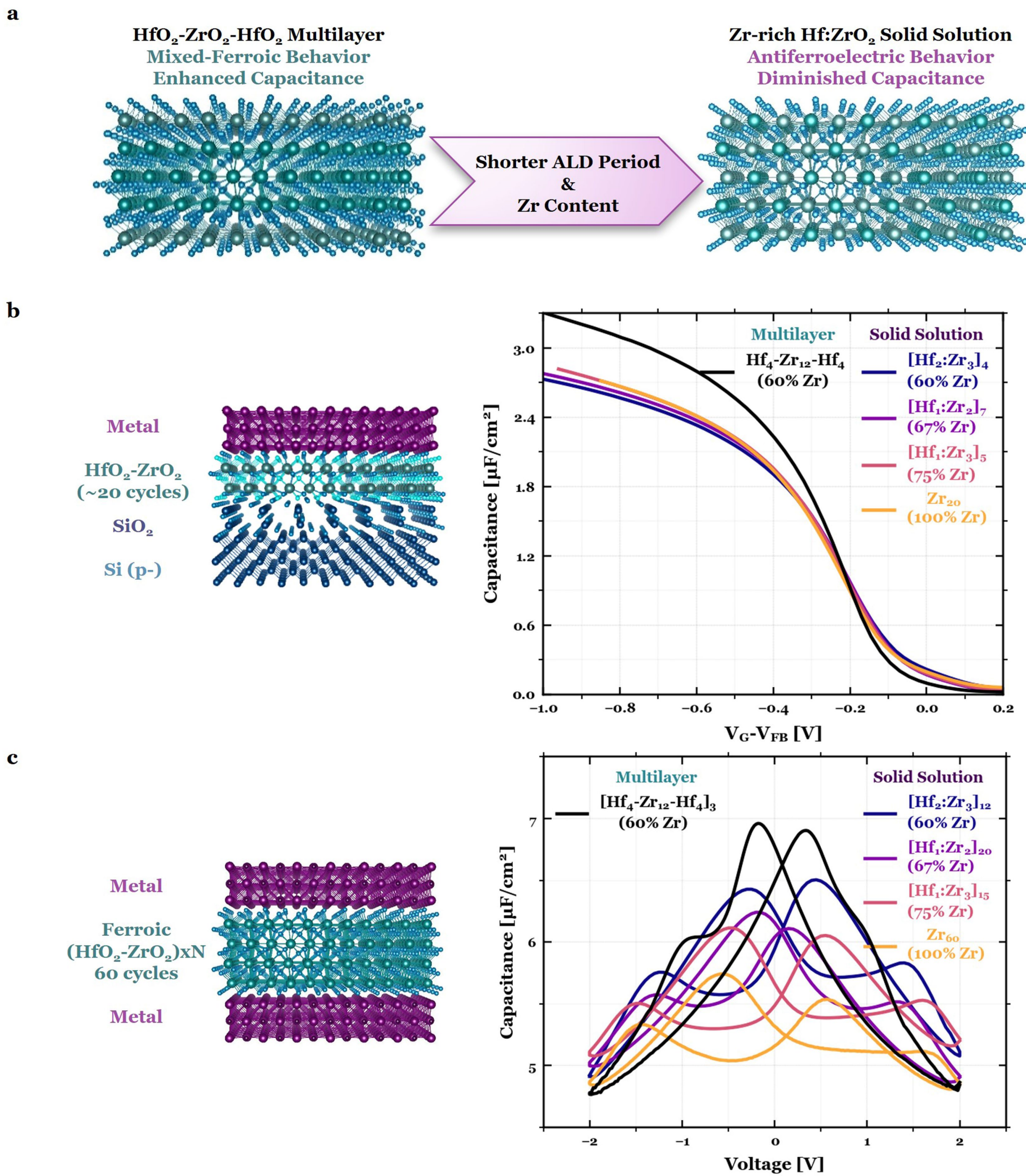
Extended Data Fig. 1 | Atomic-scale multilayer structure. a, Schematic of the HfO_2–ZrO_2 multilayer structure on SiO_2-buffered Si. **b**, Synchrotron X-ray reflectivity (XRR) of thicker HZH heterostructures (left) repeated with the same periodicity as the thinner trilayer structure; XRR fitting (right) demonstrates the presence of well separated HfO_2–ZrO_2 layers, that is, not a solid solution, for three different multilayer repeats of fixed periodicity, all approximately following the expected 4 Å–12 Å–4 Å HZH structure. **c**, Layer-resolved electron energy loss spectroscopy (EELS) of the 2-nm HZH trilayer, demonstrating clear separation of HfO_2 and ZrO_2 layers. The exact layer thicknesses are extracted from XRR, which spans a wider sample footprint, rather than the local EELS measurement in which the apparent width increase can be due to beam spreading and local thickness variation. **d**, Angle-resolved X-ray photoelectric spectroscopy (XPS) of the 2-nm HZH trilayer (left) and the extracted atomic composition (right). The presence of increasing Zr content as the grazing angle increases is expected from the multilayer structure in which Zr content increases after the surface Hf-rich layer. Therefore XRR, EELS and XPS data all indicate the presence of a multilayer structure in which the HfO_2 layer is directly on the SiO_2 layer.



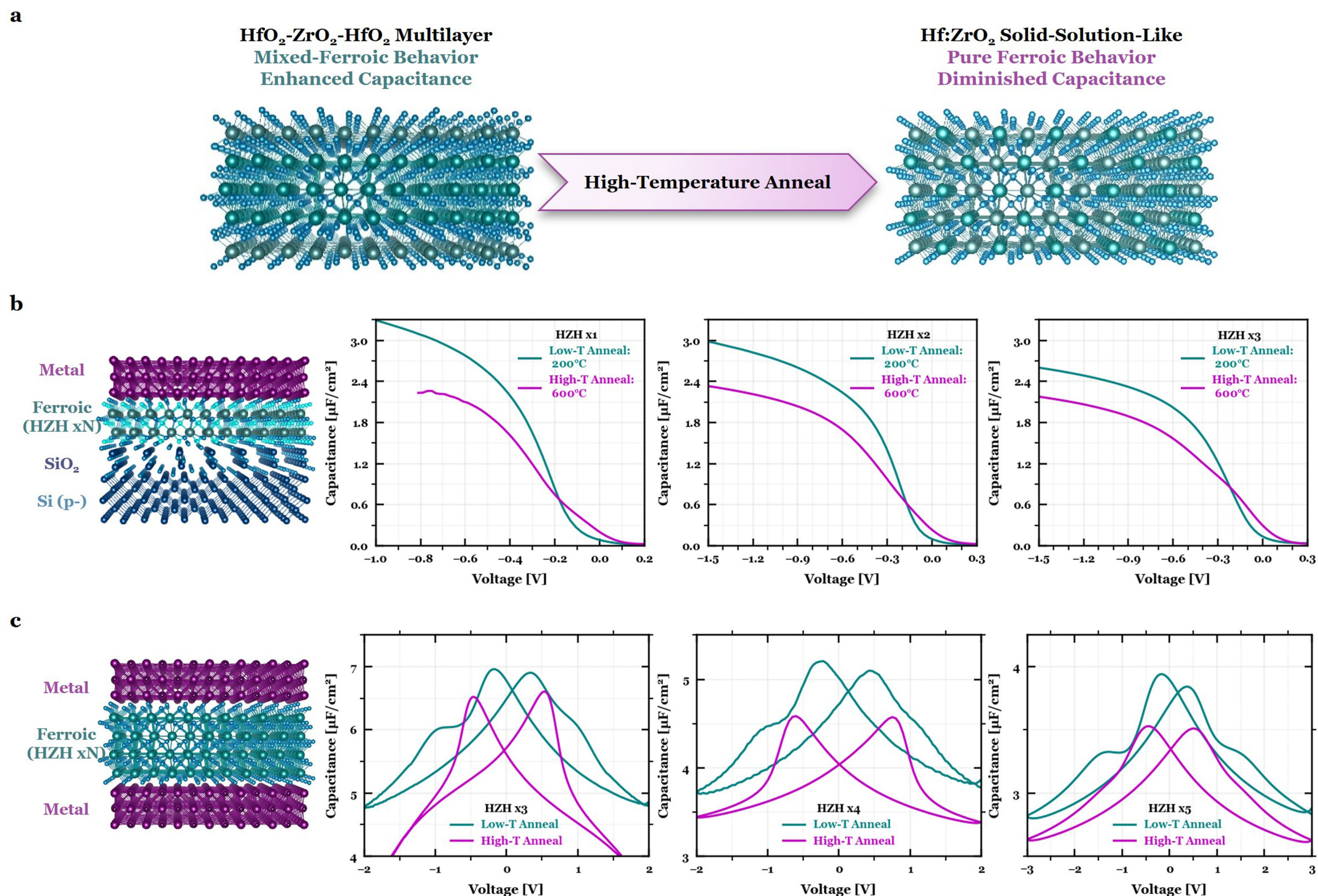
Extended Data Fig. 2 | Ferroic phase insights from structural characterization. **a**, Left, in-plane synchrotron grazing-incidence diffraction (IP-GiD) of a bare 2-nm HZH trilayer indexed to the tetragonal $P4_2/nmc$ and orthorhombic $Pca2_1$ phases. Right, magnification of the spectrum about the orthorhombic $(111)_o$ and tetragonal $(101)_t$ reflections, confirming the co-existing structural polymorphs in the 2-nm film. These two peaks were differentiated via self-consistent indexing of the entire spectrum, in which interplanar lattice spacings—determined from the $\{200\}_o$ family of reflections—closely match the *d* spacings for all other reflections—$(111)_o$, $(120)_o$, $(211)_o$, $(202)_o$—determined by Bragg's law (Methods). **b**, Two-dimensional reciprocal space map of the bare 2-nm HZH trilayer, indexed by integrating the diffraction spectrum. The lack of fully polycrystalline rings illustrates that the 2-nm HZH trilayer is highly oriented, consistent with TEM imaging. **c**, Synchrotron spectroscopy (XAS) of the bare 2-nm HZH trilayer at the Hf M_3 edge (left) and Zr $L_{3,2}$ edge (centre); right, the presence of linear dichroism (orbital polarization) provides further evidence of symmetry-breaking in these oriented thin films. **d**, Second harmonic generation (SHG) mapped across the bare 2-nm HZH trilayer; the presence of SHG intensity confirms broken inversion symmetry in these ultrathin ferroic films. **e**, **f**, Additional cross-sectional TEM providing complementary evidence of the tetragonal $P4_2/nmc$ (**e**) and orthorhombic $Pca2_1$ (**f**) phases, in which the extracted $(101)_t$ lattice spacing (~2.95 Å) and $(111)_o$ lattice spacing (~3.08 Å) extracted from IP-GiD are consistent with the average lattice spacings extracted from the periodicity of the TEM-imaged planes. The white scale bars in all the TEM images represent 1 nm.



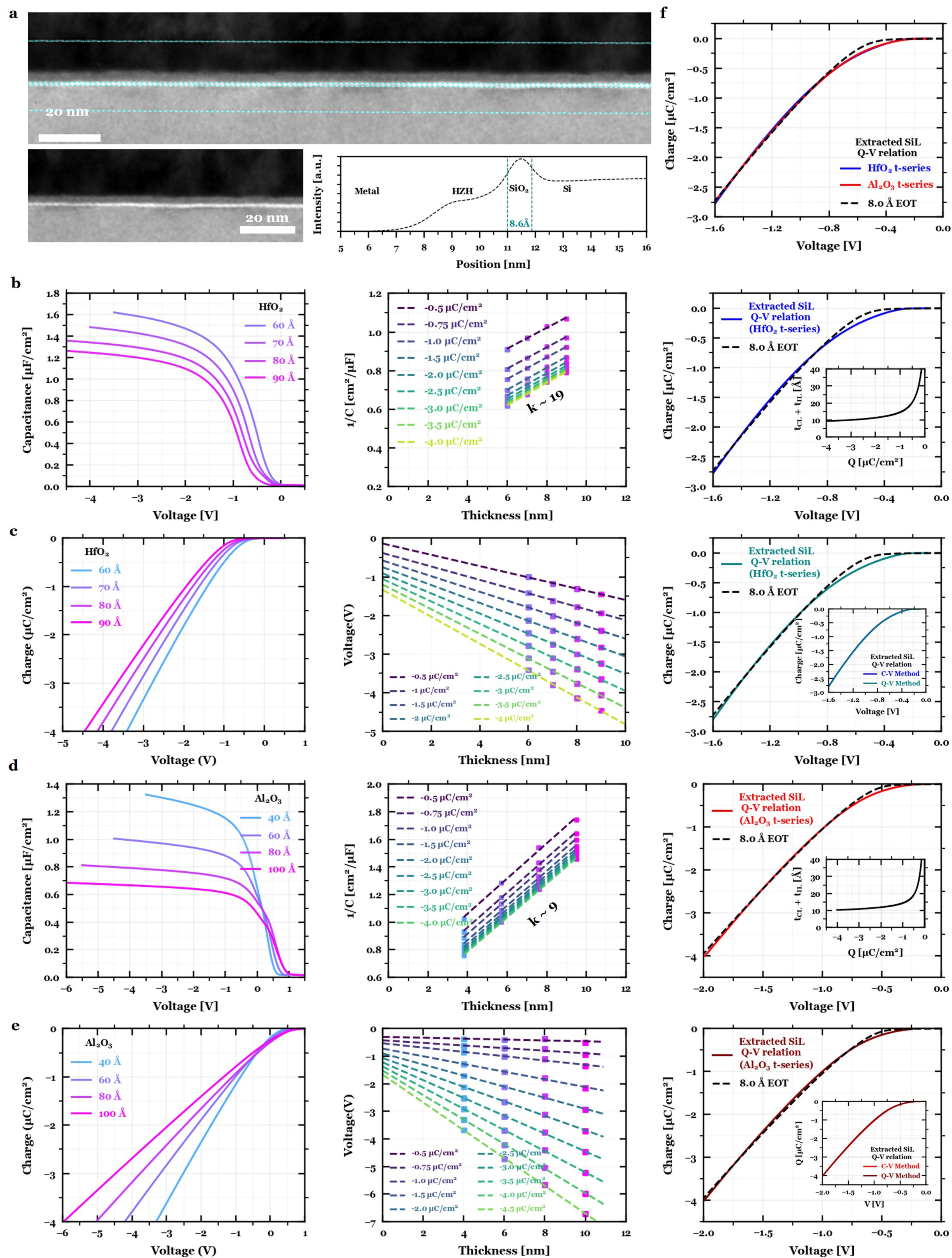
Extended Data Fig. 3 | Ferroic phase insights: proximity to temperature-dependent phase transition. **a**, Schematic of temperature-dependent AFE–FE phase evolution in fluorite-structure oxides. At lower temperatures, the higher symmetry tetragonal phase is expected to transition to the lower symmetry orthorhombic phase. **b**, Schematic crystal field splitting diagram for fluorite-structure polymorphs; the symmetry-induced *e*-splitting (rhombic distortion, Δ_R), besides the typical t_2-e splitting (tetrahedral distortion, Δ_T) present in all fluorite-structure phases, provides a spectroscopic signature for the polar O phase (Methods). **c**, Temperature-dependent XAS at the oxygen K edge for a 2-nm HZH bare film demonstrating clearer spectroscopic signatures of the FE O phase emerge slightly below room temperature. **d**, Simulated oxygen K-edge XAS spectra (Materials Project) for the respective O and T phases. XAS provides spectroscopic signatures to distinguish between the O and T phases (difficult to resolve from GI-XRD). **e**, Prototypical *C*–*V* behaviour for mixed AFE–FE (shoulder-like features in addition to the characteristic butterfly-like shape) and FE films (just butterfly-like) in MIM capacitor structures. **f**, Temperature-dependent *C*–*V* for thicker HZH multilayers of the same periodicity (in MIM capacitor structure) demonstrating an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room temperature. Thinner HZH multilayers films suffer from leakage limitations, preventing such hysteretic *C*–*V* measurements. The thicker HZH multilayers of the same periodicity—annealed at the same low-temperature condition to maintain the multilayer structure—demonstrate a similar mixed ferroic to FE phase transition slightly below room temperature as the thinner 2-nm multilayer (c).



Extended Data Fig. 4 | Solid solutions versus superlattice structure: role of ALD period and Zr content. a, Schematic of HZH multilayer and Zr-rich Hf:ZrO_2 solid-solution films. With shorter ALD periods, the mixed FE–AFE multilayer structure transitions towards a Hf:ZrO_2 solid solution with AFE-like behaviour. In the solid-solution state, the loss of the mixed ferroic order yields diminished capacitance, owing to the lack of mixed-ferroic-induced capacitance enhancement (Fig. 1a). **b**, MOS accumulation *C*–*V* of the HZH trilayer (60% Zr) compared to solid-solution films of the same thickness (2 nm) and composition (60% Zr), as well as solid-solution films of the same thickness and higher Zr composition (67%–100% Zr). **c**, MIM *C*–*V* hysteresis loops of the HZH superlattice (60% Zr) compared to solid-solution films of the same thickness (6 nm) and composition (60% Zr), as well as solid-solution films of the same thickness and higher Zr composition (67%–100% Zr). Hf:ZrO_2 solid-solution films with higher Zr content (60%–75%) are around the range attributed to the 'MPB' in thicker Hf:ZrO_2 alloys[35,55,90–93]. These results indicate that the capacitance enhancement in multilayer films is not simply driven by Zr content[32,38,57,63], but instead the atomic-scale stacking, as the solid-solution films with subatomic superlattice period do not demonstrate the same mixed-ferroic behaviour and enhanced capacitance as the superlattices.

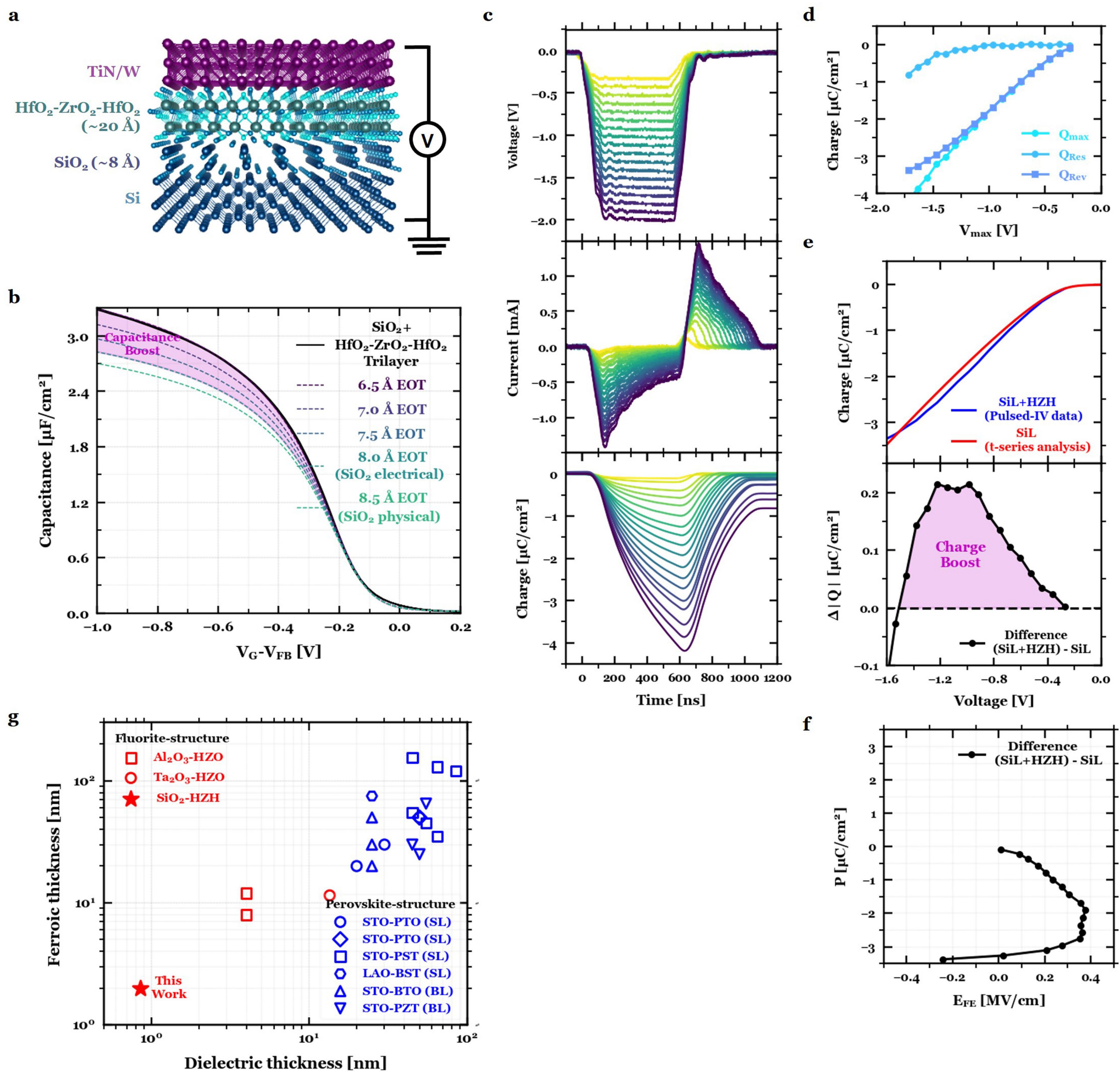


Extended Data Fig. 5 | Solid solutions versus superlattice structure: role of annealing temperature. a, Schematic of HfO_2–ZrO_2 multilayer and Hf:ZrO_2 solid-solution films. Under a high-temperature anneal, the multilayer structure transitions towards a Hf:ZrO_2 solid-solution-like structure demonstrating more FE-like behaviour. The solid-solution state yields diminished capacitance owing to the lack of both the higher-permittivity AFE phase and the mixed-ferroic-induced capacitance enhancement (Fig. 1a). **b**, Comparison of MOS capacitor accumulation *C*–*V* characteristics in HZH multilayers, where the superstructure was repeated (left) one, (centre) two, or (right) three times, under both low- and high-temperature anneals. **c**, Comparison of mixed-ferroic behaviour in low-temperature treated MIM HZH multilayers versus FE behaviour in the same multilayers annealed at high temperatures, where the superstructure was repeated (left) three, (centre) four, or (right) five times. In all instances, the high-temperature anneal (>500 °C) results in diminished accumulation capacitance compared to the low-temperature anneals, as the multilayered mixed-ferroic films presumably transition to more FE-like solid-solution alloys.

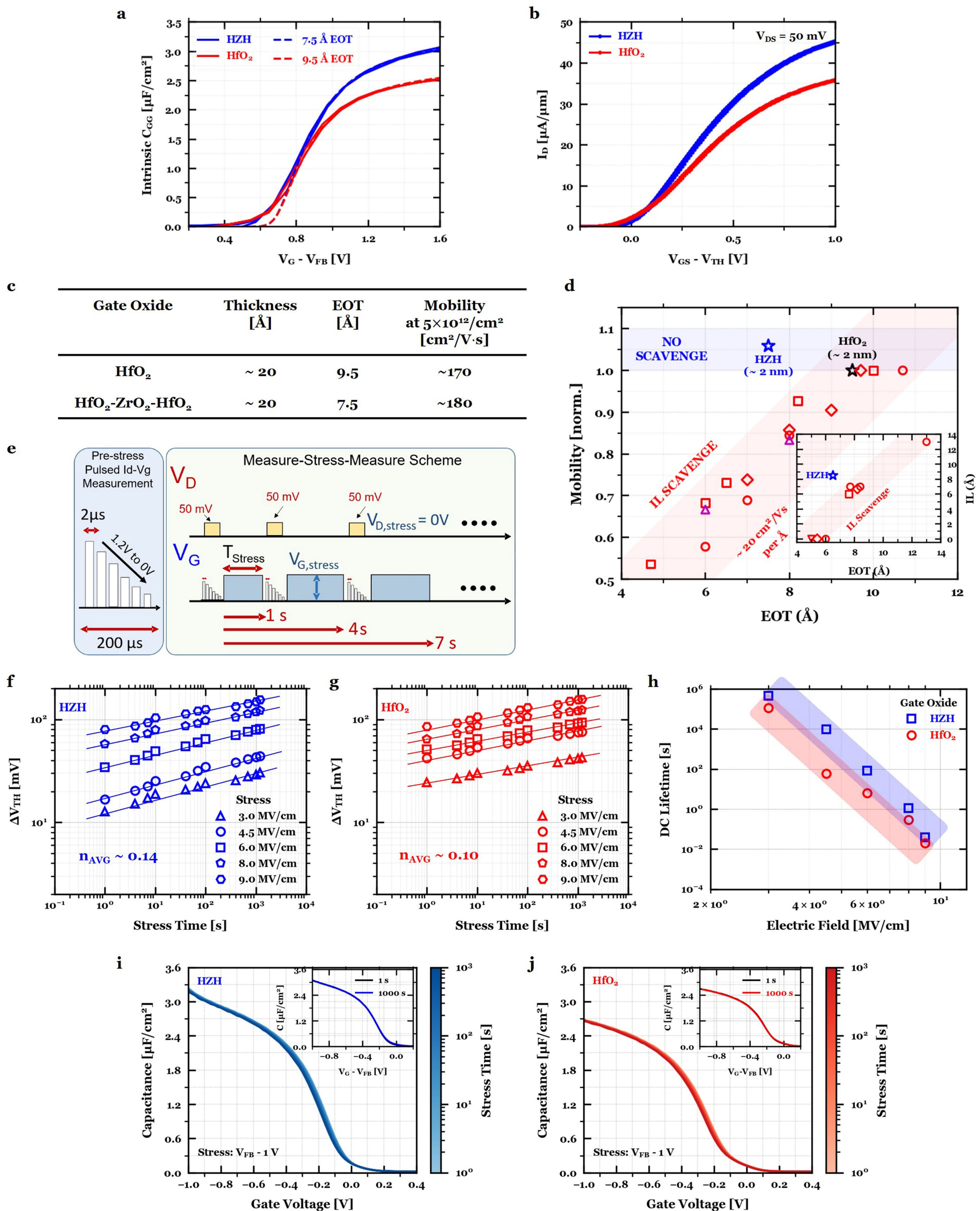


Extended Data Fig. 6 | See next page for caption.

Extended Data Fig. 6 | SiO_2 interlayer thickness. a, Wide field-of-view (FOV) cross-sectional TEM images of the HZH multilayer structure and its corresponding intensity line scan (bottom right) averaged across the entire top cross-sectional image FOV (~150 nm, teal-coloured box). Note the vertical teal-coloured lines in the intensity line scan correspond to the inner teal-coloured box in the wide-FOV image, which delineate the SiO_2 interlayer boundaries. The bottom cross-sectional TEM image highlights the thin SiO_2 interlayer (white region) without obfuscation by the teal-coloured box. A physical SiO_2 thickness of 8.6 Å is extracted from analysis of the averaged intensity line scan of the wide FOV TEM (Methods). **b**, **d**, C–V measurements of HfO_2 (**b**) and Al_2O_3 (**d**) thickness series in MOS capacitor structures (left), extracted inverse capacitance versus thickness at different charge values (centre), and extracted Q–V relation Si charge layer and SiO_2 interlayer (SiL; right), which fits to TCAD simulations for 8.0 Å SiO_2. The SiL Q–V relation was found by integrating the extracted capacitance equivalent thickness of SiL versus charge (right, inset). This electrical interlayer thickness (8.0 Å) is slightly less than the physical thickness determined by TEM (8.6 Å). As a sanity check, the extracted permittivity from this methodology for HfO_2 and Al_2O_3 corresponds to 19 and 9, respectively, as is expected (Methods section 'Permittivity extraction'). **c**, **e**, Q–V curves for HfO_2 (**c**) and Al_2O_3 (**e**) thickness series obtained from integrating MOS C–V measurements (left), extracted voltage versus thickness at various charge values (centre), and extracted Q–V relation of SiL (right). The SiL Q–V relation is consistent with the Q–V relation extracted from the C–V data (inset). **f**, Consistency in the SiL Q–V relation extracted from the C–V data from both the HfO_2 and Al_2O_3 thickness series, which both fit to 8.0 Å SiO_2 interlayer thickness.

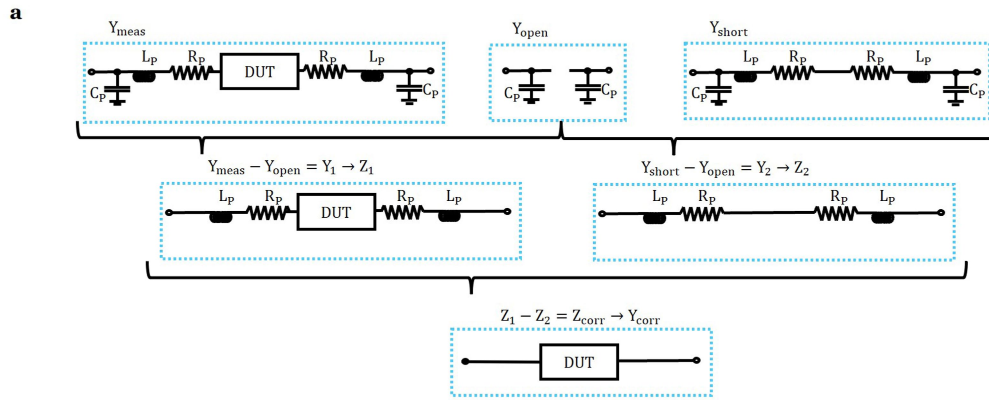


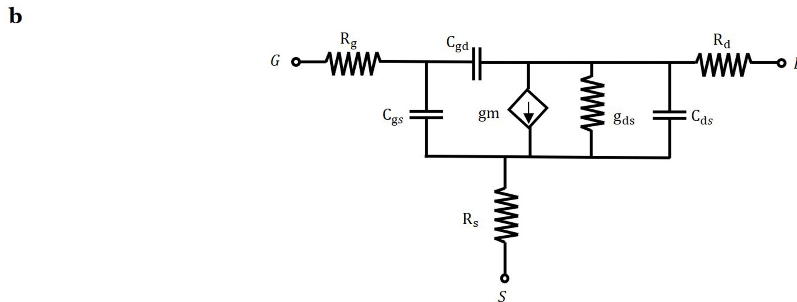
Extended Data Fig. 7 | Capacitance and charge enhancement. a, MOS schematic of the 20 Å HZH mixed-ferroic trilayer sample on lightly doped Si (10^{15} cm^{-3}) considered for the following *C*–*V* and pulsed *I*–*V* measurements. **b**, Accumulation *C*–*V* curves for 2-nm HZH grown on sub-nm SiO_2 fit to equivalent oxide thickness (EOT) simulations (Methods). Inset, externally verified MOS accumulation *C*–*V* of the same trilayer stack (Methods), demonstrating 6.5 Å EOT. The 2-nm trilayer on top of SiO_2 demonstrates lower EOT than the thickness of SiO_2 interlayer alone, carefully extracted via physical (8.5 Å) and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence of capacitance enhancement. **c**, The applied voltage pulse (top), measured current response (centre), and integrated charge (bottom) as a function of time for 2-nm HZH in MOS capacitors. **d**, The maximum charge Q_{max}, the residual charge Q_{res}, and their difference, Q_{rev}, derived from the charge versus time curve for each of the voltage pulses (Methods). **e**, The reversible charge of the MOS layer (top) compared against the extracted charge of the Si charge layer plus SiO_2 interlayer (SiL) derived electrically (Extended Data Fig. 6f). The charge boost (bottom) present in the total MOS structure (SiL plus HZH capacitors) compared to just the SiL is a signature of negative capacitance[26,69]. **f**, The polarization–electric field (P–E_F) relationship for just the 2-nm HZH layer, extracted from the charge–voltage relationship in **e**. Note that the presence of a negative slope regime in the extracted P–E_F relation corresponds to negative capacitance stabilization[26,69]. **g**, Scatter plot of reported FE–dielectric systems demonstrating capacitance or charge enhancement at the capacitor-level, via *C*–*V* or pulsed *I*–*V* measurements, respectively. The plot considers fluorite-structure bilayers[26,69] (red), perovskite-structure bilayers[29,94] (blue, BL), and perovskite-structure superlattices[30,31,47,48] (blue, SL). This work marks, to our knowledge, the thinnest demonstration of negative capacitance.

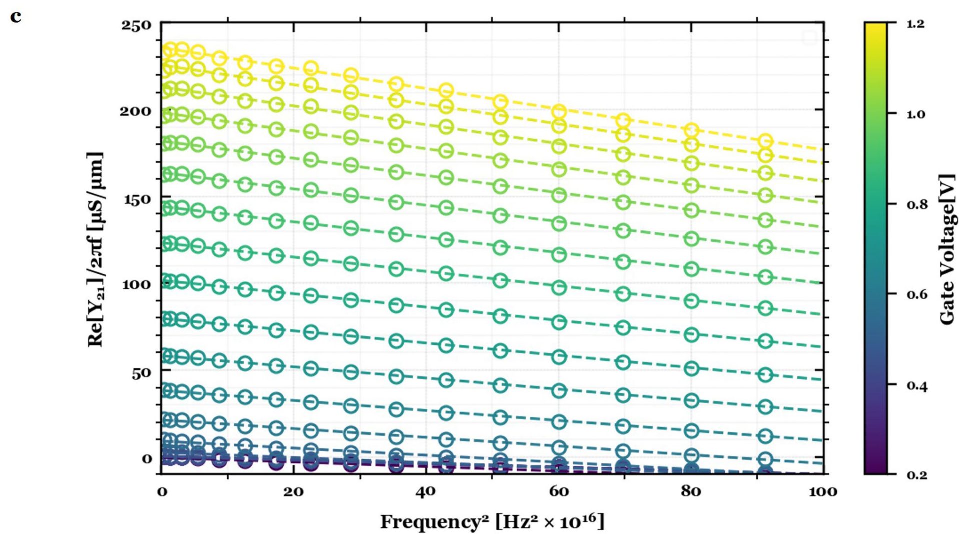


Extended Data Fig. 8 | See next page for caption.

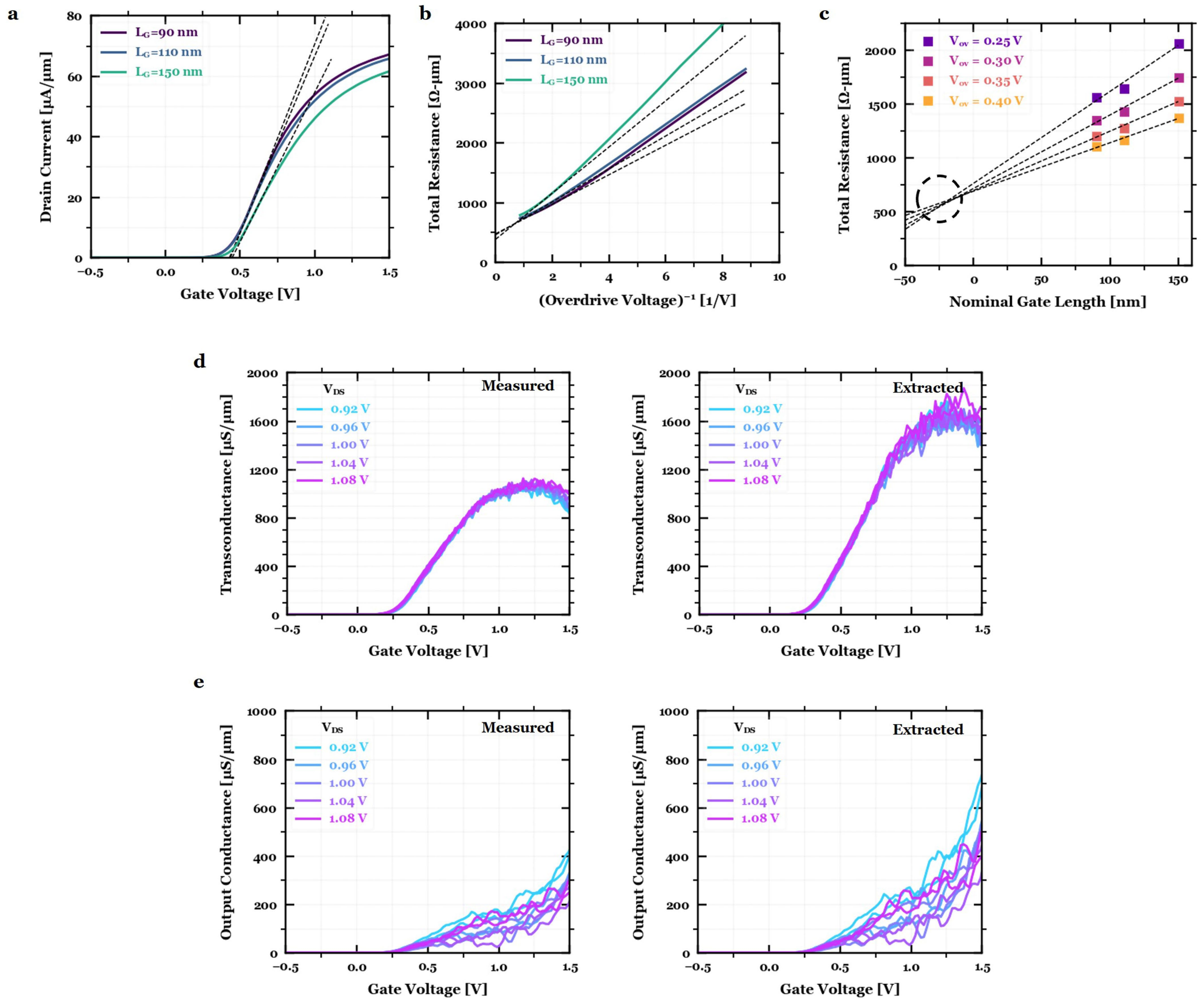
Extended Data Fig. 8 | Mobility and reliability. a, Intrinsic C_{gg} versus $V_{gs} - V_{fb}$ for ~20 Å HZH and HfO_2 gate stacks, which fit to 7.5 Å and 9.5 Å, respectively, extracted from SOI transistors. **b**, I_d versus $V_{gs} - V_T$ at V_d = 50 mV for transistors implementing HZH and HfO_2 gate stacks. **c**, EOT and mobility (at 5×10^{12} cm^{-2}) for HZH and HfO_2, demonstrating no mobility degradation. **d**, Normalized mobility versus EOT for transistors integrating the 2-nm HZH mixed-ferroic gate stack (blue) versus a 2-nm HfO_2 standard high-κ dielectric gate stack (black) of higher EOT, demonstrating no mobility degradation. These results are also benchmarked against reported HKMG literature[3] implementing interlayer-scavenged 2-nm HfO_2 (red). Inset, SiO_2 interlayer thickness versus EOT for 6.5 Å EOT HZH stack against notable HKMG literature employ interlayer scavenging[3]. This scatter plot highlights the underlying reason for the improved leakage-EOT and mobility-EOT behaviour in the ultrathin HZH gate stacks: achieving low EOT without reducing the SiO_2 interlayer thickness. **e**, Measure–stress–measure scheme used in PBTI reliability measurements. **f**, **g**, ΔV_T versus stress time for long-channel bulk transistors integrating HZH (**f**) and HfO_2 (**g**) at varying stress conditions (up to 9 MV cm^{-1}), measured at 85 °C. The extracted time exponent, n, is similar to reported high-κ HfO_2 stacks[67], which is expected considering the similar interfacial (IL) oxide and IL-high-κ interface[46]; both stacks with different EOT have HfO_2 sitting on the same SiO_2 IL (Extended Data Fig. 1). **h**, d.c. lifetime (stress time needed to induce a 50 mV ΔV_T shift) versus electric field for HZH and HfO_2, demonstrating similar rates of degradation. **i**, **j**, Evolution of MOSCAP accumulation C–V curves as a function of stress time at a stress of $V_{fb} - 1$ V for HZH (**i**) and HfO_2 (**j**).







Extended Data Fig. 9 | Radio frequency device characterization. **a**, De-embedding procedure for extracting corrected admittance parameters (Y_{corr}) by decoupling parasitic shunt capacitance and series resistance and inductance by measuring scattering parameters for the device under test (DUT) as well as open and short structures. More details can be found in Methods. **b**, Small-signal model for transistor used to extract transconductance (g_m) and total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$). **c**, De-embedded $(2\pi f)^{-1}\mathrm{Re}(Y_{21})$ points extrapolated to the zero frequency limit (dotted lines) to extract the radio frequency g_m. All data shown were extracted from bulk transistors ($L_G = 1\,\mu m$) integrating the 2-nm HZH ferroic gate stack.



Extended Data Fig. 10 | Transconductance extraction. a, Threshold voltage extraction by linear extrapolation for various channel lengths. All channel lengths give nearly constant V_T (~0.42 V), satisfying the assumption for the line resistance method. **b**, Source/drain series resistance extracted using the $1/V_{ov}$ method (Methods). By performing a linear interpolation of the total resistance for V_{ov} = 0.5–0.6 V, the extracted series resistance is ~500 Ω μm. **c**, Source/drain series resistance extracted using the line resistance method (Methods). The trend is considered down to L_G = 90 nm, which intersects at ~500–600 Ω μm—consistent with the $1/V_{ov}$ method—with an L_G offset of ~50 nm. **d**, **e**, Measured (left) and extracted (right) transconductance (**d**) and output conductance (**e**) versus V_g for V_{ds} = 0.9–1.1 V, assuming $R_s = R_d$ = 250 Ω μm for L_G = 90 nm. The de-embedding of intrinsic $g_{m,i}$ and $g_{ds,i}$ from extrinsic g_m and g_{ds} is described in Methods. All data shown were measured on SOI short-channel transistors integrating the 2-nm HZH ferroic gate stack.