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Measurement and Modeling of Single Event Transients in 12nm Inverters

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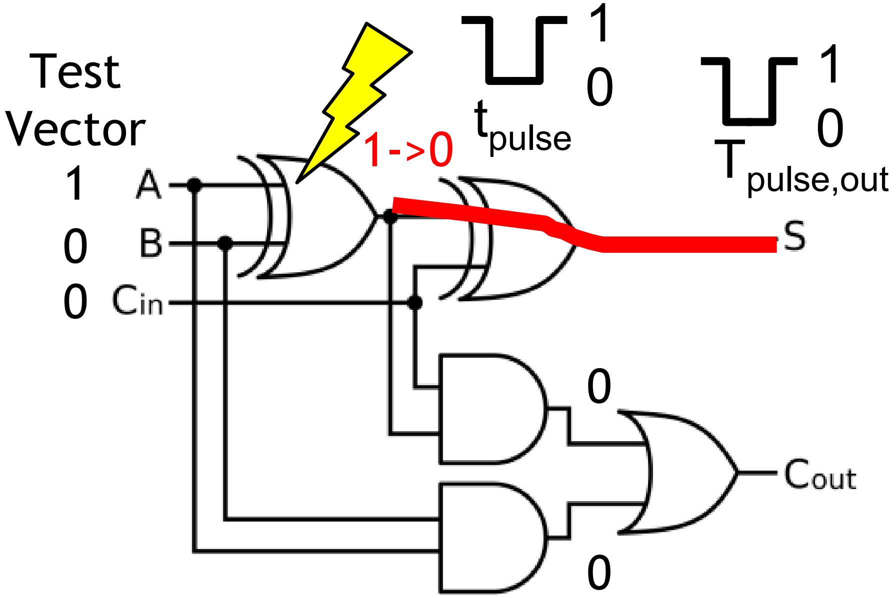
Introduction

Single-event transients (SETs) are becoming more prevalent with smaller transistor sizes and faster clocks

Methods to measure and model SET distributions are needed.

SET distributions in combinational logic can be converted into an upset at clocked register.

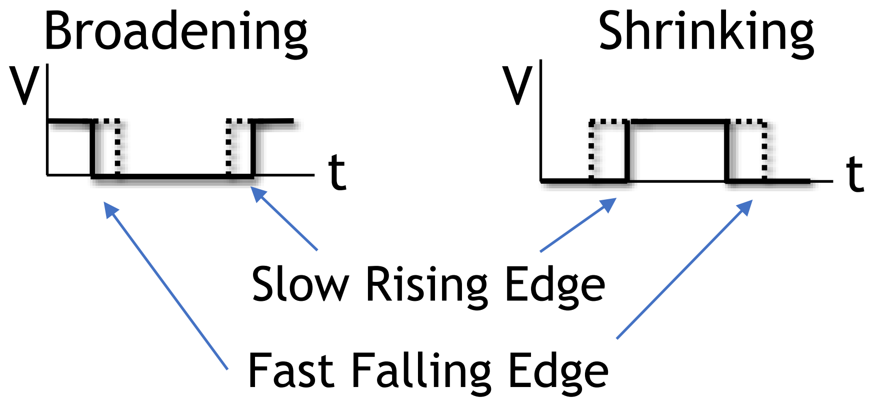


Full Adder Circuit

Probability SET Latched ≈

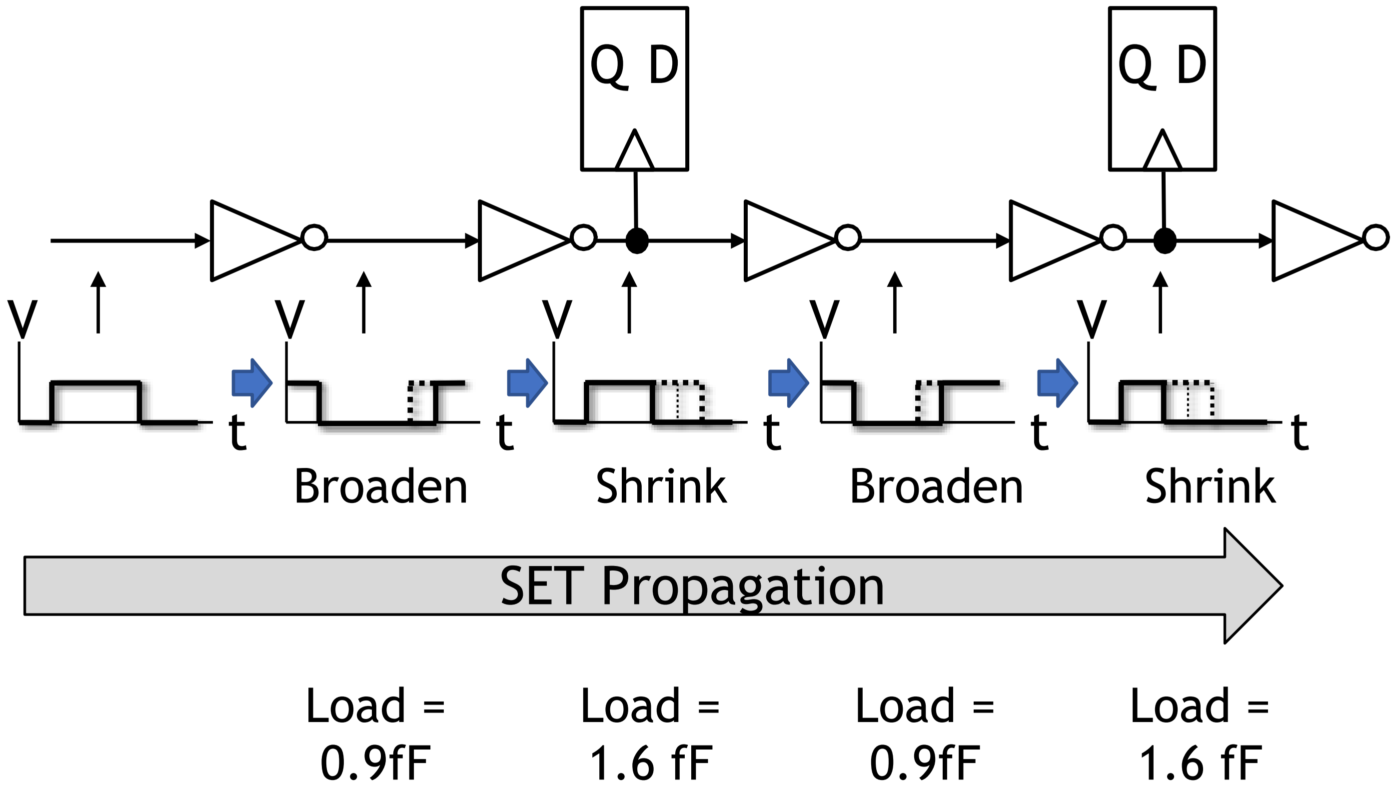
$$P_{SET} \times \frac{t_{pulse,out}}{t_{clock}}$$

Background: Alternating Loads Cause SETs to Broaden or Shrink

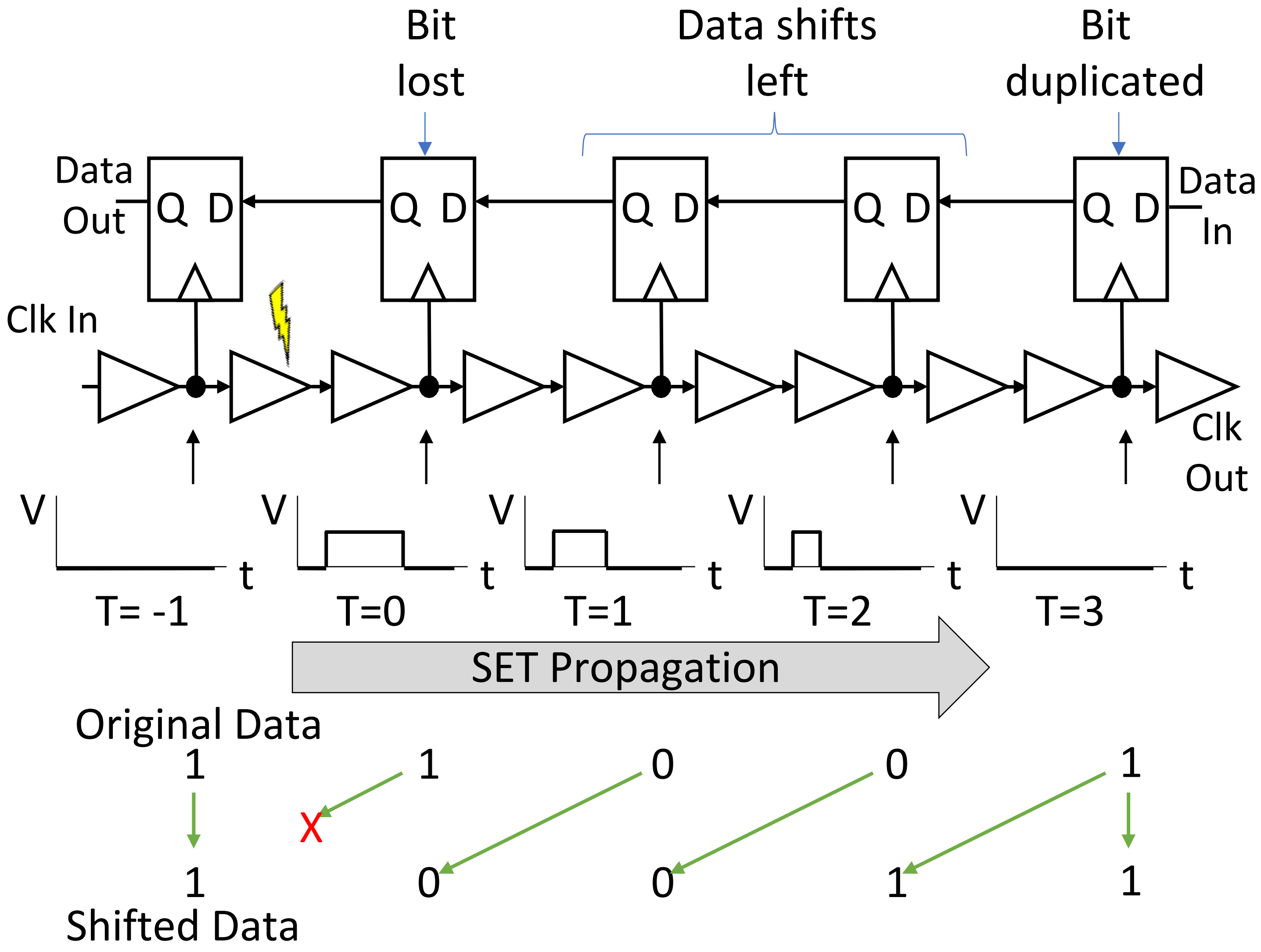


- Mismatched drive strengths cause mismatched rise and fall times
- Mismatched rise/fall times cause pulse broadening/shrinking
- The larger the load, the larger the effect

Pulse Shrinking on a D Flip Flop Scan Chain



Measure Single Event Transients and Upsets on D-Flip Flop (DFF) Scan Chain



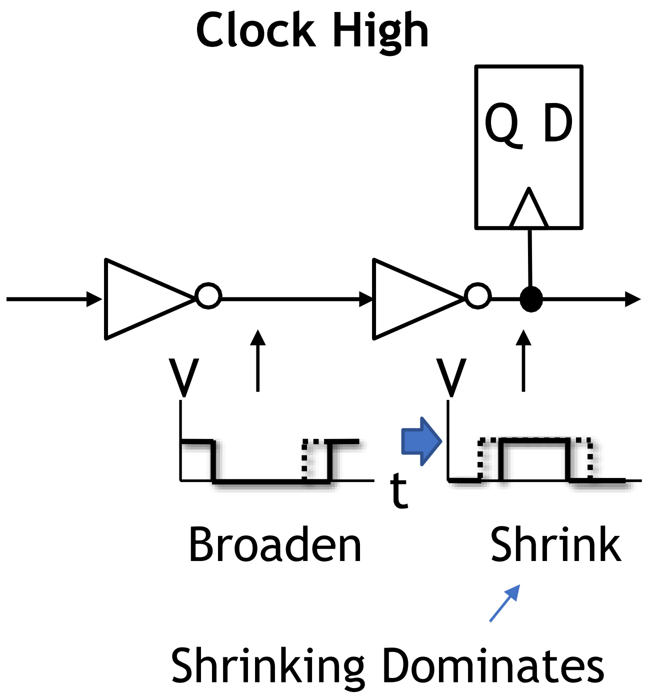
Pulse Shrinking per DFF

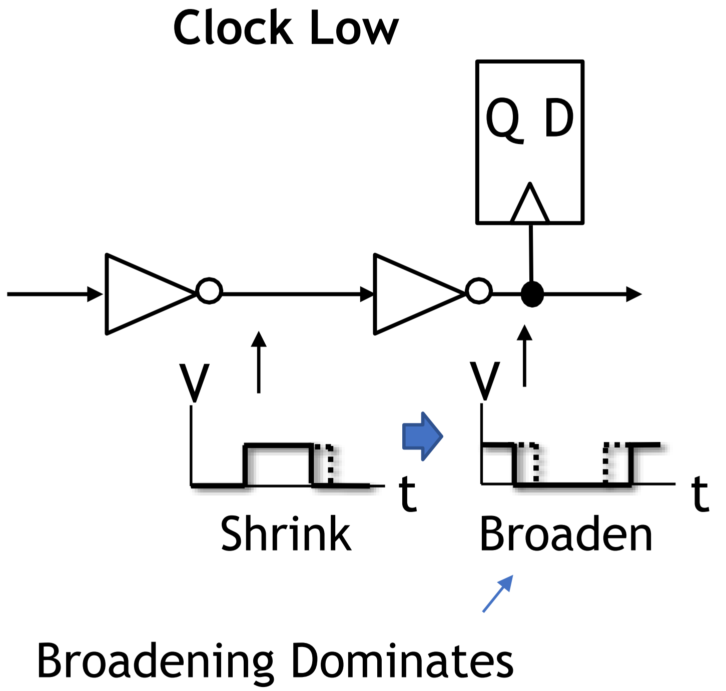
$$\text{SET Length} = 0.049\ \text{ps} \times N_{shifted\_bits} + 12.7\ \text{ps}$$

Minimum pulse width to clock DFF

Clock High vs Clock Low SETs

Measure SETs on 15,840 long chain of DFFs using 36 MeV Oxygen ions at an linear energy transfer (LET) of 6.5 MeV-cm^2/mg at Sandia Ion Beam Lab

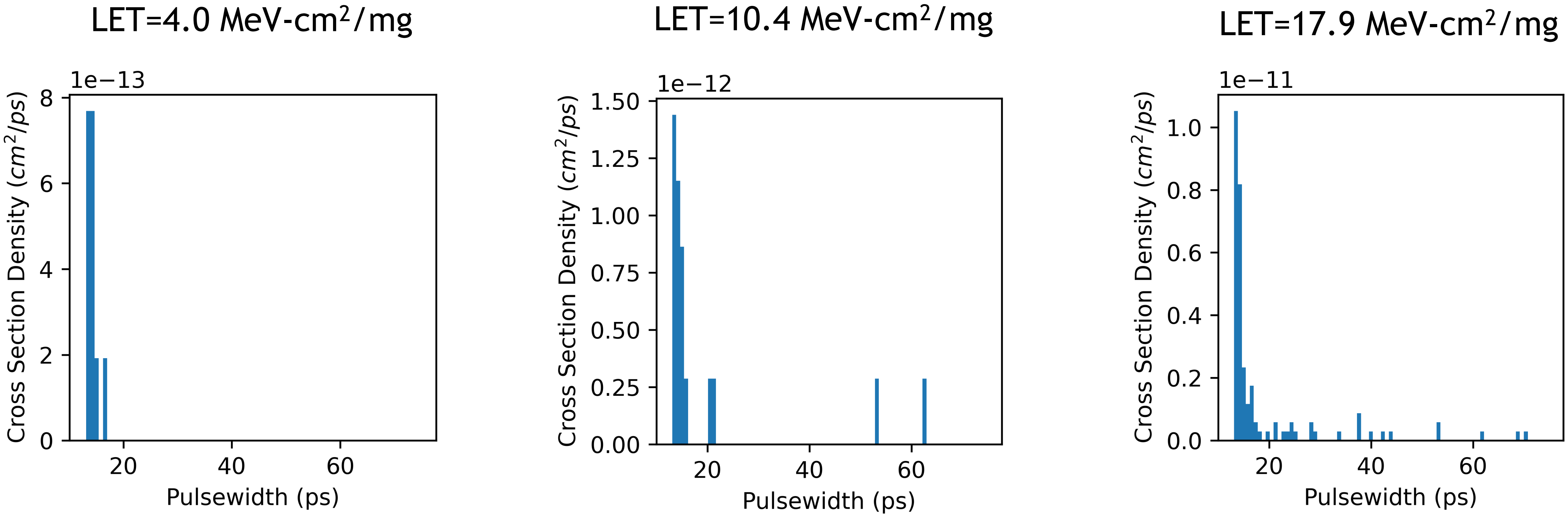




Longest SET Caused 48 DFFs to shift (15 ps)

Average SET Caused 8,918 DFFs to shift

Estimate SET Cross Section as a Function of Pulse Width

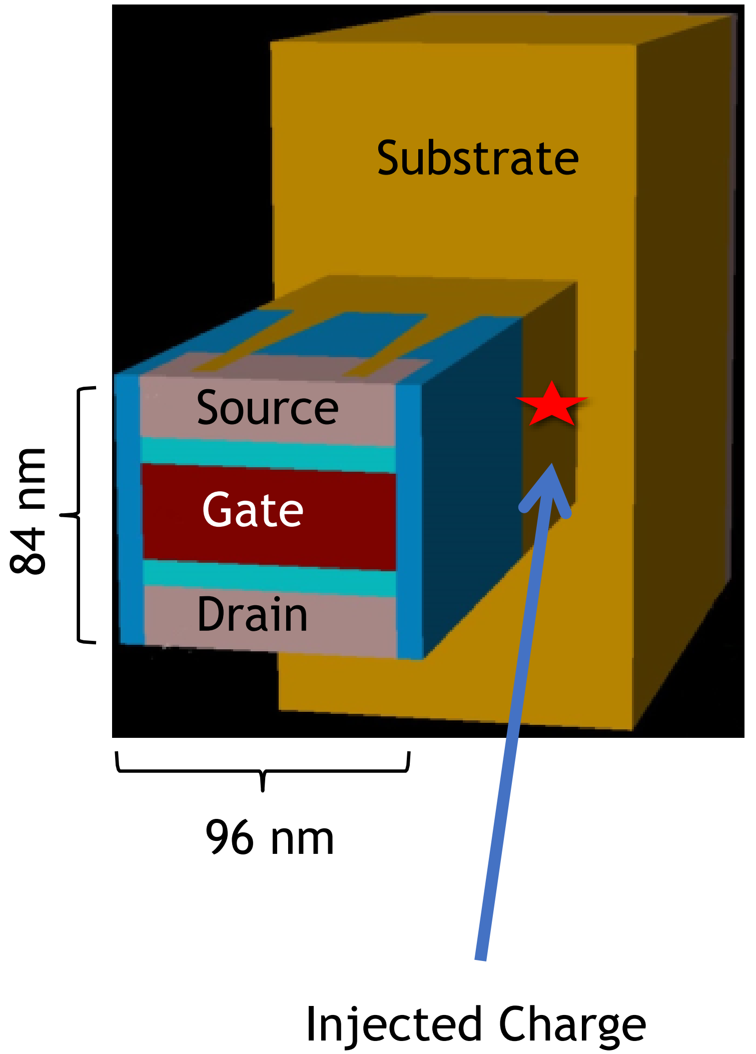


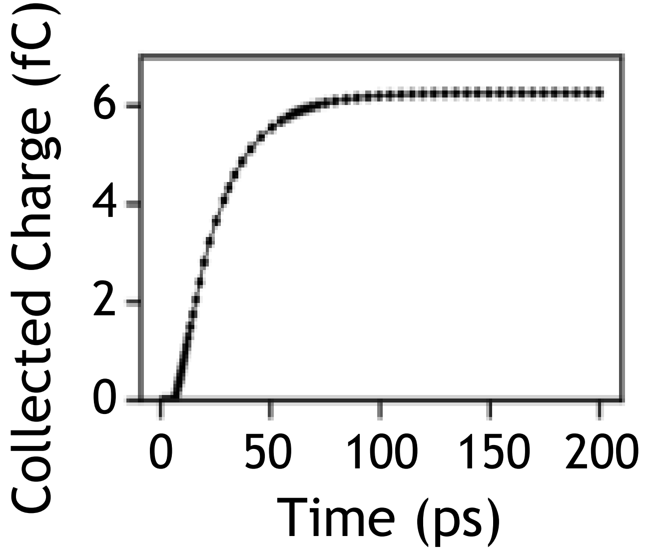
- Measured at Texas A&M University using 40 MeV Argon beam with degrader to change LET
- Used circuit simulations to estimate propagation delay per flip flop

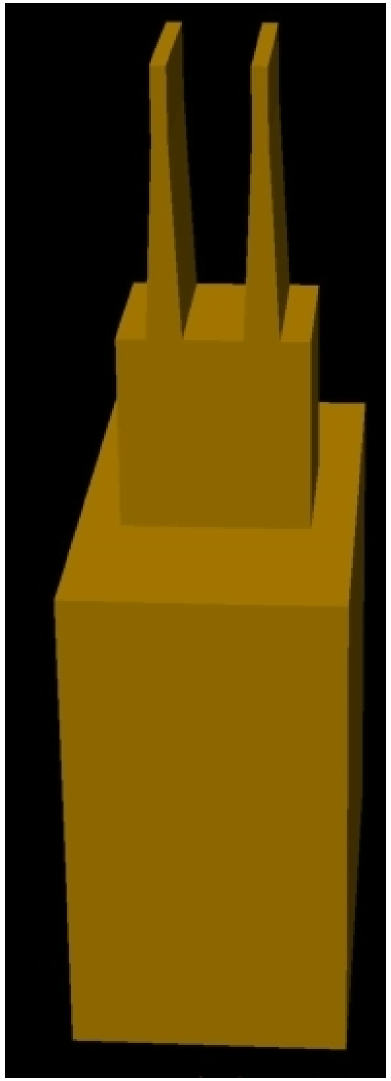
Predicting SET Cross-Section Distributions

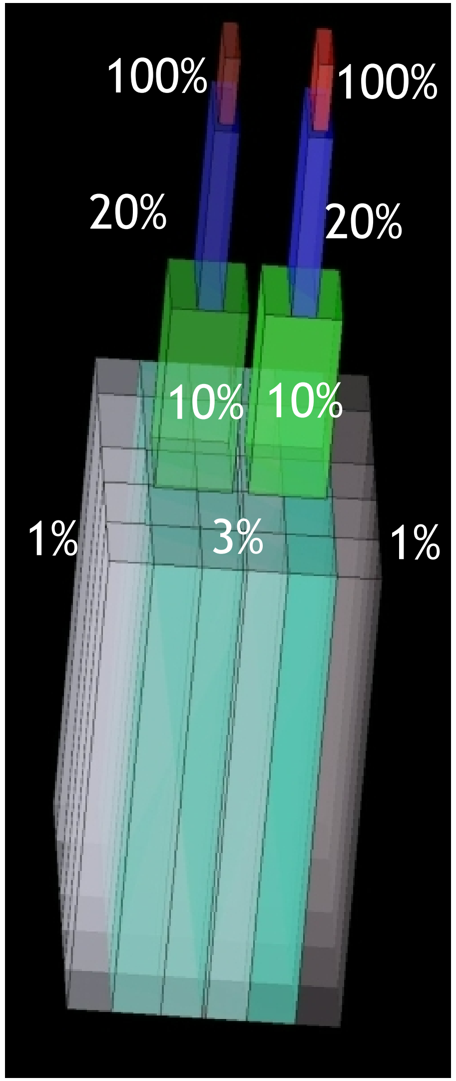
- TCAD simulations to compute charge collection efficiency
- Monte Carlo Radiative Energy Deposition (MRED) to compute deposited charge distribution
- Circuit simulations to compute pulse width for a given amount of collected charge on a given gate

Use TCAD Simulations to Determine Charge Collection Efficiency

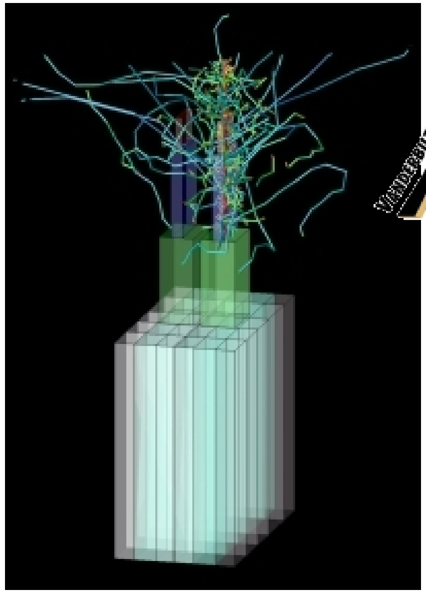




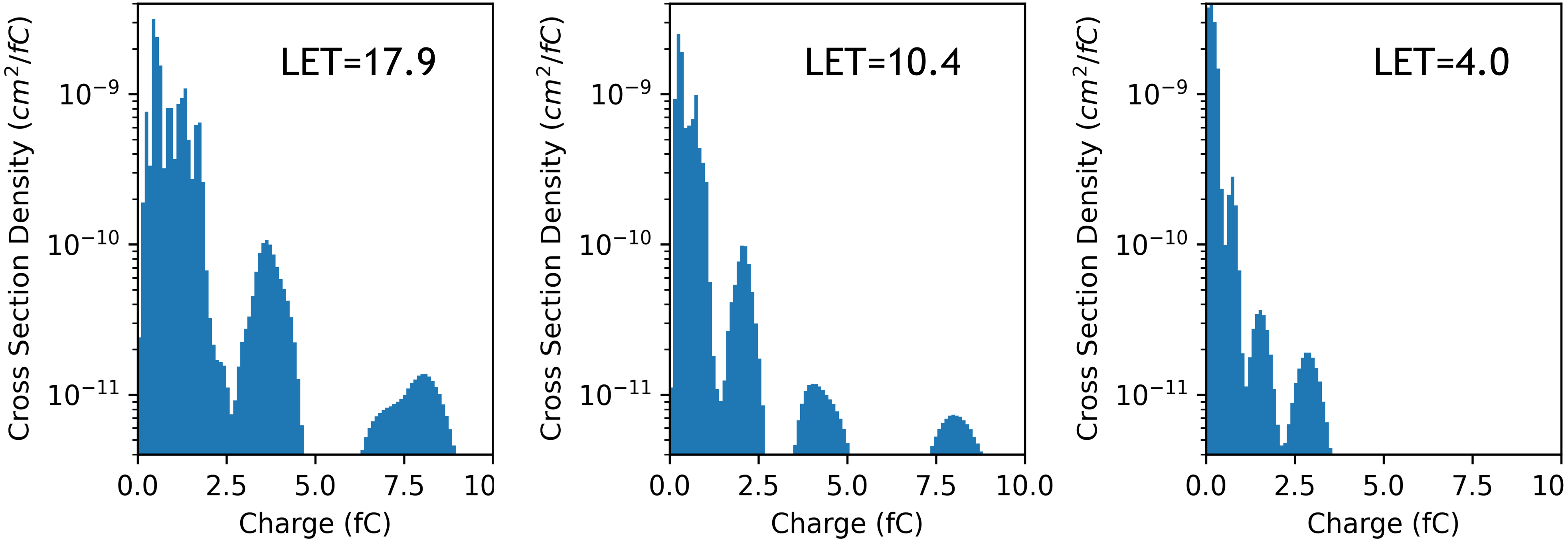




Compute Deposited Charge Using Monte Carlo Radiative Energy Deposition (MRED)



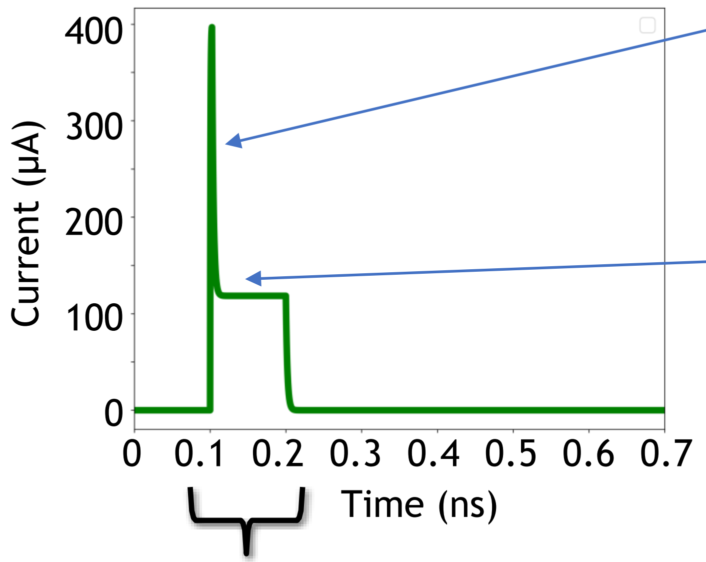
- Computed deposited charge at each location
- Integrate deposited charge multiplied by collection efficiency



Discrete data is due to binning of monte carlo simulations

Compute Pulse Width For a Given Amount of Collected Charge

Model injected current as dual double exponential



Peak current:

- Charges internal nodes, computed as current needed to flip node to opposite rail

Hold current:

- Computed as current needed to hold node at opposite rail, is within 5% of transistor saturation current

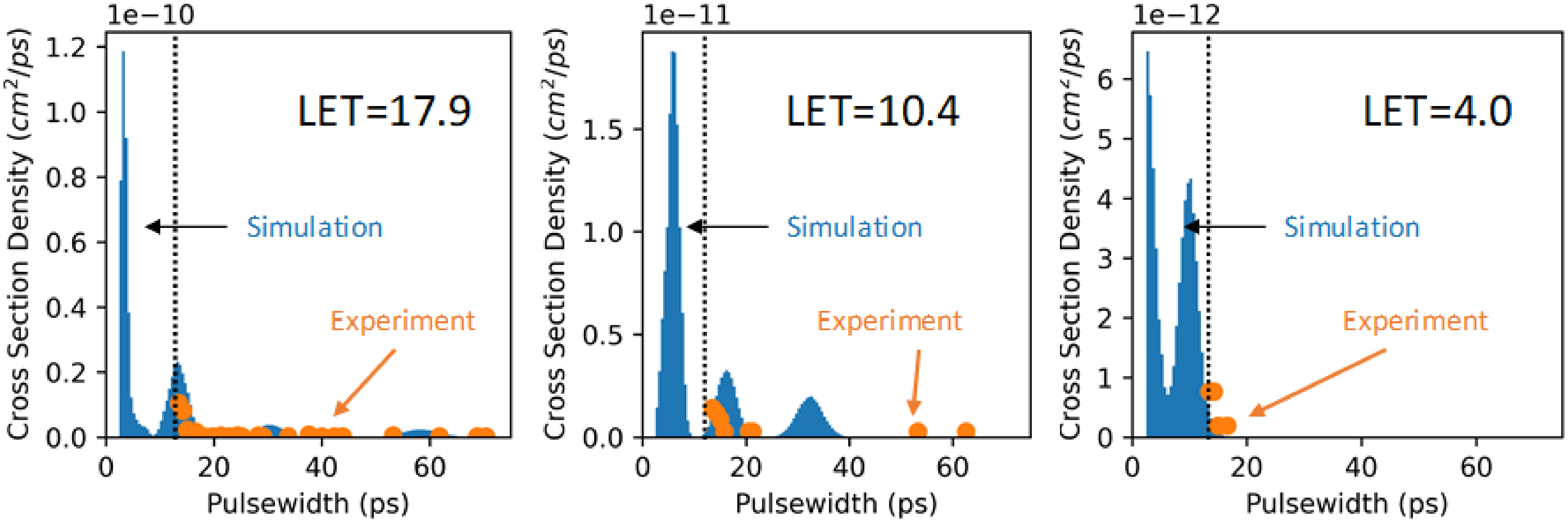
Pulse length determined by time needed to drain all injected charge

Double Exponential Current Model:

$$I(t) = \begin{cases} 0, & t < t_{d1} \\ I_0\left(1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right)\right), & t_{d1} \le t < t_{d2} \\ I_0\left(\exp\left(-\frac{t - t_{d2}}{\tau_2}\right) - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right)\right), & t \ge t_{d2} \end{cases}$$

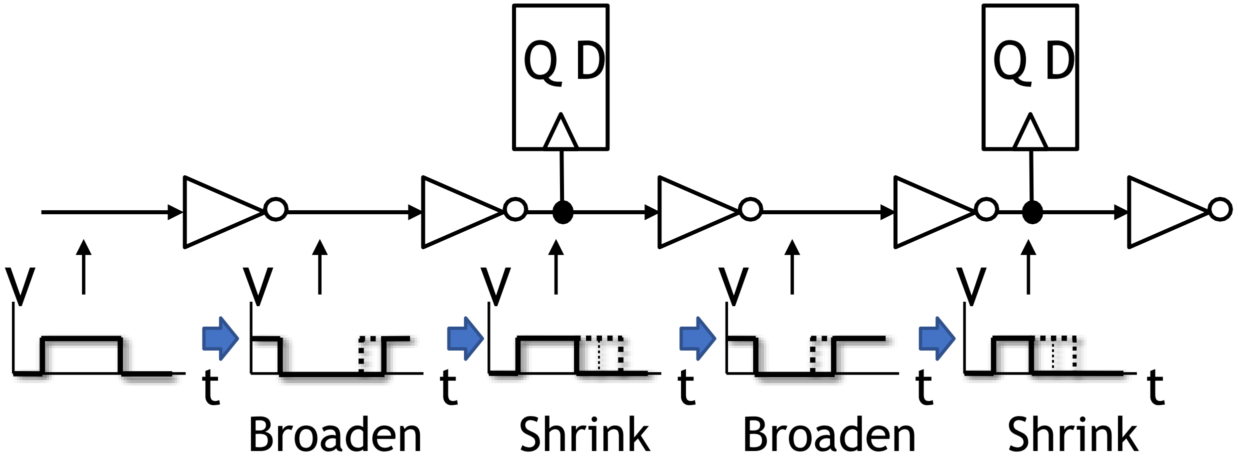
- Both peak and hold currents are fit to this model
- Time constants from TCAD, I_o from circuit simulations

Matching Modeling and Experiment! Modeling goes beyond experiment limits



Summary

- Demonstrated a new method for experimentally estimating SET pulse width



- Accurately modeled SET pulse width distribution and matched to experiment