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Deep-level optical spectroscopy in wet-treated etched-and-regrown nonpolar *m*-plane GaN vertical Schottky diodes

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Outline

Motivation	High-Power electronics / III-N material system & vertical architecture / selectively doped junctions
Etched and Regrown Diodes	Vertical *m*-plane GaN etched-and-regrown planar *p-n* diodes
Methodology and Approach	*p-n* diode design/ growth & fabrication / steady-state photocapacitance and LCV methods
Etch Enhanced Damage	Effects of etch enhanced damage on deep level states
Summary	Review of etched enhanced damage on *m*-plane diodes

Motivation: high power electronics

30% of electrical energy passes through power electronics converters today
80% of electricity could pass through power electronics by 2030 [1]

- **Electric Power Generation:** power converters and inverters
- **Electric Power Transmission:** power flow controllers
- **Motor Drives:** variable frequency drives
- **Power Supplies:** AC-DC converters
- **Automotive:** battery charging and traction drive inverters


Solar and Wind Power


Industrial Motor Drives


Computer Power Supplies


Electric Automobiles

[1] L.M. Tolbert, et al., Oak Ridge National Laboratory (2005)

III-Nitride & vertical architecture

GaN Material System

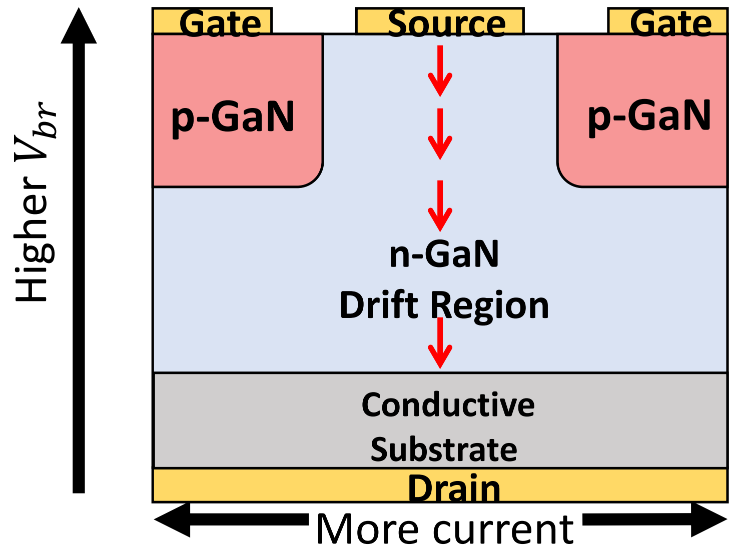
- Replace Si as a high-power electronics material
- Wide bandgap (3.4 eV)
- Large critical electric field (3.3×10^6 V/cm)
- High electron mobility (2000 cm^2/ V s)
- High Baliga Figure of Merit (67-83)
- Good thermal conductivity

		GaN	Si	4H-SiC	Diamond
Band Gap	Eg (eV)	**3.39**	1.1	3.26	5.45
Electron Mobility (high)	μ_n (cm^2/V s)	**2000**	1450	950	4000
Electron Saturation Velocity	v_{sat} (10^7cm/s)	**2.5**	1	2	2.7
Breakdown Electric Field	E_{br} (MV/cm)	**3.5-3.75**	0.3	2	5.6
Baliga Figure of Merit	BFOM (GW/cm^2)	**67-83**	0.004	6.5	355
Thermal Conductivity	K (W/cm °K)	**2.3**	1.5	4.9	20

[2] Flack, T. et al., Journal of Electronic Materials 45 (2016).
[3] Ohta, H. et al., IEEE Electron Device Letters 36(11), 1180–1182 (2015).

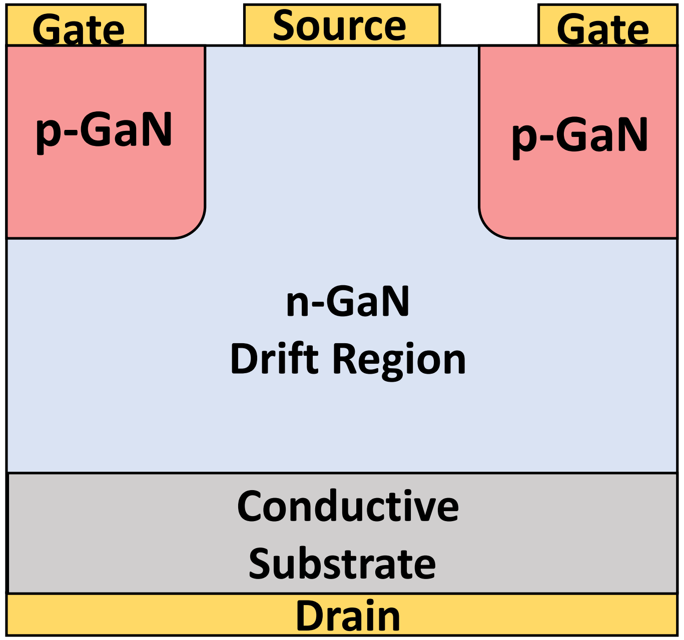
Vertical Architecture

- Increase the breakdown voltage
- Increase current handling
- Low on-resistance
- Suppressed current collapse
- Low parasitic inductance
- Small form factor

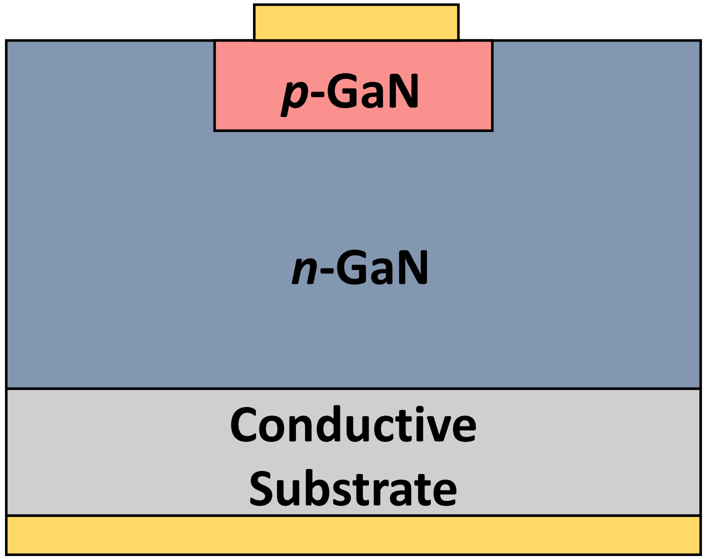


Vertical Geometry: *JFET*

Selectively doped p-n junctions



Vertical Geometry: *JFET*



Vertical selectively doped p-n junction

Selective-area ion implantation

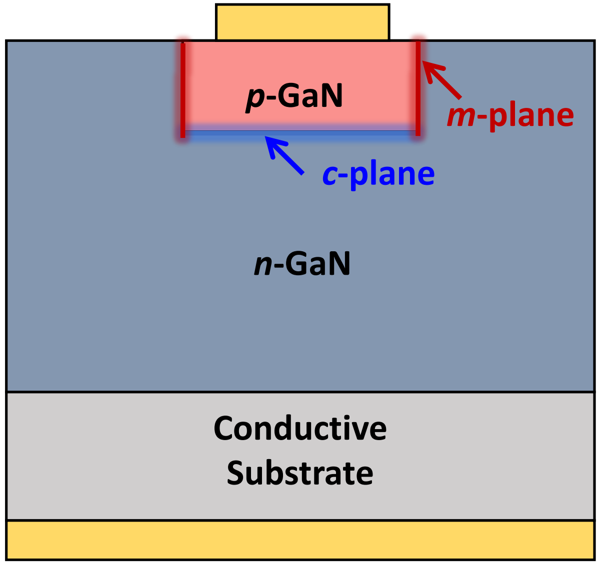
- Extreme acceptor activation conditions [4]
- Removal of implantation-induced damage

selective-area doping

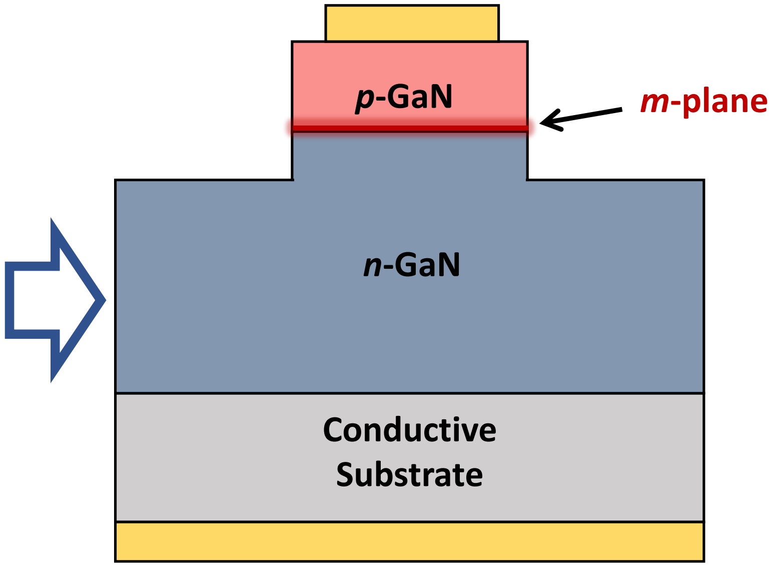
- selective etch then regrowth of the embedded region
- p-n junctions at these regrowth interfaces show considerable leakage currents [5]

[4] M Tadjer et al., *ECS J. Solid State Sci. Technol.* **5**, 124 (2016)
[5] Z. Hu et al., *IEEE Electron Device Lett.* **38**, no. 8, 1071 (2017

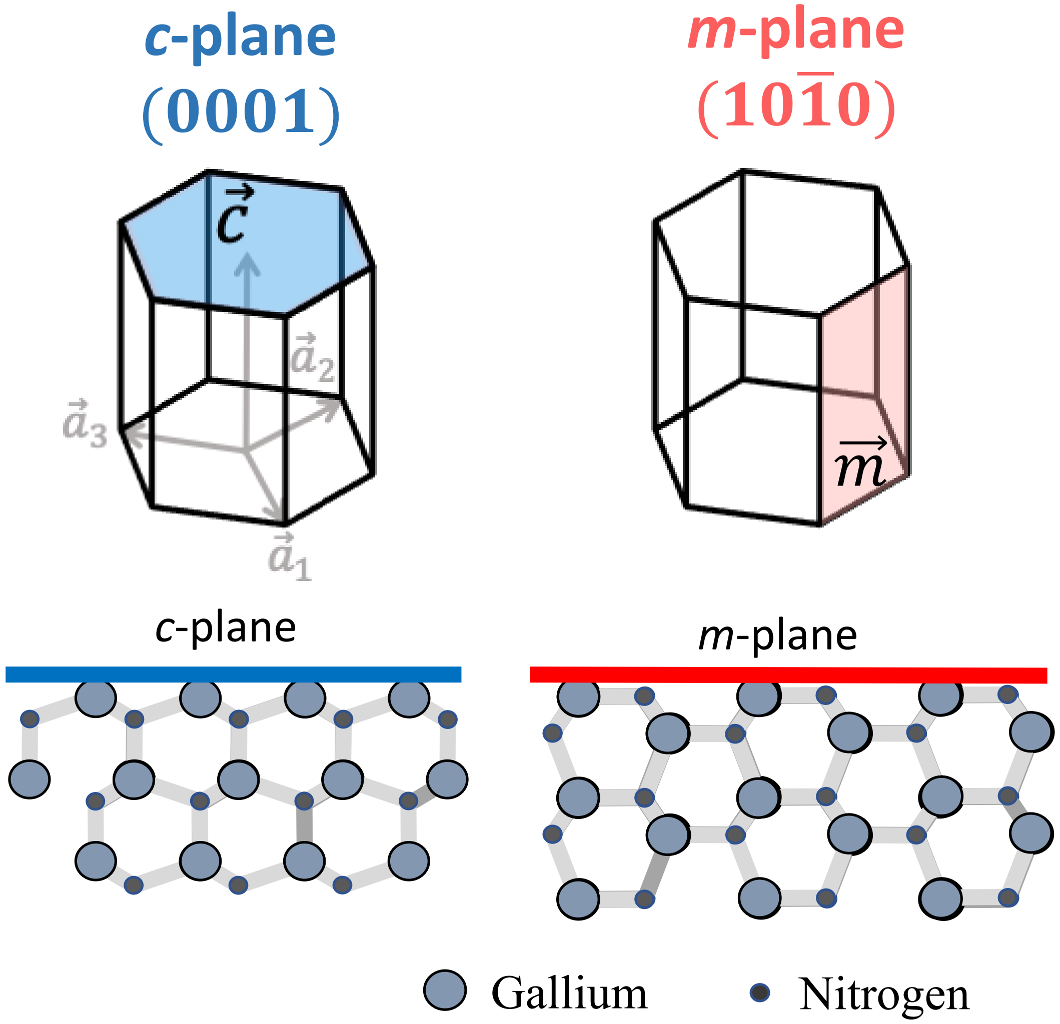
Planar *m*-plane *p-n* diodes



Vertical selectively doped p-n diode



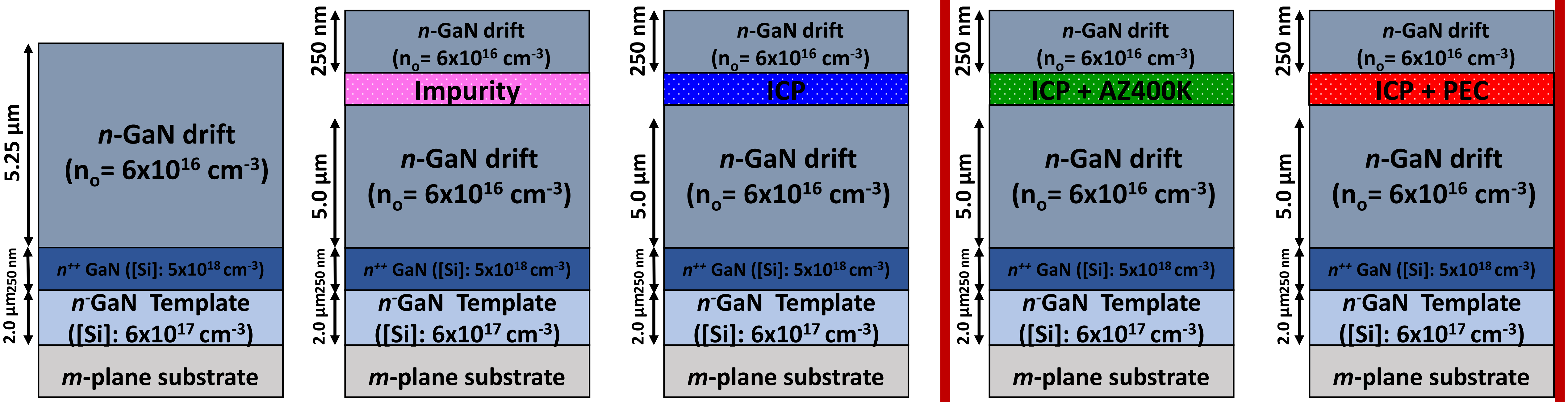
Planar vertical p-n diode



- **Investigation on planar *m*-plane diodes**
- Little investigation on m-plane for high power devices
- Higher density of N sites [6-8]
- Possibly incorporate impurities differently

[6] Fichtenbaum, N. A. et al., Journal of Crystal Growth 310(6), 1124–1131 (2008).
[7] Cruz, S. C. et al., Journal of Crystal Growth 311(15), 3817–3823 (2009).
[8] Browne, D. A. et al., Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films 30(4), 041513 (2012).

Schottky diodes for analysis



Sample 1
(Continuous)

Sample 2
(Impurity)

Sample 3
(ICP)

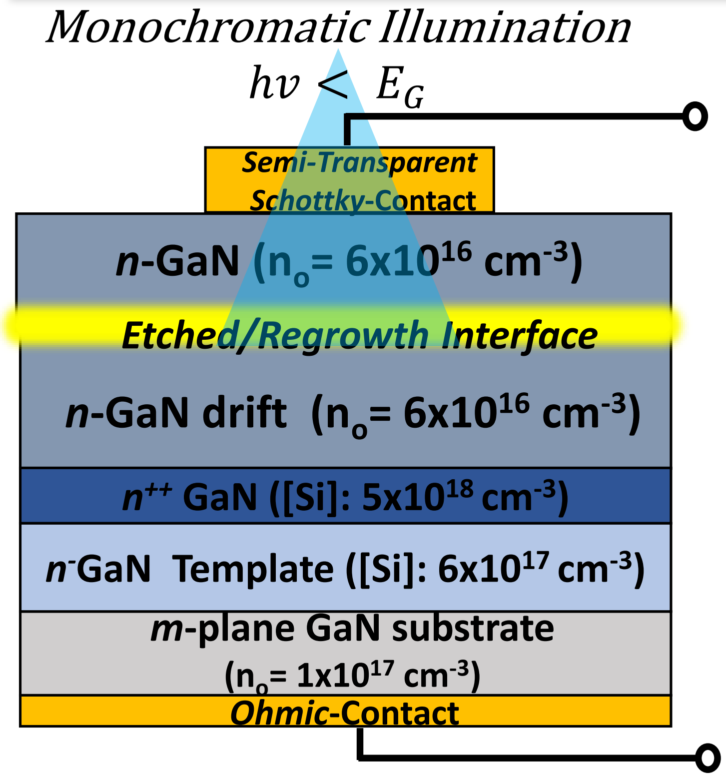
Sample 4
(ICP + AZ400K)

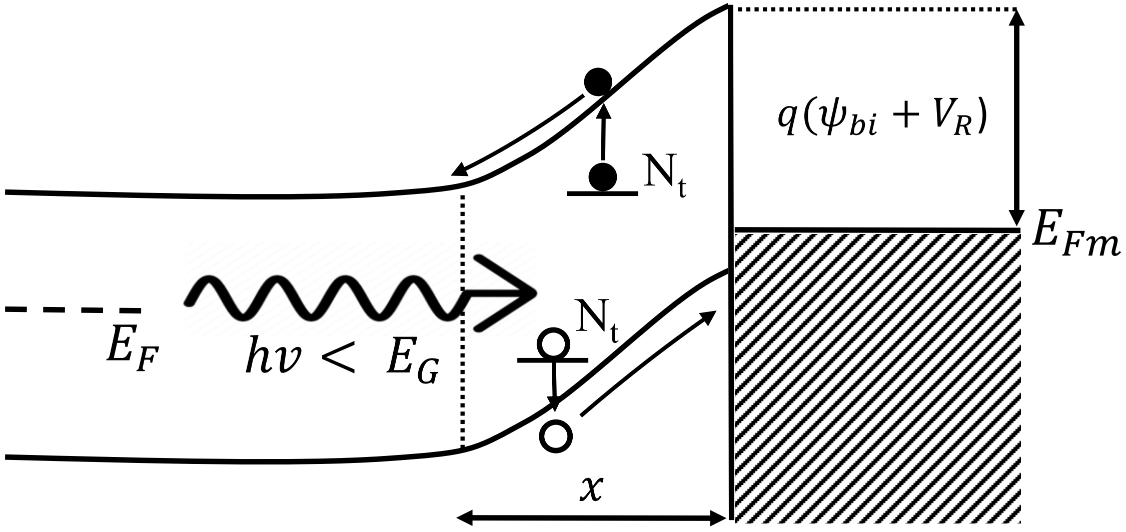
Sample 5
(ICP + PEC)

Treatments for damage mitigation

- Study the effects of impurities and etching on deep level defects
- Develop treatments to eliminate the defects or remove the damaged material

Steady-State Photocapacitance (SSP) and LCV



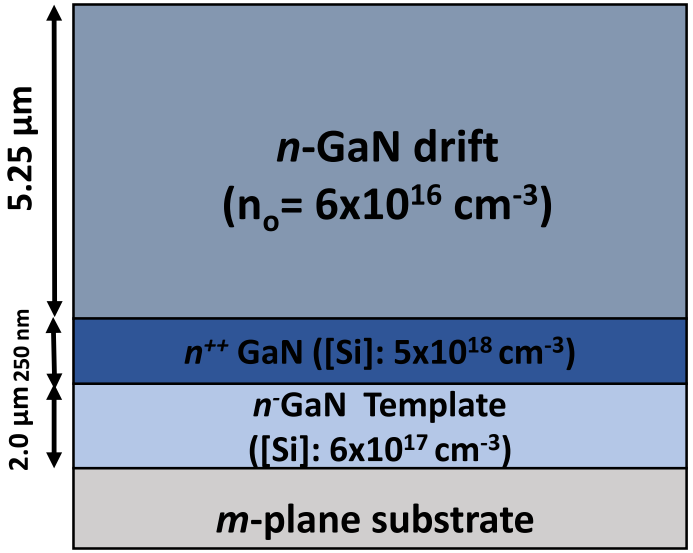


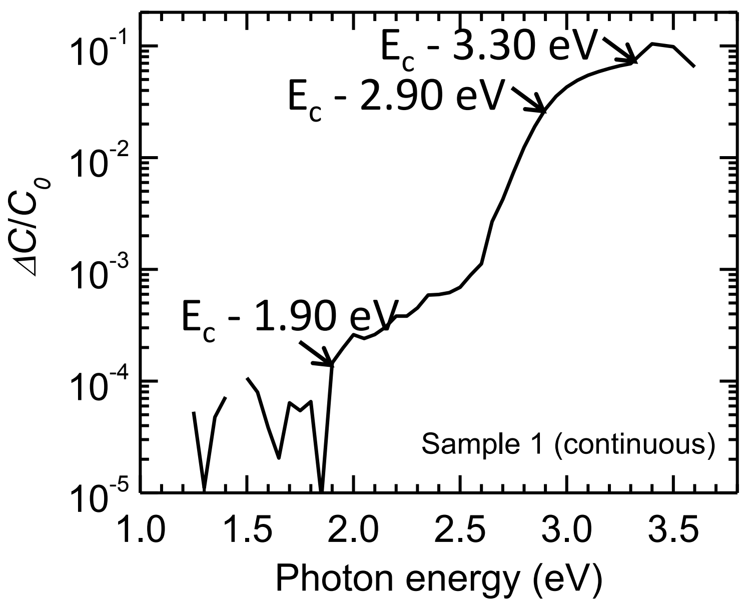
$$\frac{\Delta C_{ss}}{C_0} \cong \frac{N_t}{2N_d} \frac{\sigma_n}{\sigma_n + \sigma_p}$$

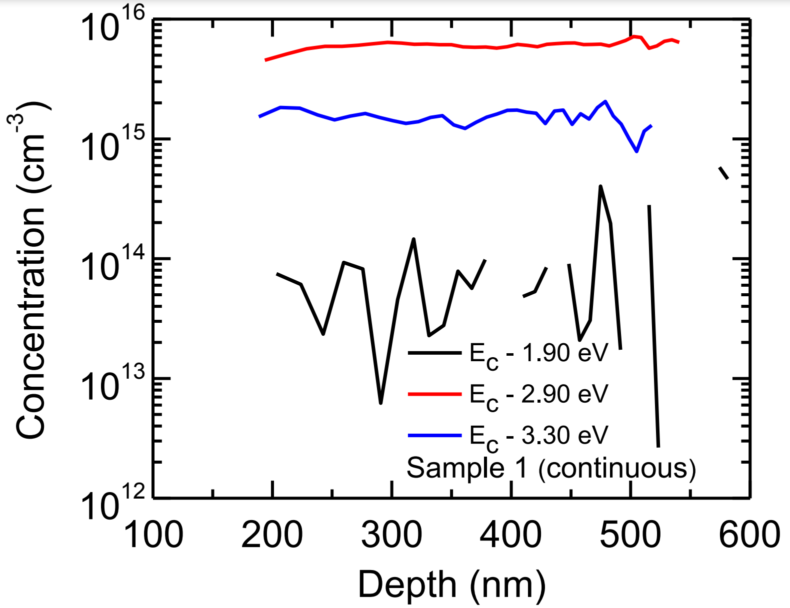
- ΔC: junction capacitance
- C_0 : dark quasi-equilibrium junction capacitance
- N_t : density of traps
- $\sigma_{n,p}$: optical cross section for electrons or holes
- E_o: : the optical energy of the defect
- d_{FC} : Franck–Condon energy

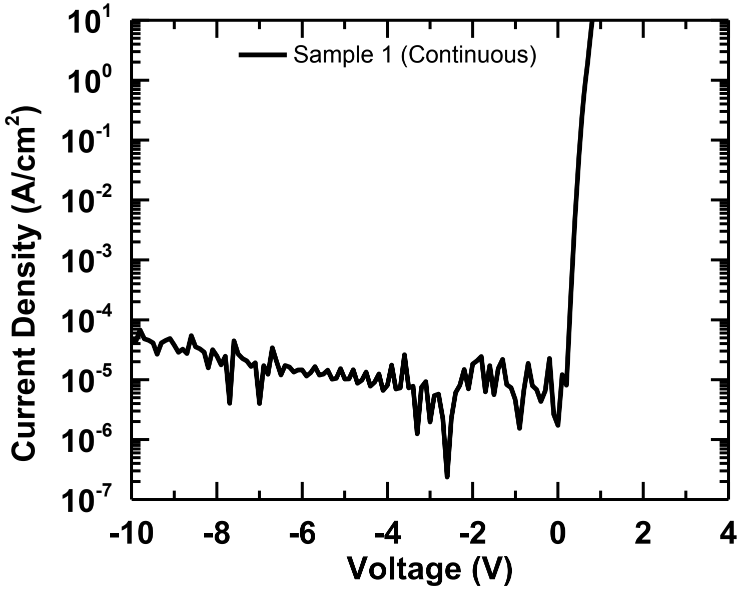
- Photoionized carriers are swept from the junction of a Schottky diode
- ΔC due to trapped carrier emission from deep levels due to incident photons
- Onsets of deep level emission occur near $hv \cong E_o - d_{FC}$
- Differentiating ΔV with respect to C provides a spatial profile of the deep level

Defect levels in continuously grown *m*-plane GaN







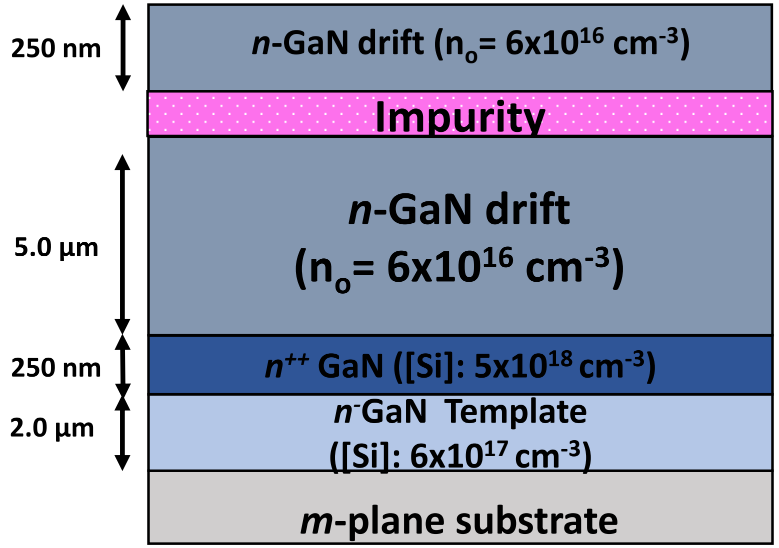


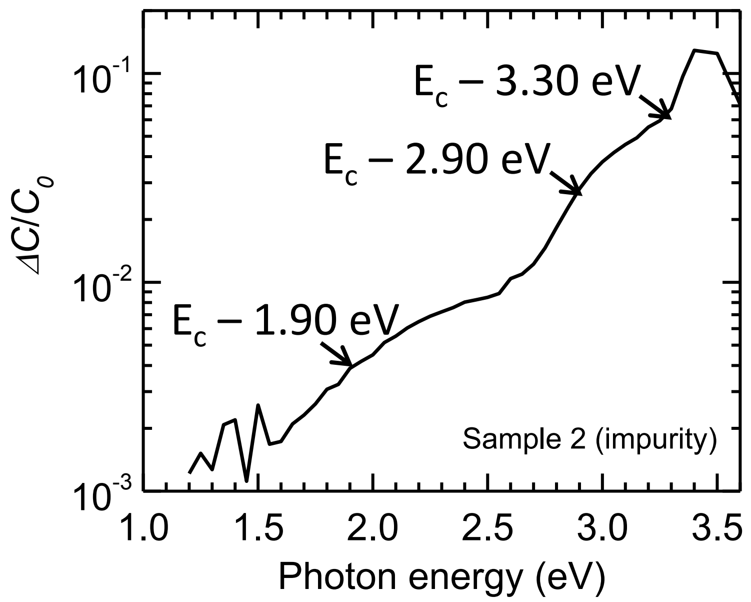
Defect levels in as-grown *m*-plane same as *c*-plane

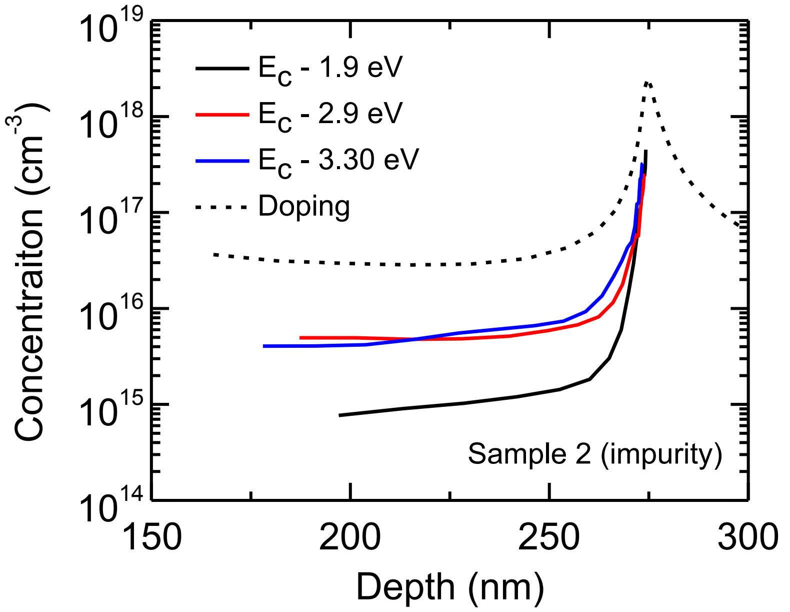
- E_c - 1.9 eV (1×10^{14} cm^{-3}) → atomic displacement [10]
- E_c - 2.9 eV (3×10^{15} cm^{-3}) → C interstitial or Ga vacancy, [11-12]
- E_c - 3.3 eV (7×10^{15} cm^{-3}) → C impurity [13]
- Reverse J ~ 4 × 10^{-5} A/cm^2 at −10 V

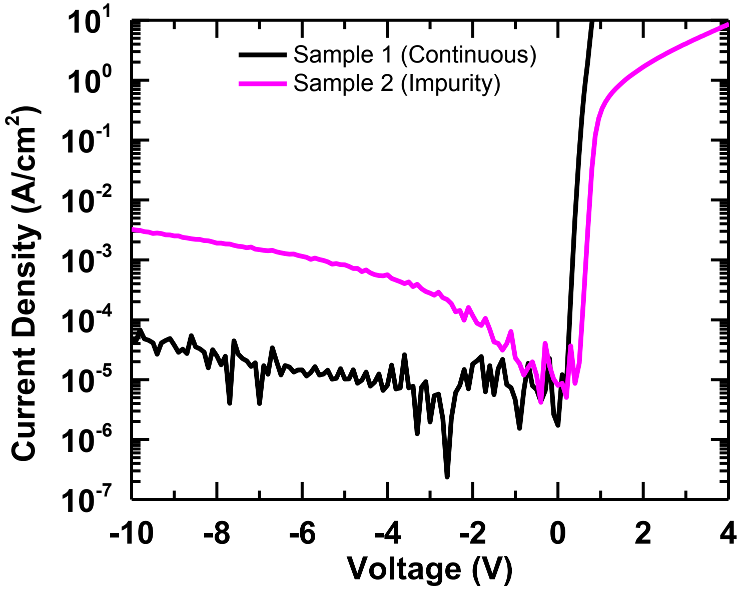
[10] S. Limpijumnong, et al., *Physical Review B*, vol. 69, no. 3, Jan. 2004, doi: 10.1103/PhysRevB.69.035207.
[11] T. Ogino et al. , *Japanese Journal of Applied Physics*, vol. 19, no. 12, p. 2395, 1980
[12] Hierro, et al. , *Appl. Phys. Lett.*, vol. 77, no. 10, pp. 1499–1501, Sep. 2000, doi: 10.1063/1.1290042.
[13]A. Armstrong, et al. *Applied Physics Letters*, vol. 88, no. 8, p. 082114, Feb. 2006, doi: 10.1063/1.2179375.

Defect levels in regrown impurity *m*-plane GaN





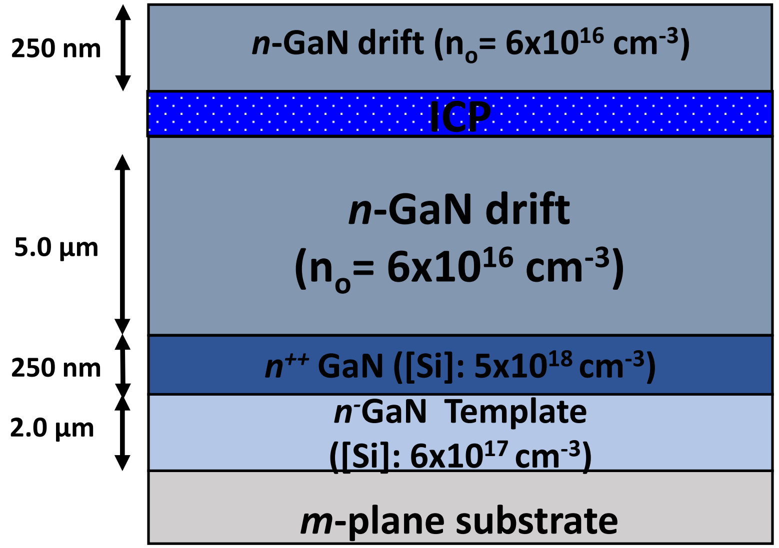


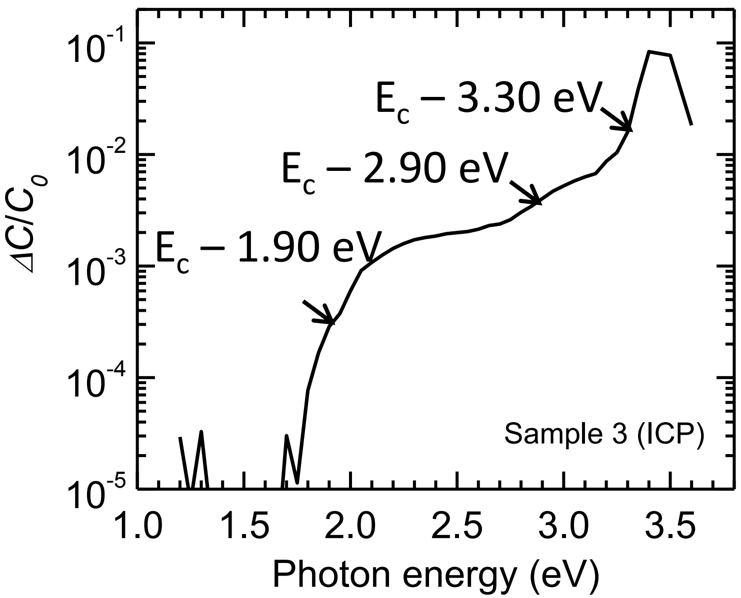


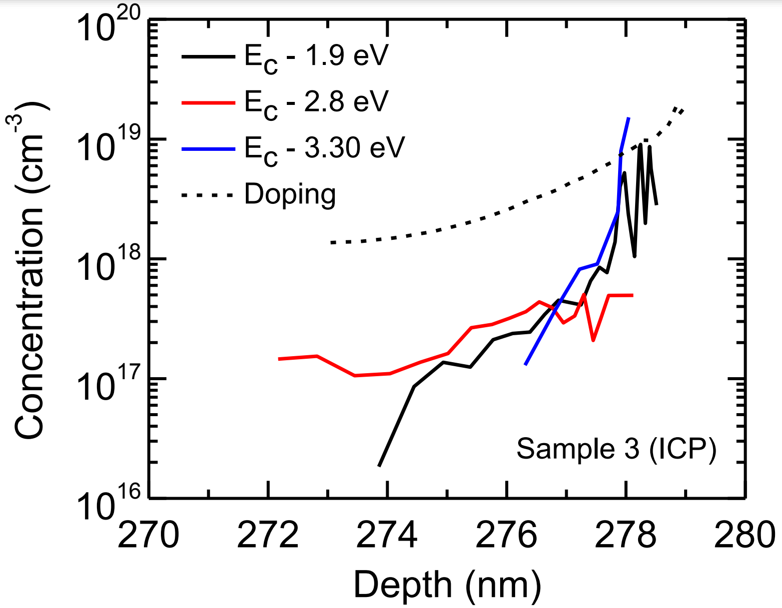
Compared to As-grown material

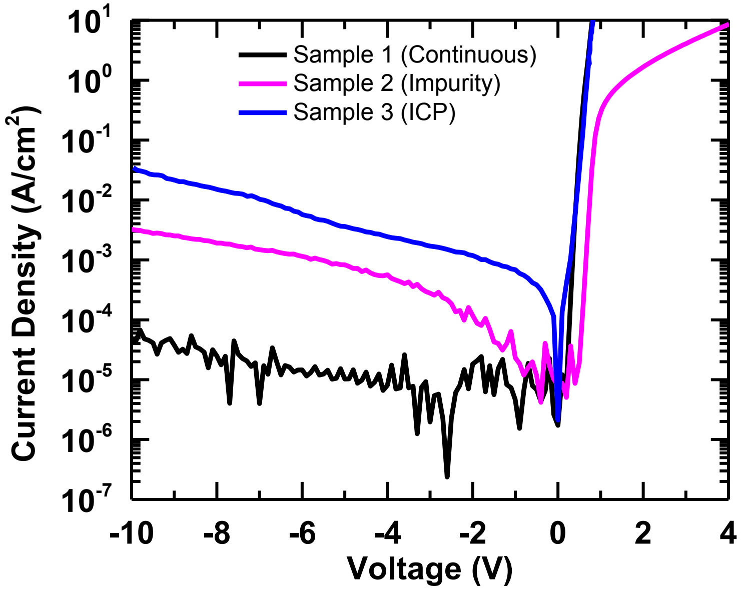
- E_c - 1.9 eV level increases ~ 2000 × (2×10^{17} cm^{-3})
- E_c - 2.9 eV level increases ~ 50 × (1.6×10^{17} cm^{-3})
- E_c - 3.3 eV level increases ~ 45 × (3.3×10^{17} cm^{-3})
- Reverse J ~ 100 × larger (3×10^{-3} A/cm^2 at −10 V)
- N_t nominally same as continuously-grown sample above interface
- Levels highly localized to the regrowth interface

Defect levels in regrown ICP-etched *m*-plane GaN









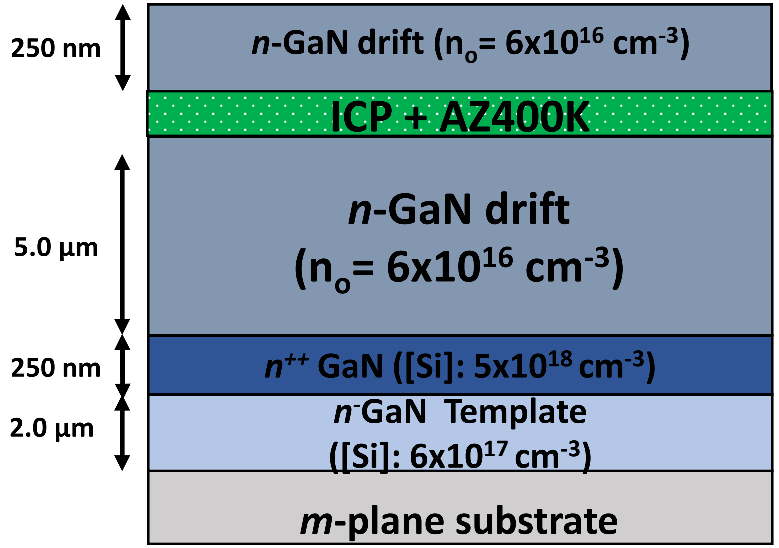
Compared to As-grown material (Near Interface)

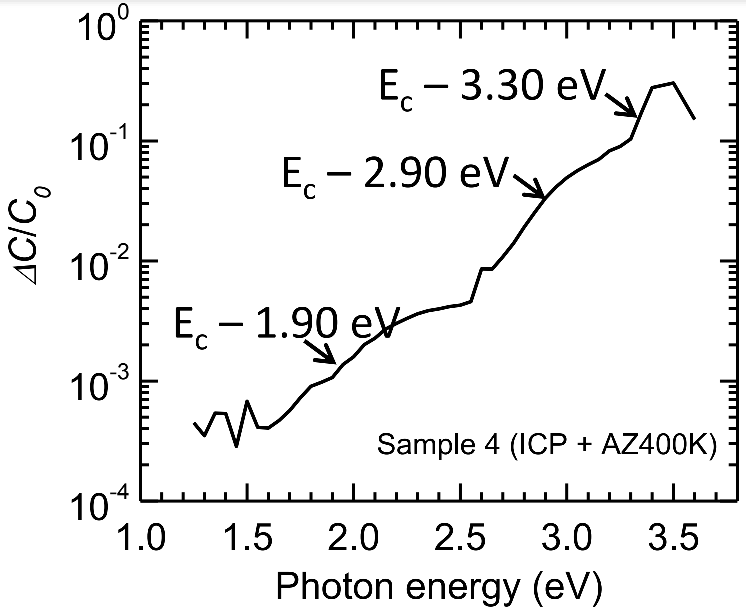
- $\boxed{E_c \text{ - 1.9 eV conc increases} \sim 86{,}000 \times (8.6\times10^{18}\,\text{cm}^{-3})}$
- E_c - 2.9 eV conc increases ~ 167 × (5.0×10^{17} cm^{-3})
- E_c - 3.3 eV conc increases ~ 1,200 × (8.2×10^{18} cm^{-3})
- Reverse J ~ 1000 × larger (3×10^{-2} A/cm^2 at −10 V)

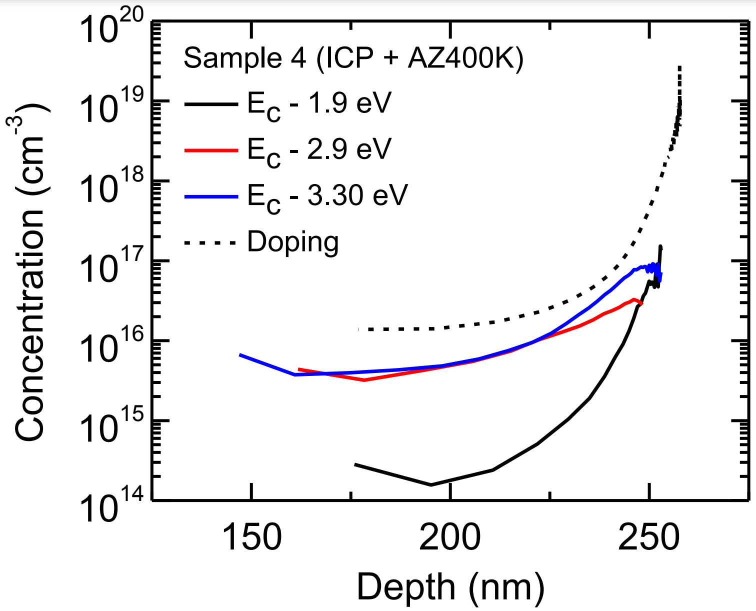
Compared to As-grown material (Above Interface)

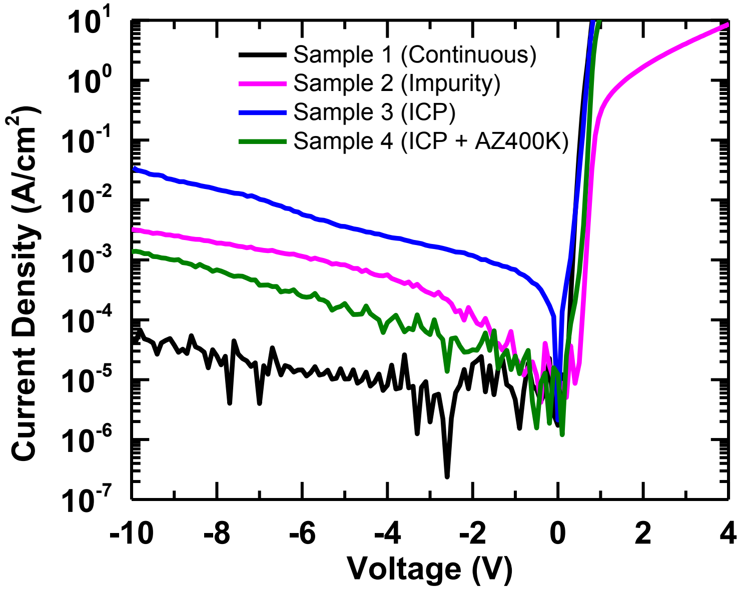
- E_c - 1.9 eV conc. increases ~ 10 × (1.0×10^{15} cm^{-3})
- E_c - 2.9 eV conc. increases ~ 60 × (2.0×10^{16} cm^{-3})
- E_c - 3.3 eV conc. increases ~ 14 × (1.0×10^{17} cm^{-3})

Defect levels in regrown ICP-etched + AZ400K treated *m*-plane GaN









Compared to ICP-etched material (Near Interface)

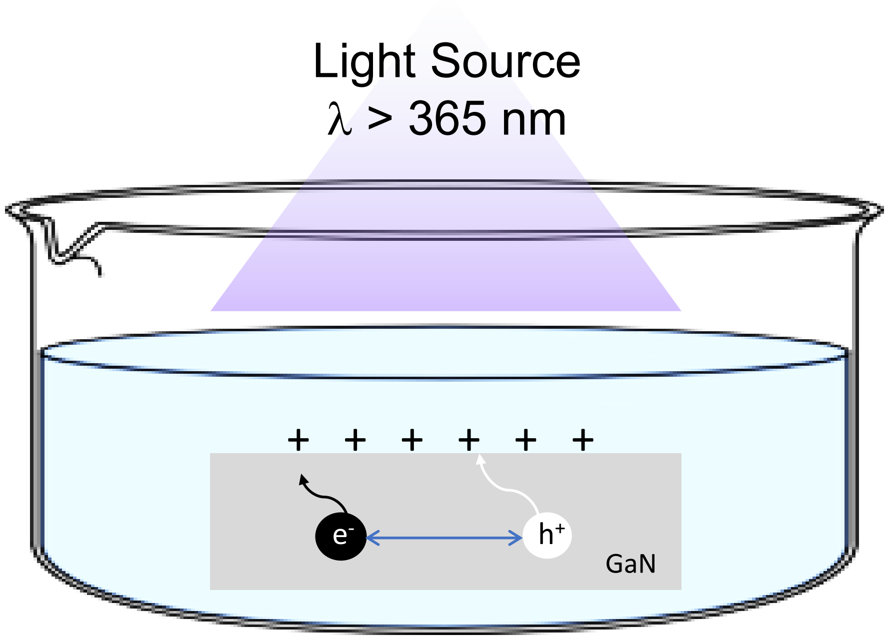
- E_c - 1.9 eV conc reduction ~ 285 × (3.0×10^{16} cm^{-3})
- E_c - 2.9 eV conc reduction ~ 17 × (2.0×10^{16} cm^{-3})
- E_c - 3.3 eV conc reduction ~ 100 × (8.0×10^{16} cm^{-3})
- Reverse J ~ 30 × lower (1×10^{-3} A/cm^2 at −10 V)

Compared to ICP-etched material (Above Interface)

- E_c - 1.9 eV conc. reduction ~ 10 × (1.0×10^{14} cm^{-3})
- E_c - 2.9 eV conc. reduction ~ 7 × (3.0×10^{16} cm^{-3})
- E_c - 3.3 eV conc. reduction ~ 35 × (3.0×10^{16} cm^{-3})

Photoelectrochemical (PEC) etching to remove ICP etch damage

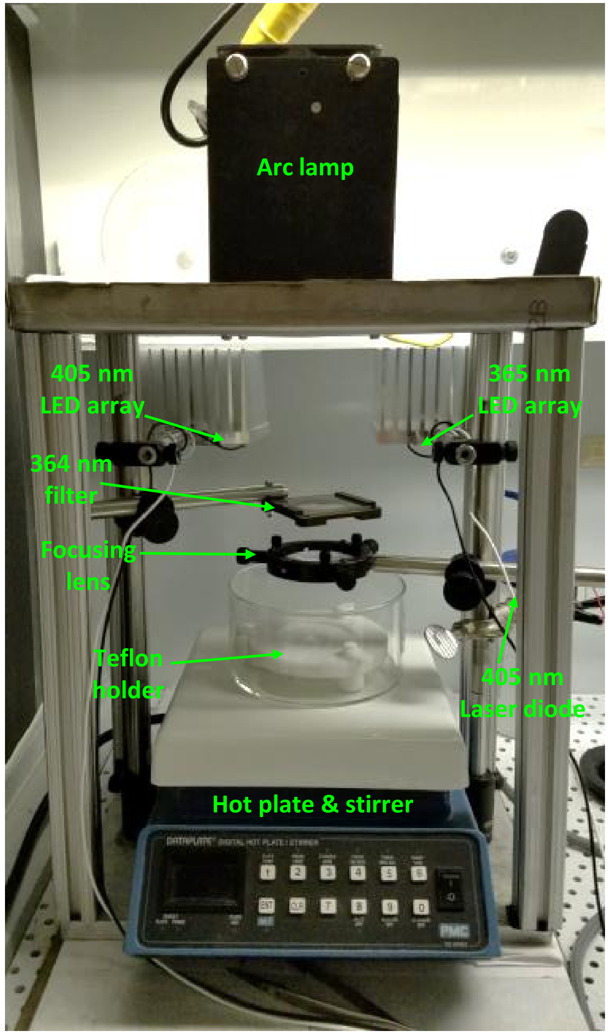
Monavarian, M., Feezell, D., **Aragon, A.**, Mishkat-Ul-Masabih S., Allerman, A., Armstrong, A.M., & Crawford, M. " Removing or preventing dry etch-induced damage in Al/In/GaN films by photoelectrochemical etching." U.S. Patent Application No. 16/684,313. *Patent pending*



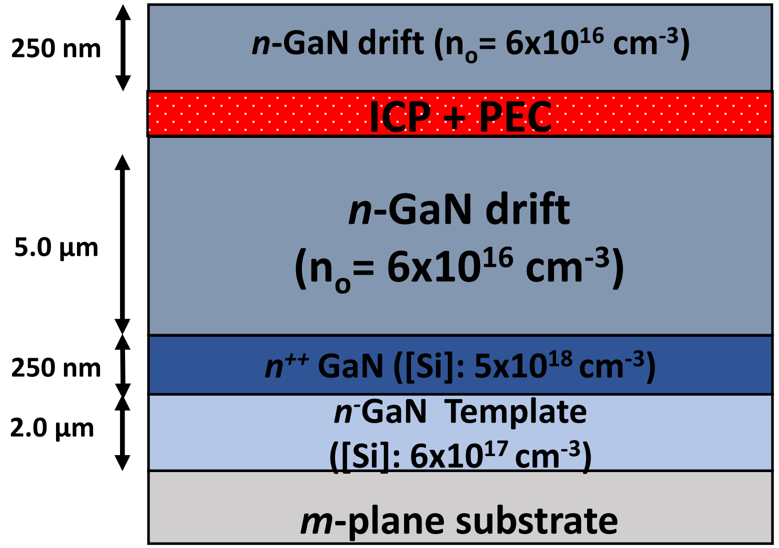
$$GaN + photon \rightarrow GaN + e^- + h^+$$
$$GaN + 3h^+ \rightarrow Ga^{3+} + \frac{1}{2} N_2$$
$$2Ga^{3+} + 6OH^- \rightarrow Ga_2O_3 + 3H_2O$$

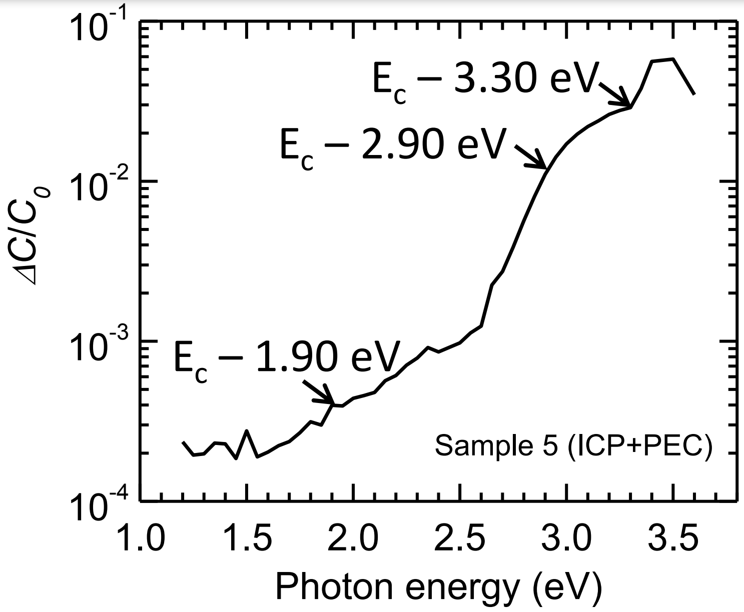
Samples patterned with metal → Immersed in electrolyte → Illuminated with light → Electron-hole pairs generated in smaller band-gap material → Separated by internal field → Oxide formation → Dissolved by electrolyte

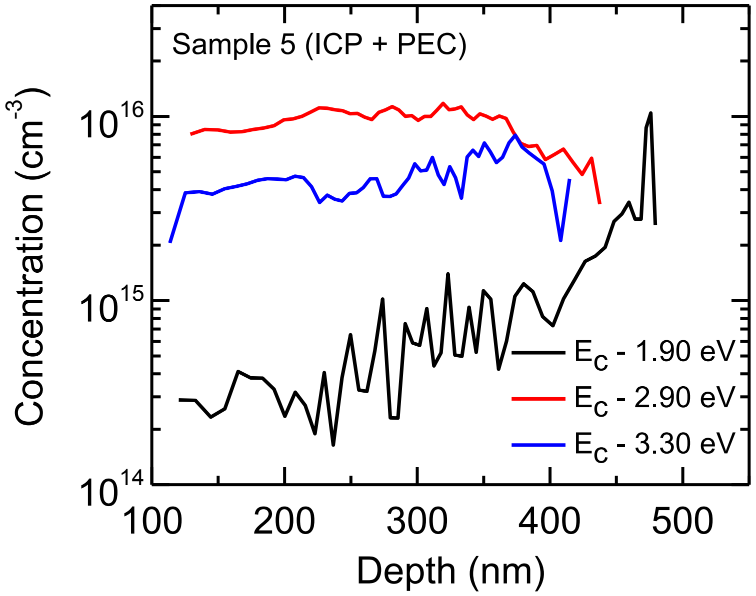
PEC etch setup

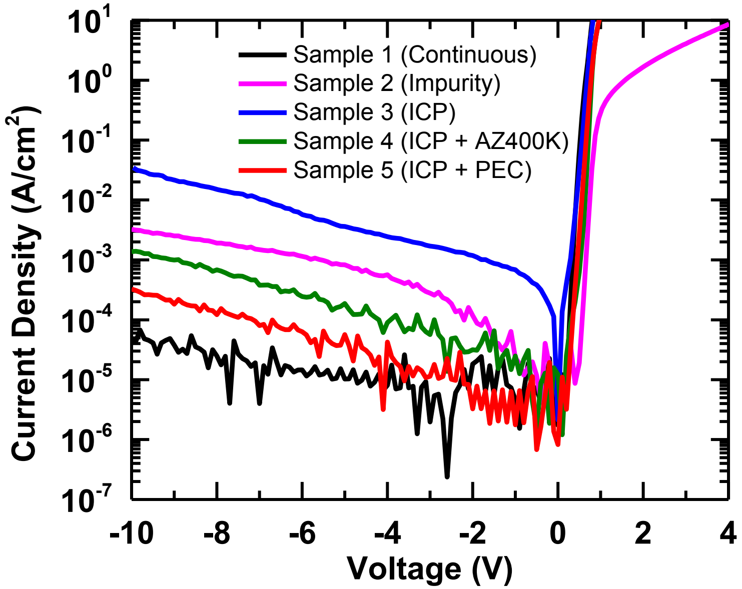


Defect levels in regrown ICP-etched + PEC-etched *m*-plane GaN









Compared to ICP-etched material (Near Interface)

- E_c - 1.9 eV conc reduction ~ 2800 × (3.0×10^{15} cm^{-3})
- E_c - 2.9 eV conc reduction ~ 100 × (5.0×10^{15} cm^{-3})
- E_c - 3.3 eV conc reduction ~ 1200 × (7.0×10^{15} cm^{-3})
- Reverse J ~ 100 × lower (~3 × 10^{-4} A/cm^2 at −10 V)

Compared to ICP-etched material (Above Interface)

- E_c - 1.9 eV conc. reduction ~ 3 × (4.0×10^{14} cm^{-3})
- E_c - 2.9 eV conc. reduction ~ 2 × (9.0×10^{15} cm^{-3})
- E_c - 3.3 eV conc. reduction ~ 33 × (3.0×10^{15} cm^{-3})

Summary

- Investigated dry-etch damage induced deep levels ($E_c - 1.9, 2.9, 3.3\ eV$)
- Localized deep levels associated with interfacial impurities
- Enhanced deep levels associated with ICP dry etching ($\sim 10^2 - 10^4$ increase)
- Increased device performance with ICP etching ($\uparrow J_{forward}, \downarrow V_B$)
- Reduced dry-etch damage via PEC method ($\sim 10^2 - 10^3$ reduction)
- Increased device performance with PEC treatment ($\downarrow\ J_{forward}, \uparrow V_B$)
- PEC as a method to replace ICP etched trenches

Thank You