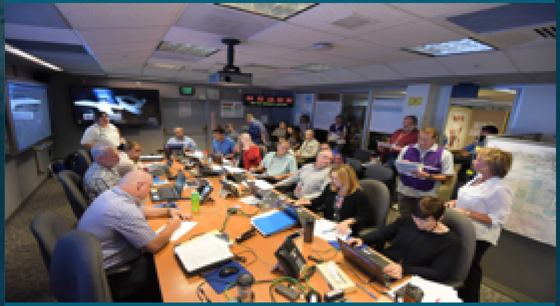
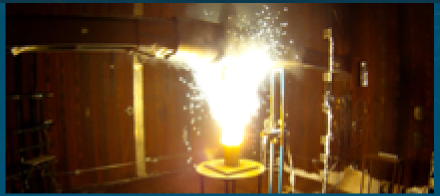
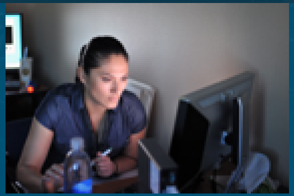
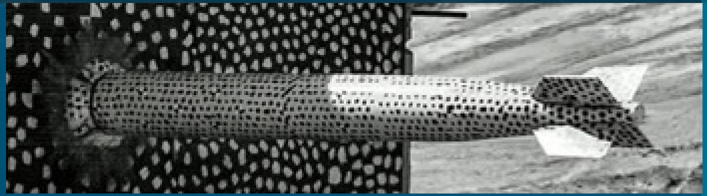
SAND2021-5947PE

Component Testing, Co-Optimization, and Trade-Space Evaluation









Jason Neely

Sandia National Laboratories

June 25, 2021

Project ID: elt223

SAND2021-XXXX C

This presentation does not contain any proprietary, confidential, or otherwise restricted information

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Overview

Timeline

- Start – FY19
- End – FY23
- 50% complete

Budget

- Total project funding
  - DOE share – 100%
- Funding received in FY19: $250k
- Funding for FY20: $350k
- Funding for FY21: $350k

Goals/Barriers

- Drive System Power Density = 33 kW/L
  - Power Electronics Density = 100 kW/L
  - Motor/Generator Density = 50 kW/L
- Power target > 100 kW
- Cost target for drive system ($6/kW)
- Operational life of drive system = 300k miles
- Design constraints include
  - Thermal limits
  - Transistor / Diode reliability
  - Capacitor reliability

Partners

- Scott Sudhoff, Steve Pekarek – Purdue University
- Jon Wierer – Lehigh University
- Woongie Sung – State University of New York (SUNY)
- Project lead: Sandia Labs, Team Members: Lee Gill, Lee Rashkin, Luke Yates, Ganesh Subramanian, Jack Flicker, Andrew Binder, Todd Monson, Bob Kaplar

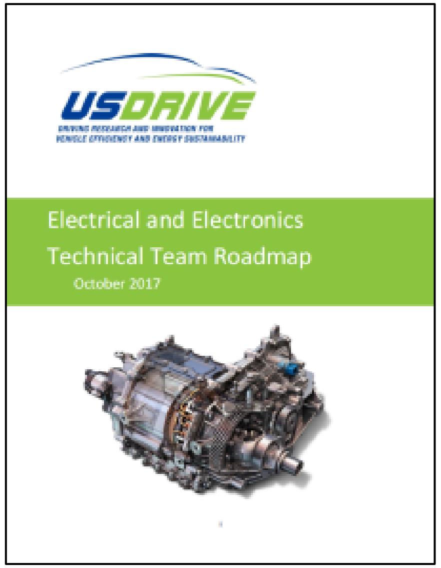
LEHIGH UNIVERSITY

PURDUE UNIVERSITY

SUNY Poly Albany Campus

Relevance and Objectives

- The primary purpose of this project is to identify electric traction drive (ETD) designs, including inverter drive and electric machine, that are predicted to meet the goals outlined in the US Drive Electrical and Electronics Technical Team Roadmap [1]:
  - Power Density target for drive system = 33kW/L or a 100 kW peak system
    - Power Electronics Density = 100 kW/L
    - Electric Motor Density = 50 kW/L
  - Operational life of drive system = 300k miles
  - Cost target for drive system ($6/kW)
- To support this design goal, this effort has four objectives
  - Evaluate options for reducing size of filter and thermal management components
  - Generate high-fidelity dimensional and electrical models for principal power electronic components within a novel inverter design
  - Demonstrate and evaluate representative converter prototypes
  - Co-Optimize inverter and machine designs for power density, reliability, and efficiency



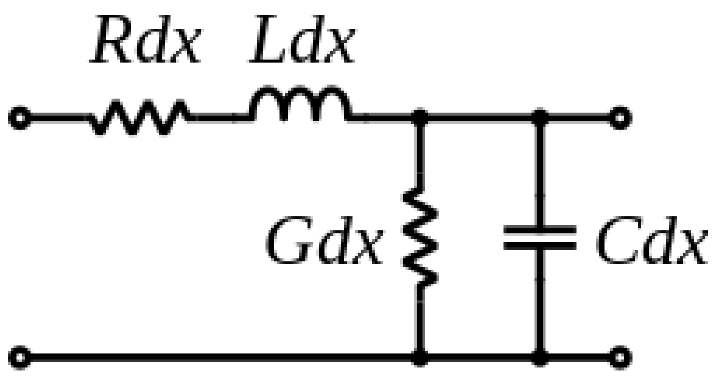
[1] See the U.S. DRIVE Partnership Plan, at https://www.energy.gov/eere/vehicles/downloads/us-drive-electrical-and-electronics-technical-team-roadmap

Approach: Distributed Bus Filter

Objective: Evaluate options for reducing size of filter components

Can we use the distributed inductance and capacitance in the transmission bus to filter out undesired frequencies, eliminating lumped-element filter components

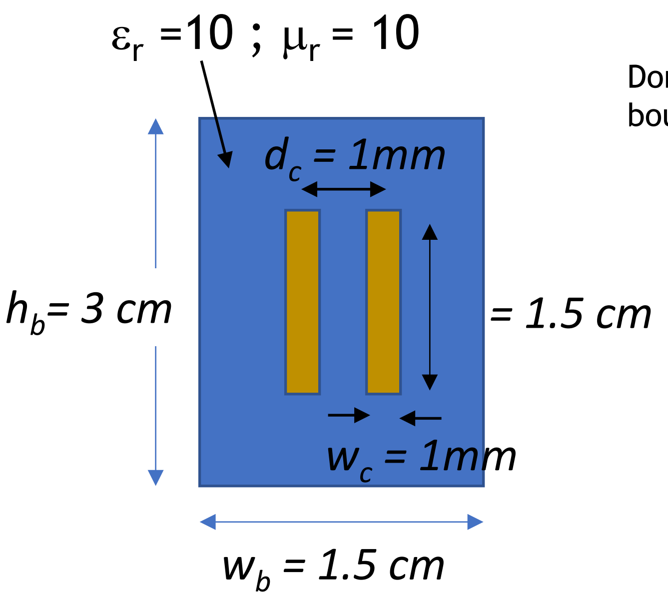
- Current ripple : Switching frequency is 100 kHz => target f_c ~ 10 kHz
- EMI: Edge rates are ~ 80 nsec => target f_c ~ 500 kHz

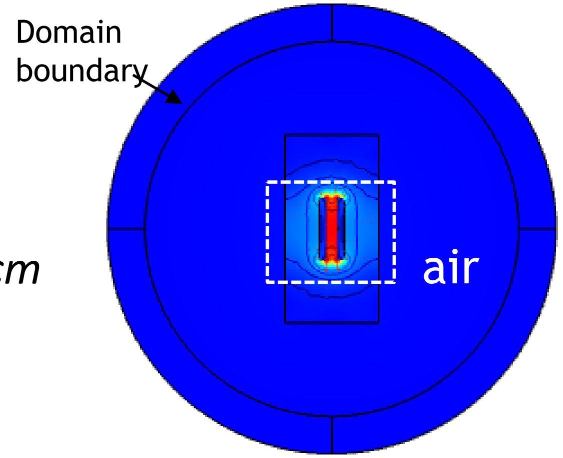


Electromagnetic simulation (COMSOL®) preliminary designs

- 2-wire system example system
- Composite background medium : ε_r =10 ; μ_r = 10
- 2D and 3D models developed to estimate performance

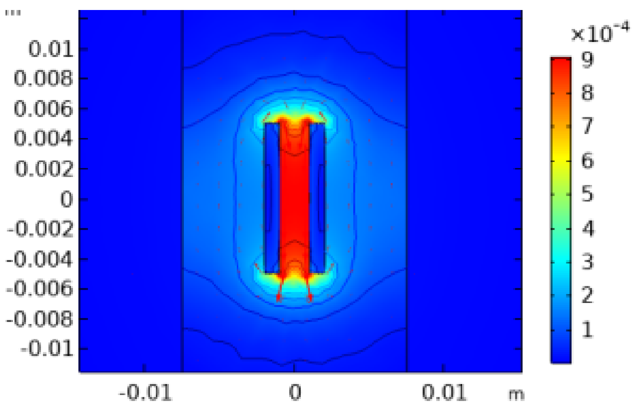
2D simulation



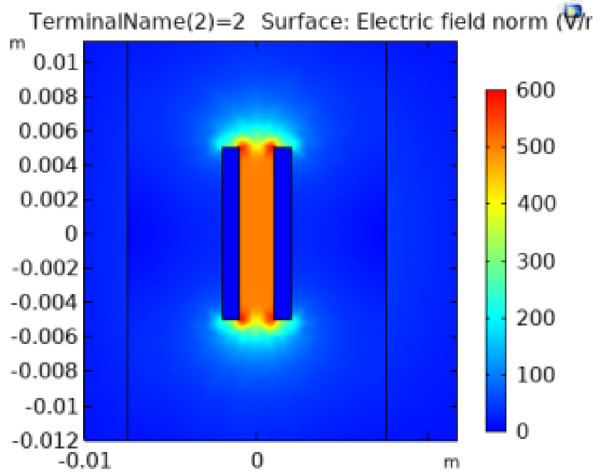


B field (@ 1KHz)

B field

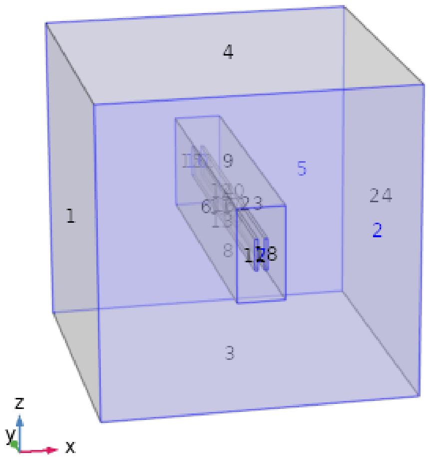


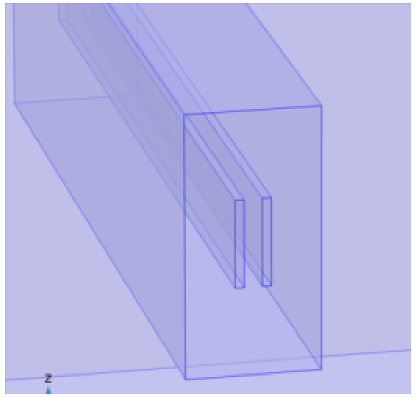
E field



Technical Accomplishments: Distributed Bus Filter

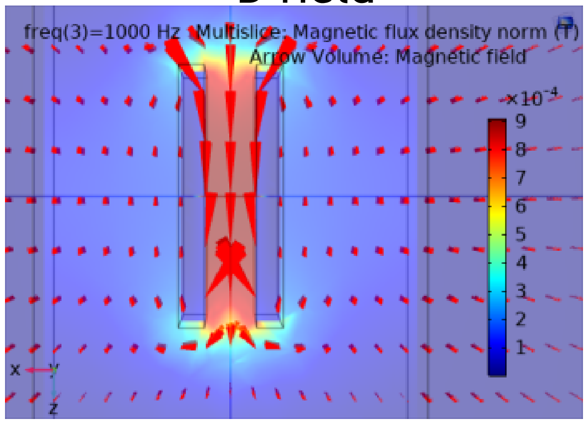
3D simulation



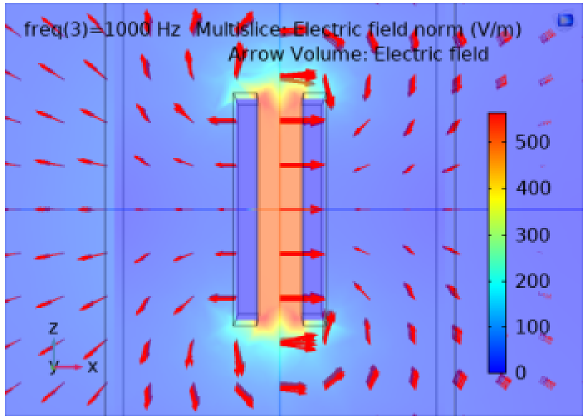


L ~ 1.8 μH/m
C ~ 588 pF/m

B field



E field

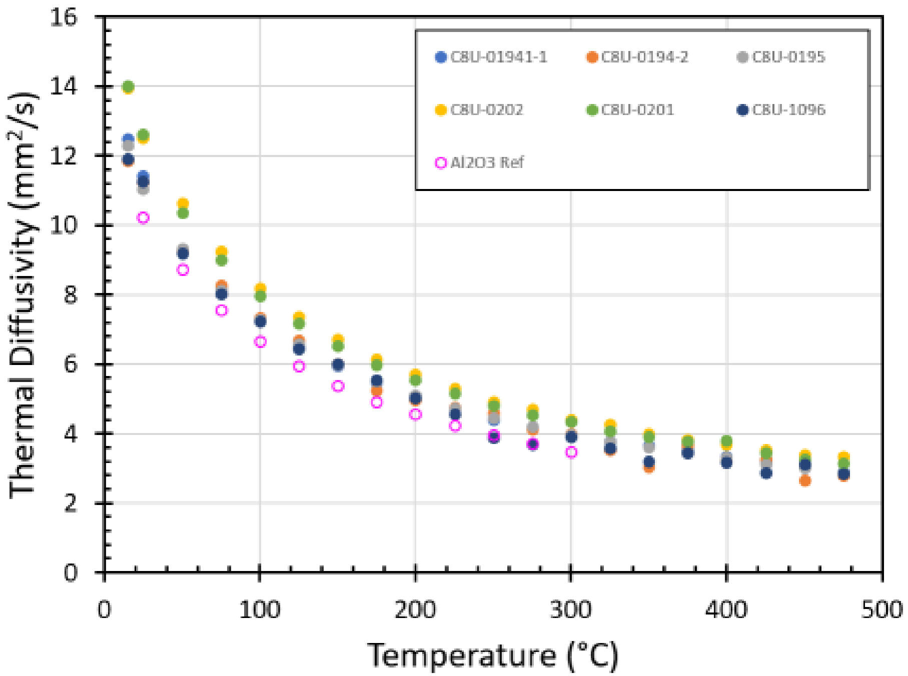


- 3D simulations gives L,C values similar to that from 2D simulations
  - 2D simulations can be a good guide : computationally expedient
- Current values of L and C are low (~ μH/m and ~ nF/m)
- Using simulation, filter cut-off frequency estimated: for *l* =20 cm, f_c ~ 24.5 MHz
- Will explore additional geometries and multiphasic design to increase L,C

Approach: Surround Cooling Concept

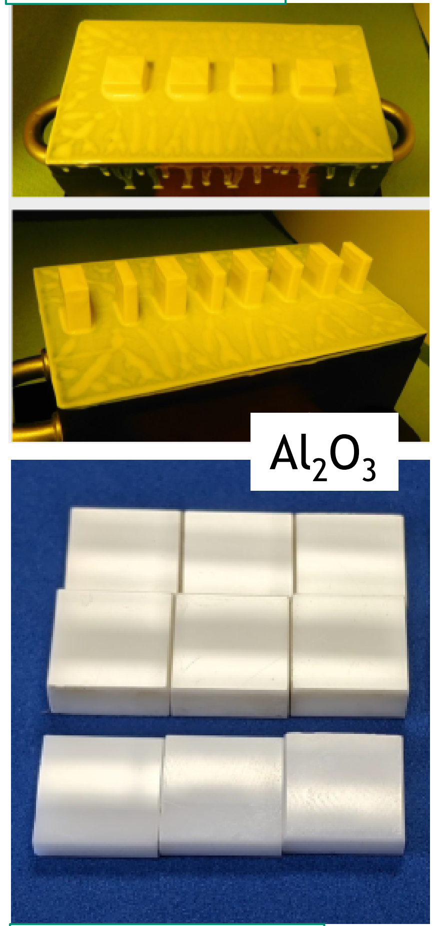
Objective: Evaluate options for reducing size of thermal management components

- State-of-the-art ceramic additive manufacturing technology allows for materials with exceptional thermal properties
- By surrounding or fully encasing a power device with a ceramic, heat spreading will result in reduced device temperatures.
- Features such as pin fins and cooling channels can be incorporated into the printed ceramic.
- Al_2O_3 samples printed by Lithoz Inc. and evaluated via flash diffusivity measurements were then fed into thermal simulations to evaluate the effectiveness of the surround cooling concept.



Printed Al_2O_3 ceramics measured thermal conductivities ranged from: 33.5 to 38.7 W/m-K and demonstrated a linear correlation with density.

As printed

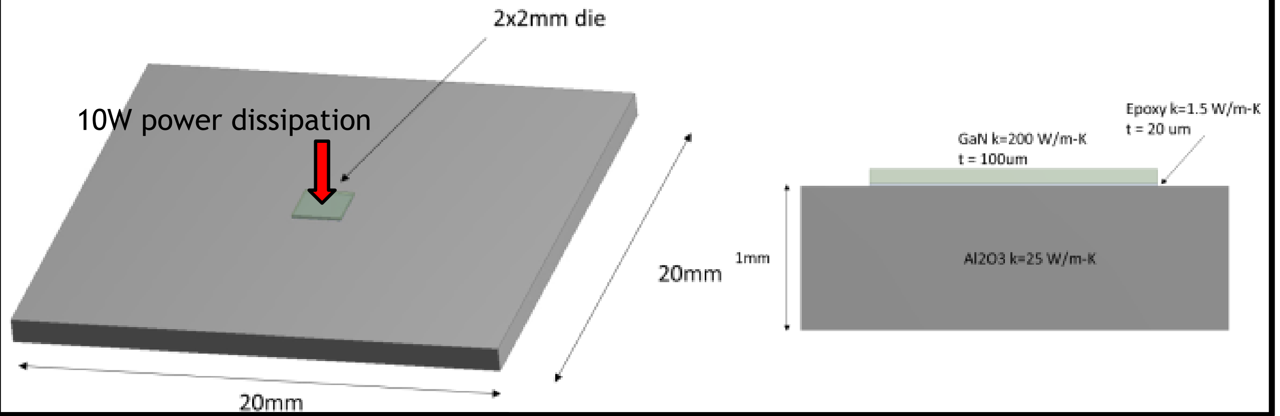


Sintered and polished

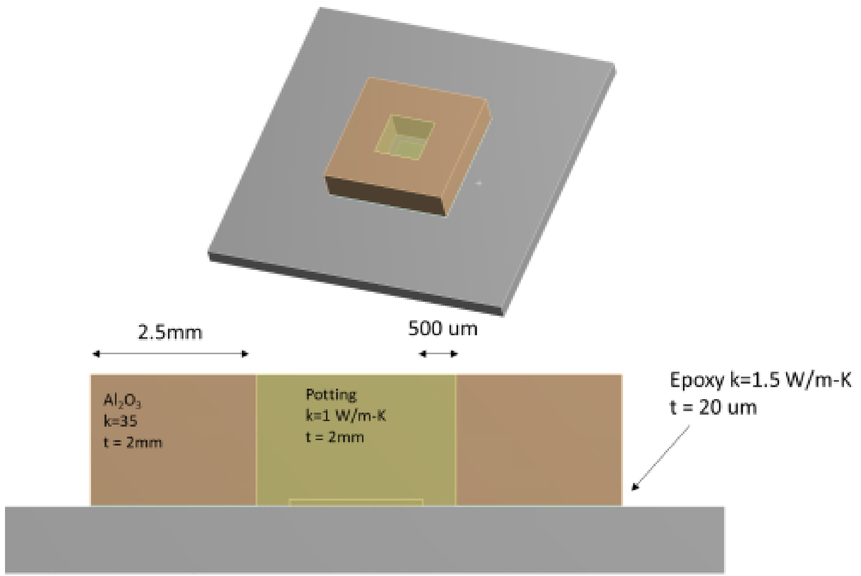
Technical Accomplishments: Surround Cooling Simulations

- Al_2O_3 3D printed ceramics can be used to surround and even encase electronic components with significant thermal loads. (high resolution features ~100 µm)
- Preliminary modeling results show a potential **29% reduction** in temperature rise for encased cooling with fins

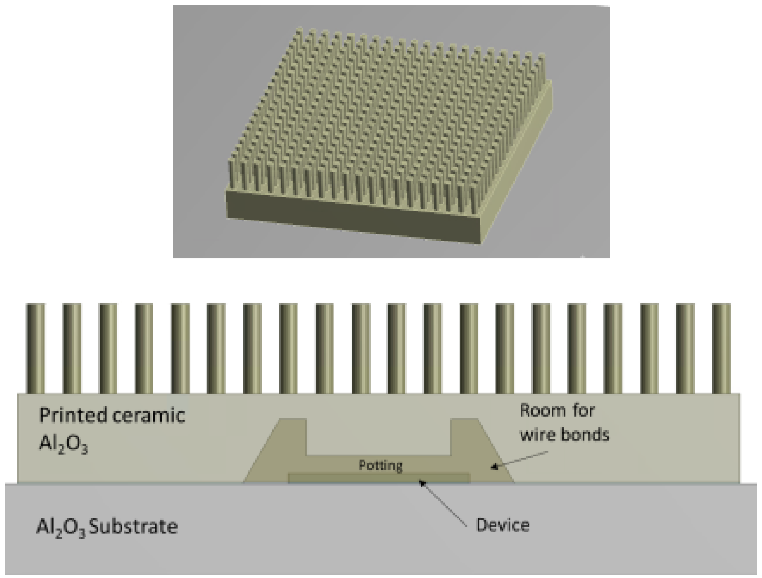
Case #1 Baseline – no surround cooling

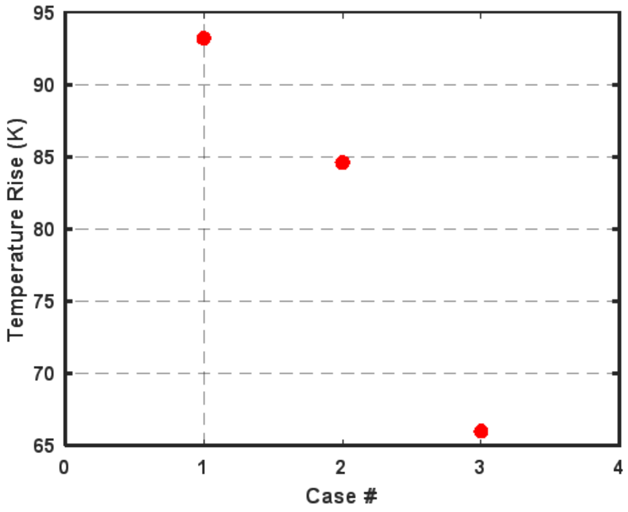


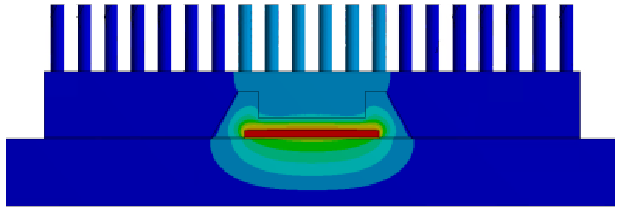
Case #2 Surround ceramic with potting



Case #3 Fully encased device with fins







Approach: Converter and Inverter Optimization

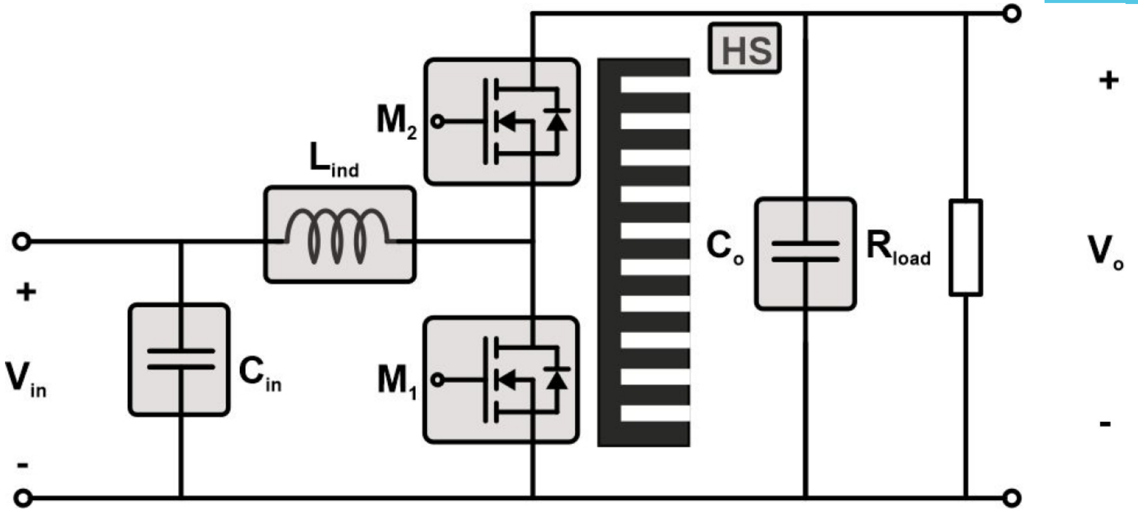
Converter optimization software exercised to optimize boost converter for power density and reliability

Mean-Time-Between-Failure (MTBF)

- Metric to evaluate or estimate the expected lifetime of repairable items.
- Defined as the probability of an individual unit of interest, operating with full functionality for a specific length of time under specific tests or stress conditions.
- MTBF of power electronic systems requires understanding of dynamics in thermal and electrical stress on a system

Boost Converter Parameters Affecting Reliability or MTBF and Power Density

- Input & output voltage on the input and output capacitors
- Switching frequency affects transistor switching and conductor losses, and core loss (thermal stress)
- Inductor current ripple factor affects the core size and transistor stress
- Capacitor ripple factor affects the capacitor volume and temperature of operation



$$MTBF = \frac{\text{Total System Operational time}}{\text{Total Number of Failures}}$$

Can also be represented as

$$MTBF = \frac{1}{\lambda}$$

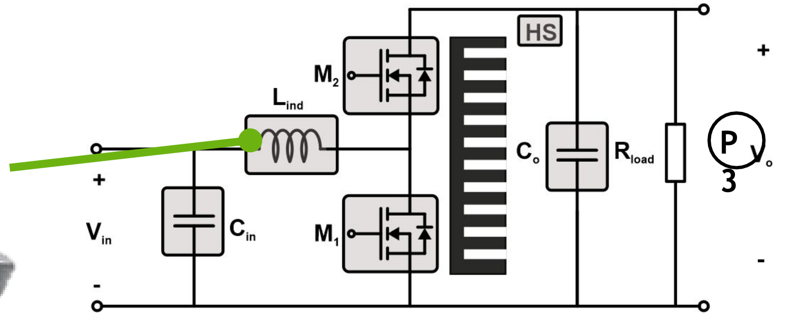
Where

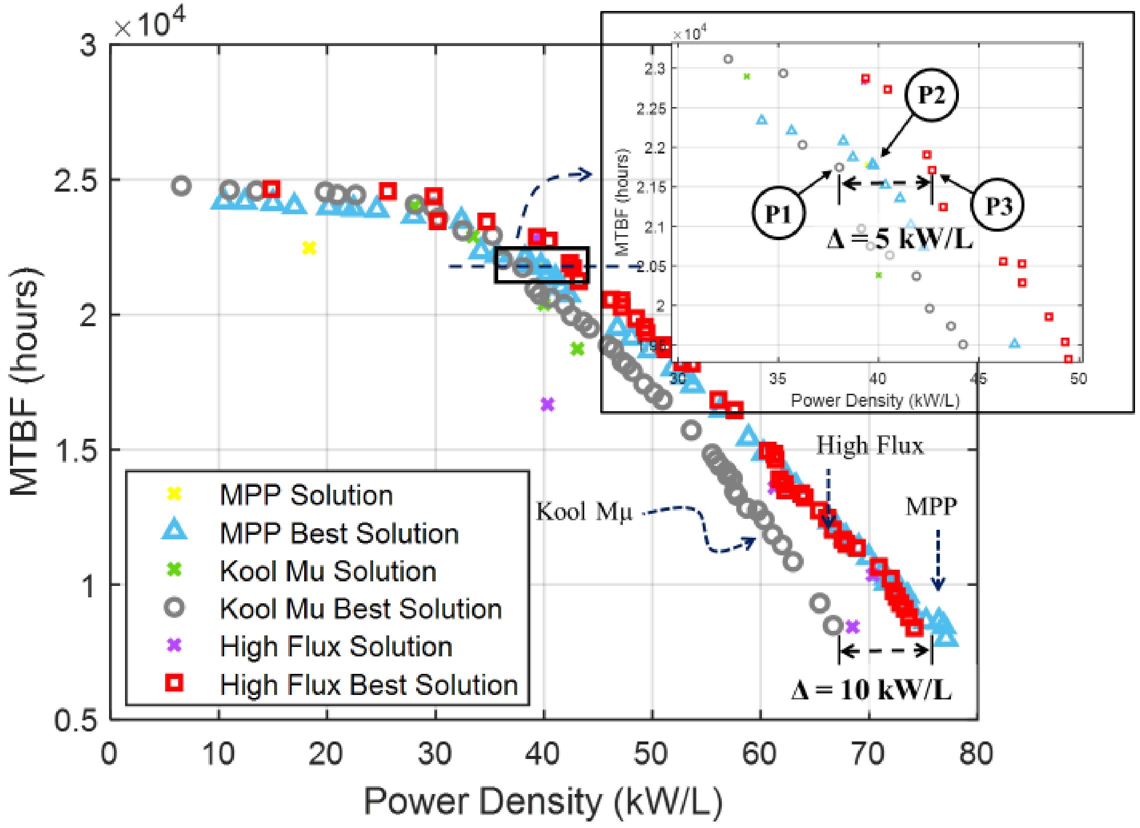
λ: Intrinsic failure rate of a component

For a given system composed of n components,

$$\lambda = \sum_{i=1}^{n} \lambda_i$$

Technical Accomplishments: Boost Converter Optimization

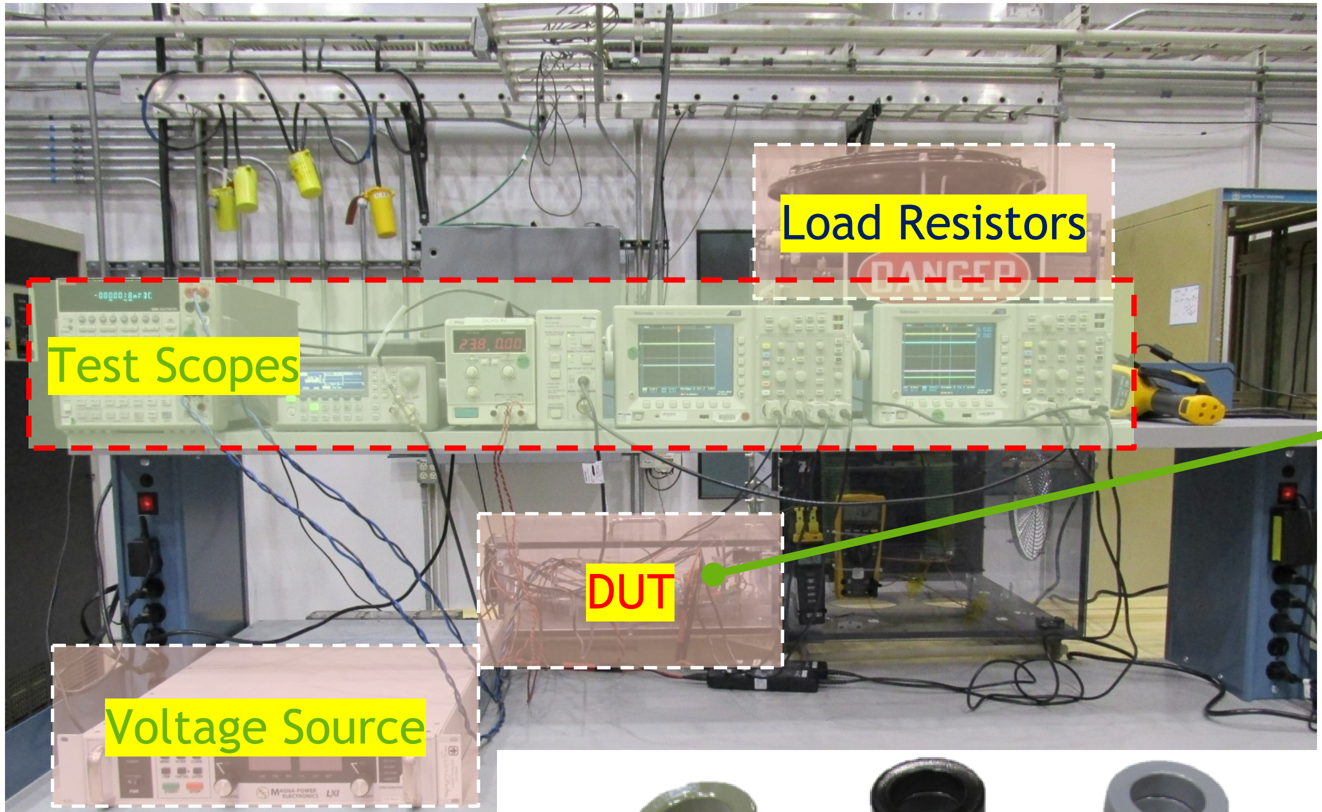


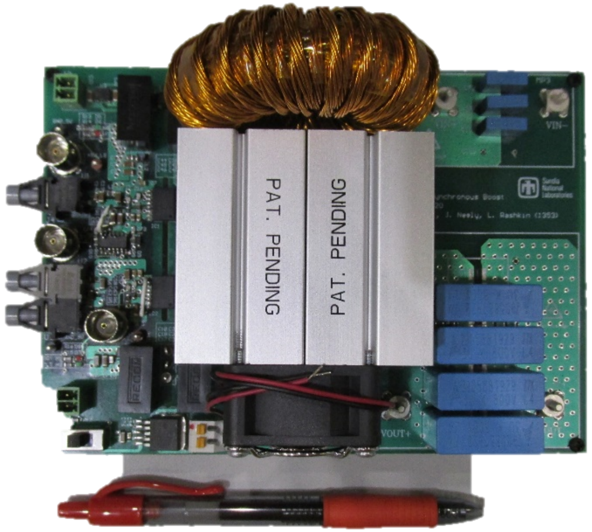


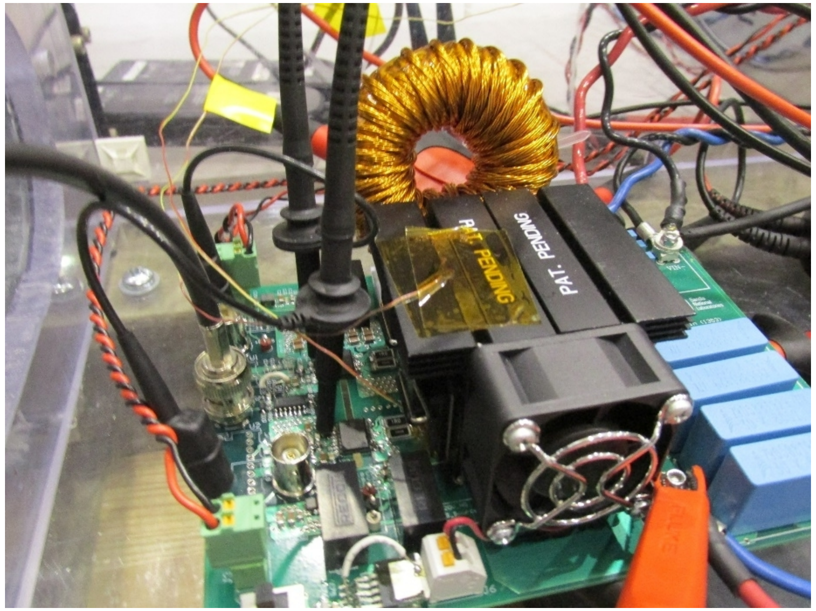
Operating Condition			
Variable	P1 (Kool Mμ)	P2 (MPP)	P3 (High Flux)
Input, Vin	400V	400V	400V
Output, Vo	500V	500V	500V
[illegible] – [illegible]	7.47-17.78A	9.9-15.35A	10.74-14.57A
[illegible]	47.37 kHz	48.7 kHz	47.87 kHz
Duty Cycle	20.81%	20.8%	21.4 %
[illegible]	78.8°C	75.19°C	75°C
Inductance	169 μH	310 μH	462 μH
Input Capacitors		**Output Capacitors**	
Model #	B32641B6682J	Model #	B32774X8305
Capacitance	3×6.8 nF	Capacitance	4×3 μF
Boost Inductor			
AWG/Strands	23 AWG/10	23 AWG/10	23 AWG/10
Model #	0077717A7	C055716A2	C058110A2
Fill Factor	20%	17.7%	24%
Turns Number	52	46	78
Loss (W/C)	10.53W/10.8W	10.89W/7.09W	7.84 W/8.8 W
Temp. Rise	48.6 °C	35 °C	90 96 °C
Low Side Semiconductor Device			
Model #	C2M0040120D	C2M0040120D	C2M0040120D
Loss (Ton/Toff/Cond)	2.09W/3.45W/1.33W	2.69W/3.13W/1.33W	2.88 W/2.98 W/1.37W
High Side Semiconductor Device			
Model #	C2M0040120D	C2M0040120D	C2M0040120D
Loss (Ton/Toff/Cond)	5.82W/2.28W/5.05W	4.68W/2.5W/5.05W	2.88 W/2.98 W/1.37 W
Total Efficiency	99.16%	99.2%	99.2 %

Technical Accomplishments: Boost Converter Optimization

- Experimental hardware was developed to represent designs from Pareto Front and validate boost converter simulation model



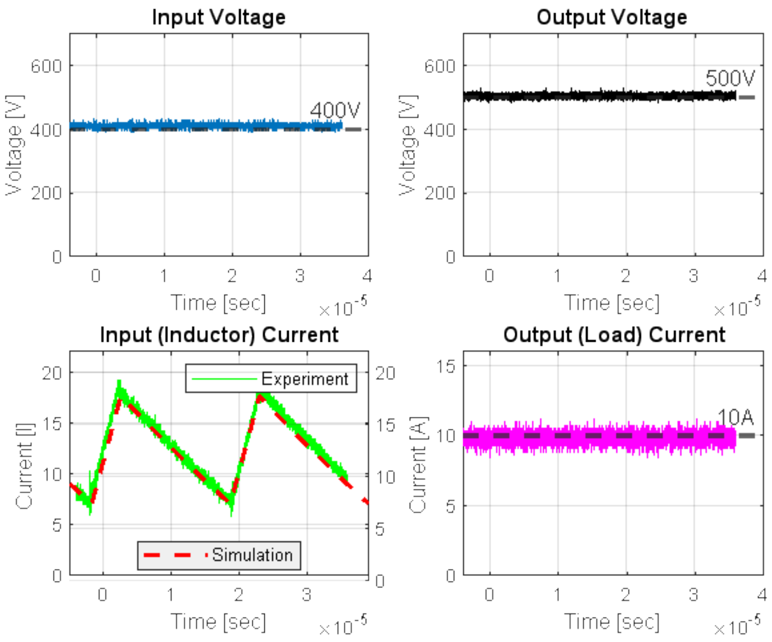




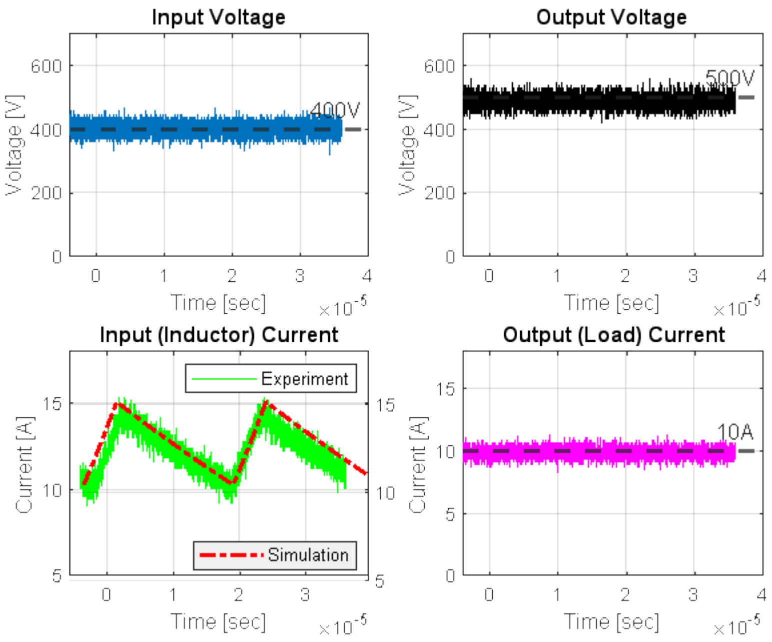
Technical Accomplishments: Boost Converter Optimization

Experimental Results and Simulation Comparison

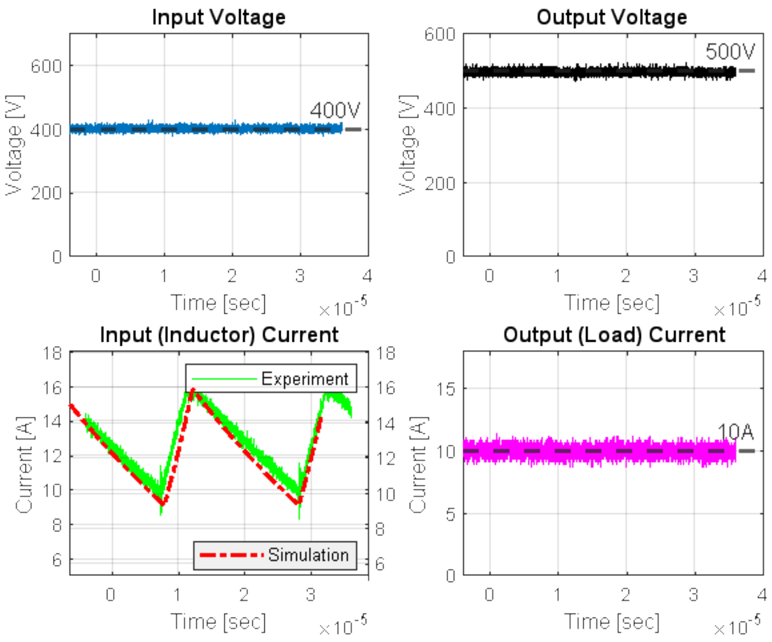
(P1) Kool Mμ



(P2) MPP

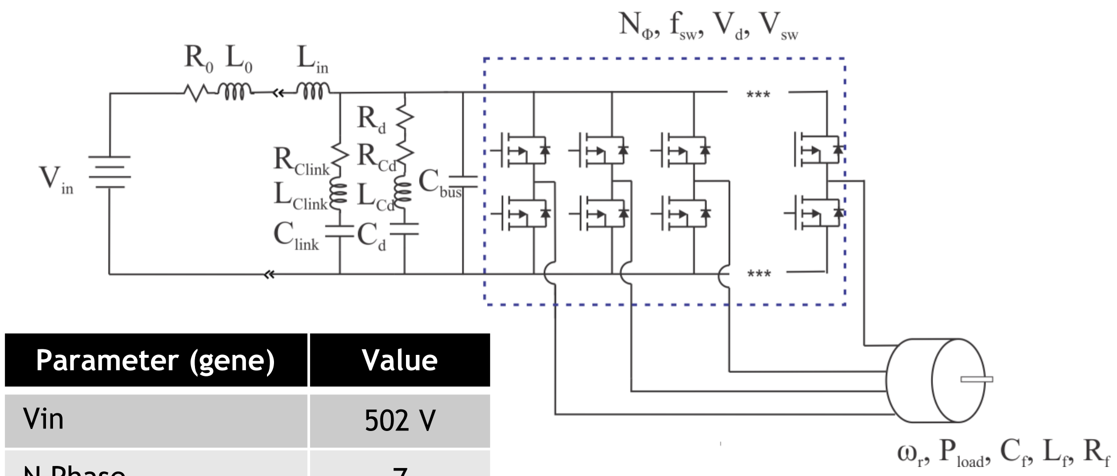


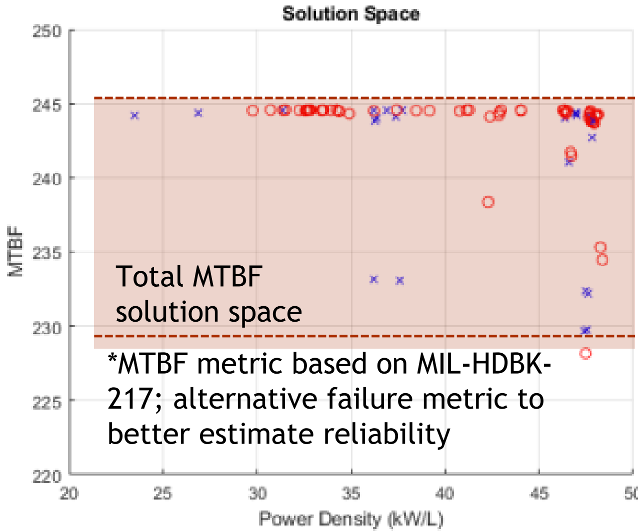
(P3) High Flux

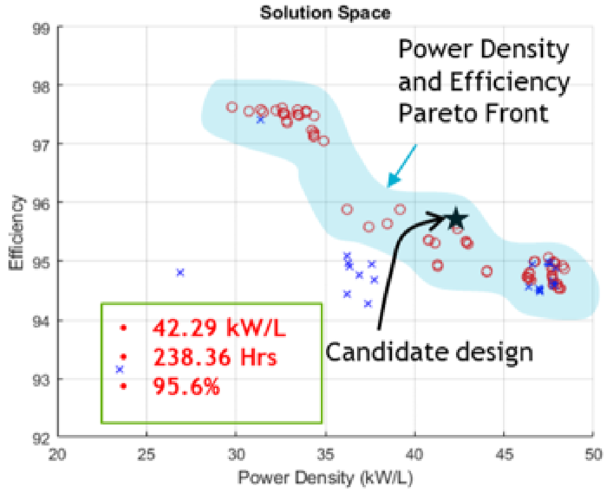


Parameter	Estimated (P1/P2/P3)	Actual (P1/P2/P3)
Efficiency	99.16% / 99.2% / 99.2%	97% / 98.8% / 98.9%

Technical Accomplishments: Inverter Optimization

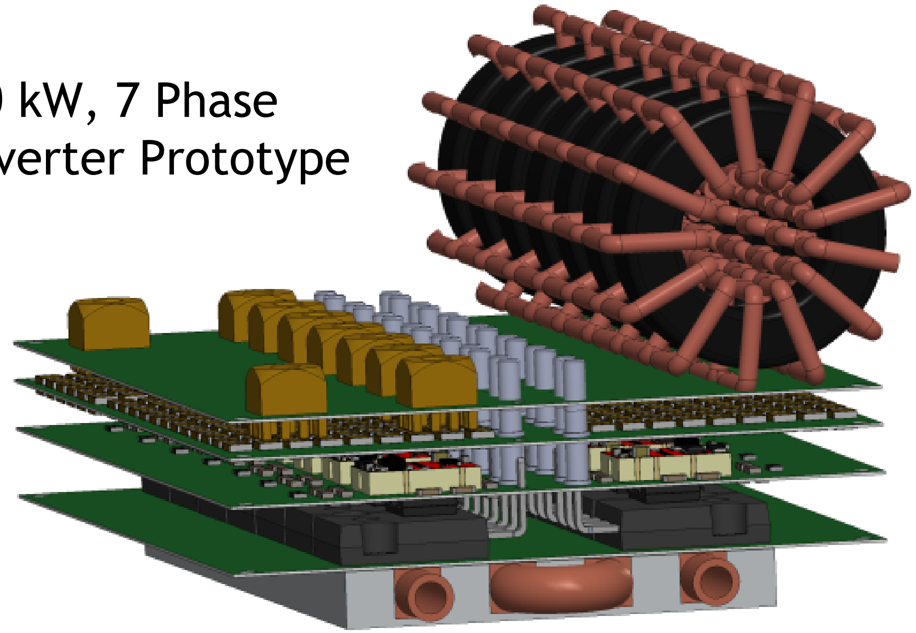






Parameter (gene)	Value
Vin	502 V
N Phase	7
Switching Frequency	46.5 kHz
Filter Inductance	16 µH
DC Link	51 µF

10 kW, 7 Phase Inverter Prototype



Module	Specifications	Power Loss	Estimated Volume	Actual Volume
DC Link	0.1µF (1808) X 512	-	19.3 mL	54.2 mL
Cooling	Cold Plate*	-	0.1218 mL*	53.14mL
Filter Inductors	0058326A2 (OD:3.5cm, HT:4cm)	185.97 W	272 mL	313.26 mL
Power Devices	1.2 kV SiC MOSFETs	408.5 W	12.8 mL	57.4 mL
Total	-	594.5 W	304.2 mL	478 mL
Remarks	-	η=95.6 %	*Possible error in cooling calculation	*Based on 3D rendering

Collaboration

PURDUE UNIVERSITY

<u>Purdue University/Sonrisa Research, Inc. (Scott Sudhoff)</u> – Working with Sandia to co-optimize motor and drive

LEHIGH UNIVERSITY

<u>Lehigh University (Jon Wierer)</u> – Working with Sandia for design/simulation/modeling of GaN JBS diodes.

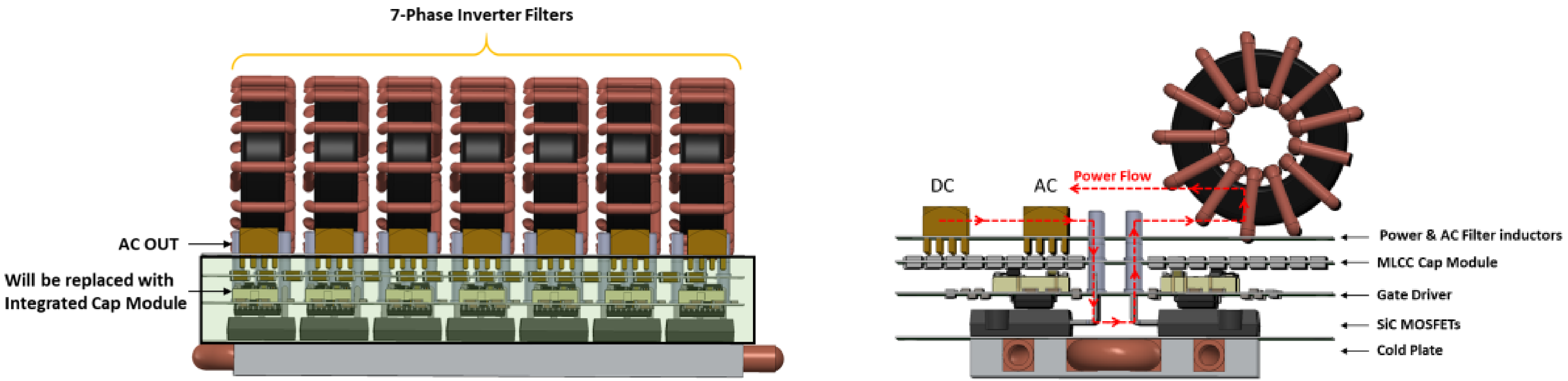
SUNY Poly Albany Campus

<u>State University of New York (SUNY) (Woongie Sung)</u> – Fabricating SiC JBS diode integrated with MOSFETs

Proposed Future Research

Remaining FY21 Tasks

- Building and Testing Reduced Scale Prototypes
  - 10 kW peak (5.5 kW continuous) Inverter Drive
- Update Optimization to identify design for 100 kW peak, 55 kW continuous



Research in FY22 and Beyond

- Co-Optimize inverter and Homo-Polar motor in development by Purdue University
- Build inverter exemplar using Sandia-developed GaN devices

* Any proposed future work is subject to change based on funding levels

Summary

- Advanced components are being developed to reduce the size of filters and thermal management components
- A research approach is identified to model, develop, and simulate power components and to optimize a power train design using multi-objective optimization tools
- This optimization approach enables a holistic-approach to the drive design
  - Design codes are first being developed to optimize candidate power electronic and motor designs separately; these will then be merged to co-optimize these two components
  - Each year, hardware prototypes will be developed to verify designs and recalibrate models
  - Sandia is working closely with Purdue; Purdue is focusing on the machine optimization
- Progress has been made on the development of modeling tools and advanced performance evaluation methods, i.e. MTBF calculation
- Candidate designs have been designed and built, focusing first on a boost converter; design codes are being applied next to inverter drives
- Next steps will focus on building and testing inverter prototypes

Reviewer-Only Slides

Publications and Presentations

- **Publications**
  - L. Rashkin, J. Neely, J. Flicker, R. Darbali; “Optimal Power Module Design for High Power Density Traction Drive System”; *IEEE Transportation Electrification Conference* (ITEC2020); Chicago, IL; June 24-26 2020.
  - L. Gill, J. Neely, L. Rashkin, J. Flicker and R. Kaplar; "Co-Optimization of Boost Converter Reliability and Volumetric Power Density Using Genetic Algorithm“; *2020 IEEE Energy Conversion Congress and Exposition* (ECCE2020); Detroit, MI; Oct 11-15, 2020.

- **Presentations**
  - J. Neely, G. Pickrell, J. Flicker, L. Rashkin, R. Kaplar ; “The Case for Vertical Gallium Nitride Devices in Electric Vehicle Drives"; *2020 IEEE Applied Power Electronics Conference* (APEC2020); Industry Session: Vehicle Electrification II, Delayed Virtual Event

Critical Assumptions and Issues

- Power density targets are based on the combined volume of all power electronic modules and machines (whether there be one centralized drive with motor or 4 in-wheel drives with motors) needed to achieve total power

- DOE targets pertaining to reliability can be established using limited laboratory testing that is scaled using reliability models.