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# Modeling and Assessment of Atomic Precision Advanced Manufacturing (APAM) Enabled Vertical Tunneling Field Effect Transistor

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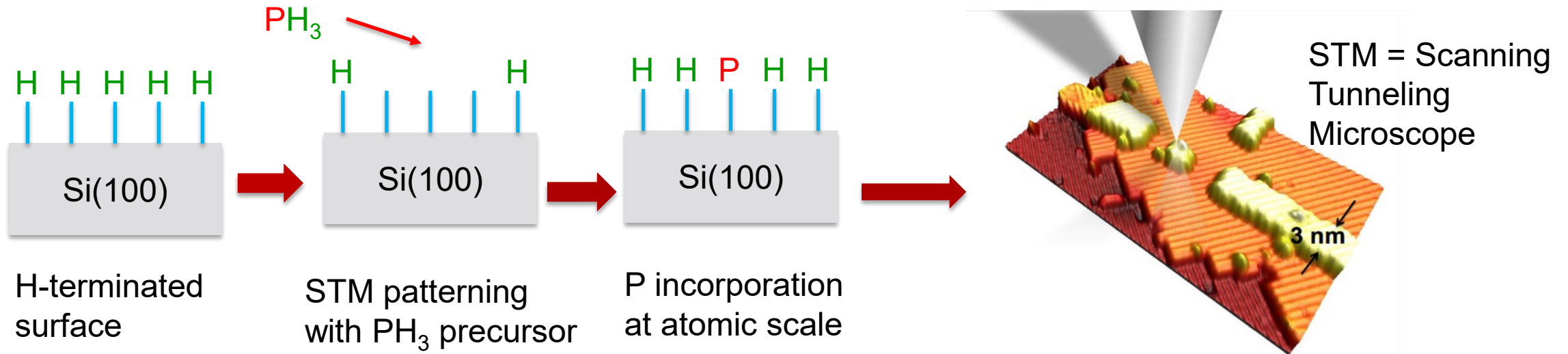
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# Atomic Precision Advanced Manufacturing (APAM)

**APAM is a process of area-selective dopant incorporation at the atomic scale**



APAM key properties (vs. standard processing)

- Atomic precision
- Extremely high density of dopants

APAM is widely used for making qubits<sup>[1]</sup> which operate at cryogenic temperatures.

Unique opportunity in microelectronic from the atomic physical limit

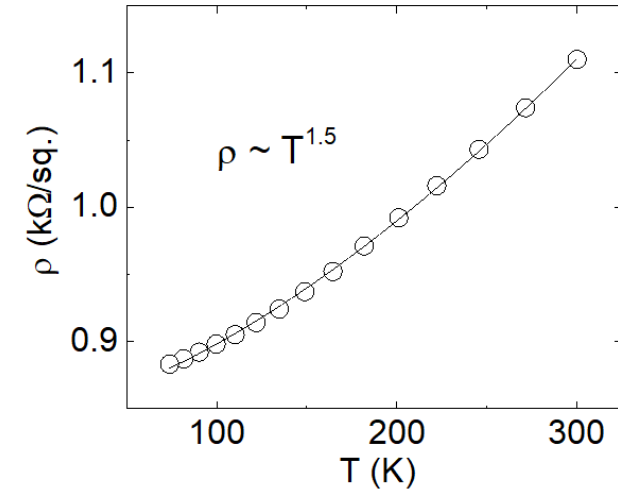
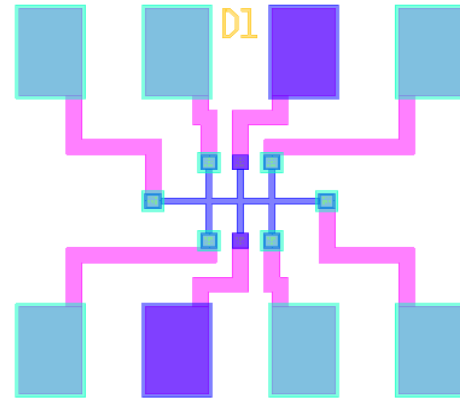
[1] Y. He, *et al.*, "A two-qubit gate between phosphorus donor electrons in silicon," *Nature*, vol. 571, pp. 371-375, 2019.

# APAM achievements toward microelectronic

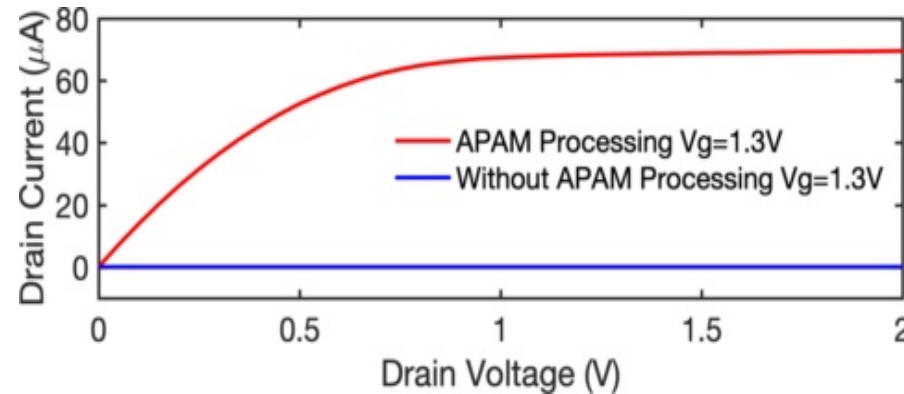
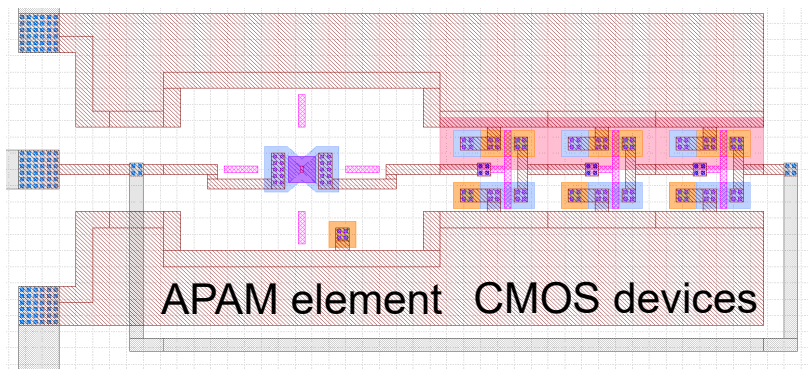
## □ Room-temperature operation

X. Gao, et al., Modeling Assisted Room Temperature Operation of Atomic Precision Advanced Manufacturing Devices, presented at 2020 SISPAD.

APAM Hall bar geometry



## □ APAM-CMOS Integration

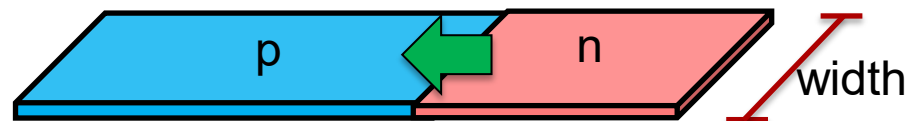


## □ APAM based vertical tunneling field effect transistor (APAM-VTFET) proposed

# Using APAM to address current TFET limitations

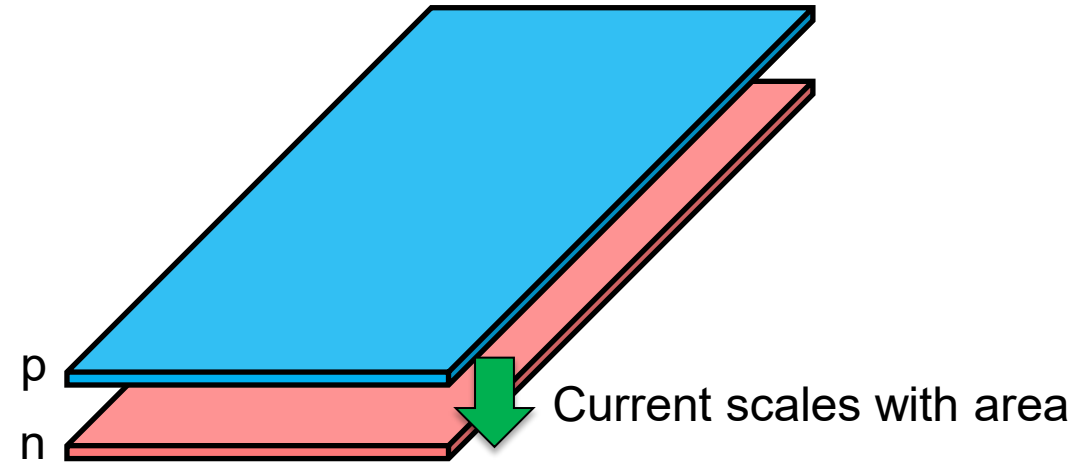
## Current TFET limitations:

- Energy efficiency of current TFETs is limited due to the intrinsically smooth implanted doping profiles
- Tunneling junction in current TFET is 1D, so that the current only **scales with width**, limiting its achievable current



Current scales with width

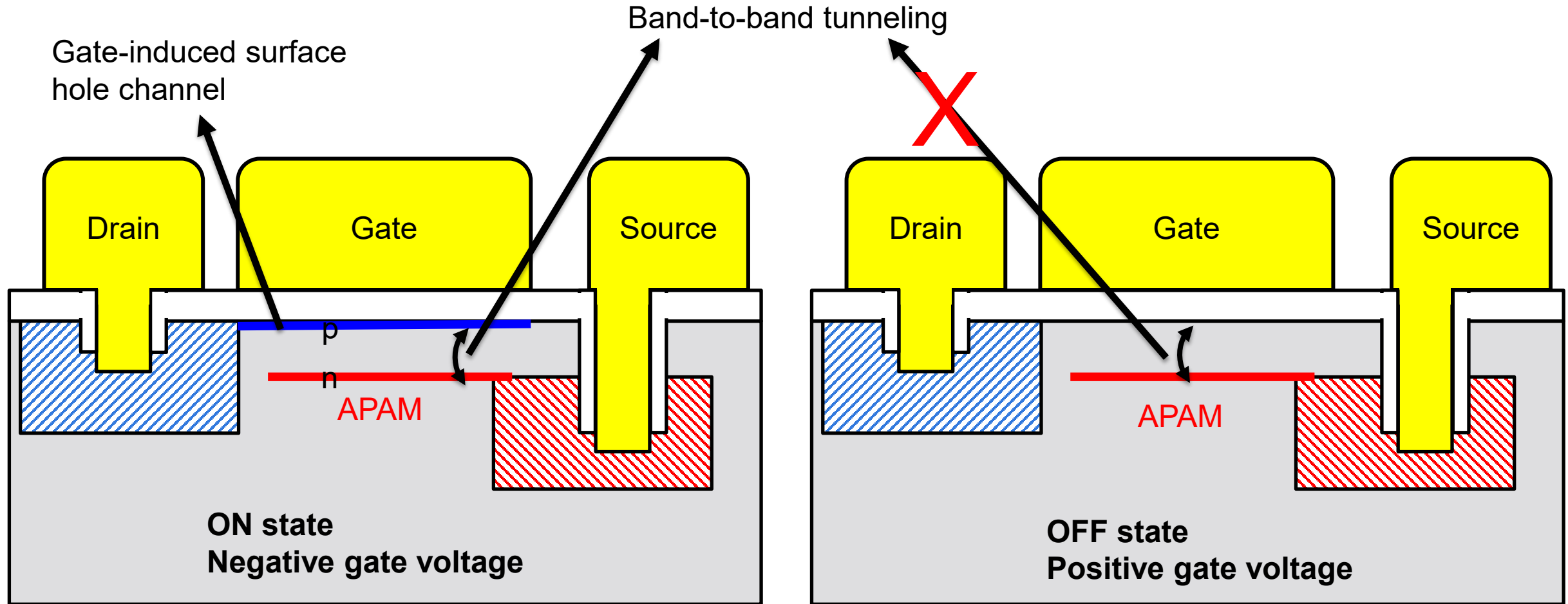
To increase current drive, we would like to accomplish 2D p-n junctions, where **current scales with area**:



Abruptness of doping profile is critical to achieve sharp turn-on for high energy efficiency.

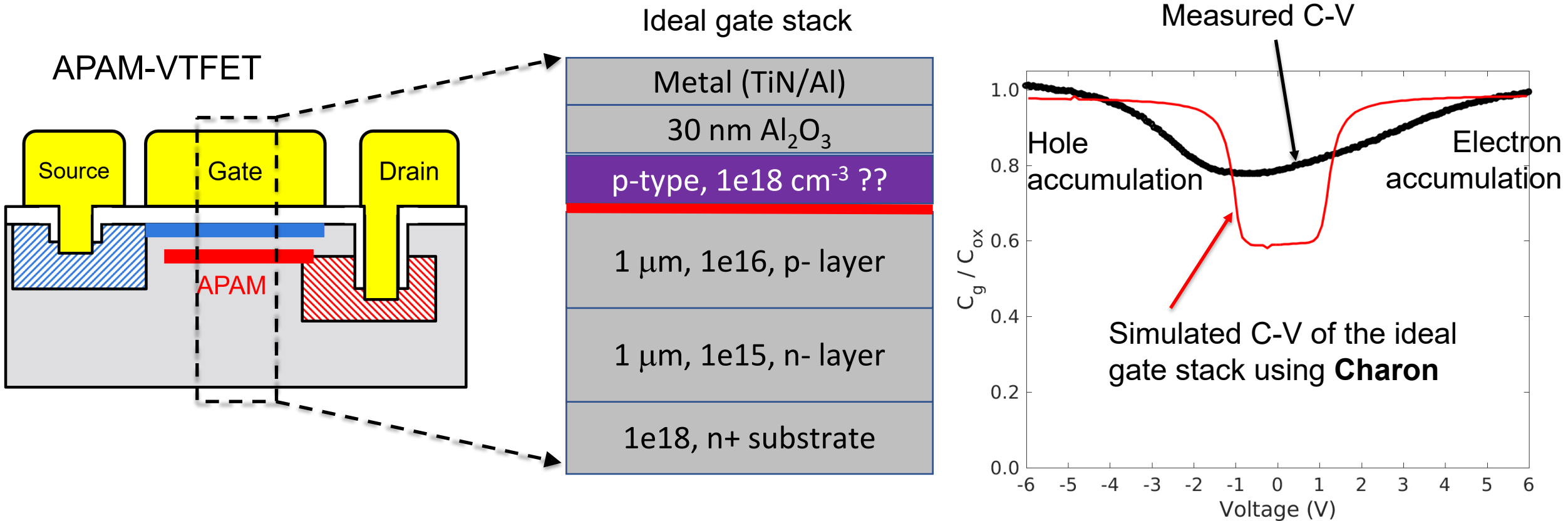
To create abrupt face-to-face p-n tunneling bilayers requires atomic precision fabrication.

# APAM-VTFET operation principles



- Atomic abruptness of APAM delta layer doping allows for high energy efficiency.
- Tunnel current scales with area, potentially large current.

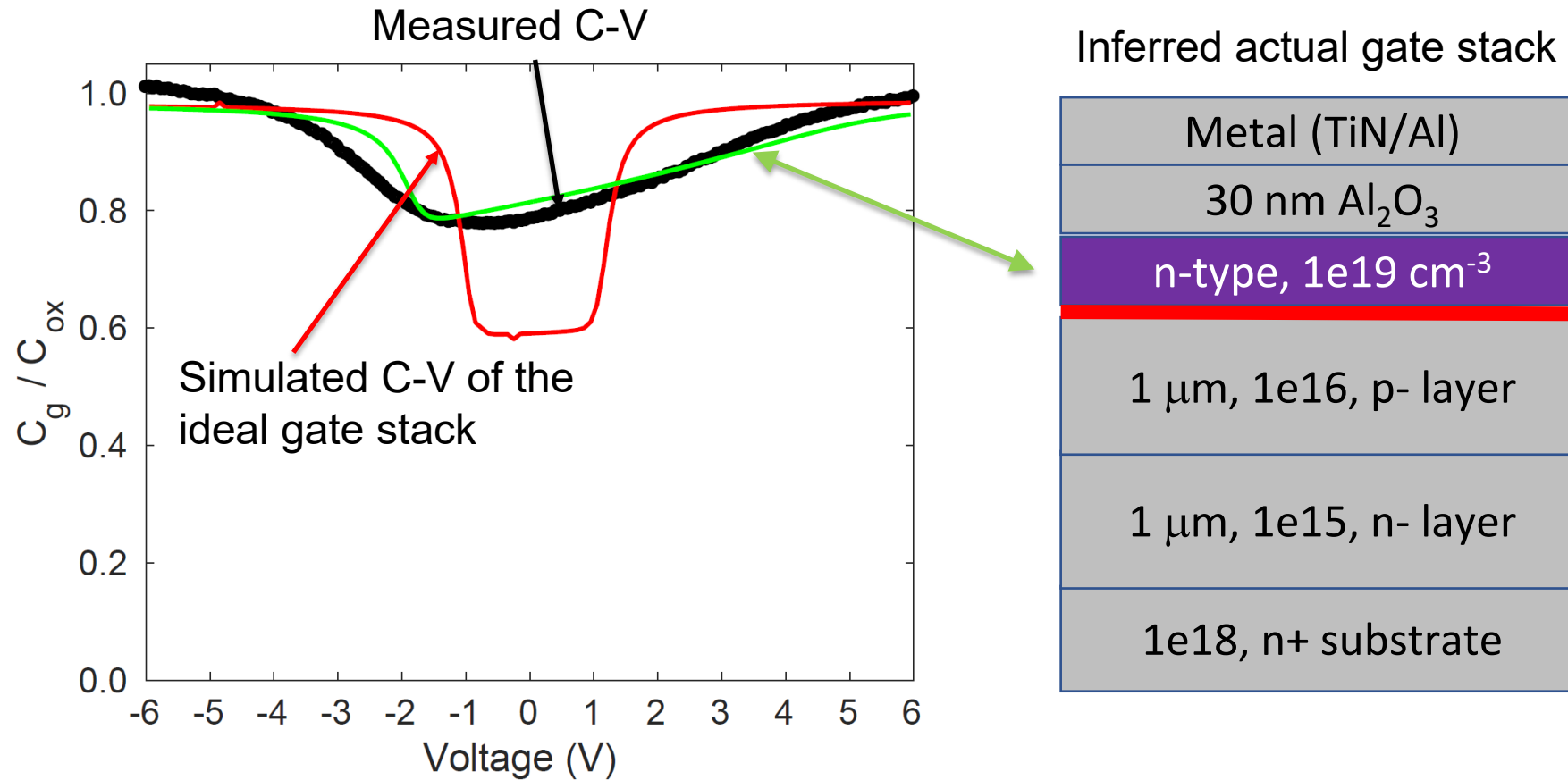
# Can we accumulate holes above APAM delta layer?



Accumulation of holes is demonstrated above the APAM layer in a gate stack.

Why is the simulated C-V assuming nominal p-type cap very different from the measured C-V?

# Simulation reveals dopant diffusion in gate stack

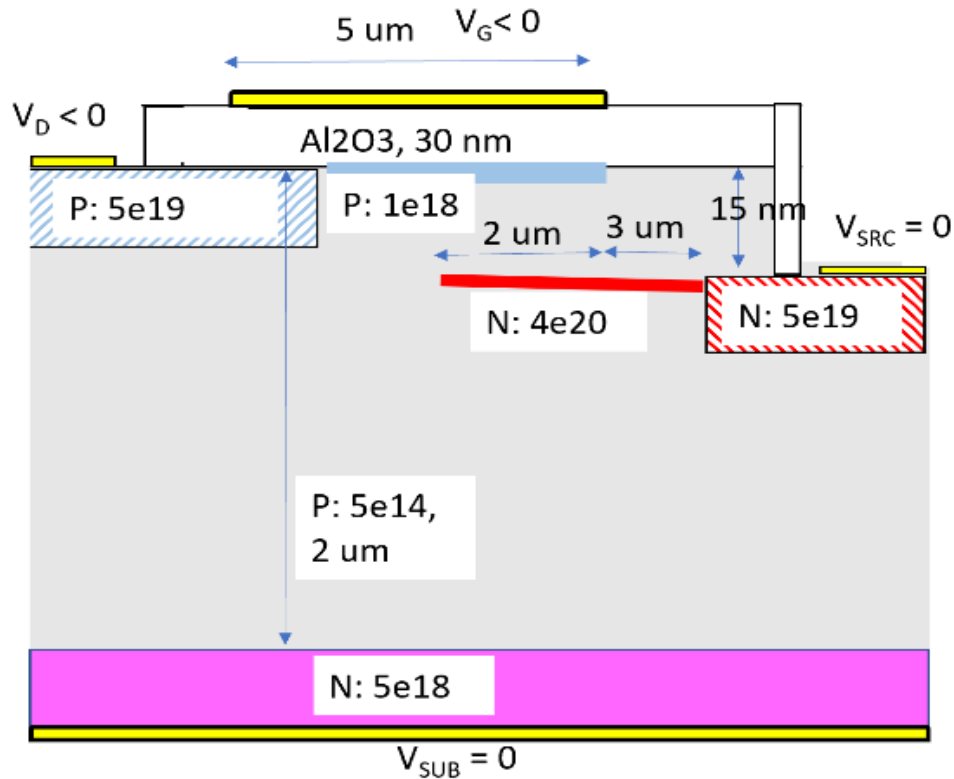


Simulation revealed **n-type cap** in the actual gate stack due to P diffusion at high temp., which was later confirmed by SIMS data.

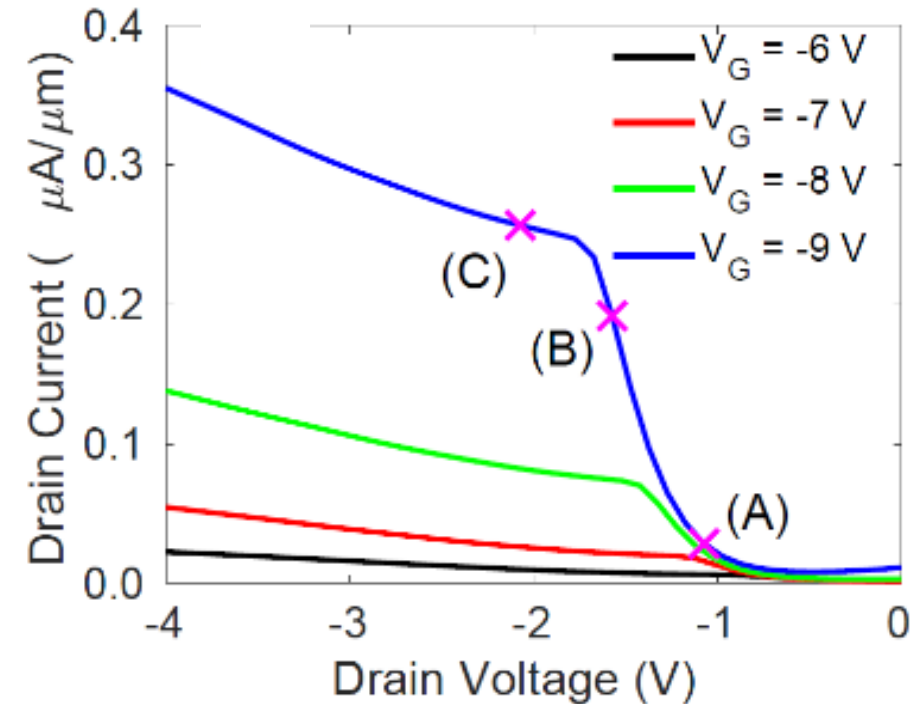
We have since found a way to suppress the P diffusion in our new samples.

# Will the proposed APAM-VTFET work?

Schematic of simulated device



Simulated  $I_D$ - $V_D$  curves (using **Charon**)

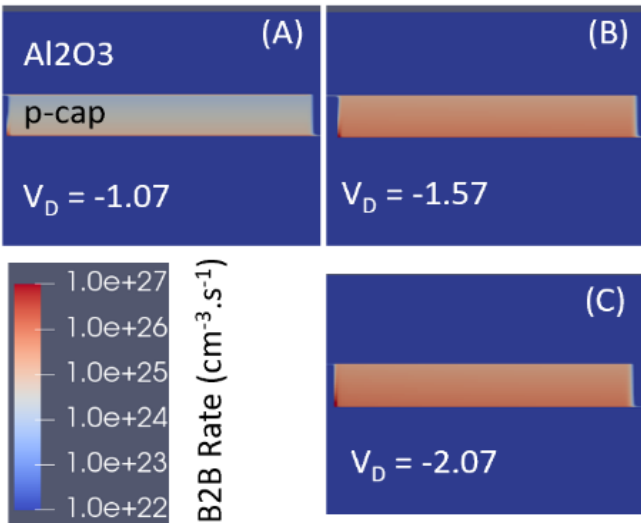
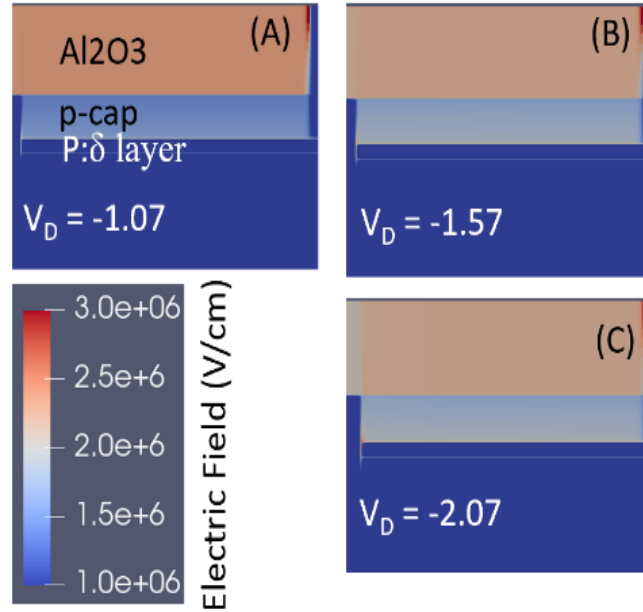


Relevant dimensions and doping values were chosen to maximize yield with our fabrication capability, as opposed to device performance.

Simulated  $I_D$ - $V_D$  curves indeed show transistor-like response, but device geometry needs optimization for better performance.

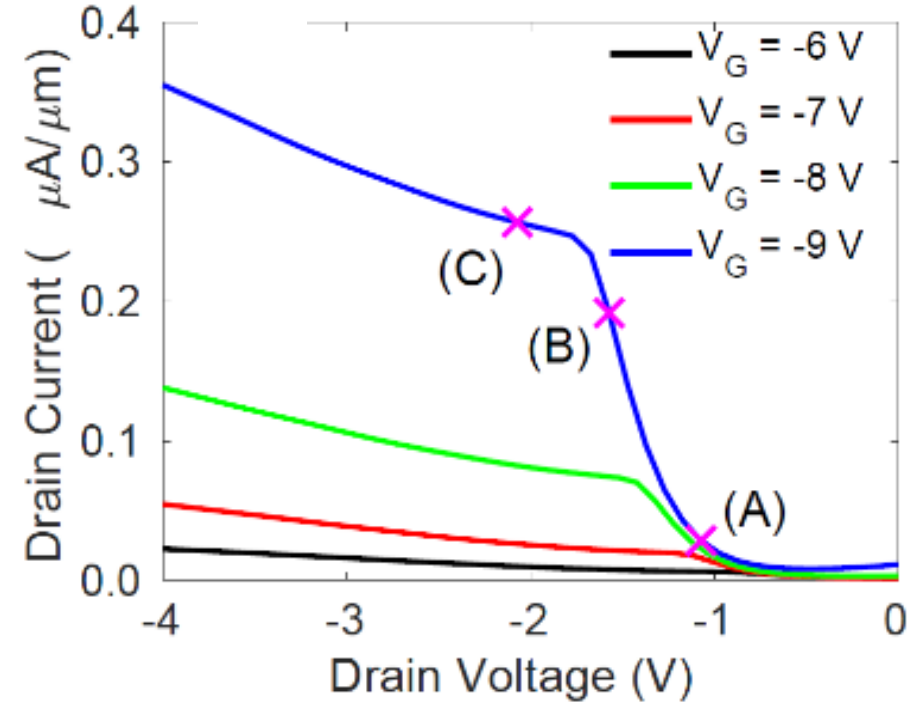
# Why are there two different slopes in the $I_D$ - $V_D$ curves?

Electric field is clearly increased from point (A) to (B), but shows little change from (B) to (C).



Band-to-band (B2B) rate follows the same pattern as the field. The B2B tunneling determines the drain current.

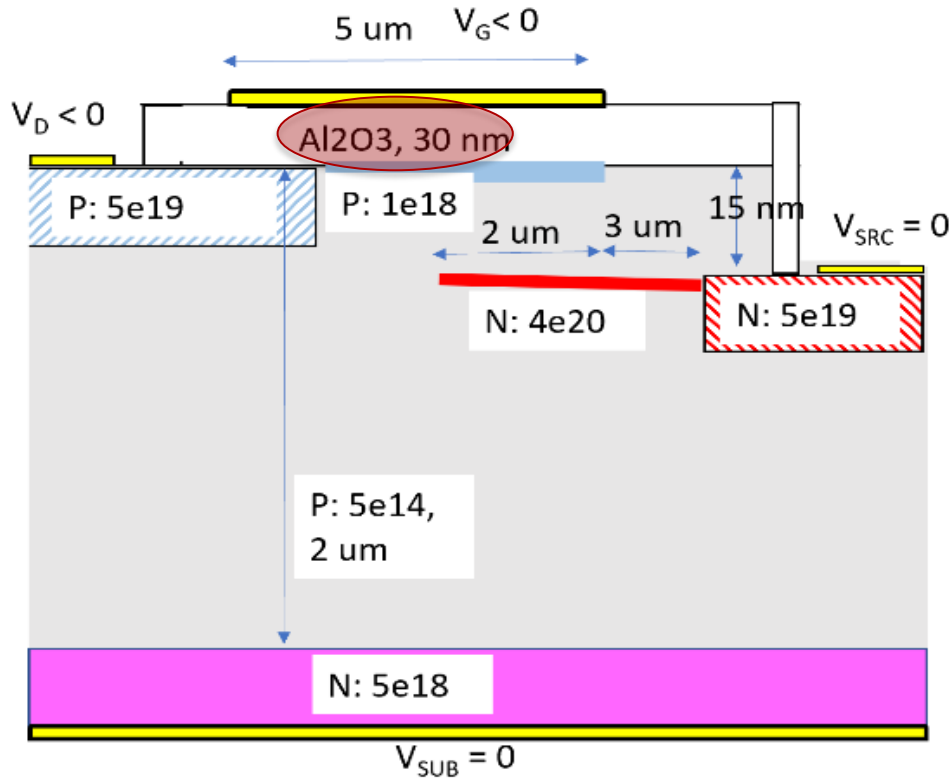
Simulated  $I_D$ - $V_D$  curves



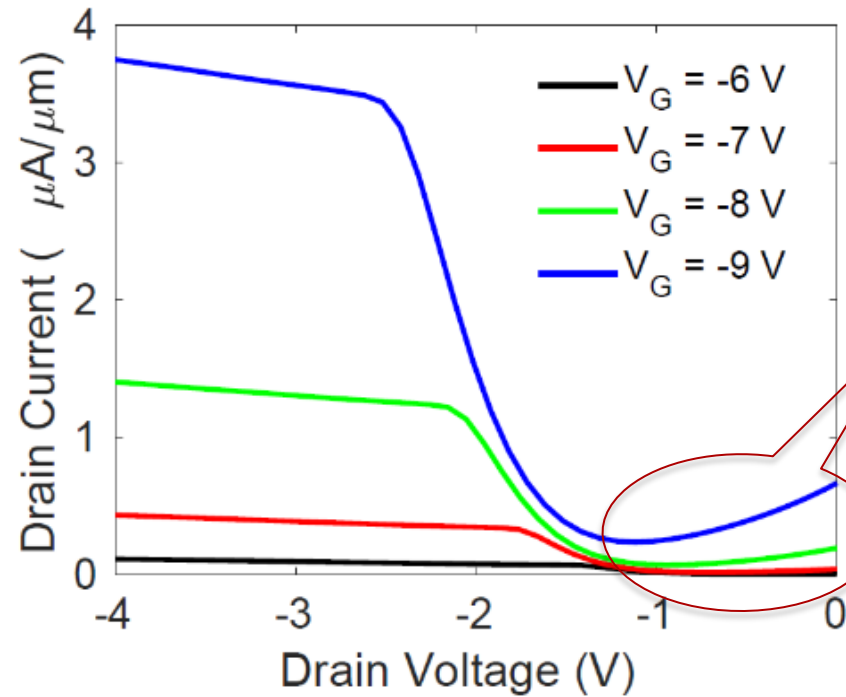
The electric field in the cap layer shows nonlinear change with drain voltage, leading to different slopes in the  $I_D$ - $V_D$  curves.

# How can we increase drain current?

Reduce gate oxide from 30 nm to 20 nm



Simulated  $I_D$ - $V_D$  curves



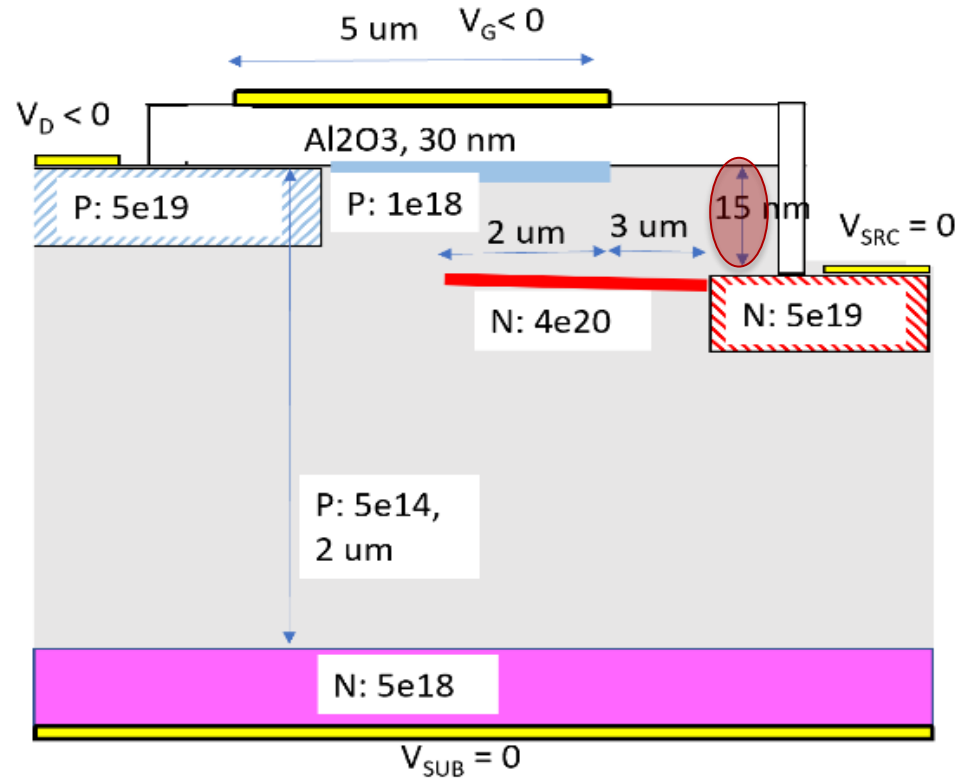
Non-zero currents at low voltages are due to the limitation in the B2B model. Need further study.

$$G_{bbt} = A|F|^\gamma e^{-B/|F|}$$

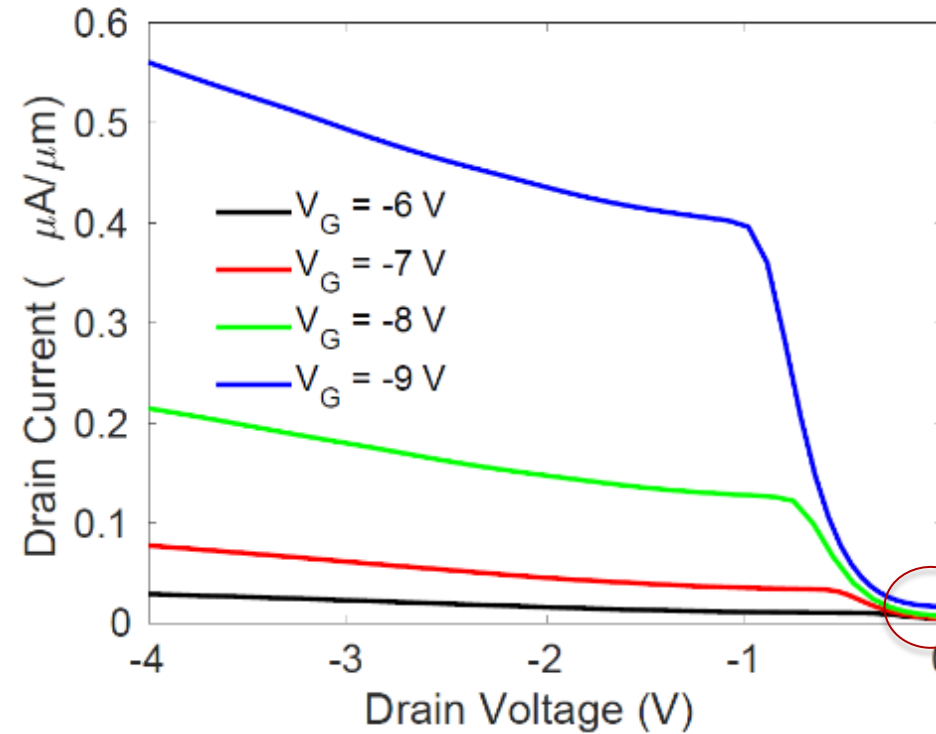
Reducing oxide thickness can significantly increase the drain current.

# How can we decrease drain turn-on voltage?

Reduce the p-type cap thickness from 15 nm to 10 nm



Simulated  $I_D$ - $V_D$  curves



Non-zero currents at low voltages are due to the limitation in the B2B model. Need further study.

$$G_{bbt} = A|F|^\gamma e^{-B/|F|}$$

Reducing cap layer thickness does not increase the drain current, but decreases drain turn-on voltage.

# Summary

- ✓ Demonstrated good gate control in APAM gate stack via experiment and simulation, an essential component of the proposed APAM-VTFET.
- ✓ Simulated current-voltage curves of APAM-VTFET showed transistor-like behavior that can be improved via geometry & doping optimization.
- ✓ More TCAD simulations will be performed to optimize geometry & doping to guide device design (APAM-VTFET prototype is in progress).

