SAND2021-4611C

Sandia National Laboratories

Atomic precision advanced manufacturing (APAM) of ultra-doped nanostructures for advanced CMOS devices and interconnects

David Scrymgeour, Esther Frederick, Connor Halsey, DeAnna Campbell, Evan Anderson, Scott Schmucker, Jeff Ivie, Andrew Leenheer, Suzey Gao, Tzu-Ming Lu, Lisa Tracy, Shashank Misra

Presented by: David Scrymgeour

April 23rd, 2021

Talk EL08.02.02
EL08: Next-Generation Interconnects—Materials, Processes and Integration

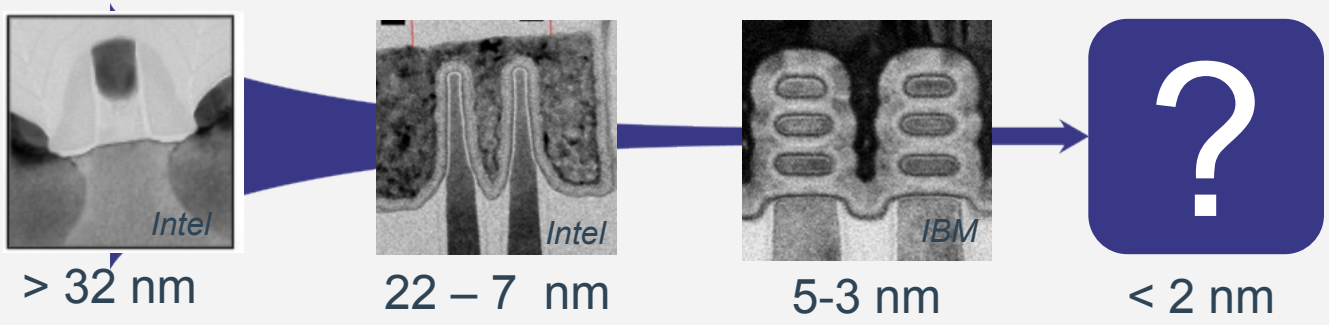
U.S. DEPARTMENT OF ENERGY NNSA National Nuclear Security Administration

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia LLC, a wholly owned subsidiary of Honeywell International Inc. for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. SAND2020-12611 C

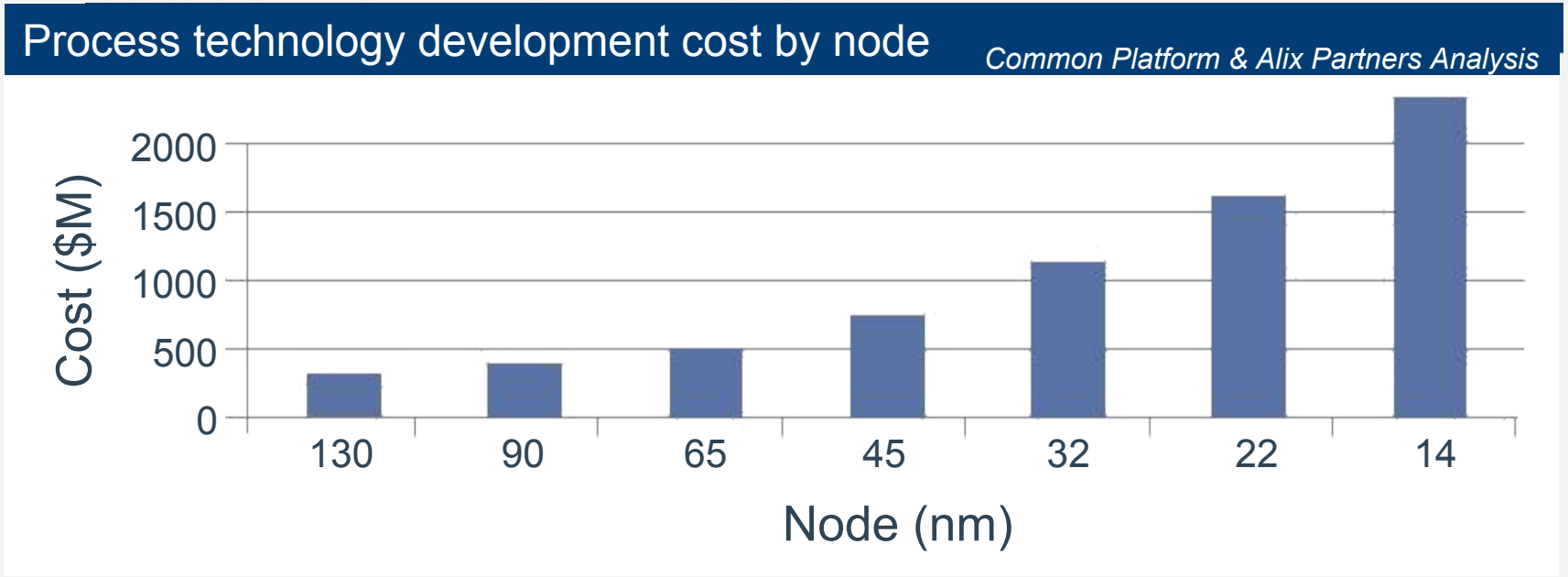
Sandia National Laboratories

Challenges in modern CMOS require path finding science!

Historically, shrink transistor → more functionality and declining cost



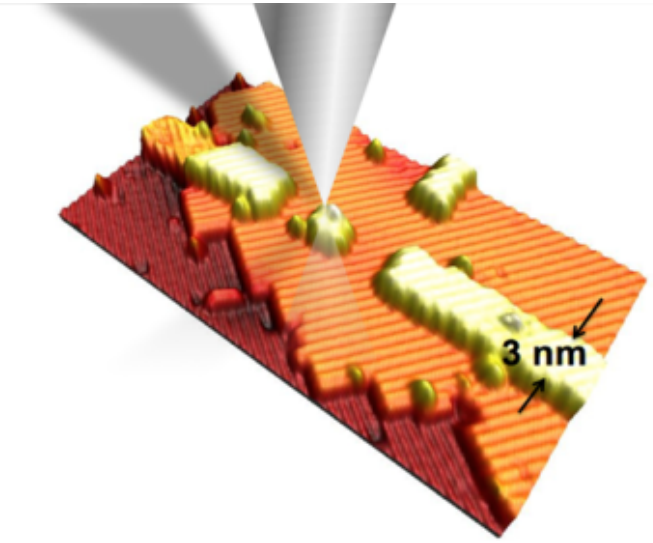
R&D costs rising exponentially → Unclear path forward

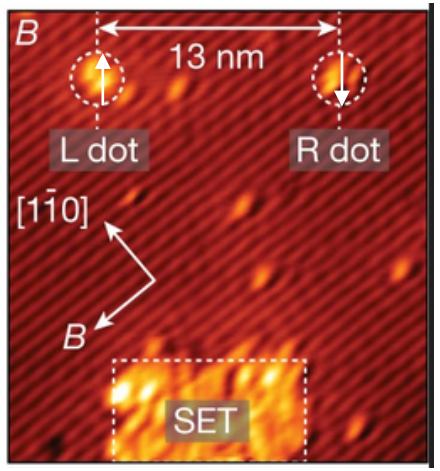


Atomic Precision Advanced Manufacturing (APAM)

Our mission: To assess the opportunities presented by APAM-enabled devices and processing for the digital microelectronics of the future

APAM for Quantum

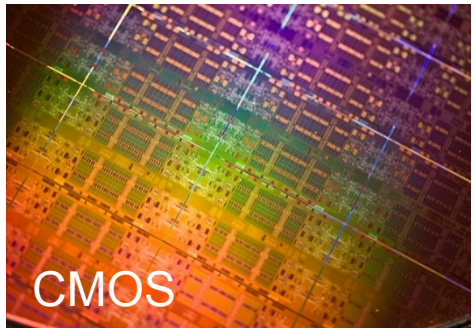


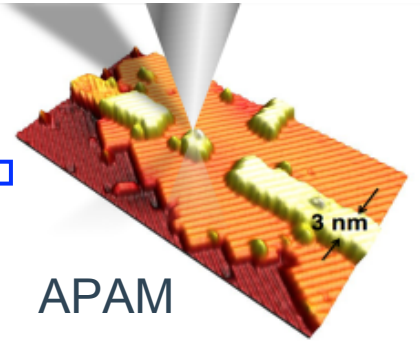


He, Nature (2019)
2-qubit device

- Place phosphorus atoms in silicon with near-single-site precision
- Problem space - manipulate spin degrees of freedom (qubits)

APAM for Digital Electronics





APAM

Science & engineering challenges:

Fabrication temperature too high! (>1200°C)

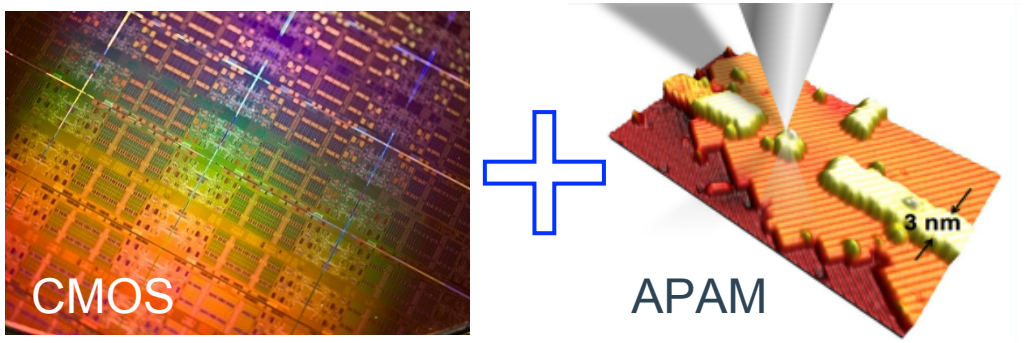
Operational temperatures too low! (4k)

Not yet manufacturable at wafer scale

Atomic Precision Advanced Manufacturing (APAM)

Our mission: To assess the opportunities presented by APAM-enabled devices and processing for the digital microelectronics of the future

APAM for Digital Electronics



Science & engineering challenges:

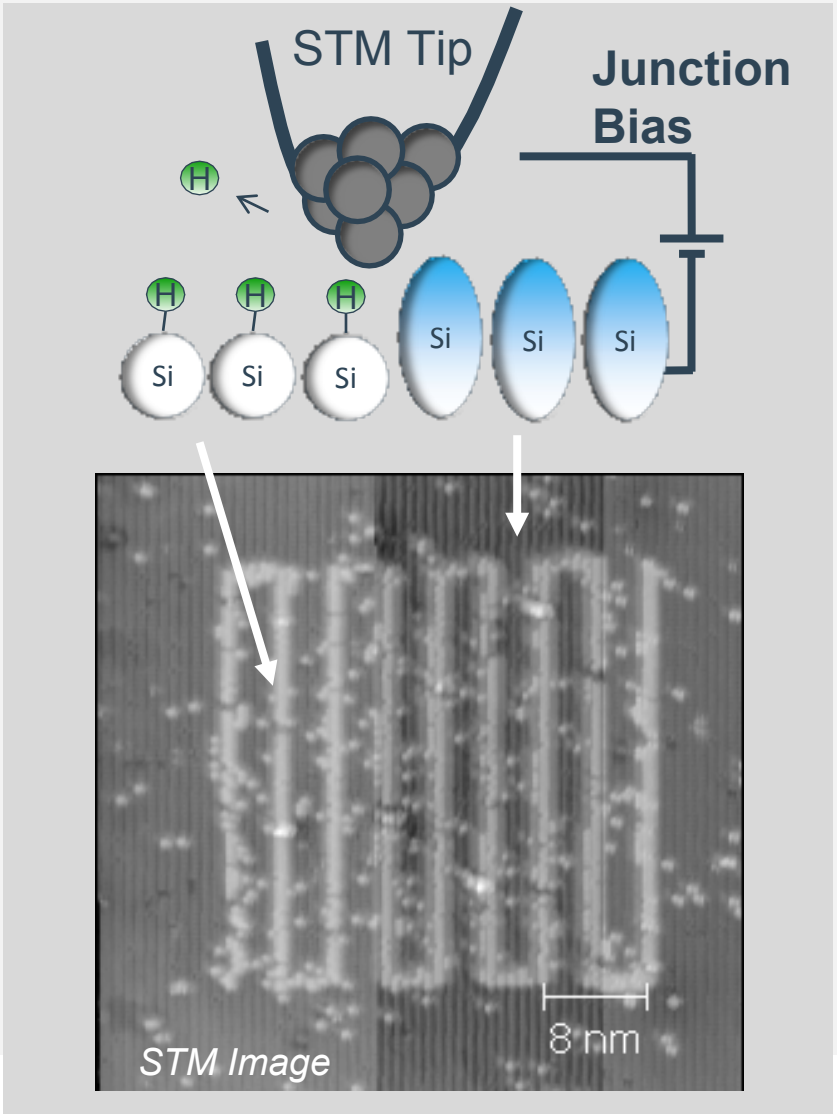
Fabrication temperature too high! (>1200°C)

Operational temperatures too low! (4k)

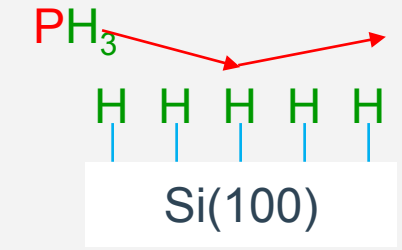
Not yet manufacturable at wafer scale

1. Inserting APAM into CMOS
2. Room temperature operation
3. Robust at operating conditions
4. Manufacturability

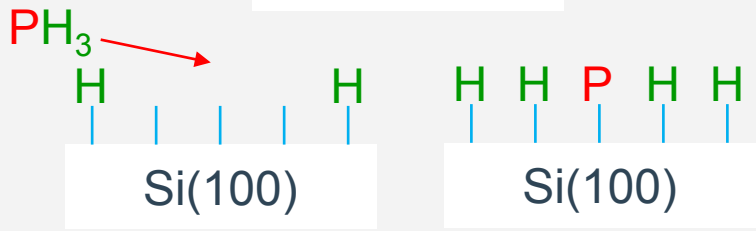
APAM leverages chemical contrast at surface for ultra-doping silicon



Unreactive H termination

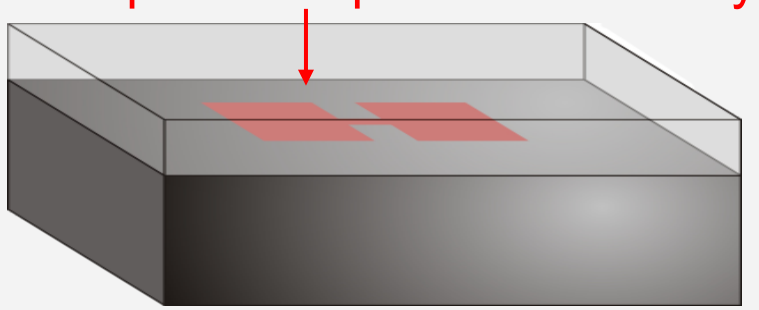


Reactive bare silicon



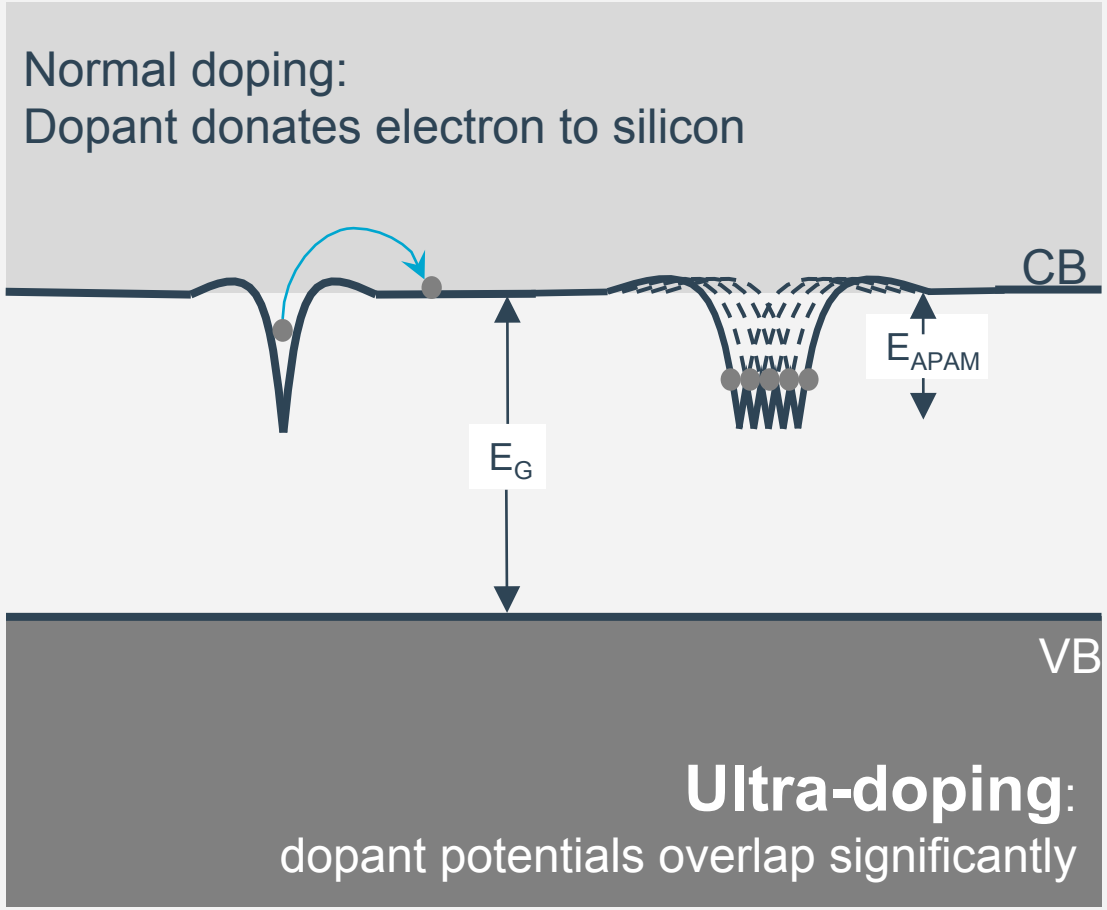
React with phosphine & cap with epitaxial Si

Ultra-doped Phosphorous delta layer

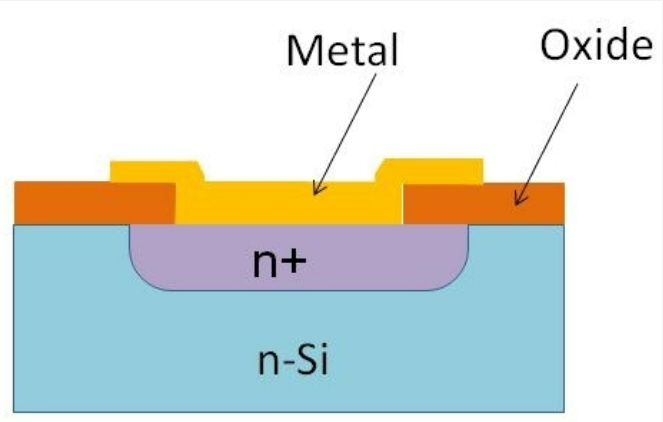


- Atomically abrupt in X, Y, and Z
- Highly conductive (~10^{21} cm^{-3})

APAM ultra-doping has intriguing electrical properties



Significant lever for modifying electronic structure

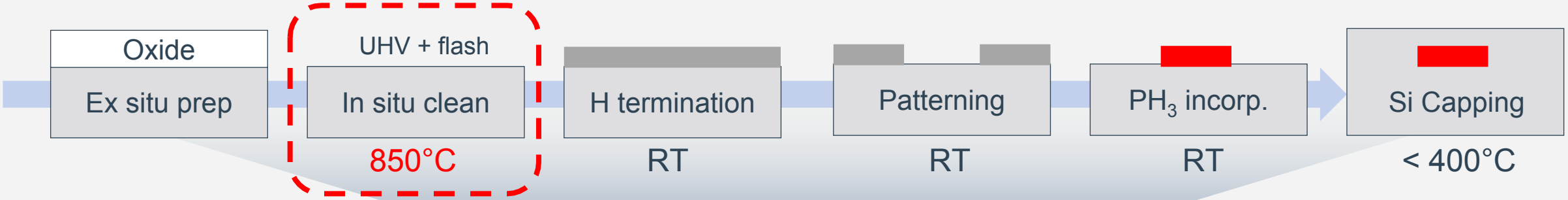


Schottky contact

Change the electronic structure of silicon fundamentally → opens door to new applications

Challenge 1: APAM + CMOS fabrication

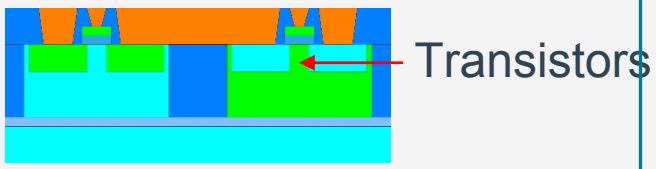
APAM Fabrication:



Split Fab CMOS + APAM:

FEOL Fabrication

Temps >850°C



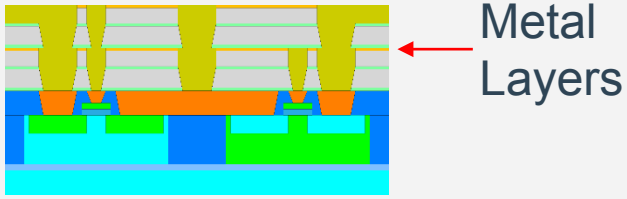
APAM Integration Step

Get to Si and make it clean!

What temp?

BEOL Fabrication

Max temp 450°C



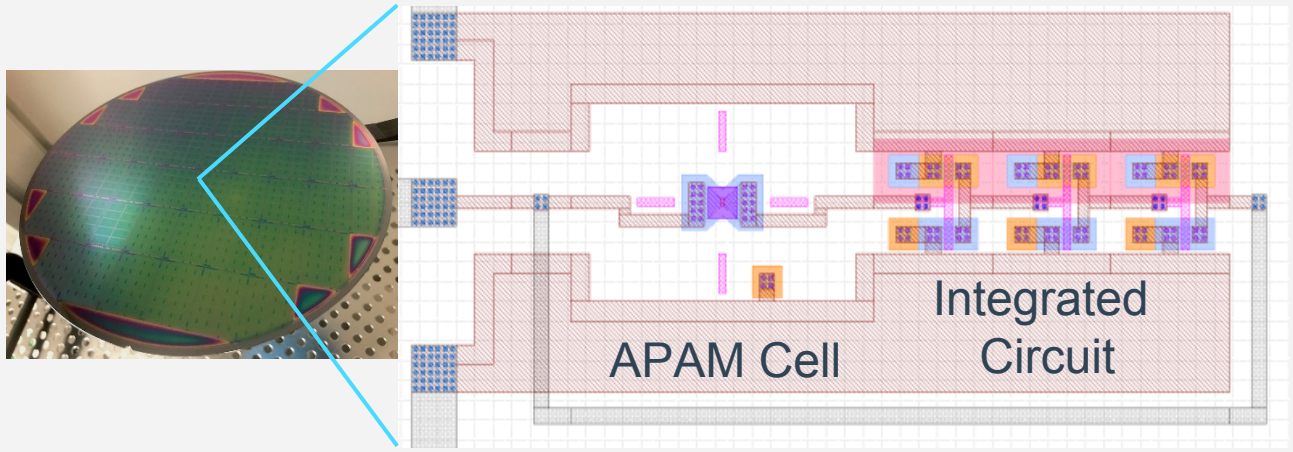
Need a new APAM surface prep!

D. R. Ward et al, "Atomic precision advanced manufacturing for digital electronics," EDFAAO, 22, 1, 4-10 (2020)

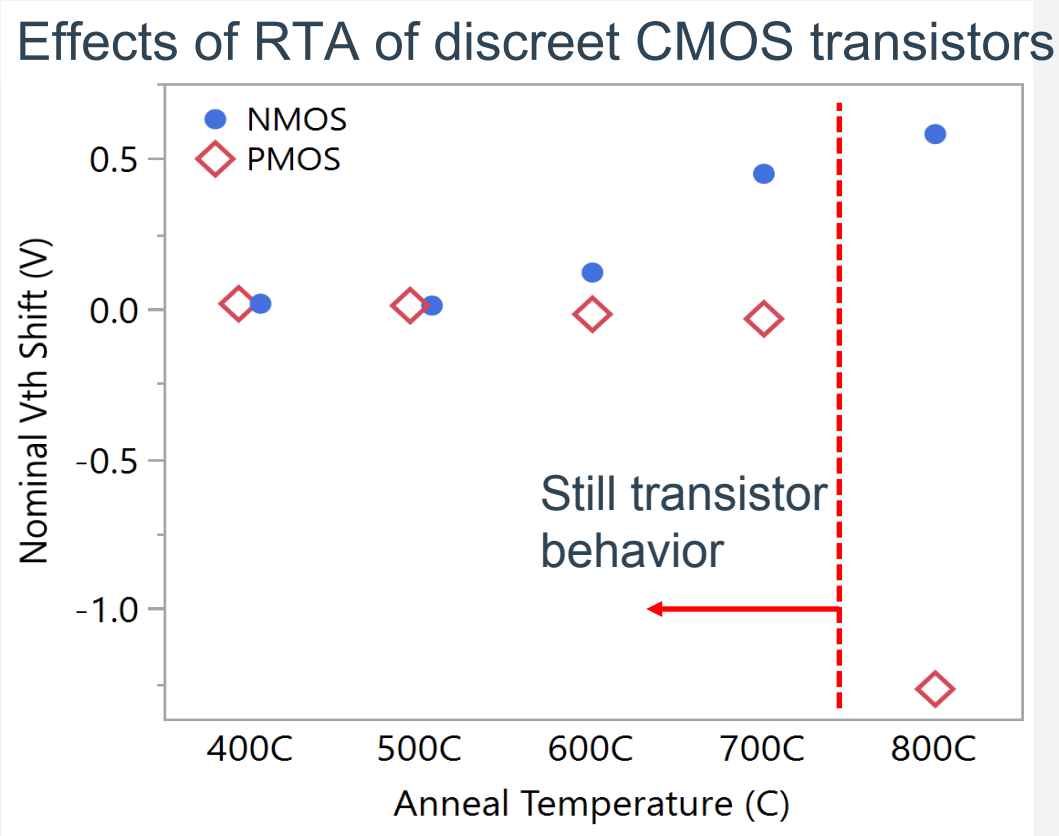
What parameters leave APAM intact?

Split fab CMOS + APAM test platform

- Wafer pulled after FEOL - transistors and W plugs
- Doing RTA thermal testing & STM processing
- Then into BEOL for metallization & testing



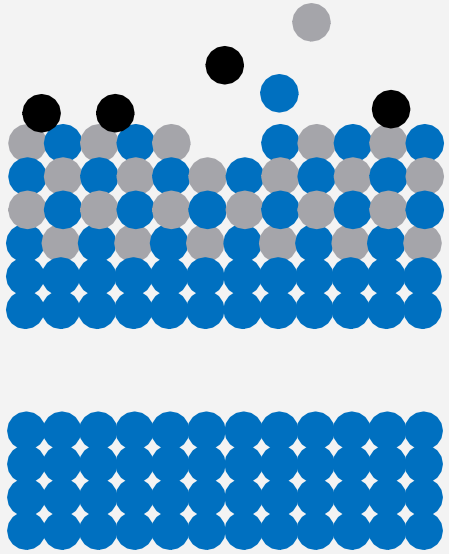
We have a thermal budget of 700°C



Nominal threshold voltage shift seen in NFET and PFET devices with respect to RTA temperature.

Can we prep APAM <700°C?

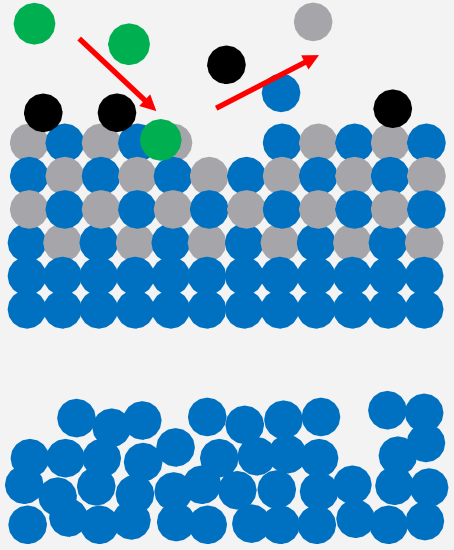
Current state of the art:
>850°C evaporation



Clean, Crystalline

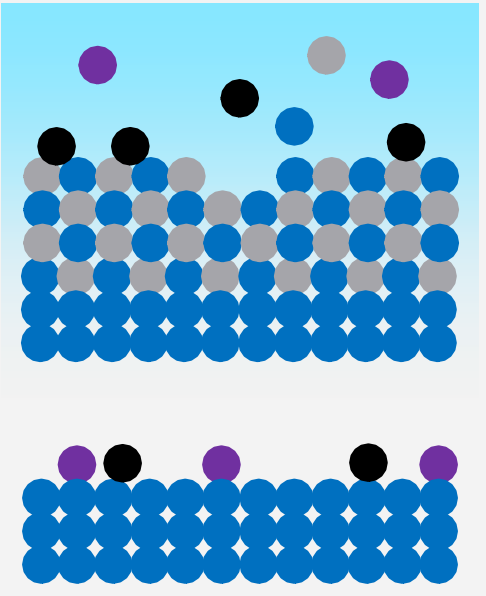
Does not work
<850°C

RT UHV Ne sputter



Clean,
Amorphous

RT Vapor HF Etch



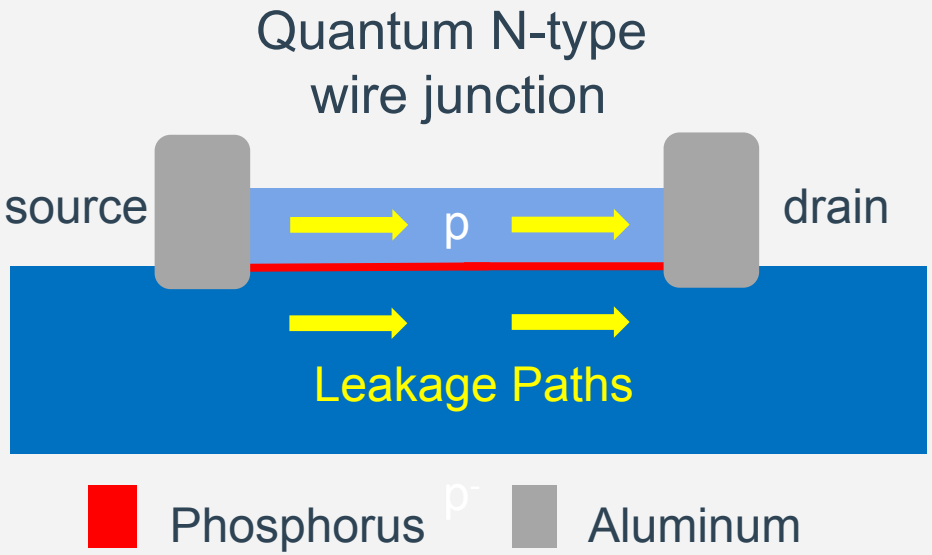
Dirty, Crystalline

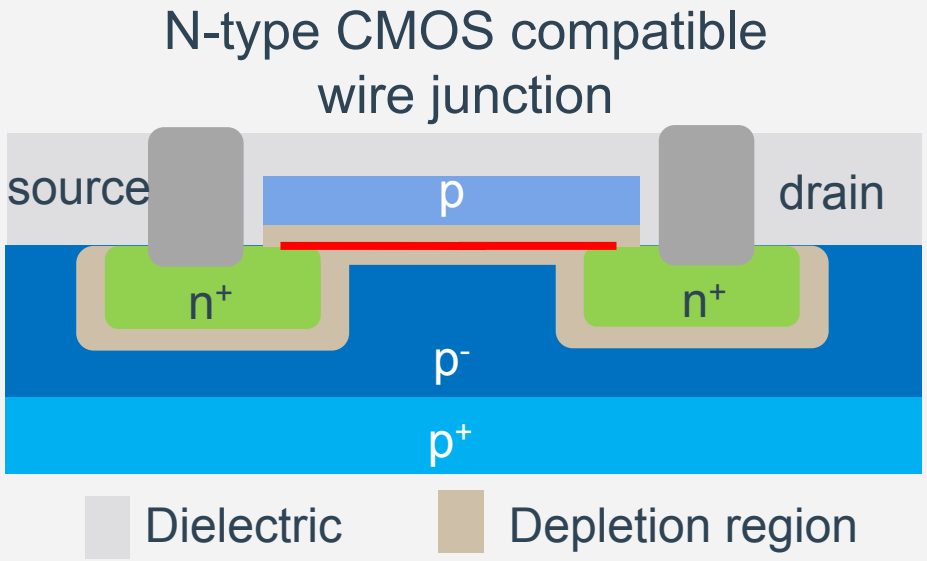
Si
O
C
X
Ne

- Multiple viable routes for low temp clean silicon
- Both processes result in minimal surface amorphization

Have a process that works – next up full integration

Challenge 2: RT Operation



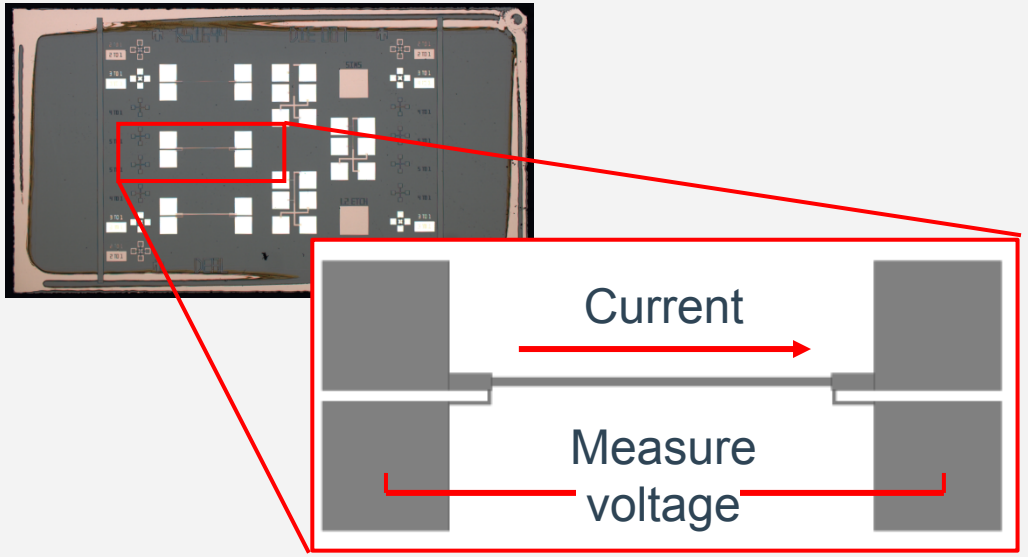


Measurement	Density (cm^{-2})	Resistivity (W/sq.)	Mobility (cm^2/Vs)
4 K Hall Bar	9×10^{13}	570	120
RT Hall Bar	8.1×10^{13}	1,070	72

Successful room temperature APAM operation using doping

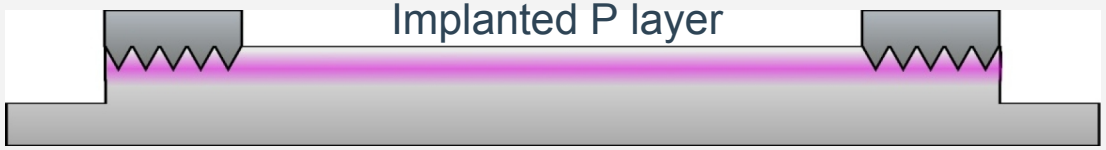
Challenge 3: Robustness with operational CMOS

- New materials (delta layer)
- New interfaces (delta layer, implant, metal)
- Accelerated lifetime testing

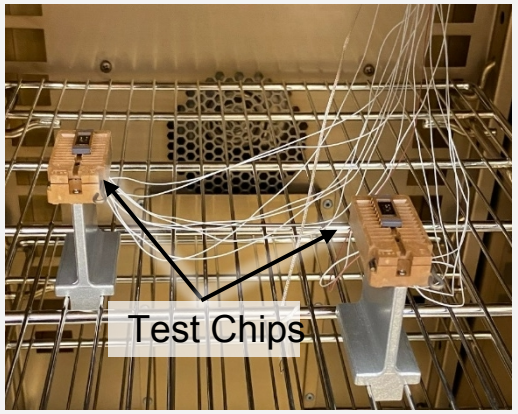


Implanted phosphorous mock delta layers:

Cross section:

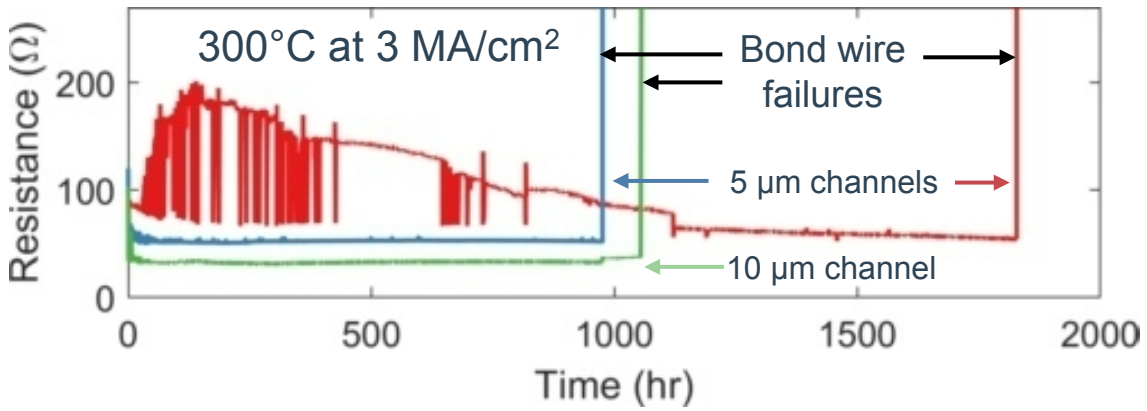


APAM delta layer devices:



Delta layers survive at high current & temperature

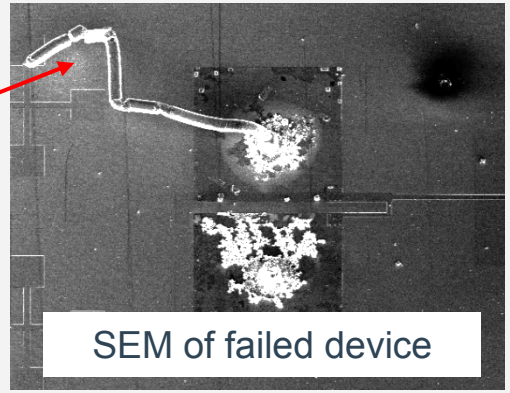
3 testers with different channel widths



Conclusions :

- Implanted & delta layer samples survived >70 days at 300°C at 3 MA/cm²
- Delta layers still conducting after aging study

Failures in bond wires due to electromigration



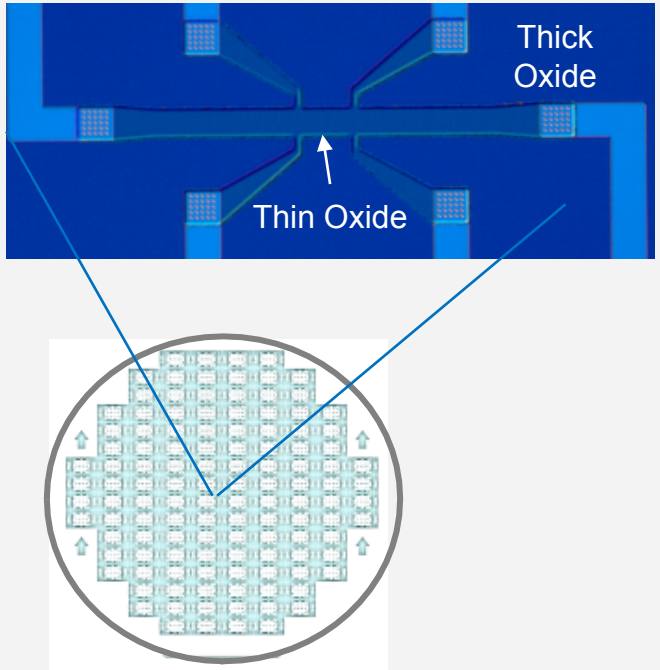
Ongoing & future work :

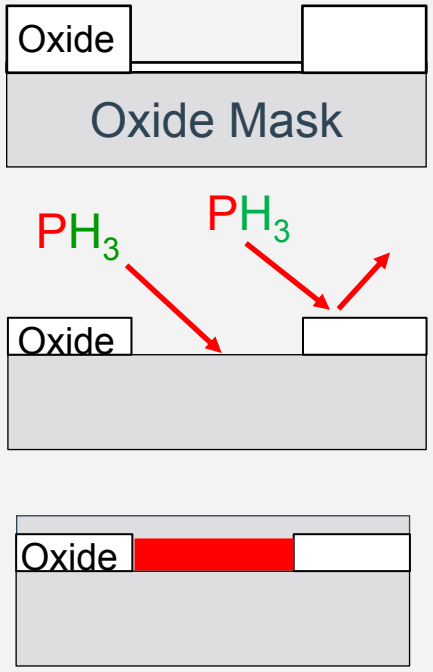
- RT Hall bar samples in oven now
- Accelerated tests on APAM + CMOS devices

Failures occur outside doped delta layer

Challenge 4: Manufacturability

Wafer Level Atomic Layer Doping





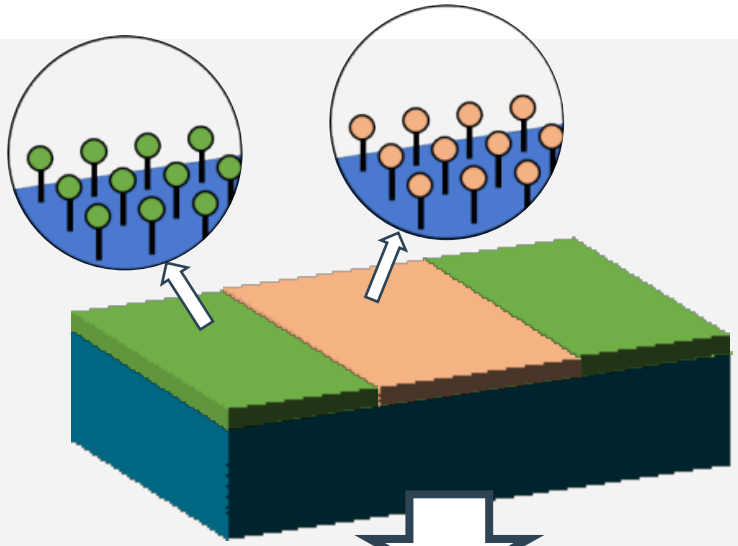
- Wafer-scale lithography defines hard mask
- Etch resolution → APAM resolution
- APAM electrical properties good

APAM-like processing in a fab tool

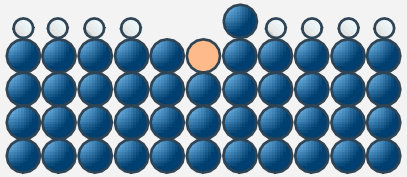
- Applied Materials & contact resistance
- Demo relevant structures

Atomic Resists: selective doping and deposition

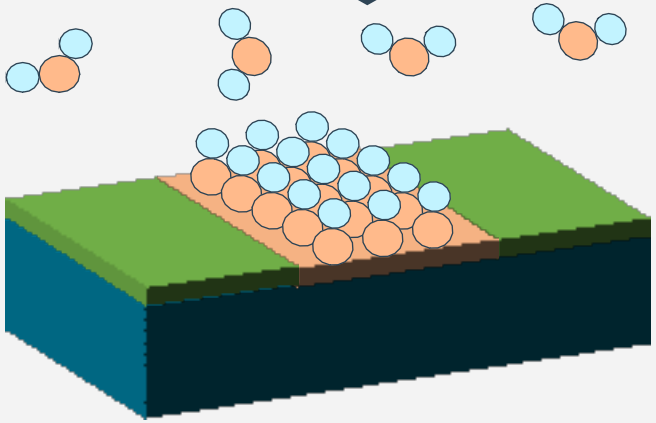
Atomic Resists



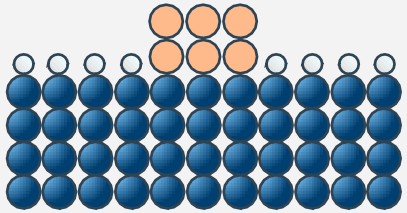
Patterned Incorporation/Doping



Selective Chemistry



Patterned Deposition

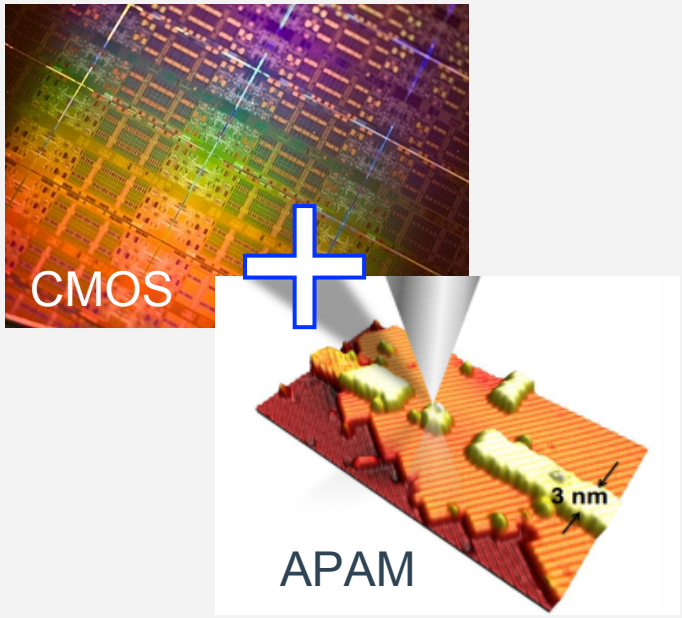


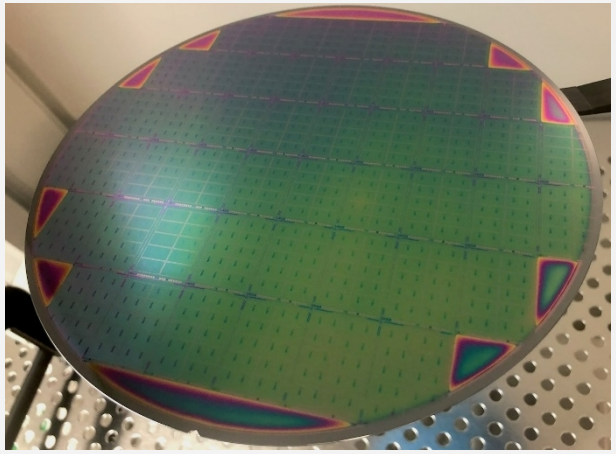
Potential new fabrication toolset!

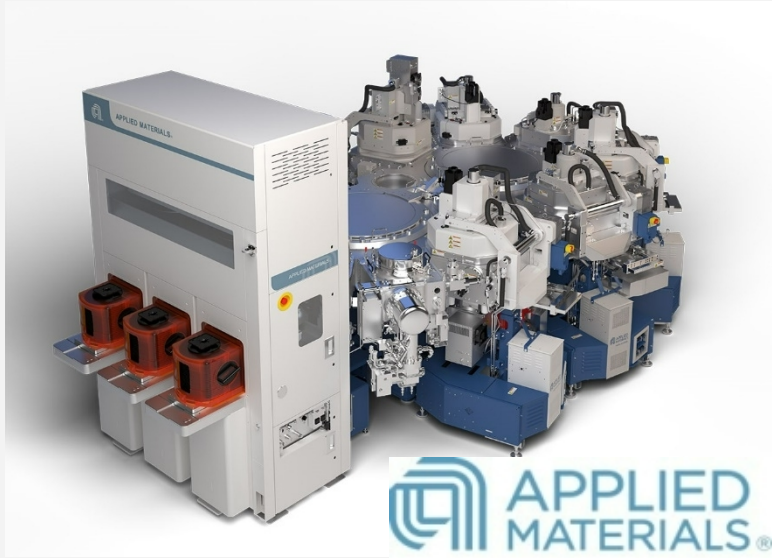
Conclusions

- Compatible APAM + CMOS manufacturability
- Room temperature and above operation of APAM devices
- Toward manufacturability at wafer scale

We are interested in creating ways to explore new transistor concepts in silicon with atomic-scale control…







… and establishing a proof-of-principle of how to manufacture them.