# Sandia National Laboratories and University of New Mexico
# Final Scientific/Technical Report
# High Voltage Regrown GaN P-N Diodes Enabled by Defect and Doping Control
# 16/CJ000/10/04

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| **Award:** | 16/CJ000/10/04 |
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| **Lead Recipient:** | Sandia National Laboratories |
| **Project Team Members** | University of New Mexico |
| **Project Title:** | High Voltage Regrown GaN P-N Diodes Enabled by Defect and Doping Control |
| **Program Director:** | Dr. Isik Kizilyalli |
| **Principal Investigator:** | Dr. Andrew Armstrong |
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## Public Executive Summary

This project studied and implemented methods to form GaN p-n diodes using selective area regrowth to achieve selective area doping. Successful selective area doping of GaN p-n diodes is an enabling factor to realize more advanced devices such as vertical transistors. The general challenge to selective area regrowth of GaN is that the primary etch method, inductively coupled plasma (ICP), damages the crystal and causes high leakage when didoes are formed by regrowth on the etched surface. Our approach used low damage etch methods following ICP etch to remove crystal damage and reduced leakage in the regrown diode. This project demonstrated 1.6 kV etched-and-regrown GaN p-n diodes using planar (non-selective) regrowth and 840 V etched-and-regrown p-n diodes using selective area regrown. Enabling factors were use of a low-damage reactive ion etch (RIE) to remove damage caused by the primary ICP etch combined with a multi-step junction terminal extension (JTE) process. Deep level defect investigation quantitatively correlated a deep level near the middle of the GaN band gap with ICP etch-induced leakage that was greatly mitigated by using a slow, low damage RIE process. This research is economically feasible for commercialization because the processes used in this project, including substrate type and source, epitaxial crystal growth and fabrication techniques are all standard to the GaN semiconductor industry. The fundamental understanding and foundational ability to produce kV-class GaN p-n diodes through etch-and-regrowth provides a path to realize high power, high efficiency GaN power switches that can significantly outperform commercial devices for next-generation electrical power conversion and transmission systems.

## Accomplishments and Objectives

This award allowed Sandia National Laboratories and the University of New Mexico to demonstrate key objectives. The focus of the project was on building a high voltage, etched-and-regrown GaN p-n diode.

Milestones were laid out in Attachment 3, the Technical Milestones and Deliverables, at the beginning of the project. The actual performance against the stated milestones is summarized here:

**Table 1. Key Milestones and Deliverables.**

| Tasks | Milestones and Deliverables |
|---|---|
| **Task 1: Control c-plane regrowth defects and impurities**<br>1.1 Understand and control Si contamination for c-plane regrowth<br>1.2 Understand and control etch-induced defects for c-plane regrowth | Remove Si spike from regrowth interface.<br>**Actual Performance:** (12/2017) Systematic removal of interfacial Si was not demonstrated, however, it was demonstrated that best practices could achieve peak Si concentration below $3\times10^{17}$ $cm^{-3}$ in the best case.<br><br>Understand Si spike influence on regrown diode leakage.<br>**Actual Performance:** (3/2018) Demonstrated that peak Si concentration < $3\times10^{17}$ $cm^{-3}$ in regrown diodes does not degrade electrical performance and Si interfacial concentration as high as $8\times10^{11}$ $cm^{-2}$ is innocuous regarding electrical performance in continuously-grown diodes.<br><br>Controllably mitigate etch-induced defects at regrowth interface.<br>**Actual Performance:** (3/2018) Observed inductively coupled plasma etch-enhanced deep level defect 1.9 eV below the conduction band and reduced concentration of this deep level from $1.8\times10^{15}$ $cm^{-3}$ to $5.0\times10^{14}$ $cm^{-3}$ using post-etch KOH-based chemical treatment.<br><br>Quantify impact of etch-induced defects on regrown junction leakage.<br>**Actual Performance:** (3/2018) Demonstrated reduction in reverse leakage from $3\times10^{-4}$ $A/cm^2$ to $6\times10^{-7}$ $A/cm^2$ at -100 V for etched-and-regrown diodes using KOH-based post-etch chemical treatment. |

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| **Task 2: Demonstrate c-plane etched-and-regrown diode**<br><br>2.1 Diode fabrication and test<br><br>2.2 Understand defect impact on regrown diode performance | Demonstrate 600 V planar etched and regrown diodes.<br>**Actual Performance:** (9/2018) Achieved planar etched-and-regrown diodes with 1 nA reverse leakage ($6\times10^{-6}$ A/cm$^2$) at 1.2 kV and breakdown at 1.6 kV using low damage reactive ion etch.<br><br>Q2: Correlate interface defects and breakdown voltage.<br>**Actual Performance:** (9/2018) Further reduced concentration of the 1.9 eV deep level correlated with reversed leakage to $1.0\times10^{14}$ cm$^{-3}$ using low damage reactive ion etch. |
| **Task 3: Control non-polar regrowth defects and impurities**<br><br>3.1 Understand and control Si and O contamination for non-polar regrowth<br><br>3.2 Understand and control etch-induced defects for non-polar regrowth | Control incorporation of impurities in non-polar regrowth.<br>**Actual Performance:** (12/2017) Systematic reduction in C, O and Si impurities was not demonstrated, however, best practices could achieve Si, O, and C peak concentrations < $10^{17}$ cm$^{-3}$ in the best case.<br><br>Quantify impact of non-polar impurities on regrown junction.<br>**Actual Performance:** (3/2018). Regrown m-plane diodes with simple mesa isolation achieved 500 V blocking voltage compared to 450 V for continuously-grown diodes, demonstrating that interfacial impurities are not debilitating for non-polar regrowth.<br><br>Controllably mitigate etch-induced defects at regrowth interface.<br>**Actual Performance:** (6/2018) KOH-based treatment reduced the etch-enhanced 1.9 eV deep level from $10^{15}$ cm$^{-3}$ to $10^{14}$ cm$^{-3}$ in etched-and-regrown m-plane diodes. Photoelectrochemical etching (KOH+UV light) reduced the interfacial concentration of the 1.9 eV deep level at the regrown junction by an additional 10x relative to KOH treatment without UV light.<br><br>Quantify impact of etch-induced defects on regrown junction leakage.<br>**Actual Performance:** (9/2018) KOH treatment of etched-and-regrown diodes reduced reverse leakage at -10 V from $3\times10^{-2}$ A/cm$^2$ to $1\times10^{-3}$ A/cm$^2$, and KOH+UV light further reduced reverse leakage to $3\times10^{-4}$ A/cm$^2$. |

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| **Task 4: Control etch-related defects in embedded, etched-and-regrown diodes**<br>4.1: Understand and control etch-induced defects for embedded regrowth<br>4.2: Develop low damage etch | Determine critical leakage pathway.<br>**Actual Performance:** (12/2018) Sidewall leakage was observed to be a critical component to mesa-isolated selective area regrown diodes from perimeter-to-area study of reverse leakage.<br>Controllably mitigate etch-induced defects at regrowth interface.<br>**Actual Performance:** (12/2018) KOH-based post-etch treatment was used on selectively regrown diodes to reduce etch-induced damage.<br>Quantify impact of etch-induced defects on regrown junction leakage.<br>**Actual Performance:** (3/2019) Comparison of post-etch KOH treatment and control sample without KOH treatment was not performed.<br>Reduce etch-induced defects at regrowth interfaces.<br>**Actual Performance:** (3/2019) Various attempts to achieve a low damage primary etch to replace the damaging inductively coupled plasma etch were attempted, including halide-based etching inside the growth reactor and photoelectrochemical etching outside of the growth reactor) but none proved feasible.<br>Quantify impact of low damage etch on regrown junction leakage<br>**Actual Performance:** (3/2019) This milestone was not achieved due because a low damage primary etch was not developed. |
| **Task 5: Demonstrate 1.2 kV patterned regrown diode**<br>5.1: Develop poly-AlN regrowth mask<br>5.2: Fabricate patterned regrowth of diode<br>5.3: Understand method of achieving 1.2 kV patterned, regrown diode | Demonstrate poly-AlN regrowth mask.<br>**Actual Performance:** (6/2019) Poly-AlN growth masks were not investigated due to time constraints.<br>Demonstrate 1.2 kV patterned, regrown diode.<br>**Actual Performance:** (9/2019) 840 V blocking for a selectively etched-and-regrown diode was demonstrated using mesa isolation. Higher voltage likely could have been attained with a multi-step junction termination extension, but this was not done due to time constraints.<br>Correlate interface defects and breakdown voltage.<br>**Actual Performance:** (9/2019) Deep level defect studies of etched-and-selectively regrown diodes were not performed due to time constraints. |

## Project Activities

This project aimed to achieve 1.2 kV etched-and-selectively regrown GaN diodes. Our approach was to use etch-and-regrowth to define the selective regions of p-type GaN. This approach has two main challenges. The first is damage caused by the ICP etch. ICP is the industry standard etch method for GaN, but it is known to produce crystal defects in the remnant material. These etch-induced defects are expected to cause significant reverse leakage in pn-diodes. The second challenge is excessive impurity incorporation during regrowth. Regrowth of GaN, even without a damaging etch, typically results in larger Si contamination of the regrowth interface. Si is an n-type dopant, and its effect is also to increase diode leakage.

We began by studying the impact of interfacial contamination during GaN regrowth without an ICP etch. Selective area doping using etch-and-regrowth therefore exposes pockets with an etched c-plane surface at the bottom surrounded by etched sidewalls. For a circular etch pattern, these sidewalls consist of a variety of crystal facets, including the m-plane of GaN. Both the c-plane and sidewalls form the electrical junction for selective area regrowth, so interfacial impurities on both surfaces likely impact device electrical performance. Thus, impurity incorporation for regrowth on the c-plane and m-plane of GaN was studied.

Figure 1 shows reverse leakage characteristics for continuously-grown and regrown c-plane GaN pn-diodes. The pn-diodes were formed with a simple mesa isolation and had no junction termination extension. Two of the diodes were grown continuously but had differing levels of Si intentionally placed at the junction to controllably emulate the impact of interfacial Si in regrown diodes. From these devices with intentional Si interfacial doping, it was observed that a Si level below $8\times10^{11}$ $cm^{-2}$ did not impact reverse leakage. The regrown diode was able to achieve equivalent electrical performance to the continuously-grown diode with blocking voltage > 700 V when using best practices to mitigate interfacial impurity incorporation, including minimizing wafer exposure to ambient. However, this result was not typical, as best practices resulted in sporadic Si interfacial levels that could be much higher than $10^{12}$ $cm^{-2}$. No systematic method for Si removal was achieved, despite efforts to using ozone followed by HF etching and TMAH etching.

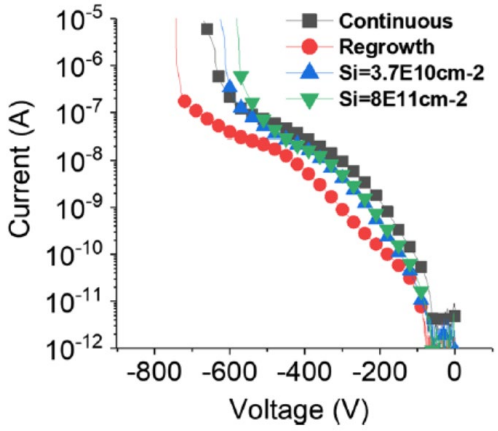


Fig. 1. Reverse leakage for continuously-grown pn-diodes with and without intentional Si interfacial doping at the electrical junction and a regrown diode. The equivalence of all diodes shows that Si interfacial concentration below $10^{12}$ $cm^{-2}$ is not inherently detrimental for diodes and that regrowth with low interfacial Si can be achieved. It is noted that this regrowth result was unusually good and systematic control of Si was not achieved.

Si incorporation and was also studied for m-plane diodes. Similar to c-plane GaN, it was found that m-plane GaN was subject to sporadic and often high levels if Si incorporation during regrowth. However, Fig. 2 shows the best case result for regrown m-plane diodes achieving equivalence to continuously-grown diodes with blocking voltage up to 540 V. Like the c-plane efforts, no systematic method was found to control Si interfacial incorporation. Nonetheless, this study demonstrated that m-plane impurity uptake, i.e. sidewall impurity uptake, is not a showstopper for regrown GaN diodes.

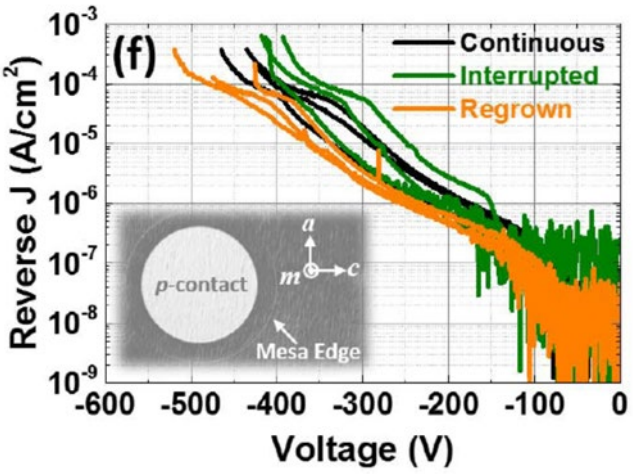


Fig. 2. Reverse leakage for continuously-grown and regrown m-plane diodes. The equivalence of all continuous and regrowth diodes shows that m-plane regrowth with low interfacial Si can be achieved. It is noted that this regrowth result was unusually good and systematic control of Si was not achieved.

Next, we studied etch-induced defects on the c-plane and m-plane of GaN and correlated changes in their concentration with changes in reverse leakage of pn-diodes. In this approach, the fast but damaging ICP etch defines the active diode area. The goal was to develop a secondary low damage etch to improve the surface quality for subsequent regrowth. Similar to the impurity studies described above, etch-induced defects were examined for both the c- and m-planes of GaN to assess basal plane and sidewall defectivity individually.

Figure 3 shows quantitative correlation between the increase in concentration of a defect state with an energy level at 1.9 eV below the conduction band and increase in reverse leakage for ICP etch-and-grown c-plane diodes relative to continuously-grown diodes. We attributed the increase in reverse leakage with ICP etch to recombination-generation current mediated by the 1.9 eV deep level. Use of a KOH-based AZ400K wet chemical treatment post-ICP etch reduced the concentration of the 1.9 eV deep level, and this deep level defect reduction was also quantitatively correlated with reduced reverse leakage relative to ICP-etched regrown diodes. However, the reverse leakage of the ICP+AZ400K diodes were still higher than for the continuously-grown diodes. No etching of the GaN c-plane was observed using the AZ400K treatment. We concluded that the AZ400K can remove surface damage caused by the ICP etch but sub-surface damage remained. Such remnant sub-surface damage could account for the elevated leakage for the ICP+AZ400K diodes vs. the continuously-grown diodes.

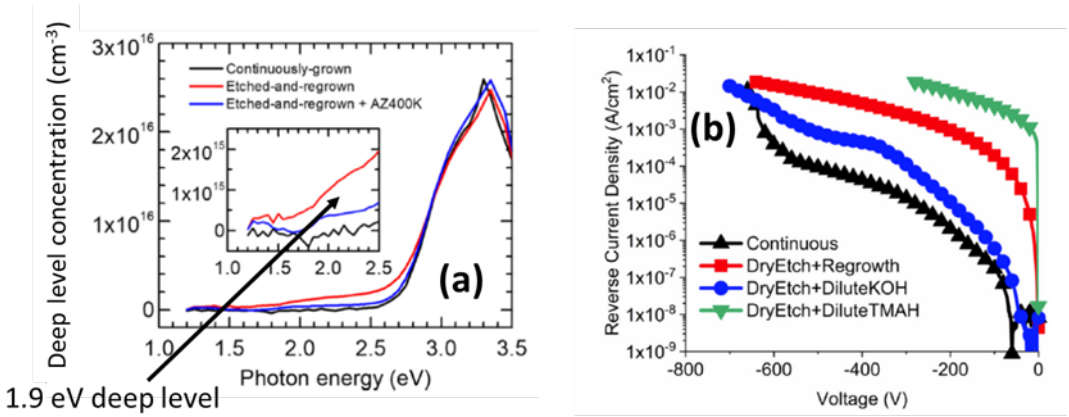


Fig. 3. (a) Deep level spectrum for continuously-grown and etched-and-regrown c-plane diodes. A 1.9 eV deep level increased in concentration with ICP etch, and its concentration was subsequently reduced with AZ400K, i.e dilute KOH treatment, after ICP. (b) Reverse leakage of continuously-grown and etched-and-regrown diodes for various post-ICP treatments. The reverse leakage and 1.9 eV defect concentration trend together quantitatively.

The efficacy of AZ400K treatment to reduce ICP etch damage and reverse leakage current on etched sidewalls was examined. We used GaN diodes that were etched and regrown on m-plane substrates as a proxy for sidewall damage in c-plane GaN diodes. Figure 4 compares the reverse leakage of m-plane diodes as a function of etch process. Similar to c-plane diodes, ICP etching significantly increases the reverse leakage current, ICP+AZ400K treatment reduced reverse leakage compared to ICP etched diodes but did not achieve leakage equivalent to continuously-grown diodes. A photoelectrochemical (PEC) etch following ICP further reduced leakage relative to ICP+AZ400K for m-plane diodes. However, this PEC process was found to be uncontrollable for ICP-etched c-plane material, yielding a high density of deep nano-pipes.

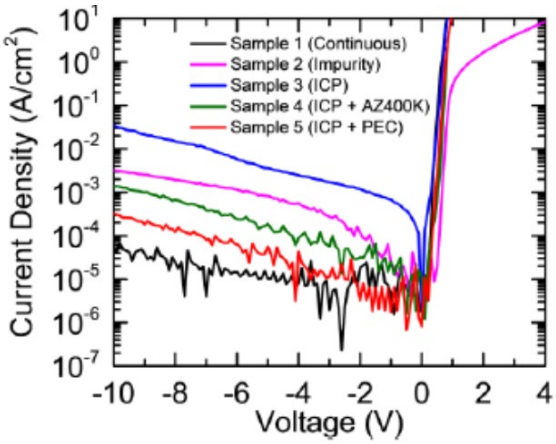


Fig. 4. Reverse leakage comparison for continuously-grown and etched-and-regrown m-plane diodes. Reverse leakage of continuously-grown and etched-and-regrown diodes for various post-ICP treatments trend similarly to c-plane GaN.

Deep level defect study of continuously-grown, ICP etched-and-regrown, and ICP+AZ400K etched-and-regrown m-plane diodes showed similar trends as for c-plane diodes. The same types of deep level defects were observed for both m-plane and c-plane continuously-grown and etched-and-regrown diodes. Figure 5 shows the change in deep level density vs. etch process, where the most dramatic changes occurred for the 1.9 eV deep level. The 1.9 eV deep level concentration increased from ~ $10^{14}$ $cm^{-3}$ in the drift region of the continuously-grown diode to ~ $10^{19}$ $cm^{-3}$ near the etched-and-regrown junction for the ICP diode. ICP+AZ400K treatment reduced the concentration of this deep level to ~ $10^{17}$ $cm^{-3}$ at the etched-and-regrown interface and to ~ $10^{14}$ $cm^{-3}$ in the drift region for the m-plane diodes. As in the case of c-plane didoes, these trends in deep level concentration match those for reverse leakage for m-plane diodes. These findings indicate that ICP+AZ400K treatment is likely to reduce the concentration of etch-related defects and leakage for the c-plane and sidewalls in selectively etched-and-regrown pn-diodes grown on c-plane substrates.

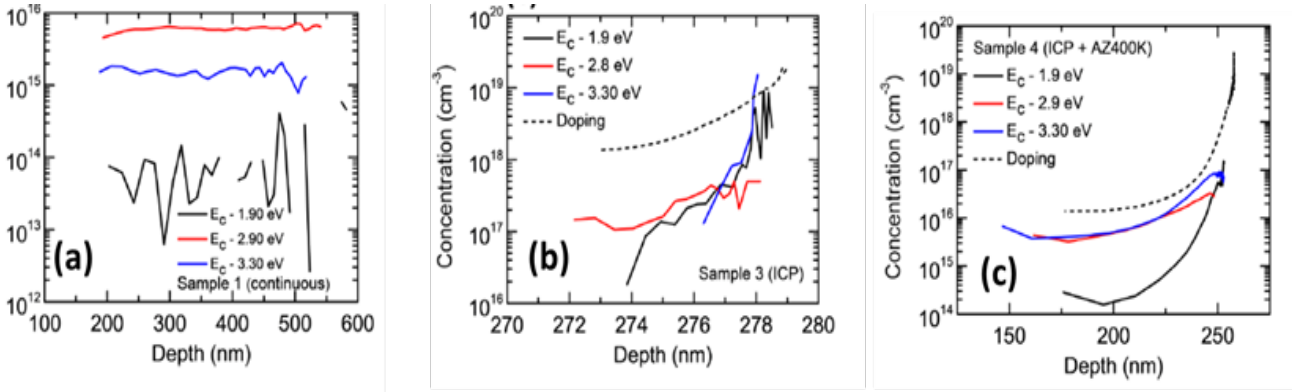


Fig. 5. Deep level concentration for continuously-grown and etched-and-regrown m-plane diodes for various post-ICP treatments. The ICP+AZ400K treatment showed similar efficacy as in c-plane GaN for reducing the 1.9 eV etch-enhanced deep level.

The ICP+AZ400K etch process was employed for selective area doping via etch and regrowth. Figure 6 shows a secondary electron microscopy cross-section of an etched-and-regrown pn-diode on a c-plane substrate. An ICP etch formed wells in the n-GaN layer, a wet AZ400K followed the ICP etch, and p-GaN regrowth filled the wells and planarized the surface. Regrown diodes were formed by depositing p-metal within the regrown wells. Control diodes were also formed by depositing p-metal in regions where p-GaN was regrown on planar, unetched surfaces. Mesa isolation of all diodes was achieved by etching through the p-GaN layer around the p-metal. Blocking voltages > 600 V were observed for selectively etched-and-regrown diodes, and the reverse leakage of etched-and-regrown diodes were comparable to that of the diodes regrown on epitaxial, unetched surfaces. A perimeter-to-area comparison of leakage for diodes of different areas suggested that sidewall leakage due to the ICP mesa isolation etch was a significant contributor to leakage. From these observations, we conclude that ICP+AZ400K does mitigate etch-induced leakage for etched-and-regrown junctions, but additional leakage paths also need to be addressed in practice when realizing high voltage diodes.

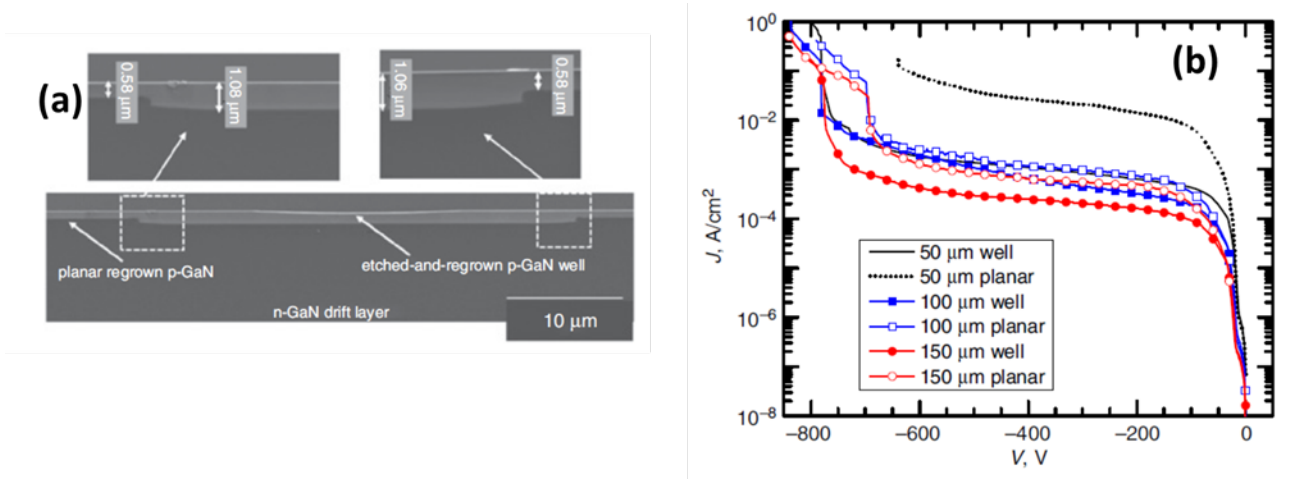


Fig. 6. (a) SEM cross-section of an etched-and-regrown c-plane diode using ICP+AZ400K. Planar diodes were also formed on p-GaN regions between the etched wells. (b) Reverse current comparison showing equivalent electrical performance was observed for both diode types with blocking voltages > 600 V, but sidewall leakage was found to be significant.

We addressed the issue of remnant sub-surface defectivity of the ICP+AZ400K process by including an additional post-ICP etch step. A slow (0.02 nm/s) reactive ion etch (RIE) was added following the AZ400K wet process to remove damaged material. We demonstrated 20x reduction of the 1.9 eV defect level using the ICP-RIE technique compared to ICP alone. Significantly, this reduced the 1.9 eV deep level defect density in the ICP+RIE samples to that of continuously-grown pn-diodes. The pn-diodes formed using ICP+RIE with a simple mesa isolation achieved equivalent performance to continuously-grown diodes, as shown in Fig. 7. A junction termination extension was included for a new ICP+RIE device to maximize electrical performance. Fig. 8 shows that planar etched-and-regrown diodes formed in this way achieved 1.6 kV. Selectively etched-and-regrown diodes using the RIE method were not realized due to time constraints, however, achieving kV-class etched-and-regrown GaN diodes using industry-standard practices demonstrates a feasible pathway to commercializing more advanced power devices such as vertical power transistor switches.

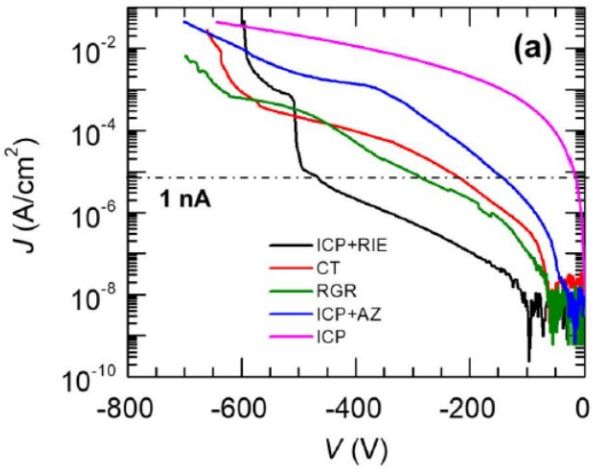


Fig. 7. Reverse leakage for etched-and-regrown c-plane GaN diodes using an ICP+RIE process. Inclusion of an RIE etch achieved electrical equivalence for etched-and-regrown diodes compared to continuously-grown diodes.

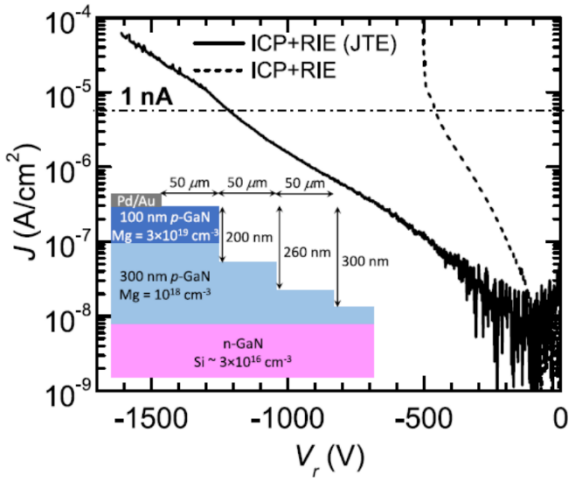


Fig. 8. Reverse leakage for etched-and-regrown c-plane GaN diodes using an ICP+RIE process with a multi-step junction termination extension. kV-class performance was achieved when combining a low damage etch process with advanced electrical field control structures.

## Project Outputs

### *A. Journal Articles*

1. A.M. Armstrong, A.A. Allerman, G.W. Pickrell, M.H. Crawford, C.E. Glaser, and T. Smith, IEEE Journal of the Electron Devices Society 9, 318 (2021).

2. Y. Liu, B. Raghothamachar, H. Peng, T. Ailihumaer, M. Dudley, R. Collazo, J. Tweedie, Z. Sitar, F. Shadi Shahedipour-Sandvik, K.A. Jones, A. Armstrong, A.A. Allerman, K. Grabianska, R. Kucharski, and M. Bockowski, Journal of Crystal Growth 551, 125903 (2020).

3. A. Aragon, M. Monavarian, G. Pickrell, M. Crawford, A. Allerman, D. Feezell, and A.M. Armstrong, Journal of Applied Physics 128, 185703 (2020).

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7. G.W. Pickrell, A.M. Armstrong, A.A. Allerman, M.H. Crawford, K.C. Cross, C.E. Glaser, and V.M. Abate, J. Electron. Mater. 48, 3311 (2019).

8. M. Monavarian, G. Pickrell, A.A. Aragon, I. Stricklin, M.H. Crawford, A.A. Allerman, K.C. Celio, F. Léonard, A.A. Talin, A.M. Armstrong, and D. Feezell, IEEE Electron Device Letters 40, 387 (2019).

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11. Z. Warecki, A. A. Allerman, A. M. Armstrong, A. A. Talin, and J. Cumings, “High-resolution planar electron beam induced current in bulk diodes using high-energy electrons,” Appl. Phys. Lett., vol. 119, no. 1, p. 014103, Jul. (2021).

### *B. Dissertations*

“Etched-and-regrown diodes on m-plane GaN for next generation power electronic devices,” Andrew A. Aragon, University of New Mexico, May 5 2021.

### *C. Patent Applications/Issued Patents*

Method to remove etch damage by photoelectrochemical etching, Invention Report Number 0687308-18-0001

## Follow-On Funding

None.