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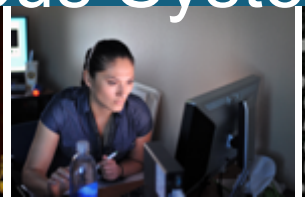
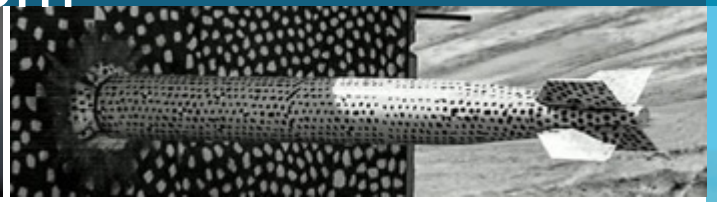
Sandia National Laboratories

Enabling Guaranteed Correctness and Leading Edge Performance under Radiation with a Heterogeneous System





Ben Feinberg, Arun F. Rodrigues, Matthew J. Marinella, Sapan Agarwal

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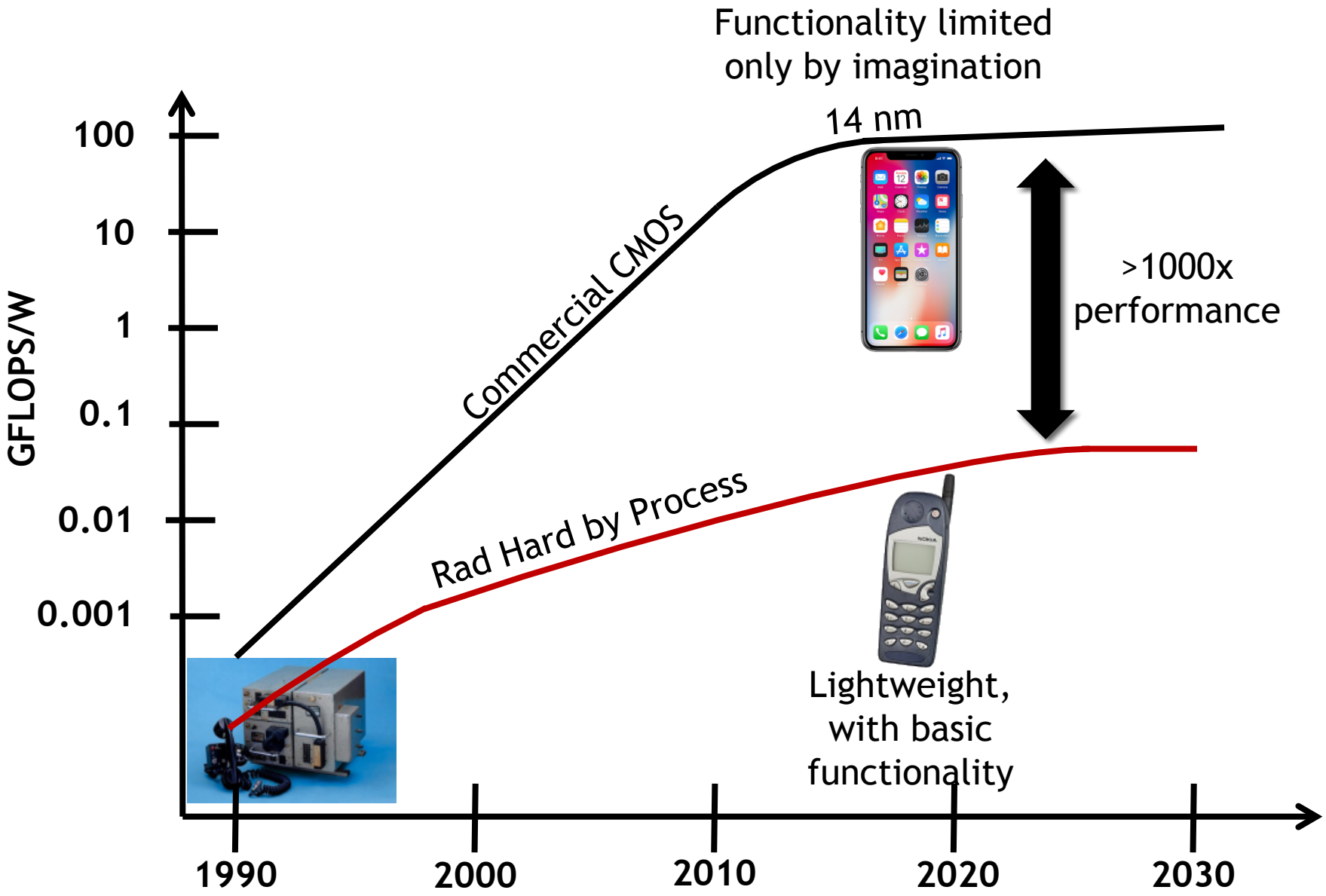
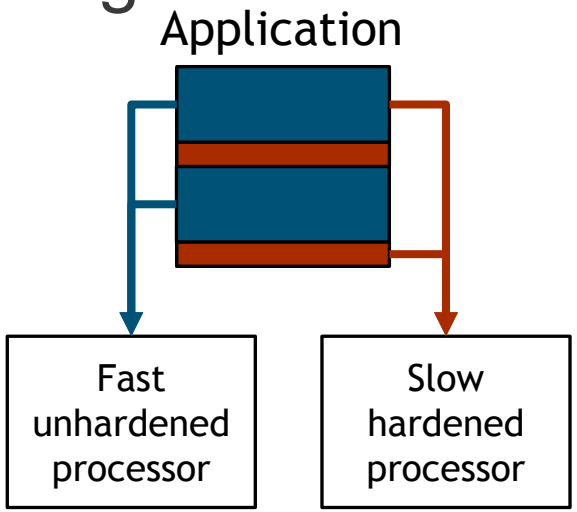
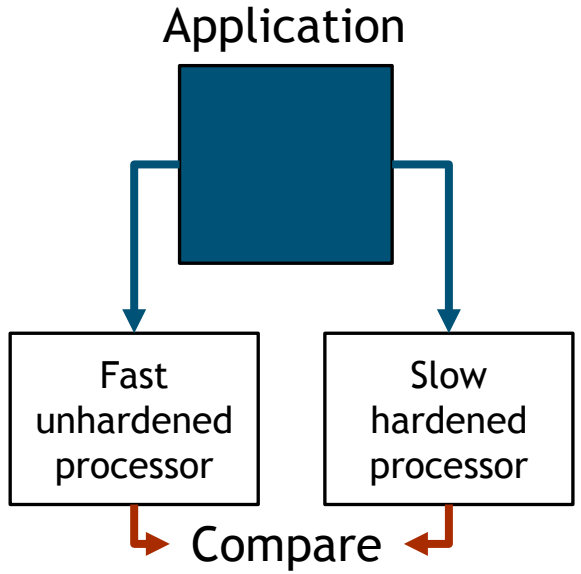
Rad Hard By Process ICs Lag Commercial CMOS ICs



Bridging the Performance Gap with Heterogeneous Integration





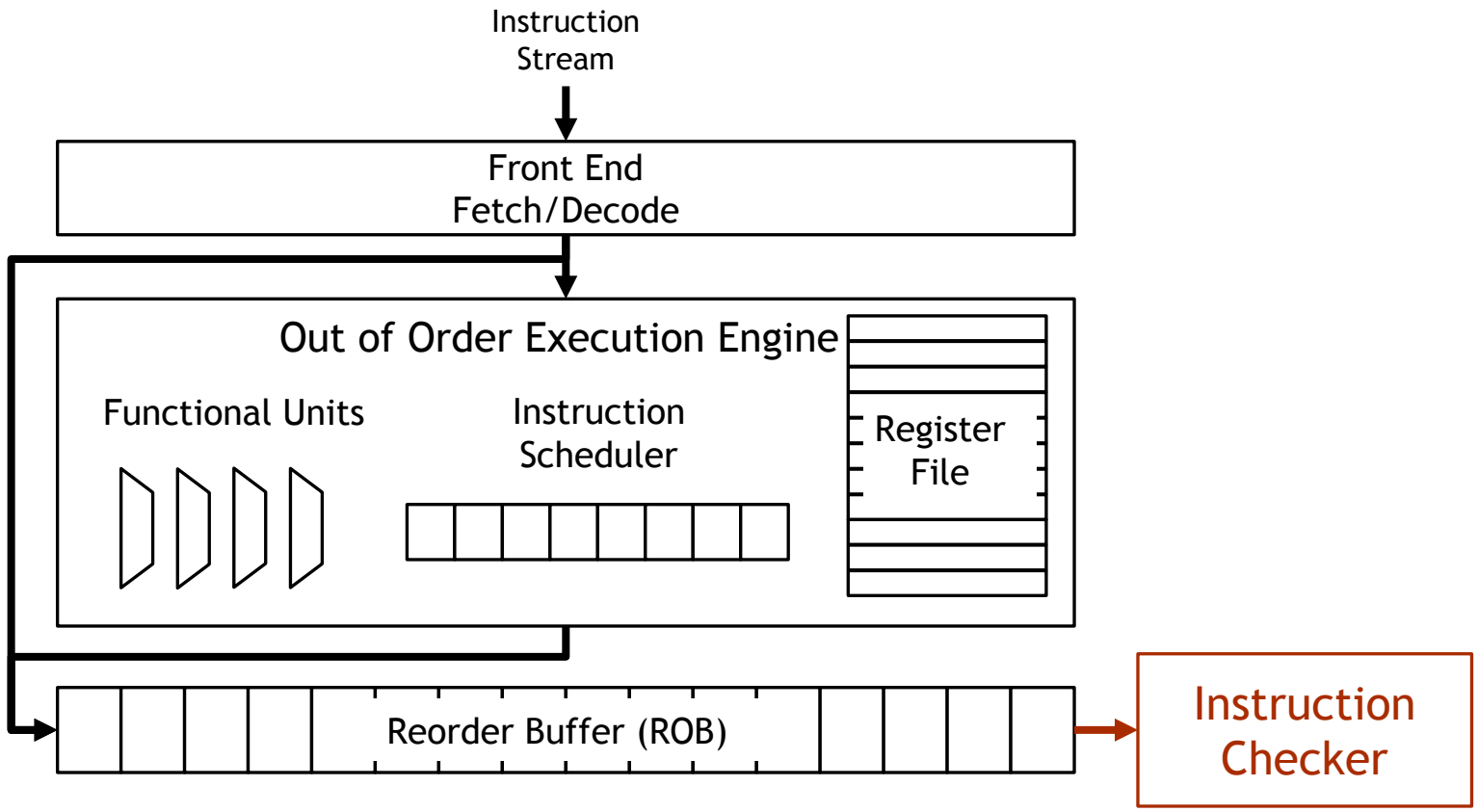
Algorithmic Heterogeneity:

- Partition algorithms to enable a slower processor to check the correctness of computation on a faster processor
- May not be feasible for all applications

Architectural Heterogeneity:

- Tightly couple processors into a single heterogeneous self-checking system
- Transparent to the programmer
- Requires modifications to existing cores

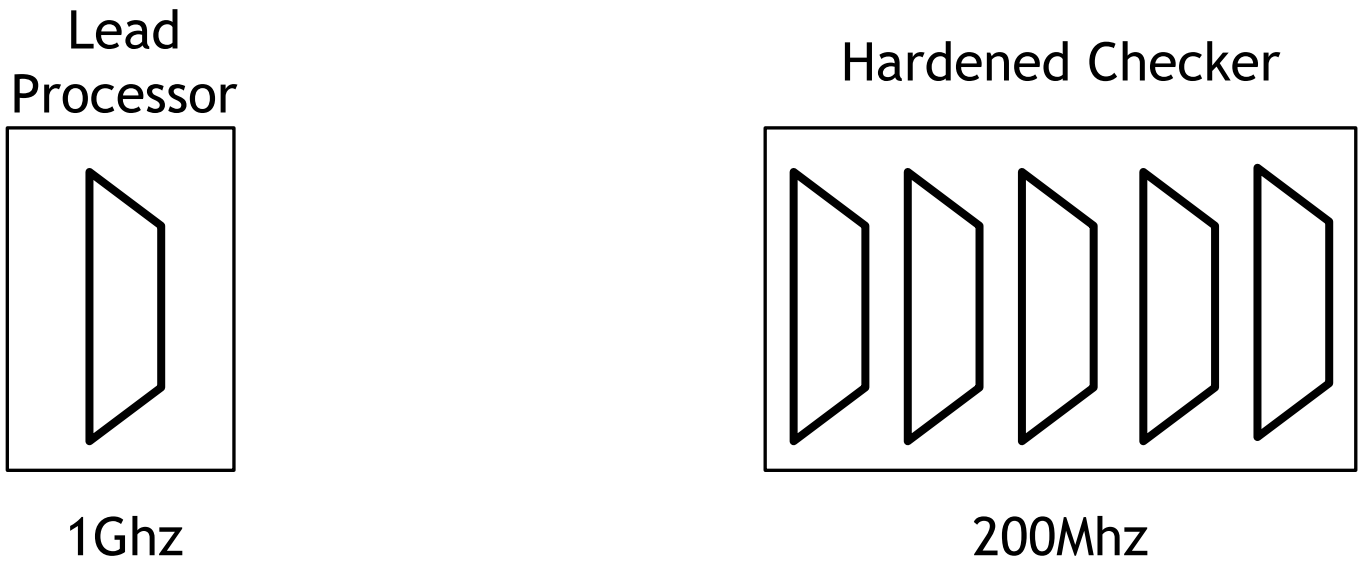
Integrating Checking into an Out of Order Core



Dynamic instruction checking can be directly integrated into an Out of Order (OoO) processor using the same recovery mechanisms used for handling speculation

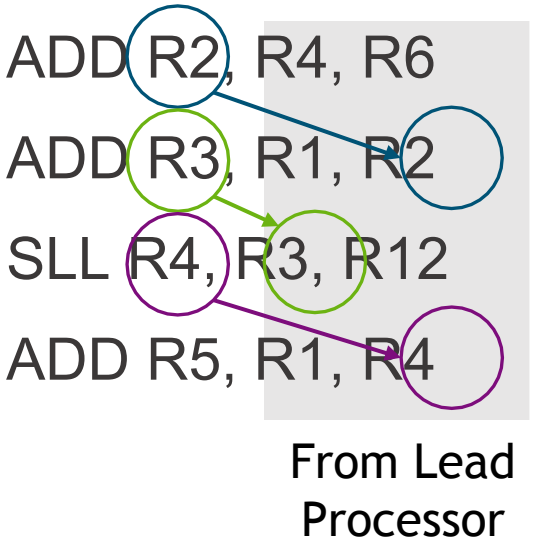
T. M. Austin, “DIVA: A reliable substrate for deep submicron microarchitecture design,” in International Symposium on Microarchitecture (MICRO), 1999, p
196–207

Matching Lead Processor Throughput



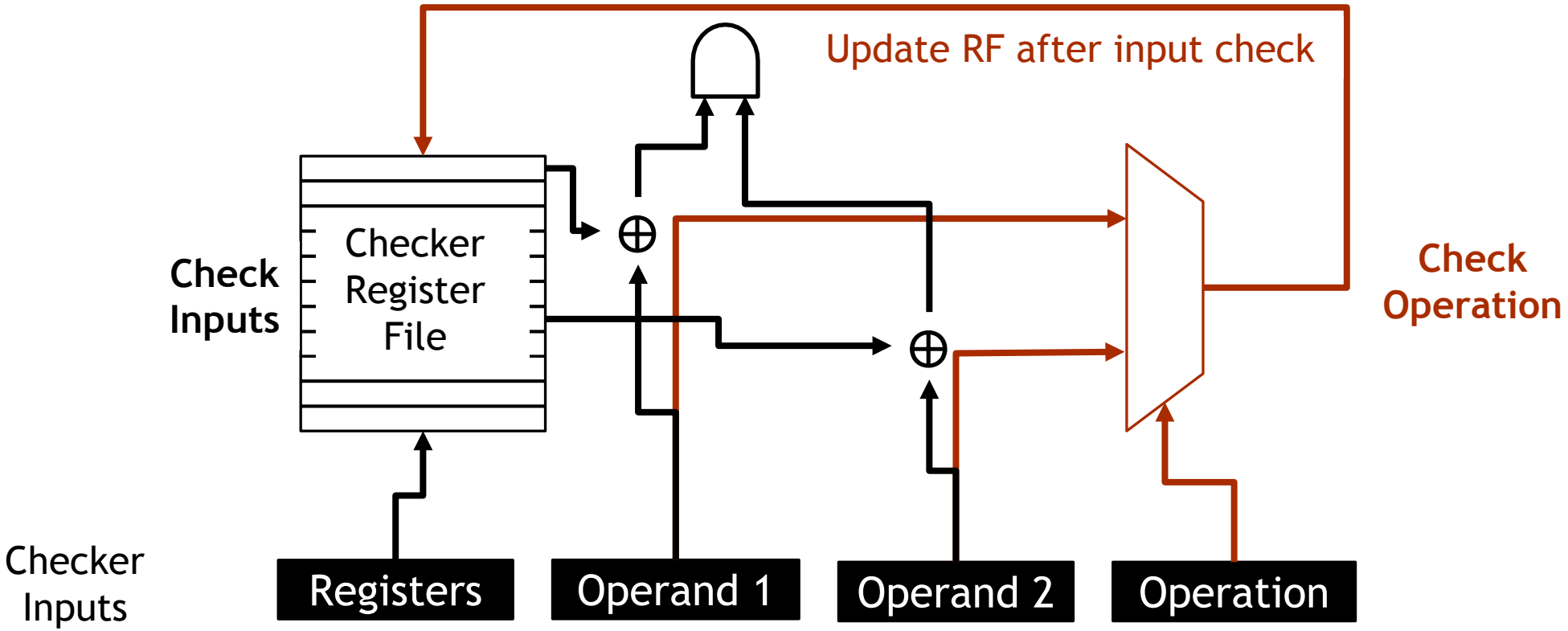
- Using a wide checker (many functional units) enables the checker to compensate for a significantly lower clock frequency
- A checker can avoid many of the disadvantages associated with wide processor pipelines.

Accelerating Checking with Data from the Lead Processor



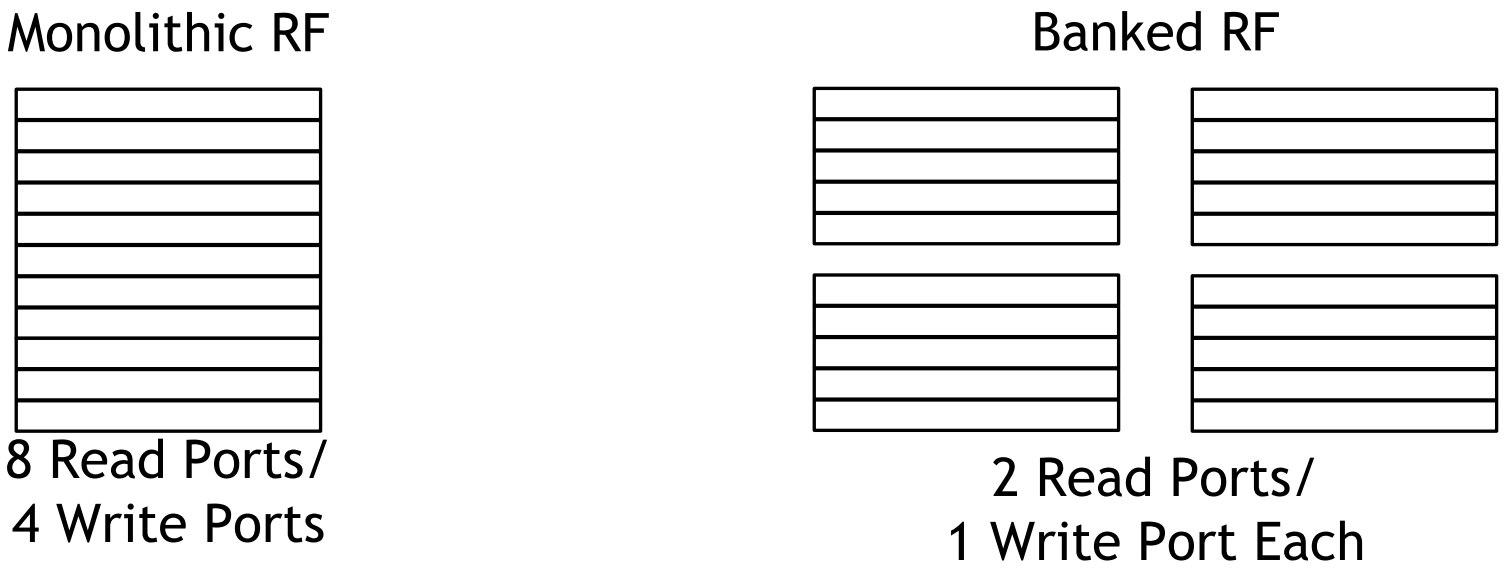
- Dependency chains can be partially checked in parallel if the input operands for each instruction are transferred from the lead processor to the checker
- Updating the checker register file requires serializing dependency chains

Wide Checker Architecture



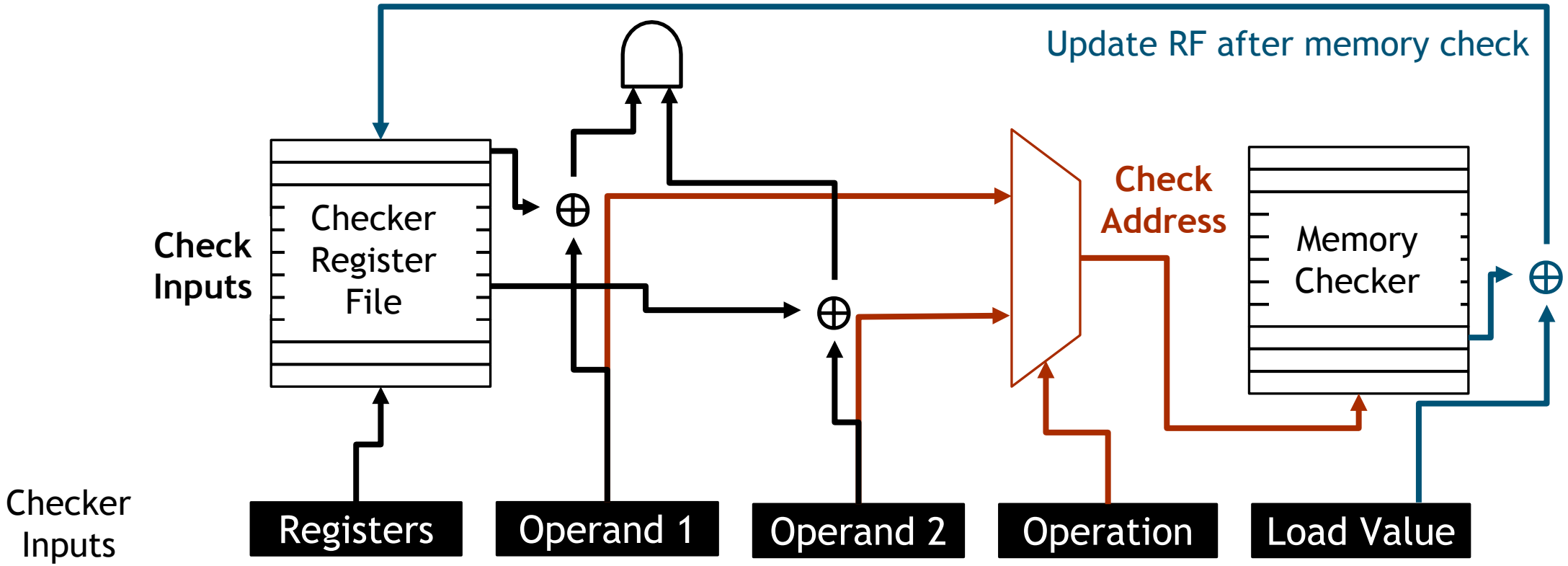
- Two separate checking steps, check the operation given the inputs and check the inputs against the checker register file
- If the inputs match the checker register file, the computed result is used to update the checker register file

Checker Register File



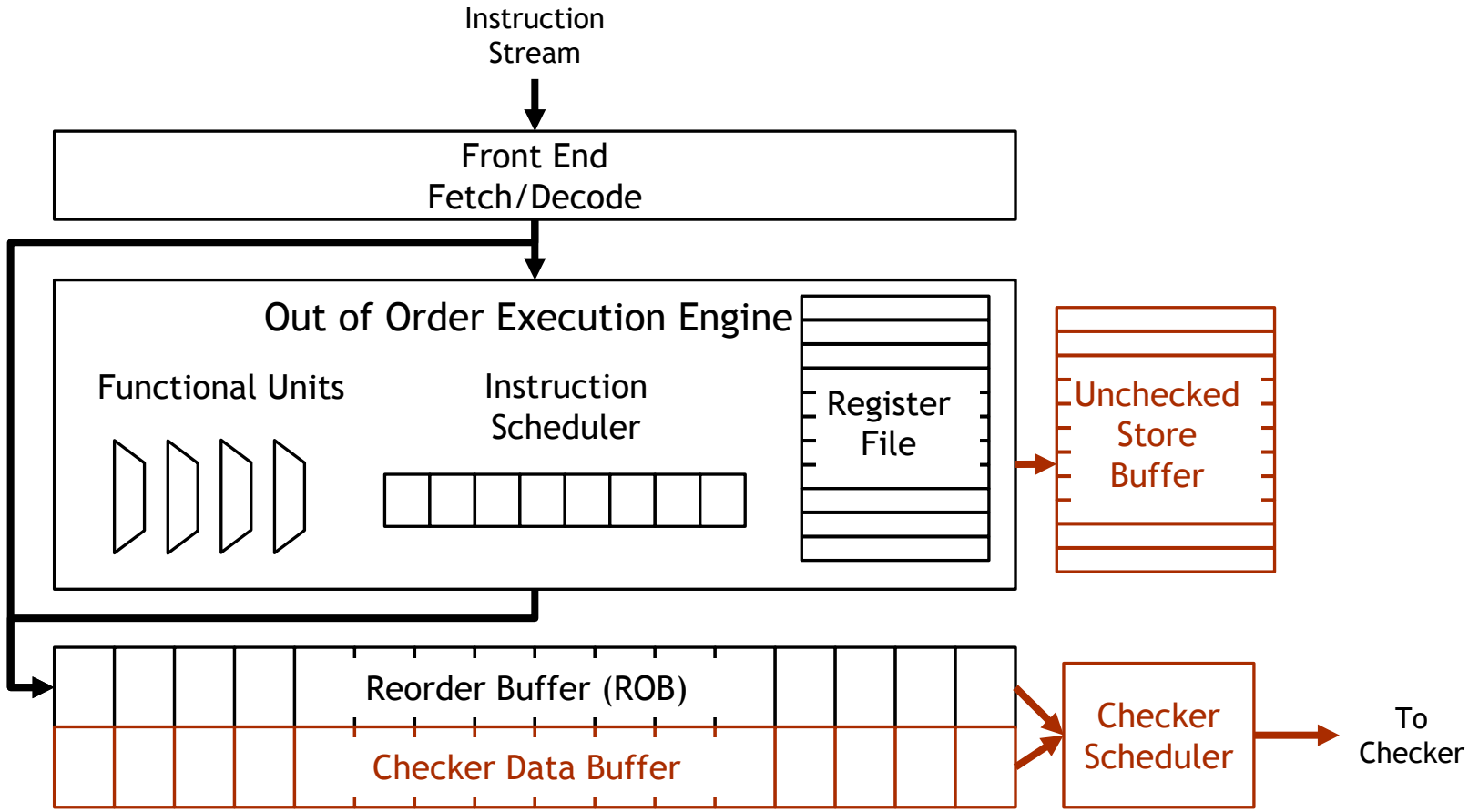
- Very wide cores typically require heavily multi-ported register files
- Multiple register file banks can reduce the porting overhead at the cost of additional scheduling complexity
- The lead processor schedules accesses when instructions leave the ROB

Memory Accessing Instructions



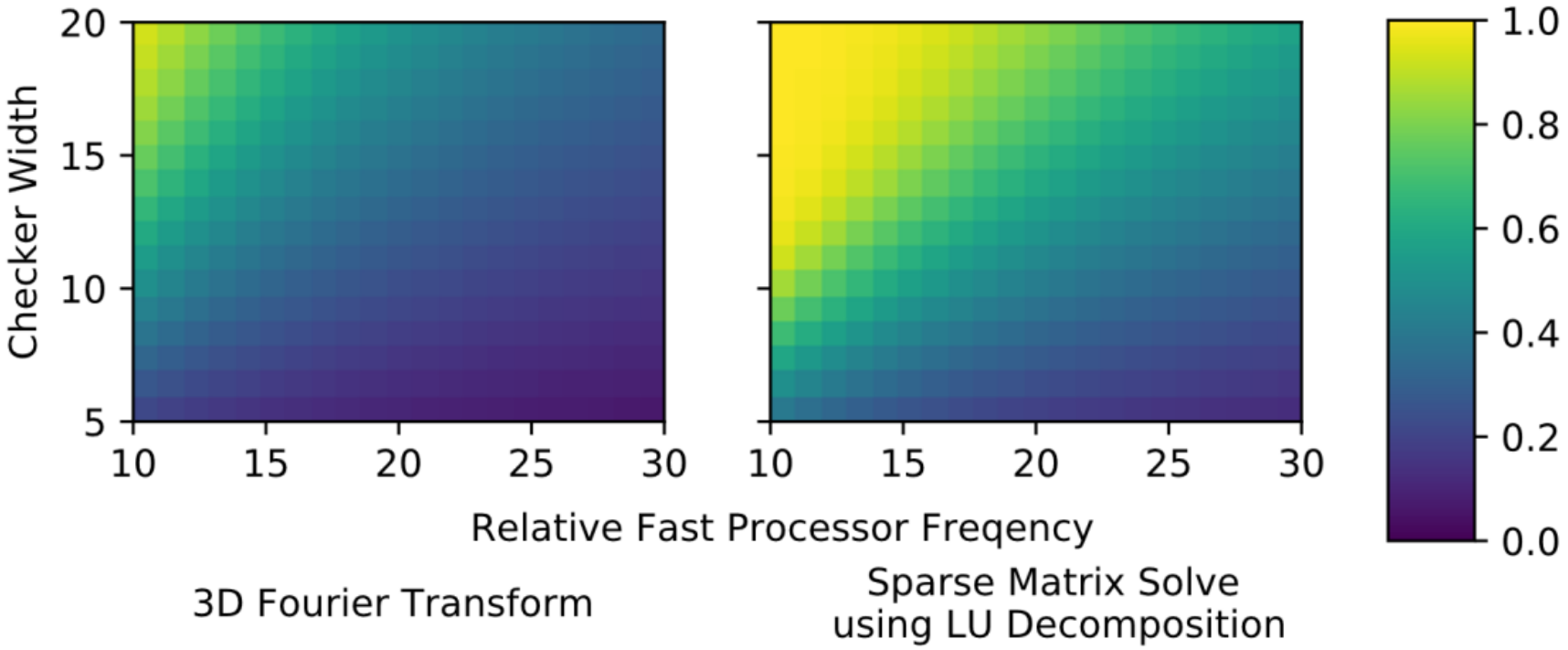
- Load instructions require checking inputs, address generation, and the memory access
- The memory checker can store only error detection metadata to reduce capacity
- Since the memory checker stores only error detection data, the fast processor must transmit the loaded value to update the checker register file

Lead Processor Modifications



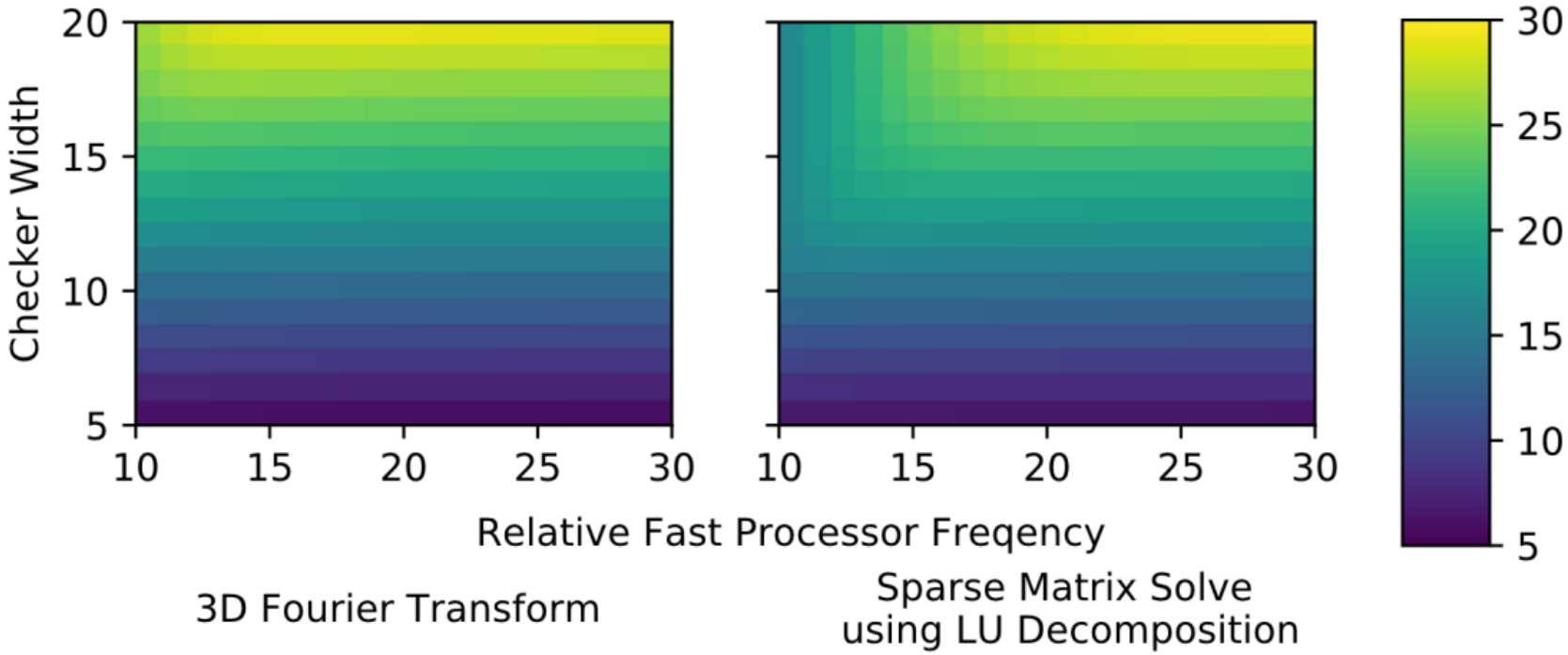
Lead processor requires three new structures to support the heterogeneous checker

Performance Compared to Lead Processor



The heterogeneous system can provide sufficient throughput to avoid a bottleneck for many applications

Performance Compared to Hardened Processor

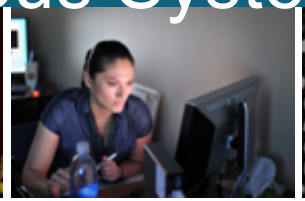
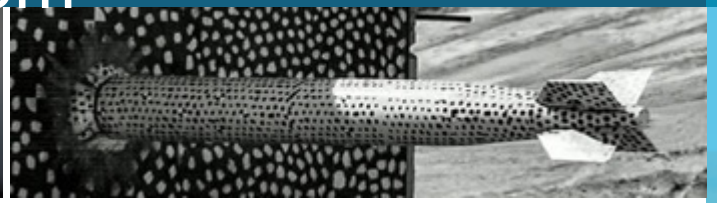


The heterogeneous system can outperform an in-order processor by more than improvement expected by increasing checker/processor width

Conclusion

- Architectural heterogeneity shows significant potential to improve the performance of heterogeneous radiation hardened systems.
- Exploiting architectural heterogeneity requires new architectures with modifications to the lead processor and newer checking cores.
- Balancing the width of the checker with the throughput of the lead processor is essential to avoid bottlenecks and wasted energy.

Enabling Guaranteed Correctness and Leading Edge Performance under Radiation with a Heterogeneous System

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