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A Current-fed High Gain Multilevel DC-DC Converter for BESS Grid Integration Applications

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***Abstract*—This paper presents a new high gain, multilevel, bidirectional DC-DC converter for interfacing battery energy storage systems (BESS) with the distribution grid. The proposed topology employs a current-fed structure on the low-voltage (LV) BESS side to obtain high voltage gain during battery-to-grid mode of operation without requiring a large turns ratio isolation transformer. The high-voltage (HV) side of the converter is a voltage-doubler network comprising two half-bridge circuits with an intermediary bidirectional switch that re-configures the two bridges in series connection to enhance the boost ratio. A seamless commutation of the transformer leakage inductor current is ensured by the phase-shift modulation of HV side devices. The modulating duty cycle of the intermediary bidirectional devices generates a multilevel voltage of twice the switching frequency at the grid-side dc link, which significantly reduces the filter size. The presented modulation strategy ensures zero current switching (ZCS) of the LV devices and zero voltage switching (ZVS) of the HV devices to achieve a high power conversion efficiency. Design and operation of the proposed converter is explained with modal analysis, and further verified by detailed simulation results.**

***Index Terms*—Bidirectional DC-DC converter, current-fed topology, power electronic interface, multilevel converter, BESS, renewable energy.**

I. Introduction

The intermittent nature of renewable power sources necessitates an energy storage for their integration to the distribution grid [1]-[2]. Battery energy storage system (BESS) is the most widely used energy storage due to its high source and sink capability, fast start-up and high efficiency [3]. However, a BESS requires careful power processing and control for safe operation, which is usually achieved by a step-up dc-dc converter to interface the low voltage battery with the grid side inverter. The desired characteristics of this grid interface converter include high voltage gain, bidirectional power processing, a small battery current ripple, high efficiency over a wide load range, etc. [4]-[5].

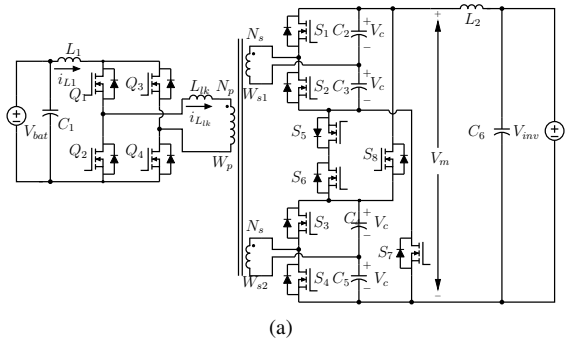
A parallel input, series output dual active bridge converter is presented for high-gain, bidirectional operation [6]. The converter uses partial paralleling of the switching bridges to extend the operating range and reduce the current stress on the LV side devices. However, the input current ripple is high due to the absence of a filter on the LV side. Current-fed step-up topologies mitigate this challenge due to presence of the boost inductor which helps to reduce the battery current ripple. Various current-fed topologies for step-up dc-dc conversion have been proposed in literature. Although current-fed topologies have low current ripple on the LV side, they suffer from current commutation challenges for the transformer leakage inductor. This can lead to high voltage spikes across the switches during turn-off. Various clamping circuits have been proposed in literature to overcome this challenge [7]-[11]. A current-fed flyback converter with active clamp circuit to interface renewable sources with the dc grid is presented in [7]. The three-phase active clamped interleaved boost converter with series output achieves a high gain at the expense of substantial increase of the magnetic footprint [8]. High-gain operation with soft switching for LV devices is also observed for the resonant push-pull topology [9]. A flyback snubber circuit to limit the voltage stress across the switches was reported in [10]. Although the clamping circuits alleviate the current commutation issue, the required additional circuitry leads to increased losses and reduced overall efficiency of the topology.

Soft commutation or natural commutation is the process of transferring the current flowing through devices to be turned-off to the devices to be turned-on for the next conduction cycle seamlessly through modulation strategies . Natural commutation technique for current-fed push-pull converter is presented in [12]. Various modulation strategies for natural commutation of full-bridge boost-type converters have been proposed in [13]-[17]. However, the voltage gain is not sufficient for a very high step-up application.

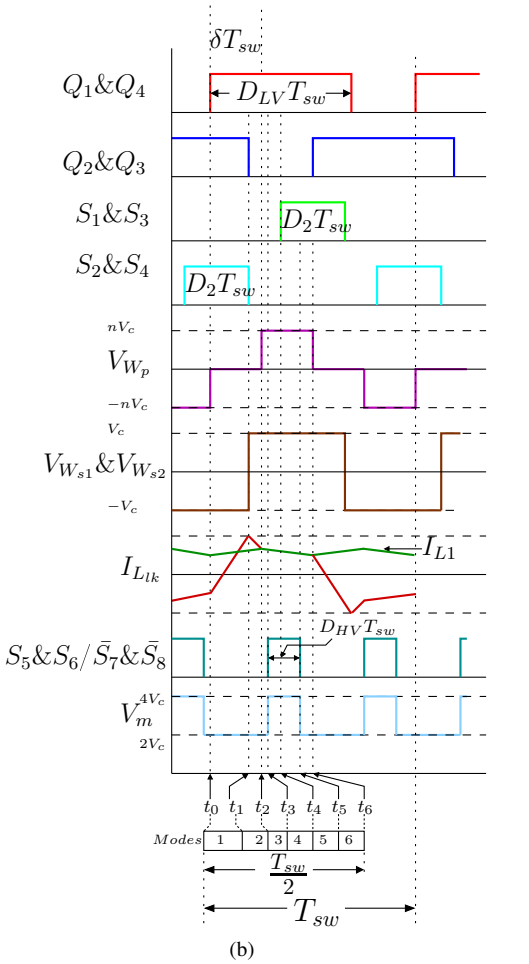
This paper presents a high-gain, isolated, multilevel, bidirectional dc-dc converter to alleviate the above issues in grid interfacing operation. The proposed multilevel structure reduces the output voltage ripple to lower the filter size. A combined duty cycle and phase-shift modulation strategy ensures natural commutation of the leakage inductor current. Soft switching of LV and HV devices increase the converter efficiency. Section II illustrates the operating principle of the proposed converter.

Converter design guidelines are presented in Section III, which is further verified by detailed simulation results in Section IV.

II. Topology Structure and Modes of Operation



(a)



(b)

Fig. 1: (a) Proposed multistage DC-DC topology. (b) Steady-state operating waveforms.

The schematic for proposed multilevel dc-dc converter is shown in Fig. 1(a). The topology comprises of a current-fed full bridge consisting of a boost inductor L_1 and switches Q_1 - Q_4 on the BESS (LV) side. The grid (HV) side of the topology is composed of two half-bridge switching networks (S_1-S_2 and S_3-S_4). The two half-bridges are configured in series/parallel through the conduction of the switches S_5 and S_6 to generate a high-frequency multilevel voltage V_m. L_{lk} represents the equivalent leakage inductance of the transformer referred to the LV winding W_p. The dc voltage gain is dependent on the charging duration of the boost inductor L_1 as well as the multilevel duty cycle. The half-bridge capacitor voltages (V_c) are assumed to be equal in the steady-state. Voltage and current waveforms during a switching period are shown in Fig. 1(b). As seen from the figure, one half of the switching cycle in battery discharging process can be divided into six modes of operation. The equivalent circuits of the converter during the six modes are depicted in Fig. 2. The HV side switches S_7 and S_8 are given gating signals complimentary to switches S_5 and S_6, respectively. A suitable dead time is applied between gating signals of switches S_5-S_6 and S_7-S_8 to avoid any short circuit of the half-bridge capacitors. This dead time also ensures the ZVS turn on of switches S_7 and S_8.

Mode-1 ($t_0 < t < t_1$)**:** This mode corresponds to the boost inductor charging. Prior to this mode, the LV side devices Q_2 and Q_3 were conducting to transfer power from the battery to the grid. At $t = t_0$, Q_1 and Q_4 are turned on to connect the boost inductor L_1 across the battery. The inductor charging current flows through two paths, namely $V_{bat} - L_1 - Q_1 - Q_2$ and $V_{bat} - L_1 - Q_3 - Q_4$. For natural commutation, the leakage inductor current $i_{L_{lk}}$ has to exceed the charging boost inductor current i_{L_1}. The positive rate-of-rise of $i_{L_{lk}}$ is obtained by the conduction of HV switches S_2 and S_4, which imparts a negative voltage of magnitude nV_c across the LV winding W_p. The leakage inductor current path is shown in Fig. 2 (a) in blue arrows. $i_{L_{lk}}$ reaches its peak at $t = t_1$. Due to the conduction of their antiparallel diodes, S_7 and S_8 turn on with ZVS condition and the multilevel voltage during this mode is $2V_c$. The inductor L_1 charging current during this mode is evaluated from the following equation

$$V_{bat} - L_1 \frac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = 0 \tag{1}$$

Also, from Fig. 2(a), the leakage inductor current is found from (2) as

$$-nV_c + L_{lk} \frac{\mathrm{d}i_{L_{lk}}}{\mathrm{d}t} = 0 \tag{2}$$

where n is transformer turns ratio $= \frac{N_p}{N_s}$. Hence the reflected voltage assists in the discharge of the energy stored in L_{lk} and thus the commutation process. The

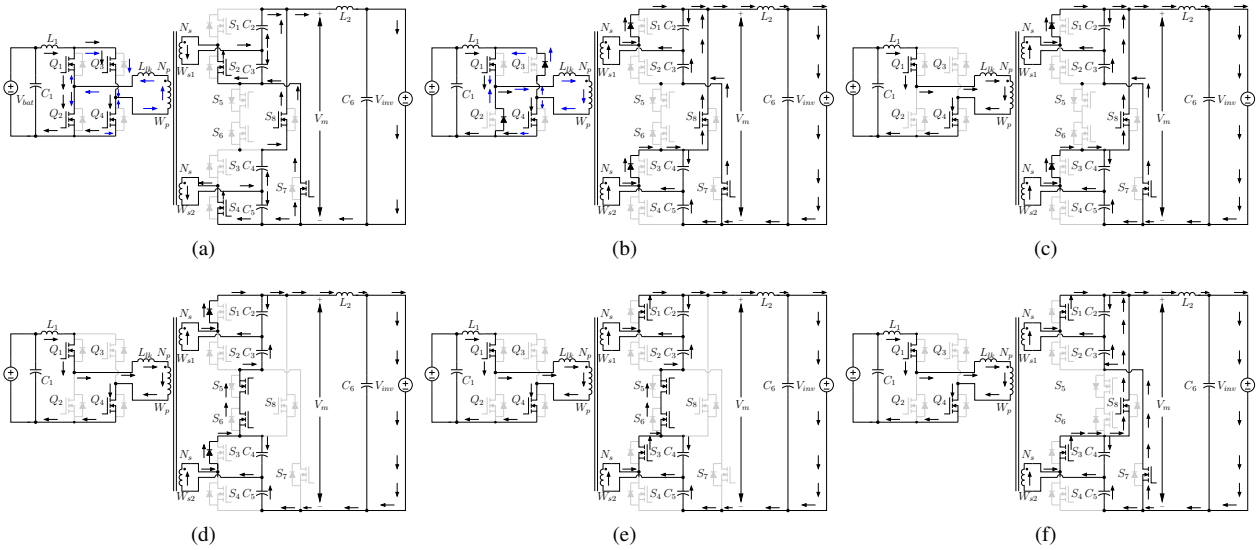


Fig. 2: Modes of operation. (a) Mode-1. (b) Mode-2. (c) Mode-3. (d) Mode-4. (e) Mode-5. (f) Mode-6.

overlap period of the LV side devices is selected in such a way that the leakage inductor current reverses and becomes greater than the battery input current to ensure natural commutation ($i_{L_{lk}} > i_{L_1}$).

Mode-2 ($t_1 < t < t_2$)**:** The circuit configuration in Mode-2 is shown in Fig. 2(b). At $t = t_1$, Q_2, Q_3, S_2 and S_4 are turned off. The battery current i_{L_1} continues to increase with the slope of V_{bat}/L_1 due to conduction of the antiparallel diodes of Q_2 and Q_3. Thus the current i_{L_1} is still represented by (1). Meanwhile, the current direction in the HV winding forces the antiparallel diodes of S_1 and S_3 into conduction. Consequently, the voltage across the W_{s1} and W_{s2} windings and the corresponding reflected voltage in W_p winding reverses. This initiates the discharge of L_{lk}. The current $i_{L_{lk}}$ is found from the following equation

$$L_{lk}\frac{\mathrm{d}i_{L_{lk}}}{\mathrm{d}t} + nV_c = 0 \tag{3}$$

This mode concludes when $i_{L_{lk}}$ becomes equal to i_{L_1}. Q_2 and Q_3 transit into voltage blocking state once their antiparallel diodes are turned off, which indicates ZCS of Q_2 and Q_3. The intermediary switches S_5 and S_6 remain off during this mode.

Mode-3 ($t_2 < t < t_3$)**:** The leakage inductor current $i_{L_{lk}}$ equals i_{L_1} at the time instant $t = t_2$, which initiates the power transfer from the battery to grid. The battery current flows through the series path $V_{bat} - L_1 - Q_1 - L_{lk} - W_p - Q_4$, as shown in Fig. 2(c). The inductor current ($i_{L_1}/i_{L_{lk}}$) during this mode is given by

$$V_{bat} - L_1\frac{\mathrm{d}i_{L_1}}{\mathrm{d}t} = nV_c \tag{4}$$

The HV winding current is conducted by the antiparallel diodes of S_1 and S_3. The multilevel voltage during this mode remains $2V_c$ due to no change in the modulation of switches S_5 and S_6.

Mode-4 ($t_3 < t < t_4$)**:** Just before the start of this mode, the devices S_7 and S_8 are turned off to transfer the device currents to the antiparallel diodes. After the dead time interval, switches S_5 and S_6 are turned on at $t = t_3$, reverse biasing the anti-parallel diodes of S_7 and S_8. All other devices remain in the same switching state as Mode-3 during this mode. The HV windings W_{s1} and W_{s2} are connected in series due to the conduction of S_5 and S_6, which increases the multilevel voltage (V_m) to $4V_c$. The current paths and the conducting devices during this mode are shown in Fig. 2(d). Since there is no change in voltages across the transformer windings and capacitor voltages, the currents through L_1 and L_{lk} remain with similar slopes as expressed by (4).

Mode-5 ($t_4 < t < t_5$)**:** This mode corresponds to zero voltage switching of the devices S_1 and S_3 to reduce the diode conduction period and improve efficiency. Gate pulses are given to the HV side switches S_1 and S_3 at $t = t_4$. Due to prior conduction of the antiparallel diodes, S_1 and S_3 undergo ZVS turn-on. All other devices remain in the same conduction state as in Mode-4. The current path on the HV side of converter is shown in Fig. 2(e). Also, the intermediary switches S_5 and S_6 continue to conduct during this mode, hence the multilevel voltage remains at $4V_c$. Equation (4) represents the boost and leakage inductor current.

Mode-6 ($t_5 < t < t_6$)**:** At the onset of this mode, S_5 and S_6 are turned-off. Consequently, the two half bridges are reconfigured in parallel due to the conduction of the

antiparallel diodes of S_7 and S_8, as shown in Fig. 2(f). The gate pulses of the switches S_7 and S_8 are given after appropriate dead time for synchronous rectification which reduces the conduction losses otherwise incurred by the antiparallel diode conduction. Thus, the resulting multilevel voltage during this mode is $2V_c$.

III. Design Guidelines

The converter design involves determination of parameters L_{lk}, L_1, L_2, C_6, N_p, and N_s. The parameter δ is the time duration during which the transformer leakage inductor current changes its direction and becomes equal to boost inductor current [14]. The expression for determining δ is given by

$$\delta = \frac{t_2}{T_{sw}} = \frac{1}{2}(1 - \frac{V_{bat}}{nV_c}) \tag{5}$$

The parameter δ_{max} is calculated for the minimum battery voltage $V_{bat_{min}}$ and is only dependent on the operating conditions of the converter i.e the output voltage V_{inv} and transformer turns ratio n. As D_{LV} is the duty ratio of LV side devices (Q_1-Q_4) and T_{sw} is the switching time period of devices, then from Fig. 1(b),

$$t_6 - t_1 = (1 - D_{LV})T_{sw} \tag{6}$$

The duration $D_{LV}T_{sw}$ for which the LV side devices conduct, can be evaluated from Fig. 1(b) as

$$2(t_1 - t_0) + t_6 - t_1 = D_{LV}T_{sw} \tag{7}$$

Replacing (6) in (7), D_{LV} is computed as

$$D_{LV} = \frac{t_1 - t_0}{T_{sw}} + 0.5 \tag{8}$$

Similarly, from symmetry, the duty cycle of the HV side half-bridge devices (S_1-S_4), denoted by D_2, can be written as

$$D_2 = \frac{t_6 - t_4}{T_{sw}} + D_{LV} - 0.5 \tag{9}$$

The duty cycle of the HV side intermediary device S_5 is denoted by D_{HV} and is given by $S_5 - S_8$ modulate at twice the frequency of the switches $Q_1 - Q_4$ and $S_1 - S_4$)

$$D_{HV} = \frac{t_5 - t_3}{T_{sw}/2} \tag{10}$$

The multilevel voltage V_m has two distinct levels of $2V_c$ and $4V_c$. Also, the voltage remains $4V_c$ while devices S_5 and S_6 are on i.e. during the interval $D_{HV}2T_{sw}$. The volt-second balance for the filter inductor L_2 yields the following equation.

$$(2V_c - V_{inv})(1 - 2D_{HV})T_{sw} + (4V_c - V_{inv})2D_{HV}T_{sw} = 0 \tag{11}$$

Simplifying (11) , the capacitor steady state voltage V_c is expressed in terms of the output voltage V_{inv} as

$$V_c = \frac{V_{inv}}{2(1 + 2D_{HV})} \tag{12}$$

TABLE I: Designed Parameters of the Converter

Component & Symbol	Value
Transformer turns ratio $\frac{N_p}{N_s} = n$	0.92
Transformer leakage inductor L_{lk}	10 μH
Boost inductor L_1	100 μH
Filter inductor L_2	100 μH
Filter capacitor C_6	100 μF
Switching frequency ($Q_1 - Q_4$ & $S_1 - S_4$) f_{sw}	50 kHz
Switching frequency ($S_5 - S_8$)	100 kHz

Following expressions can be used to derive the key design parameters of the converter:

1) Leakage inductance of transformer L_{lk}

$$L_{lk} = \frac{n^2 V_c^2 \delta_{max}(1 - 2\delta_{max})}{2 f_{sw} P_{max}} \tag{13}$$

2) Transformer turns ratio

$$\frac{N_p}{N_s} = n = \frac{V_{bat}(1 - D_{LV_{max}})}{2V_c} \tag{14}$$

3) Boost inductor L_1

$$L_1 = \frac{V_{bat}(nV_c - V_{bat})}{4\Delta i_{L1} f_{sw}(nV_c - 2V_{bat})} \tag{15}$$

4) Filter inductor L_2

$$L_2 = \frac{2V_c D_{HV}(1 - D_{HV})}{4\Delta i_o f_{sw}} \tag{16}$$

5) Filter capacitor C_6

$$C_6 = \frac{V_{inv}(1 - D_{HV})D_{HV}}{64 L_2 \Delta V_{inv} f_{sw}^2} \tag{17}$$

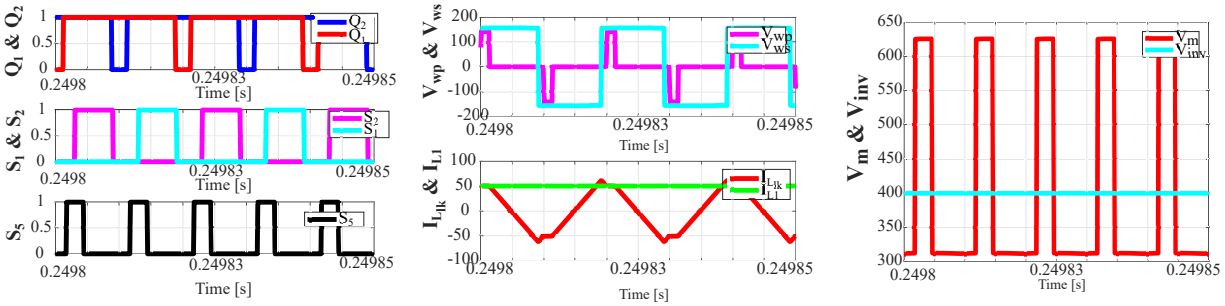
The designed parameters used in the simulation are listed in Table I.

IV. Simulation Results

The converter performance is evaluated by simulation in MATLAB/Simulink environment with the design parameters listed in Table I. The model is simulated with BESS voltage V_{bat} maintained at 20V while the output voltage is regulated at 400V. The rated output power of the converter is 1 kW. Fig. 3(a)-3(c) show the modulation signals, transformer voltages and currents and the multilevel voltage waveform at full load. The various gating signals and transformer waveforms verify the modes of operation of the converter and proposed natural commutation of leakage inductor current.

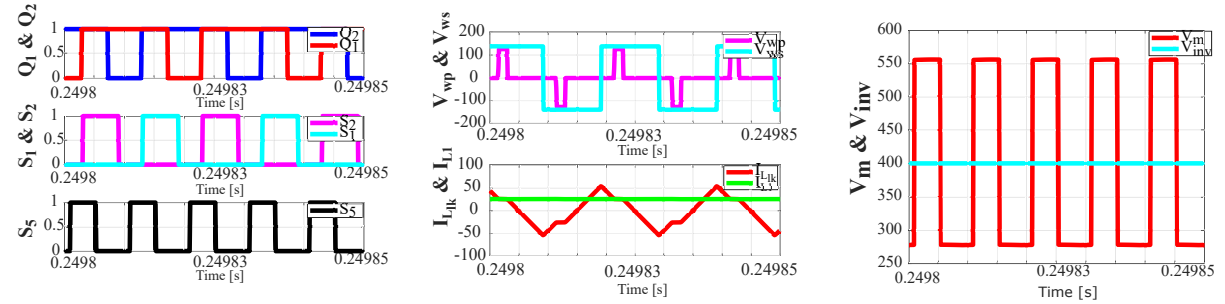
The simulation waveforms for 50% load 500W are shown in Fig. 4(a)-4(c). As seen from Fig. 4(a), the V_{inv} voltage regulation is achieved through the adjustment of the control parameters D_{LV} and D_{HV}. In addition, the effect of D_{HV} on voltage levels of V_m as described by (12) can also be verified by the comparison of Fig. 3(c) and Fig. 4(c).

The transformer voltage waveforms in Fig. 3(b) and Fig. 4(b) show that the W_s winding voltage stress due to



(a) Device gate pulses. (b) Transformer waveforms. (c) Multilevel and output voltages.

Fig. 3: Simulation results for converter at full load 1kW.



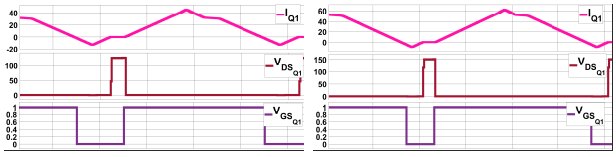
(a) Device gate pulses. (b) Transformer waveforms. (c) Multilevel and output voltages.

Fig. 4: Simulation results for converter at half load 500W.

the reflected voltage from HV side is half of the output voltage (V_{inv}) due to the doubler structure on the HV side. As mentioned in Section III, the leakage inductor design is dependent on the maximum power transfer capability and sensitive to phase shift between LV and HV side devices. The modulation of the intermediary switch (S_5/S_6) alleviates this issue.

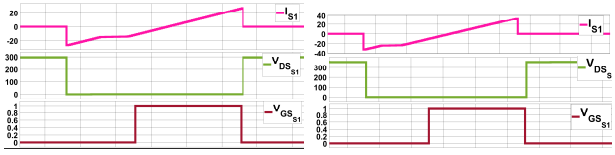
The proposed converter modulation scheme achieves zero current soft turn-off for the full-bridge devices Q_1-Q_4 and zero voltage turn-on for the half-bridge devices S_1-S_4. The zero current turn-off for Q_1 at full and half loads has been shown in Fig. 5(a) and Fig. 5(b), respectively. Fig. 6(a) and Fig. 6(b) show ZVS turn-on for switch S_1 at half and full loads, respectively. As evident from Fig. 5 and Fig. 6, the designed converter achieves soft switching over a wide load range.

Simulation results for the converter operating in battery charging mode (grid-to-battery) are shown in Fig. 7. The proposed converter's operation in this mode employs phase-shift power transfer principle. The switches S_1 and S_3 are given identical gate pulses and are complimentary to switches S_2 and S_4. The device pair Q_1 and Q_4 are given identical gate signals which are phase shifted w.r.t S_1 to control the power transfer. A suitable



(a) Half rated load (b) Full load

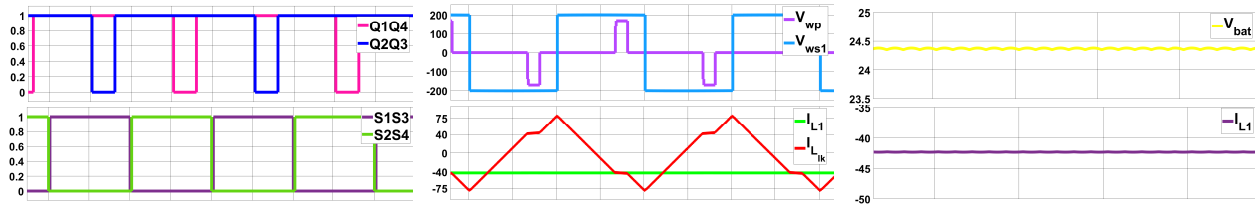
Fig. 5: ZCS turn-off for Q_1



(a) Half rated load (b) Full load

Fig. 6: ZVS turn-on for S_1

overlap period between the conduction of the pair of switches Q_1, Q_4 and Q_2, Q_3 is implemented for the natural commutation of the leakage inductor current. The gate pulses for various switches are shown in Fig. 7(a). Corresponding transformer waveforms are shown in Fig. 7(b). The battery voltage and current to achieve 1kW



(a) Device gate pulses. (b) Transformer waveforms. (c) battery voltage and current.

Fig. 7: Simulation results for converter at full load (1kw) in battery charging mode.

charging power have been shown in Fig. 7(c).

V. Conclusion

A current-fed multilevel dc-dc converter is presented in this paper. Detailed modal analysis has been presented along with the detailed design guidelines. The converter operation is evaluated by elaborate simulation results at the rated and 50% rated load. The proposed converter achieves high voltage gain in battery discharging mode. In addition, the converter also features multilevel output at HV ports which reduces the filter sizing. The proposed solution also provides additional voltage control in the form of the intermediary device duty cycle. This degree of freedom is beneficial in the optimal leakage inductor design of the high frequency transformer. The battery charging operation further justifies the suitability of the proposed dc-dc converter for energy storage application.

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