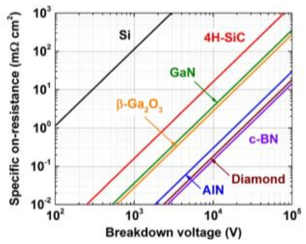
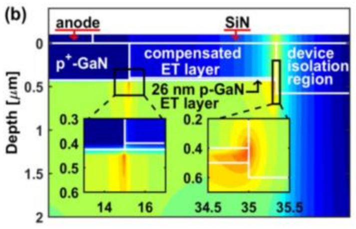
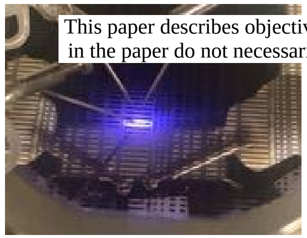
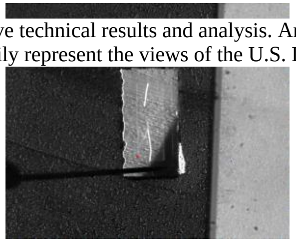
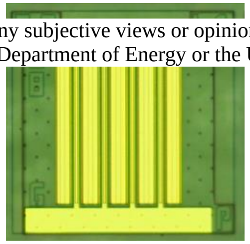






This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.





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U.S. NAVAL RESEARCH LABORATORY

Vertical GaN Power Electronics – Opportunities and Challenges

APS physics MARCH MEETING 2021 MARCH 15-19 ONLINE

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March 18, 2021

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Outline

- Overview of WBG Power Electronics
- Medium-Voltage Vertical GaN Devices
  - PN Diodes
- Vertical GaN Devices for Electric Vehicles
  - JBS Diodes and MOSFETs

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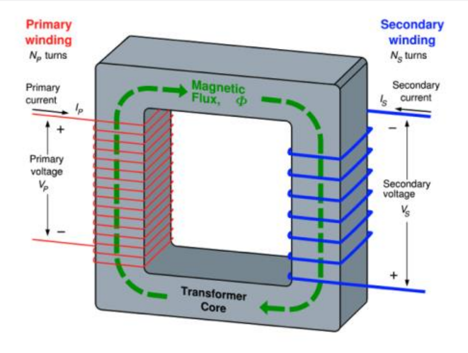
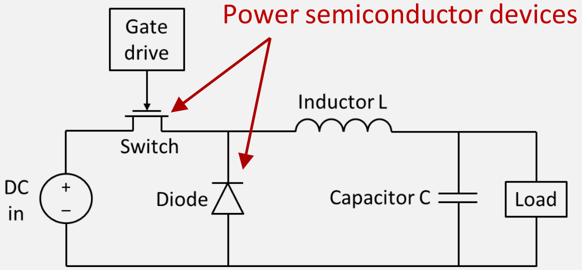
What Are Power Electronics?

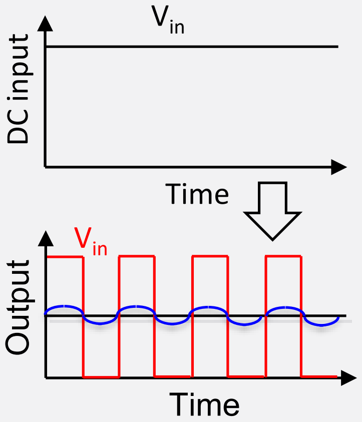
***Power electronics*: Application of solid-state electronics for routing, control, and conversion of electrical power**

Passive transformers (dumb)



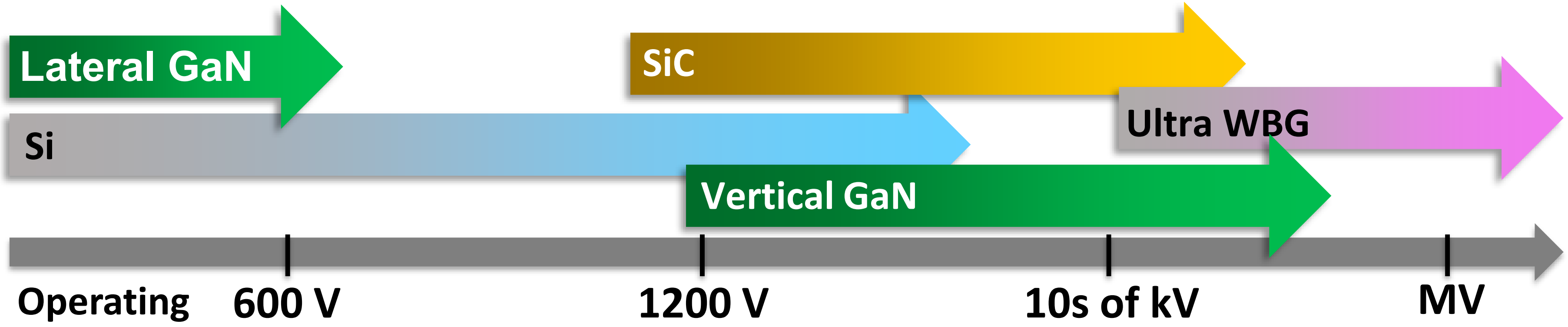
Power Electronics – active switching (smart)





- **Current power electronics are limited by the properties of Silicon semiconductor devices**
- **New system capabilities are enabled by:**
  - **Higher switching frequency (enables better SWaP)**
  - **Lower power loss**
  - **Higher temperature operation**
- ***Motivation for WBG/UWBG semiconductors***

Power Electronics for Energy Efficiency



Motor drives
Electric vehicles

- Reduce or eliminate passive components (capacitors, inductors)
- Spectral purity extends motor lifetime
- Operate at higher temperatures without liquid cooling

PV inverters

- Higher voltages, lower resistive losses

Electric distribution
Grid energy storage
Electric rail
Electric aviation

- AC subsystems to 13.8 kV

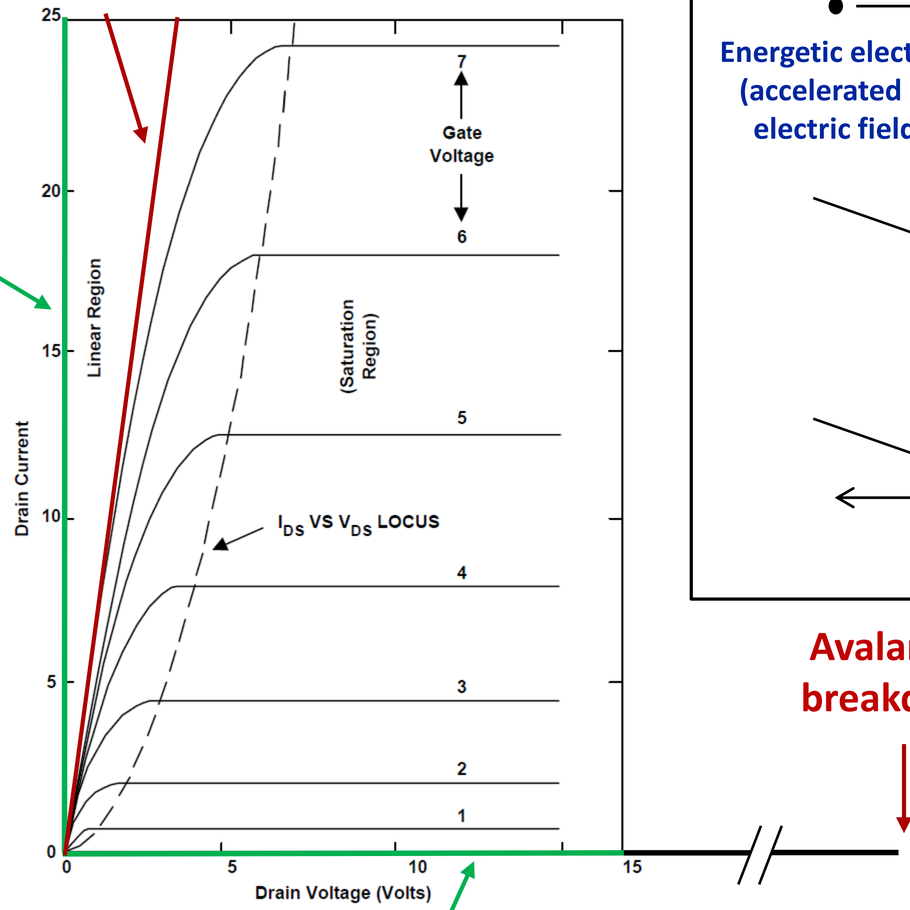
HV-DC transmission

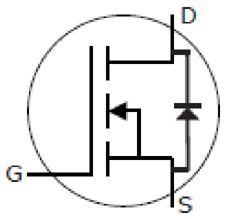
- Increase grid resiliency
- Less resistive energy loss
- Replace expensive IGBT / Thyristor stacks

Power Electronic Devices and Circuits

1/slope = On-resistance

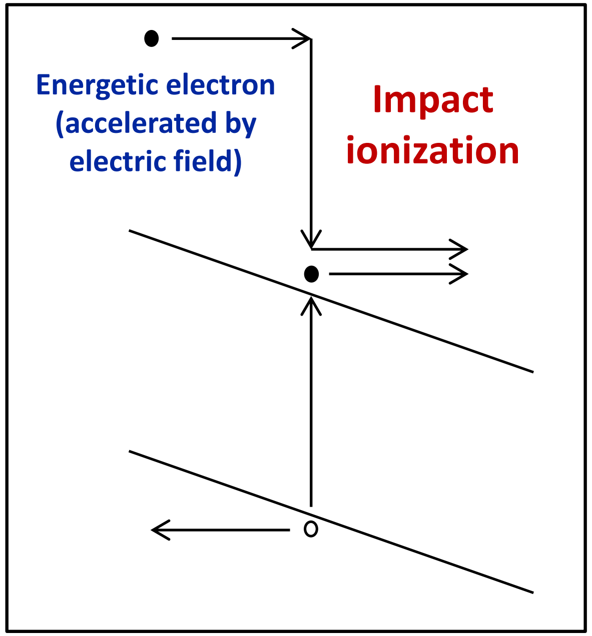
Ideal switch on-state





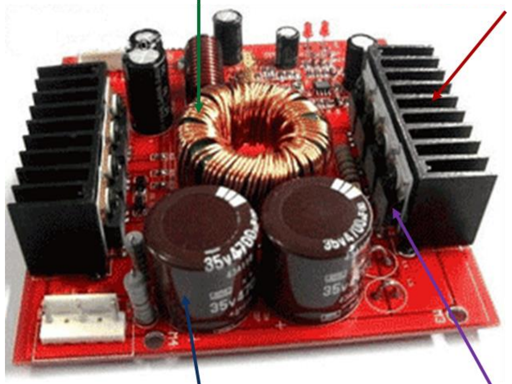
Ideal switch off-state

Avalanche breakdown



Magnetics

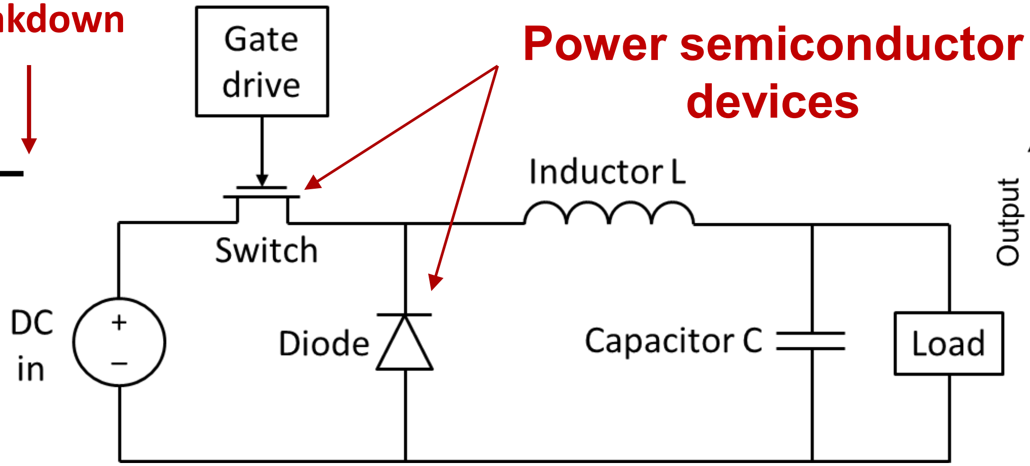
Thermal management

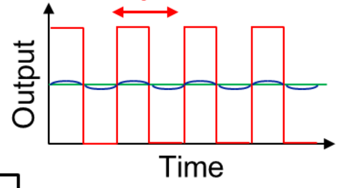


Capacitors

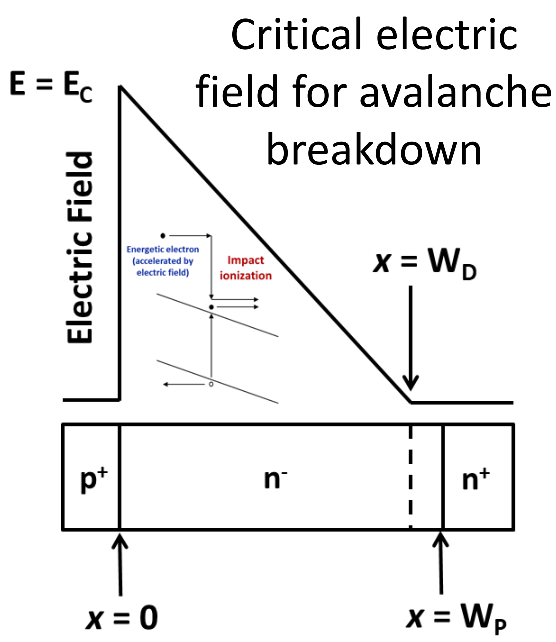
Semiconductor switches

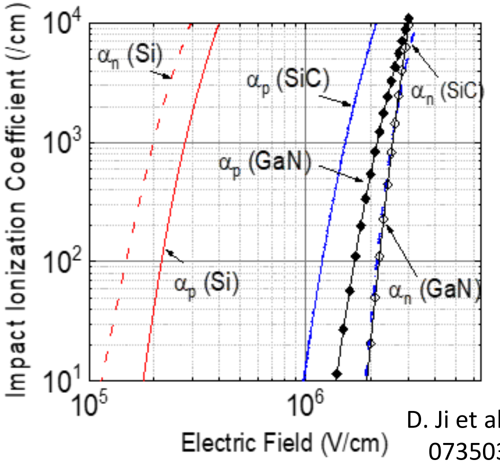
Power semiconductor devices





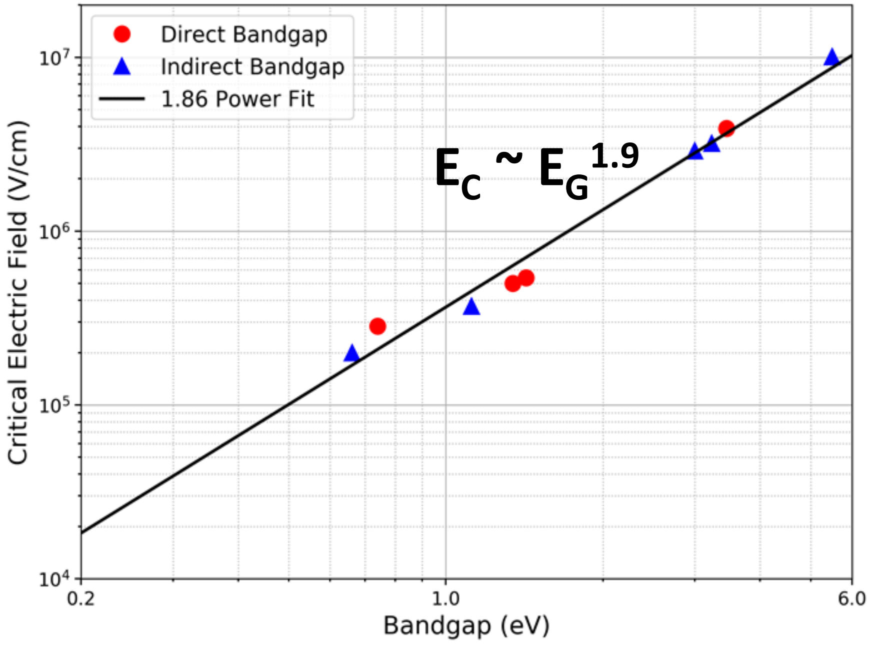
Advantages of WBG/UWBG Semiconductors

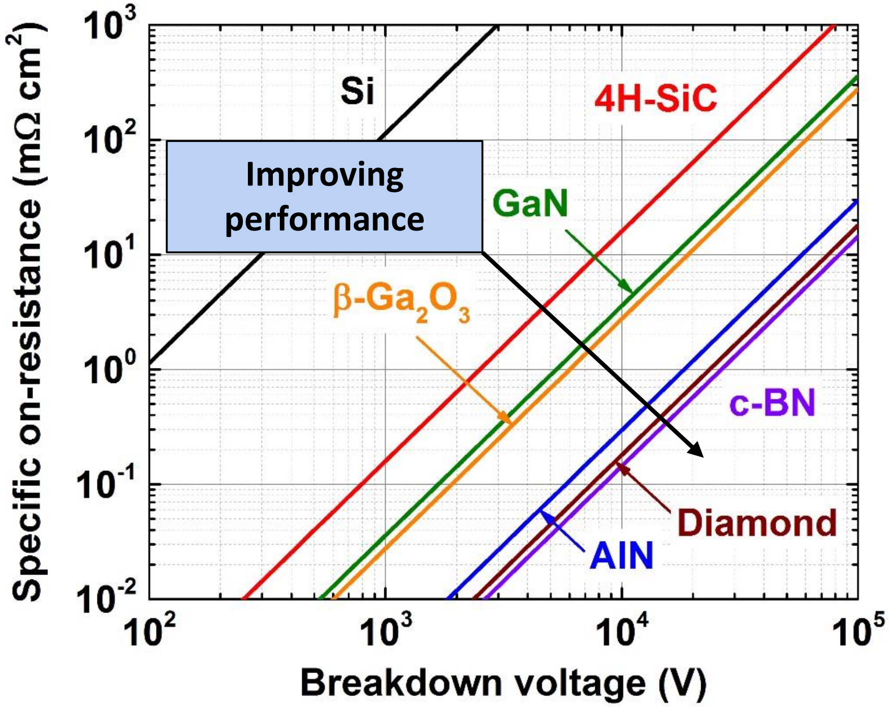




Impact ionization coefficients

D. Ji et al., APL **115** 073503 (2019)





Vertical device:

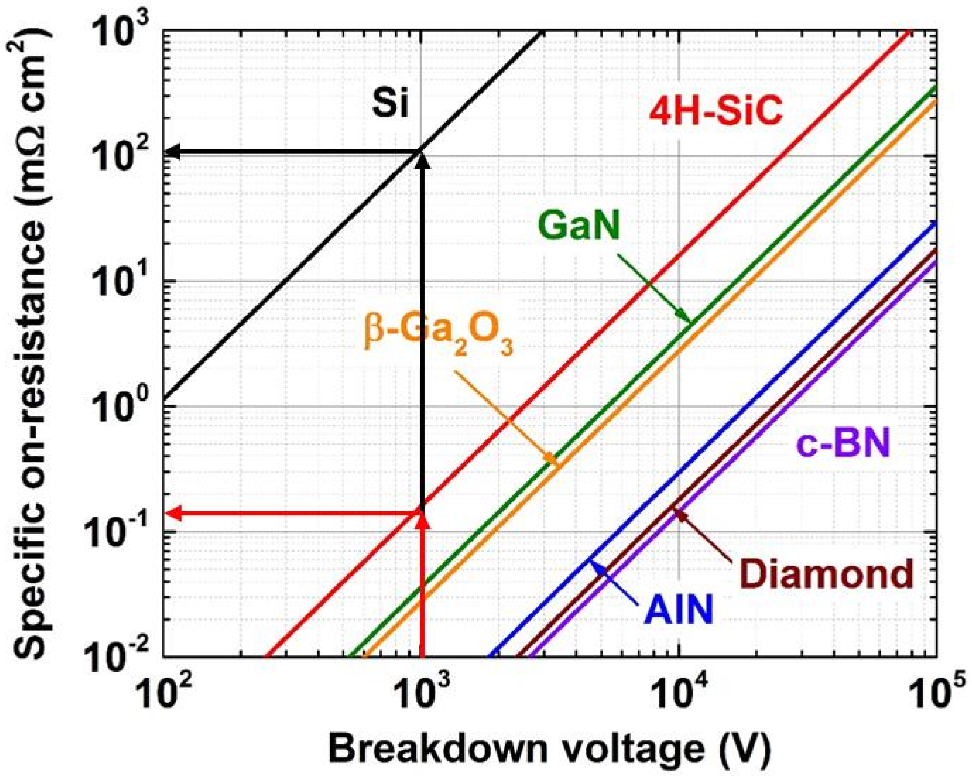
$$\mathrm{UFOM} = V_B^2/R_{on,sp} = \varepsilon\mu_n E_C^3/4$$

Lateral device:

$$\mathrm{LFOM} = V_B^2/R_{on,sp} = q\mu_{ch} n_s E_C^2$$

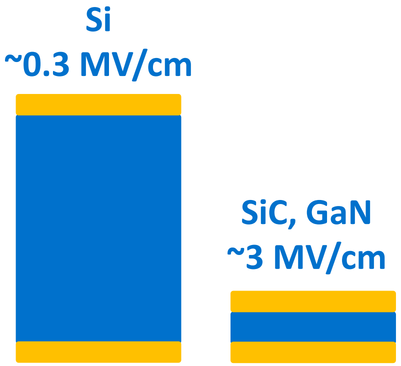
Kaplar et al., *ECS* (2019); J. Y. Tsao et al., *Adv. Elec. Mat. Adv. Elec. Mat.* 4, 1600501 (2018)

Scaling of WBG/UWBG Power Devices

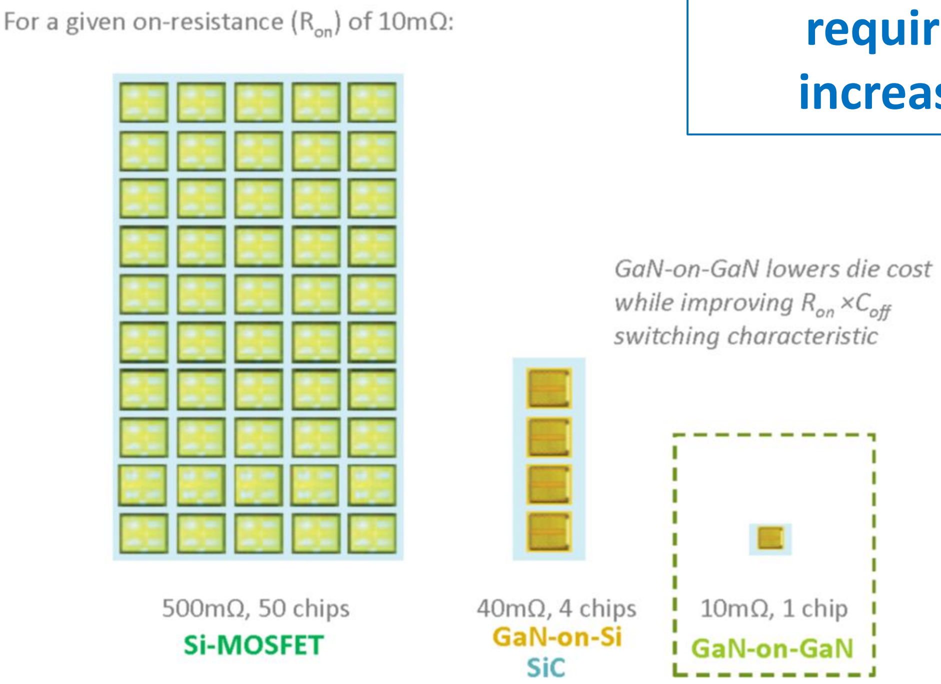


The scaling that results from the properties of WBG and UWBG materials can be utilized to optimize for switching frequency, conduction loss, and switching loss

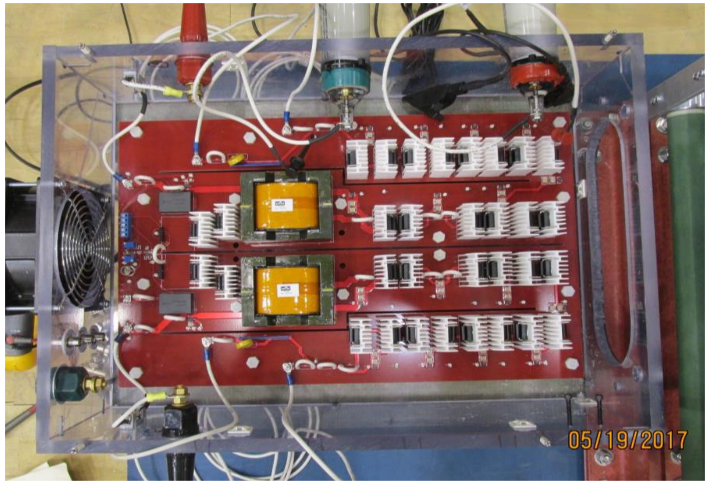
- For equivalent breakdown voltage, get lower $R_{on}A$ for (U)WBG device
  - For same R_{on}, (U)WBG device can have *smaller area*
  - Smaller area results in *less capacitance*
  - Gives a *faster switching transient* and *lower loss per switching cycle*



Thinner drift layers required for increasing E_C



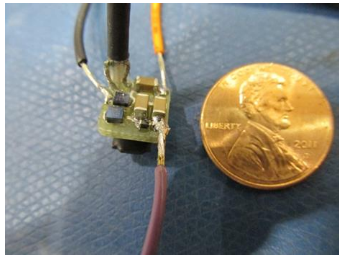
Improvements in Converter Power Density



SNL SiC hybrid switched-capacitor boost converter (ARPA-E)

- **First prototype: 0.5 kV → 10.1 kV (gain = 16.8) at 2.6 kW, 95.3% efficient, 410 in^3**
- **Second prototype: +2% efficiency, 55% volume**

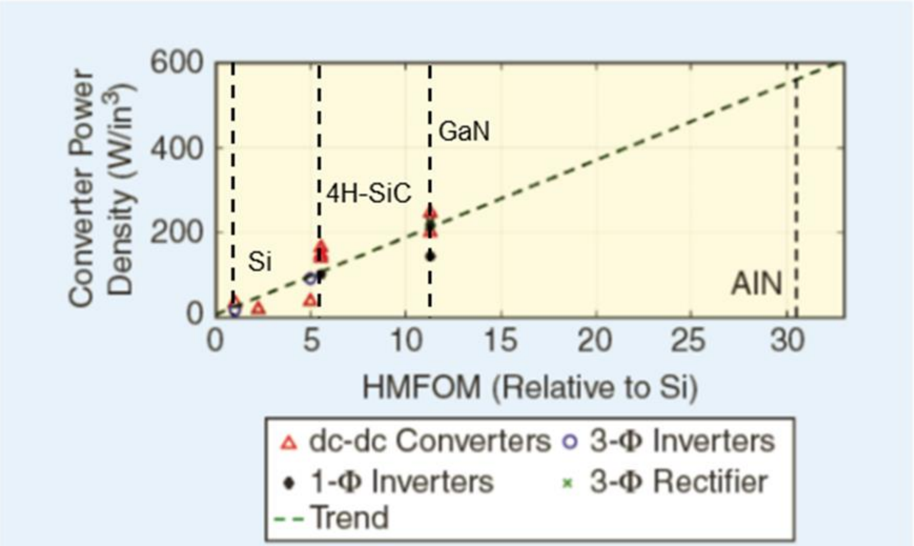
Over an order of magnitude improvement in power density is enabled by WBG and UWBG semiconductors compared to Si



SNL GaN HEMT "Coin Converter"
90 V, 90 mA → 215 W/in^3

SNL GaN HEMT microinverter
400 W in 2.4 in^3 → 167 W/in^3

SOA commercial microinverter
250 W in 59 in^3 → 4.2 W/in^3



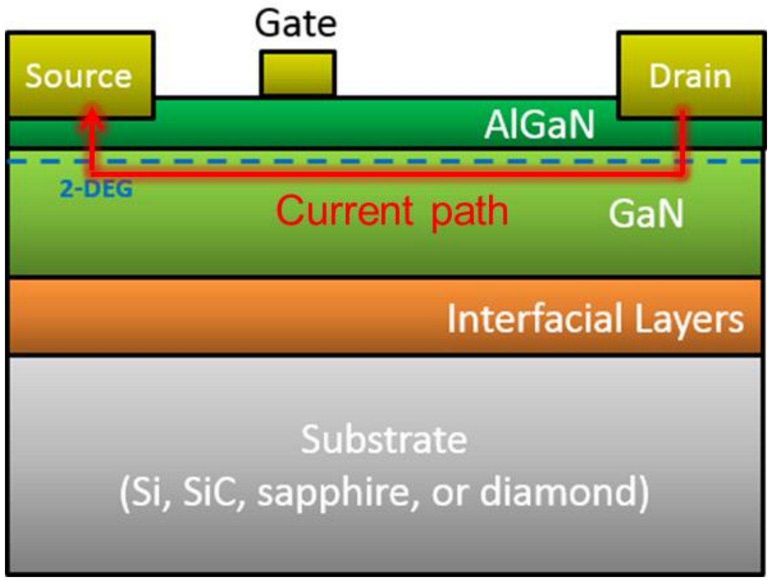
R. J. Kaplar, J. C. Neely, et al., *IEEE Power Electronics Magazine* (March 2017)

Relative Figures of Merit:

- **Vertical UFOM = $\varepsilon\mu_n E_C^3$**
- **Lateral LFOM = $q\mu_{ch} n_s E_C^2$**
- **Huang Material FOM = $E_C \mu_n^{1/2}$**
- ***HM-FOM seems to be a good predictor of power density in a variety of power converter types***

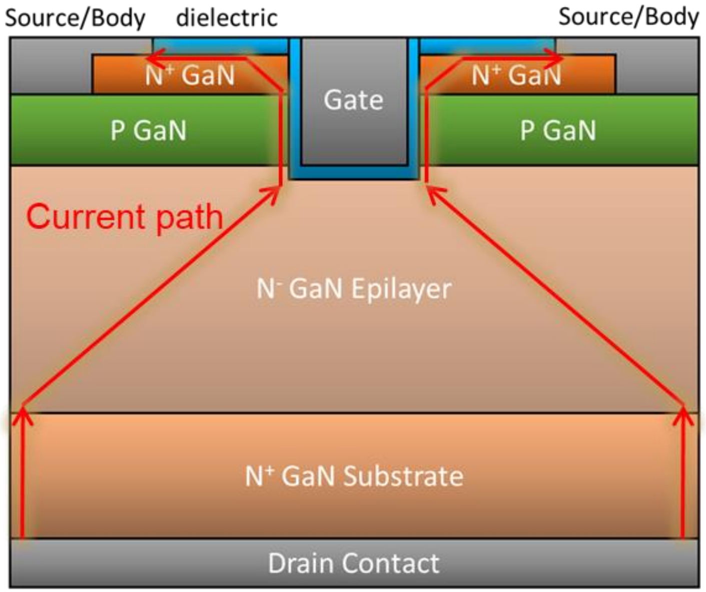
Lateral vs. Vertical GaN Power Devices

Lateral Current Flow (HEMT)



- Polarization-doped heterostructure
- High electron mobility in 2DEG for low R_{ON}
- High-frequency operation (up to ~1 MHz)
- Low blocking voltage (< ~650V, scales with area)
- Typically grown on foreign substrate
- Commercially available

Vertical Current Flow (Trench MOSFET)

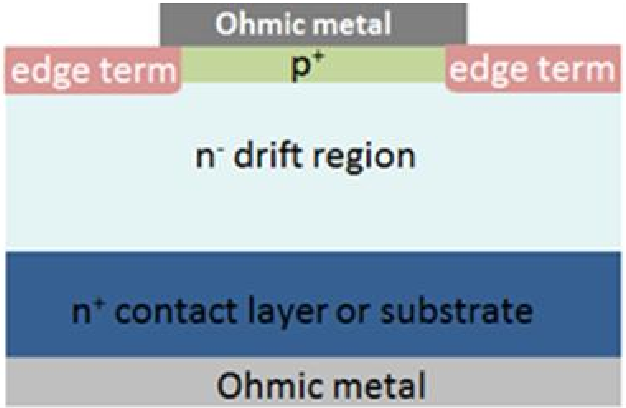


- Selective-area impurity doping required
- Mobility limited by channel
- Capable of large blocking voltages (> 1200 V, not dependent on area)
- Grown on native GaN substrates

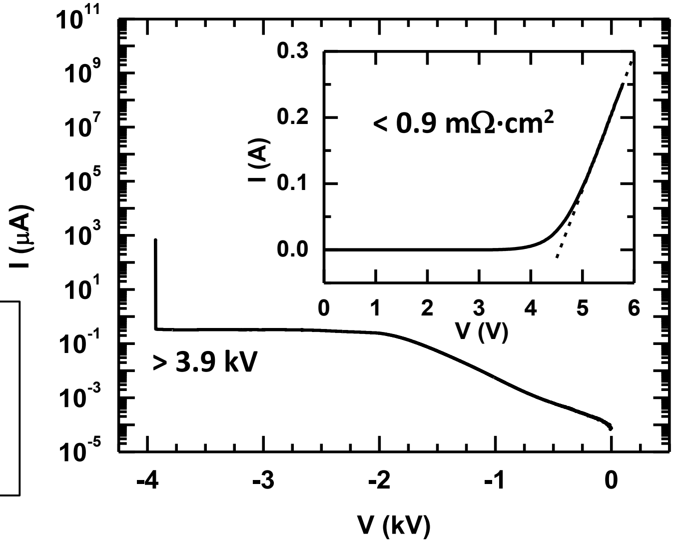
Outline

- Overview of WBG Power Electronics
- **Medium-Voltage Vertical GaN Devices**
  - **PN Diodes**
- Vertical GaN Devices for Electric Vehicles
  - JBS Diodes and MOSFETs

Overview of Vertical GaN Technology

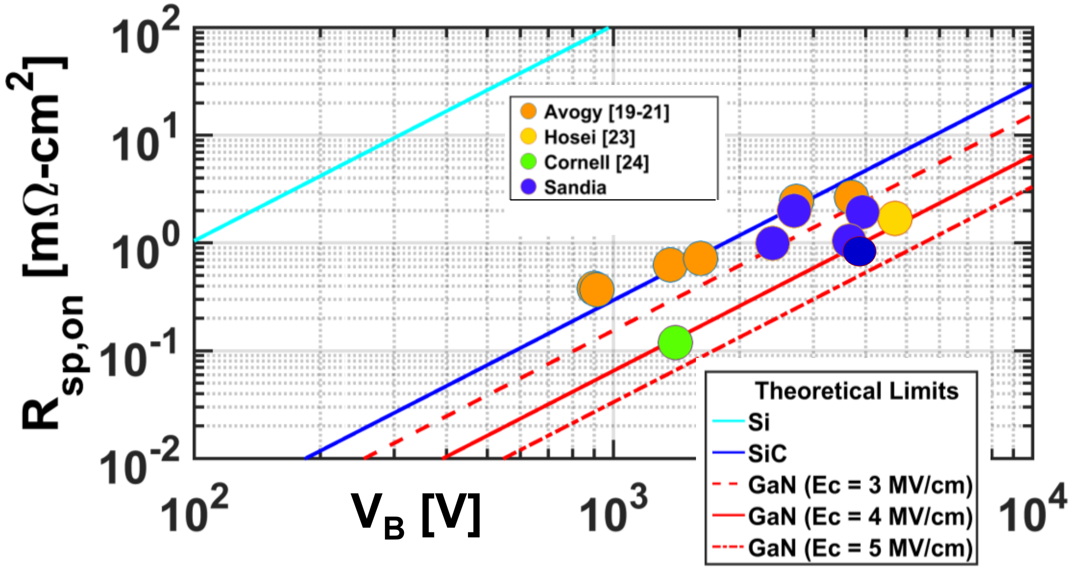


Breakdown is due to avalanche!



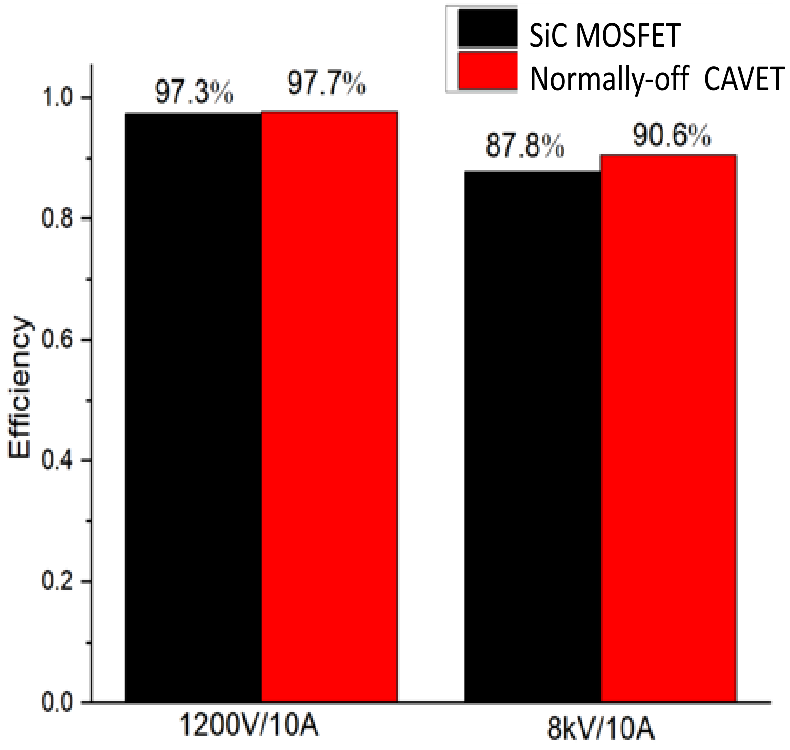
A. Armstrong et al., Elec. Lett. 52(13), 1170 (2016)

- Need to extend the limits of vertical GaN power device technology for medium-voltage applications (~1.2-20 kV)
  - Need to increase V_B by 4x from today's SOA
  - Challenges: Thick drift region, low net doping, edge termination
- Need to establish a domestic foundry process for vertical GaN power devices



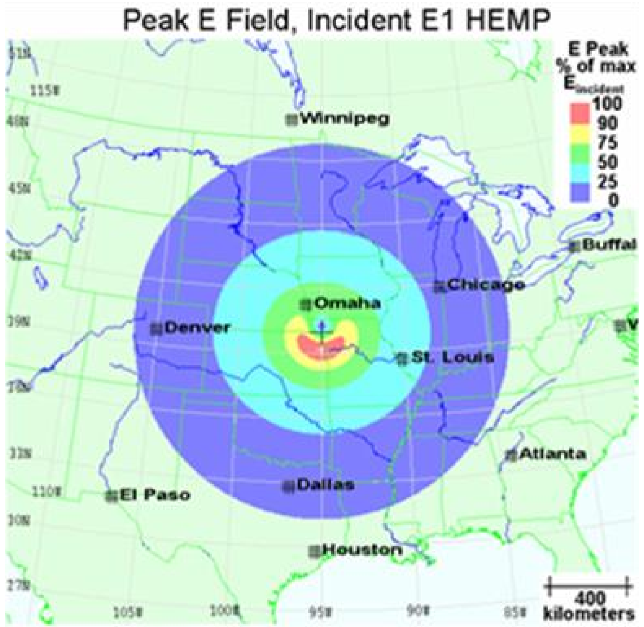
Vertical GaN Advantages for MV Power Electronics

- Critical field of GaN ~2.8 MV/cm at $N_D = 1\times10^{16}$ cm^{-3} and room temperature based on most recent impact ionization measurements [1]
- Slightly higher than E_C of SiC at the same temperature and doping [2]
- But higher mobility of GaN ~1200 cm^2/Vs [3] compared to ~950 cm^2/Vs for SiC [2] at the same doping and temperature lead to improvements in power converter efficiency [4], ***particularly for medium-voltage devices (> 1.2 kV)***
- But devices are not widely available – ***a vertical GaN foundry is needed that monitors yield, reliability, etc.***

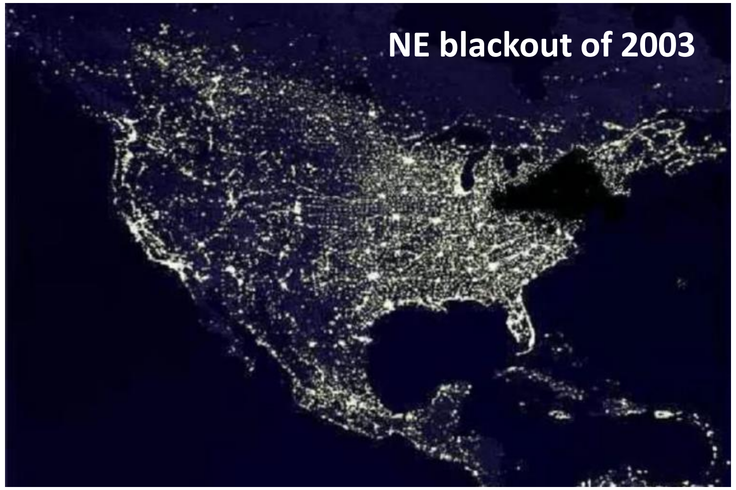


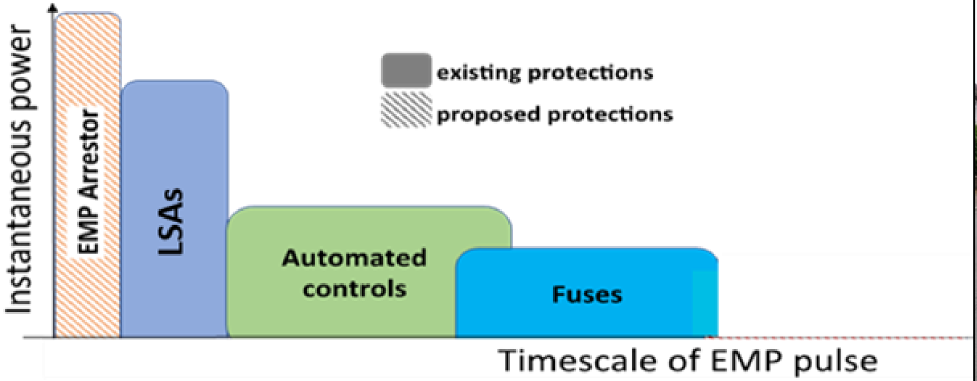
[1] D. Ji, B. Ercan, and S. Chowdhury, “Experimental Determination of Impact Ionization Coefficients of Electrons and Holes in Gallium Nitride Using Homojunction Structures,” *Appl. Phys. Lett.* **115**, 073503 (2019).
[2] J. A. Cooper and D. Morisette, “Performance Limits of Vertical Unipolar Power Devices in GaN and 4H-SiC,” *Elec. Dev. Lett.* **41**, 892 (2020).
[3] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, “Vertical Power PN Diodes Based on Bulk GaN,” IEEE Trans. Elec. Dev. 62(2), 414 (2015).
[4] D. Ji and S. Chowdhury, “On the Progress Made in GaN Vertical Device Technology – Special Issue on Wide Band Gap Semiconductor Electronics and Devices,” *Int. J. High-Speed Elec. Sys.* **28(01n02)**, 1940010 (2019).

Fast Protection for the Electric Grid



- Electromagnetic pulses are a threat to the grid
  - Very fast E1 component (< 1 μs)
  - Unaddressed by current SoA technology (LSAs)





- Transient protection is needed for MV grid-connected systems

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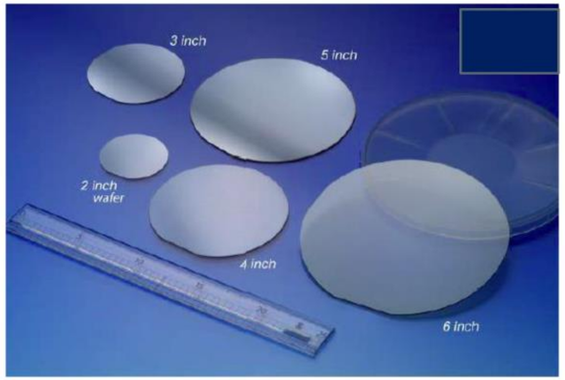
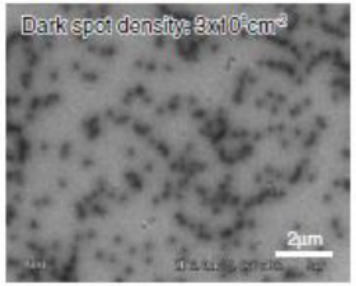
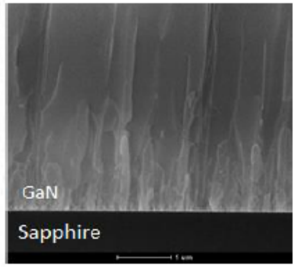
J. S. Foster Jr. et al., "Report of the Commission to Assess the Threat to the United States from Electromagnetic Pulse (EMP) Attack: Critical National Infrastructures," *Defense Technical Information Center* (2008).

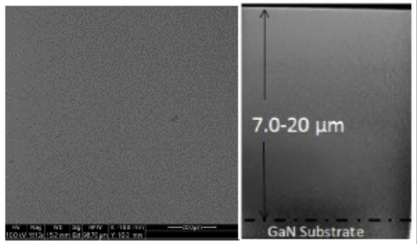
Native Substrates for Vertical GaN Devices

Attributes	GaN on Si	GaN on SiC	GaN on Bulk-GaN
Defect Density (cm^{-2})	10^9	$5x10^8$	10^3 to 10^6
Lattice Mismatch, %	17	3.5	0
CTE Mismatch, %	54	25	0
Layer Thickness (µm)	< 5	< 10	> 50
Breakdown Voltage (V)	< 1000	< 2000	> 5000
OFF State Leakage	High	High	Low
Device Types	Lateral	Lateral	Vertical and Lateral



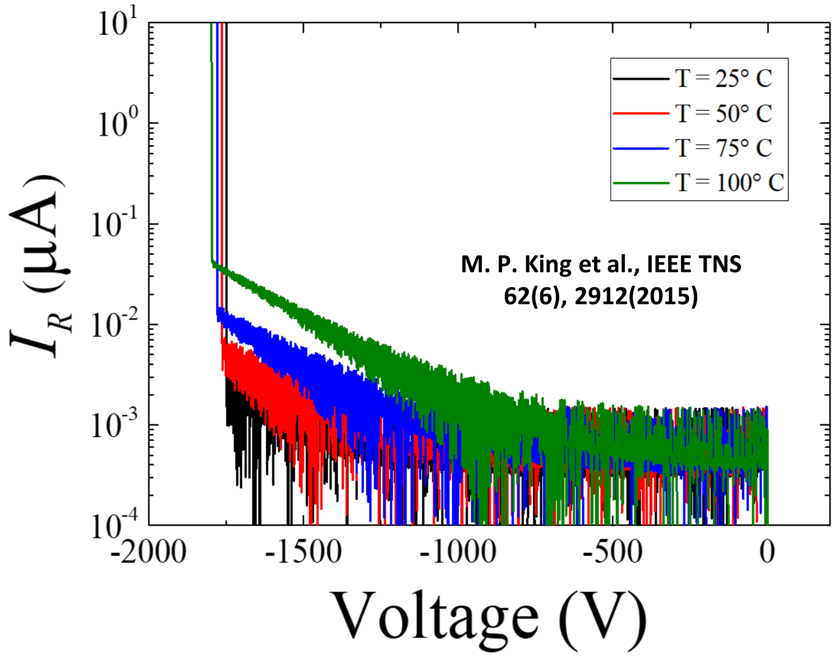


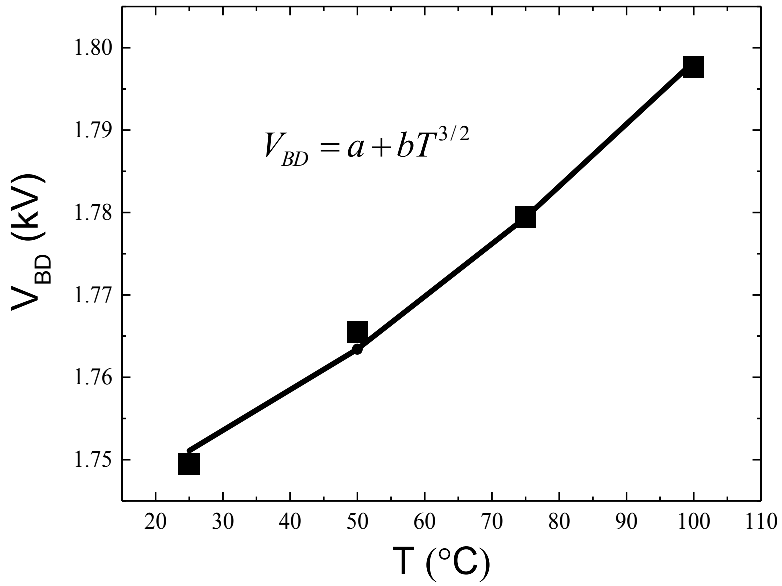


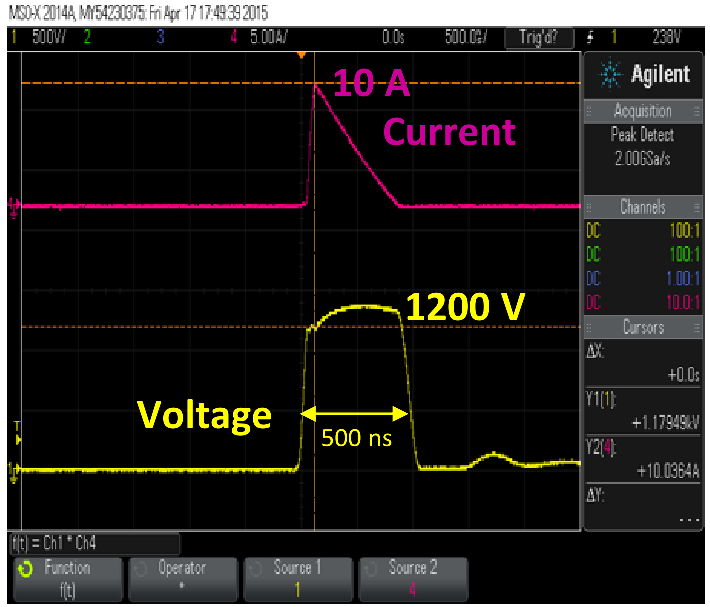


Avalanche Ruggedness of Vertical GaN

- **Avalanche breakdown mechanism demonstrated via temperature dependence**
- **Avalanche ruggedness demonstrated in real power switching circuits**
- ***Very different from the situation for GaN-on-Si power devices, where avalanche breakdown does not occur***







O. Aktas and I. C. Kizilyalli, IEEE EDL 36(9), 890 (2015)

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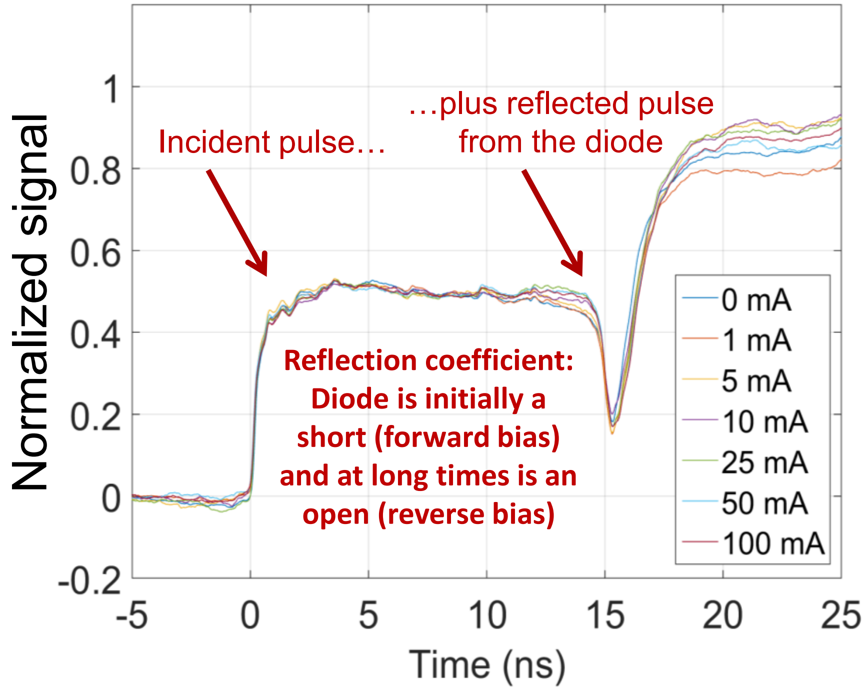
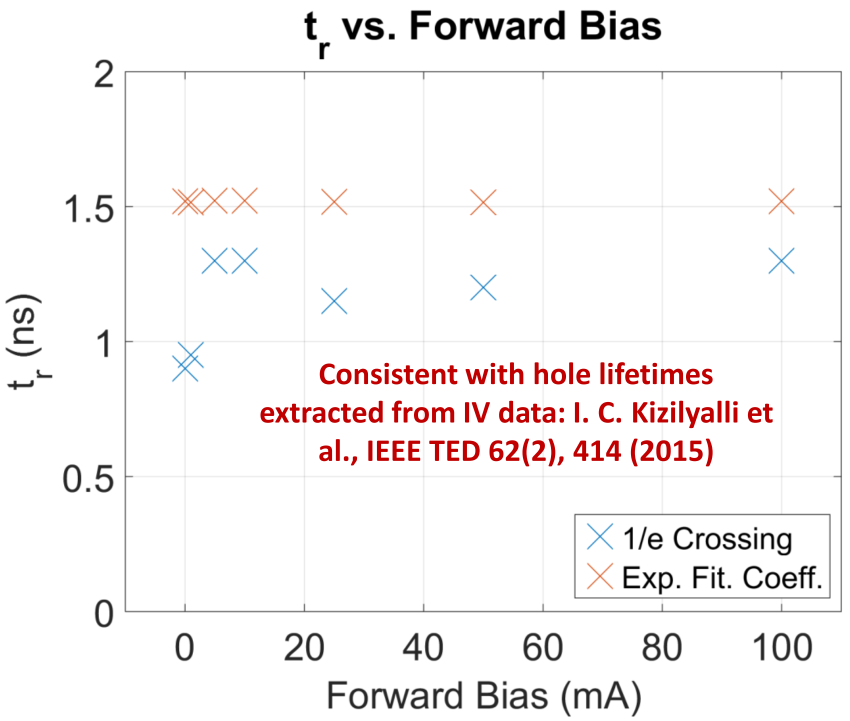
Carrier Transport in Vertical GaN

Reverse recovery measurements on vertical GaN diodes to determine carrier lifetime

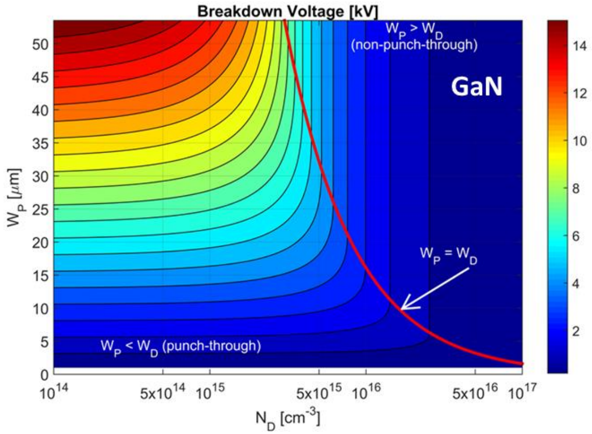
- **100 V reversing pulses used with various forward currents**
- **Reverse-recovery time is invariant to forward bias, implying t_r is limited by capacitance**
- **Measured times provide an upper limit for hole lifetime – $\tau_h \approx 2$ ns**





Edge Termination for Vertical GaN Diodes

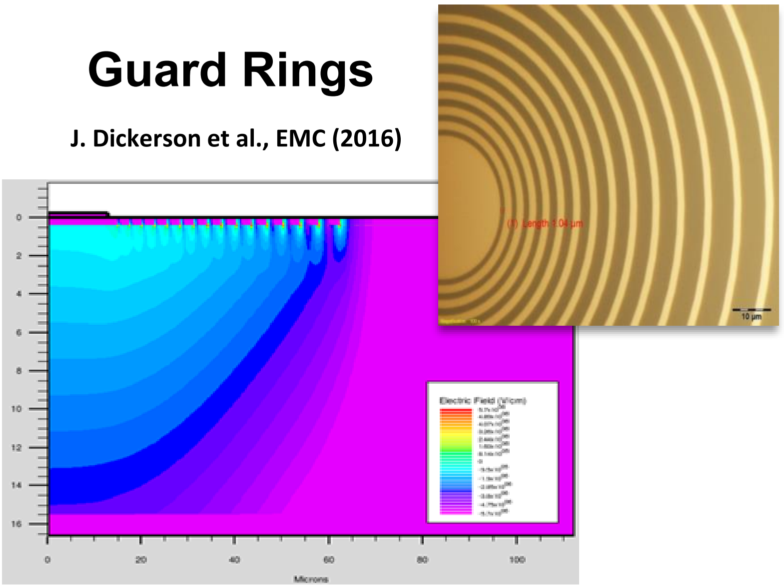
Ideal planar limit of GaN breakdown depends on drift layer thickness and doping:

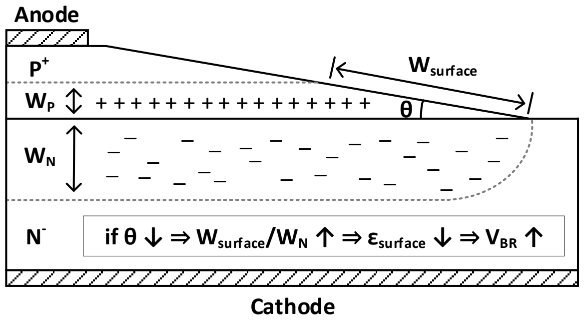


But premature breakdown will occur at the device surface, edge, etc. unless mitigations are taken to prevent this – edge termination

Guard Rings

J. Dickerson et al., EMC (2016)

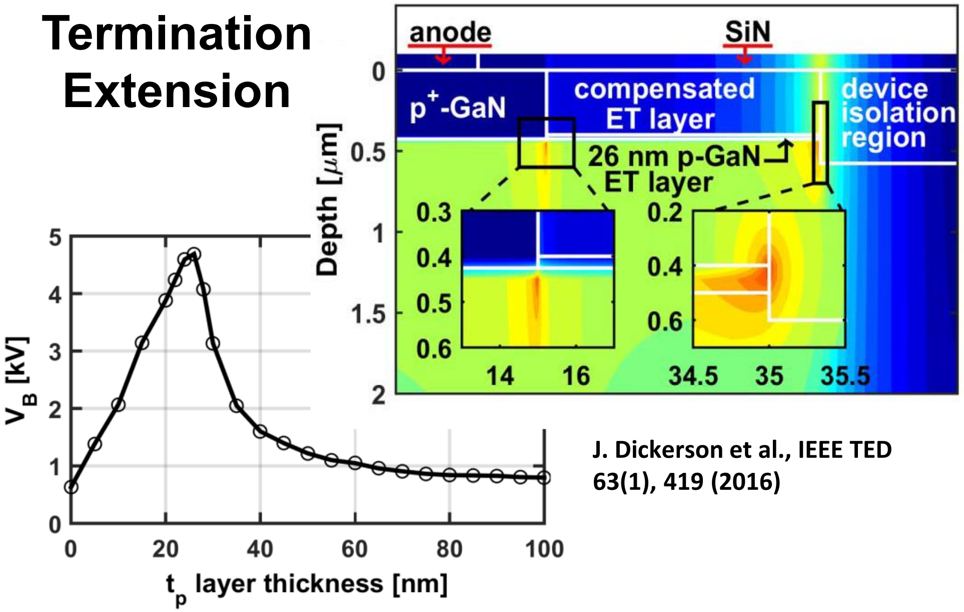




A. Binder et al., WiPDA (2019)

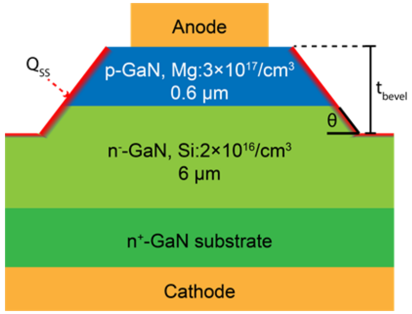
Various approaches to edge termination

Junction Termination Extension



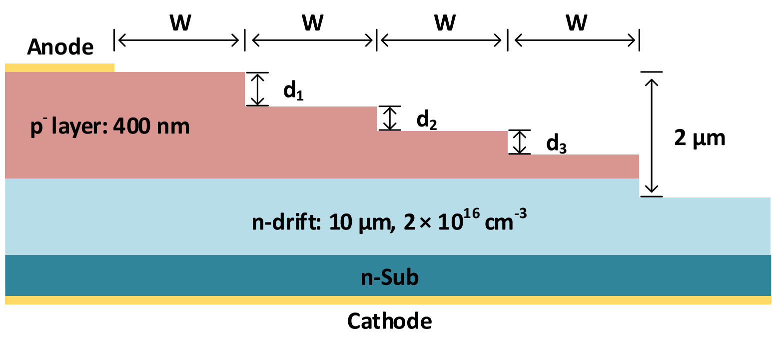
J. Dickerson et al., IEEE TED 63(1), 419 (2016)

Bevel

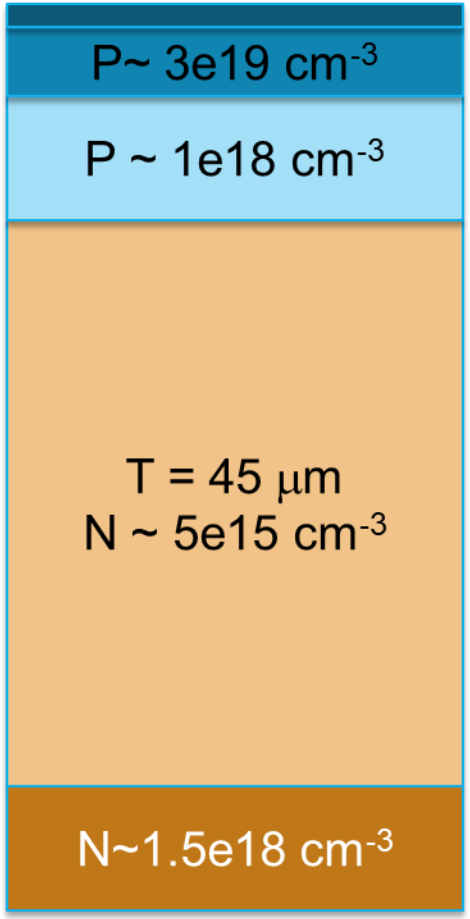


K. Zeng

Stepped JTE

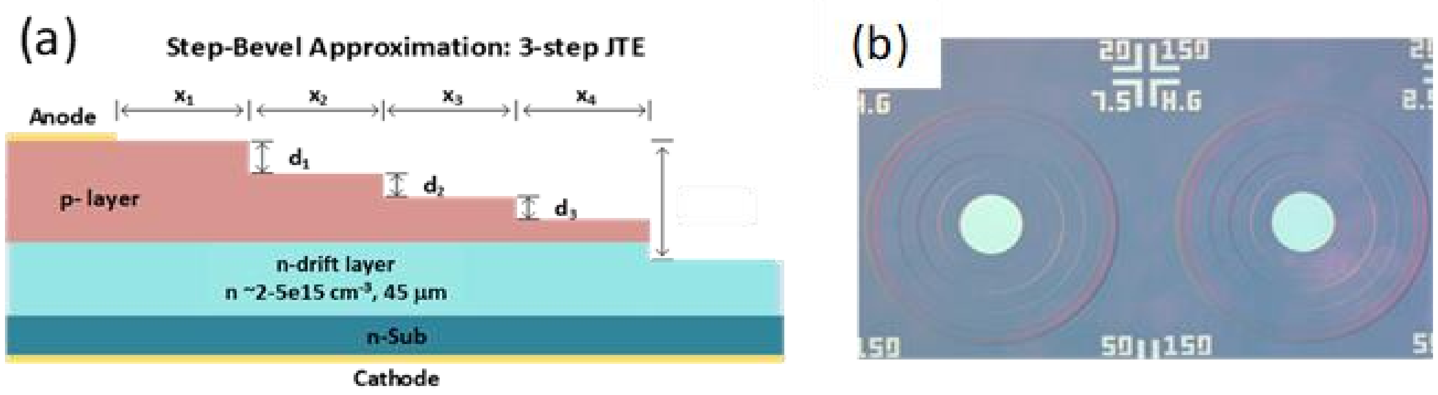


Fabrication of PN Diodes with Thick Drift Regions



C-V mapping confirmed highest reverse breakdown voltage devices from regions of wafer with drift region carrier density ~2.2-3.0×10^{15} cm^{-3}

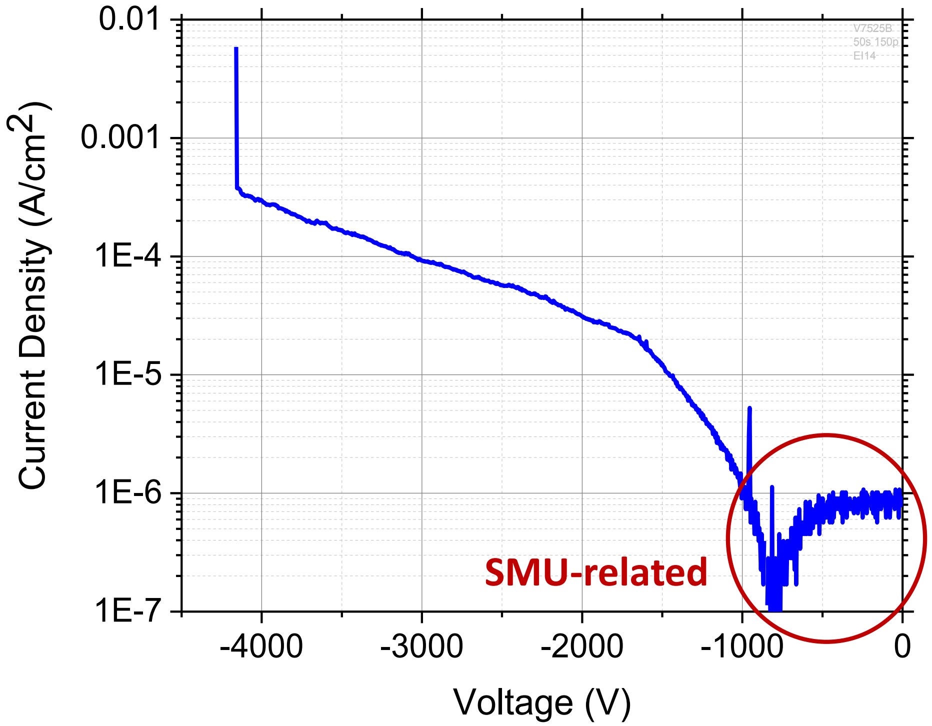
Edge termination: Multi-step ICP-etched JTE



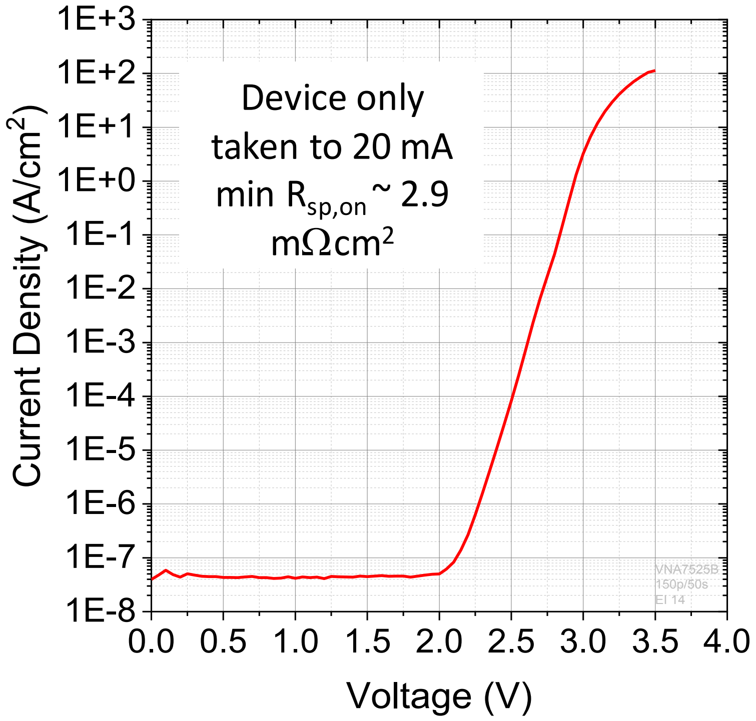
M. Crawford, A. Allerman, SNL

Performance of Medium-Voltage GaN Diodes

REVERSE I-V



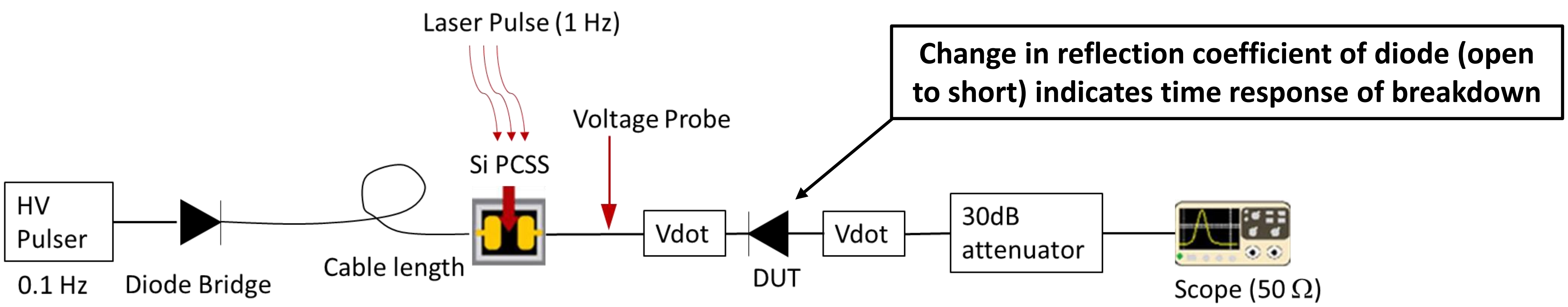
FORWARD I-V



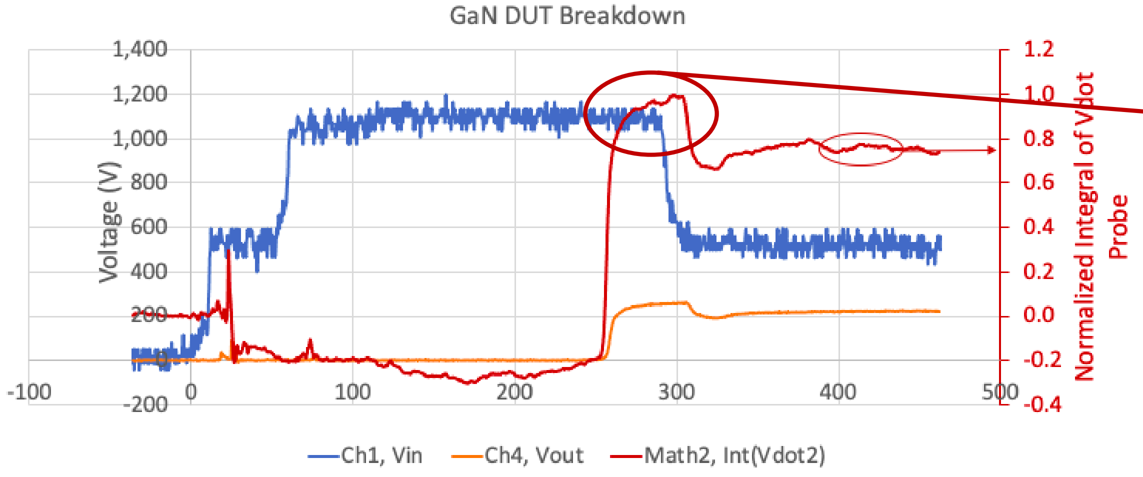
- **Best devices > 4 kV; estimate ~70% V_B of ideal planar diode**
- **Less than 1 mA/cm^2 leakage @ 80% V_B target**

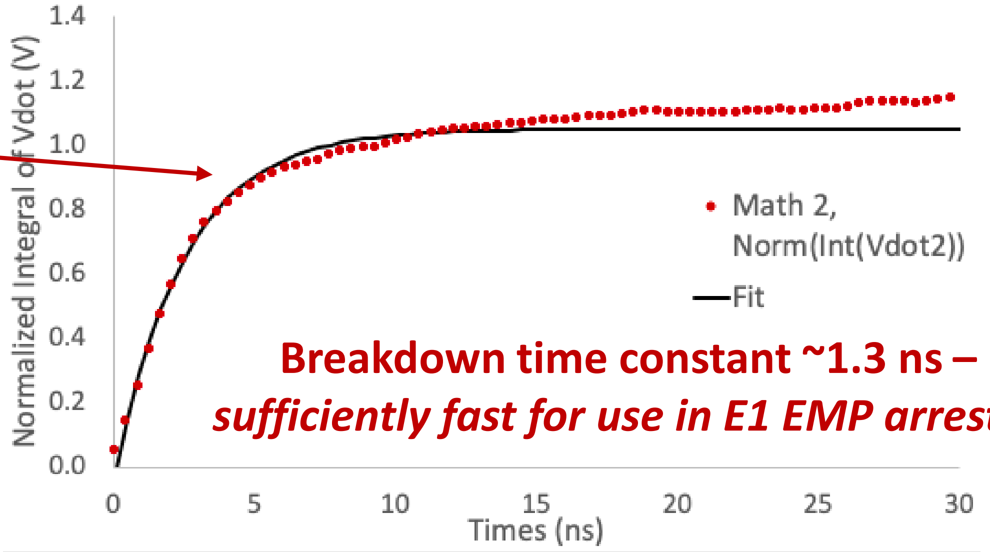
M. Crawford, A. Allerman, SNL

Time Response of GaN Avalanche Breakdown



Tested 1.2 kV vertical GaN diode



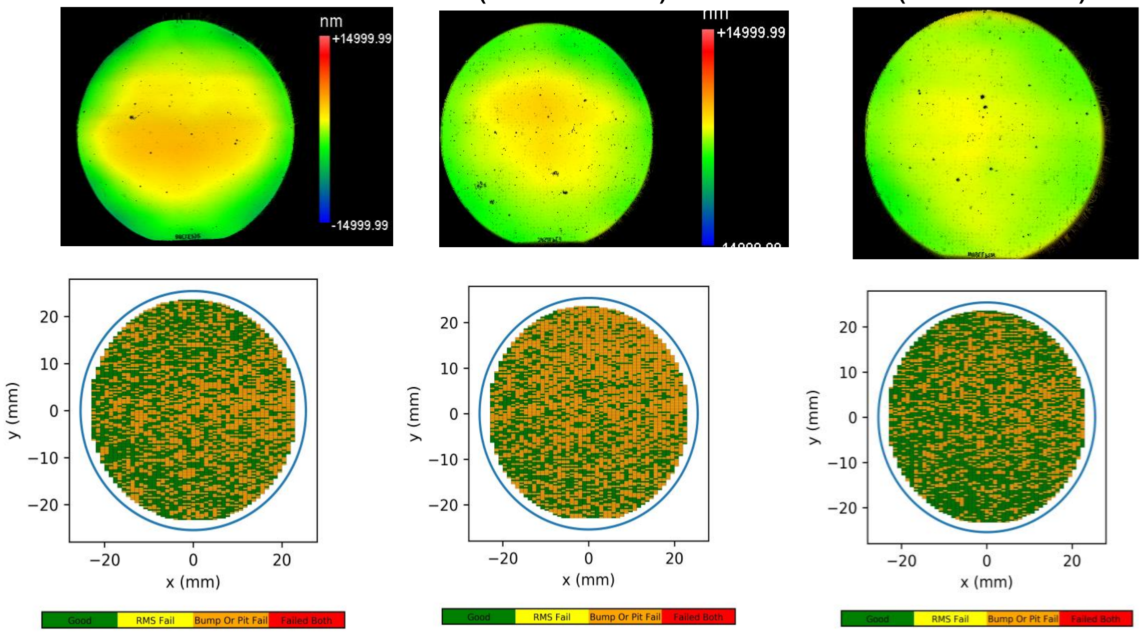


Breakdown time constant ~1.3 ns –
sufficiently fast for use in E1 EMP arrestor

J. Flicker, SNL

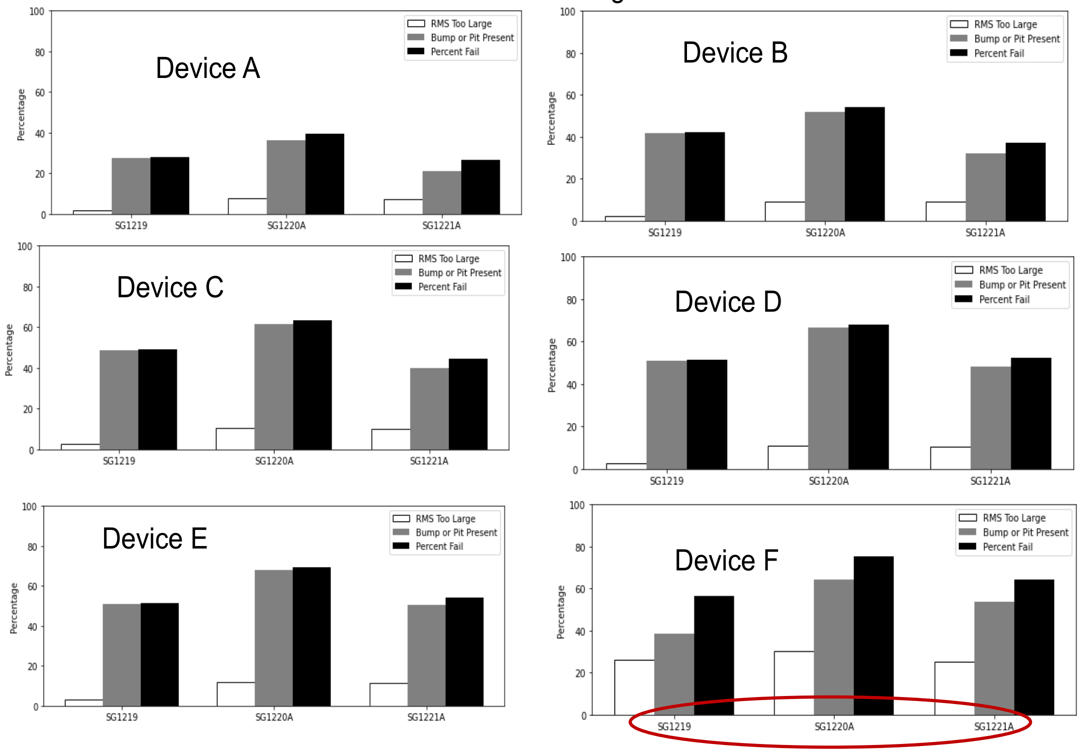
Vertical GaN Foundry Wafer Metrology

SG1219A (8um drift)	SG1220A (10um drift)	SG1221A (12um drift)



Good | RMS Fail | Bump/Pit Fail | Fail Both

Percent of devices meeting a "fail" criteria



Three wafers

- **Evaluate yield based on particles/pits and RMS roughness**
- **No clear trend in RMS roughness with drift layer thickness**
- **Evaluating yield for device geometries A-F**

Geometry	Area (mm^2)	Devices (per 2" wafer)
A	0.105	280
B	0.215	280
C	0.325	150
D	0.430	150
E	0.535	150
F	1.05	140
Total		1150

RMS Fail

Bump/Pit Fail

Overall Fail

T. Anderson, NRL

Sandia National Laboratories

U.S. NAVAL RESEARCH LABORATORY

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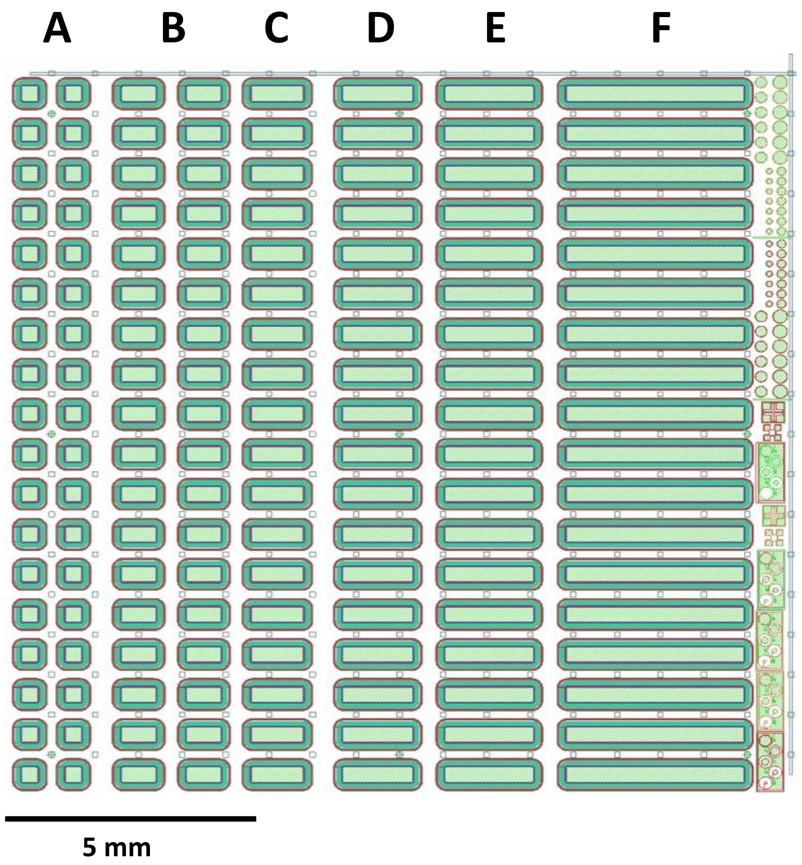
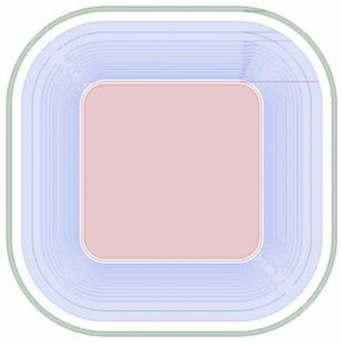
Foundry Mask Layout





Base cell:
0.35×0.35 mm² anode

Larger devices scaled only in *x*-direction to avoid crossing dot-cores (for now)

Geometry	Area (mm²)	Devices (per 2" wafer)
A	0.105	280
B	0.215	280
C	0.325	150
D	0.430	150
E	0.535	150
F	1.05	140
Total		1150

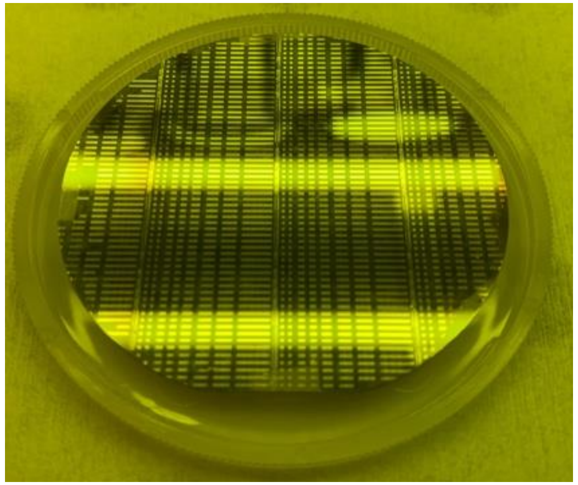
Features:

- Global alignment
- P-GaN ohmic CTLM
- P-GaN Hall
- Isolation test
- Termination test
- Small diameter circular diodes
- JTE and GR termination designs
- Passivation / overlay for packaging

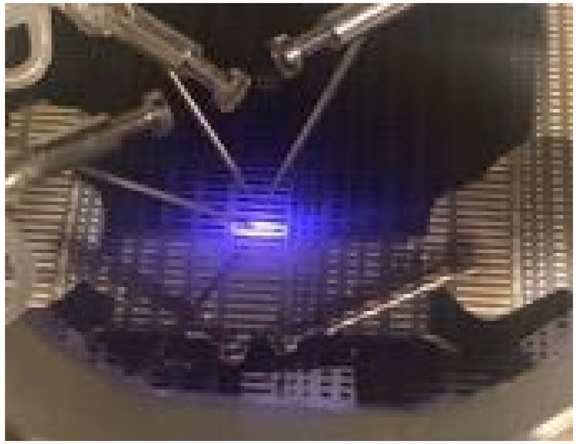
T. Anderson, NRL

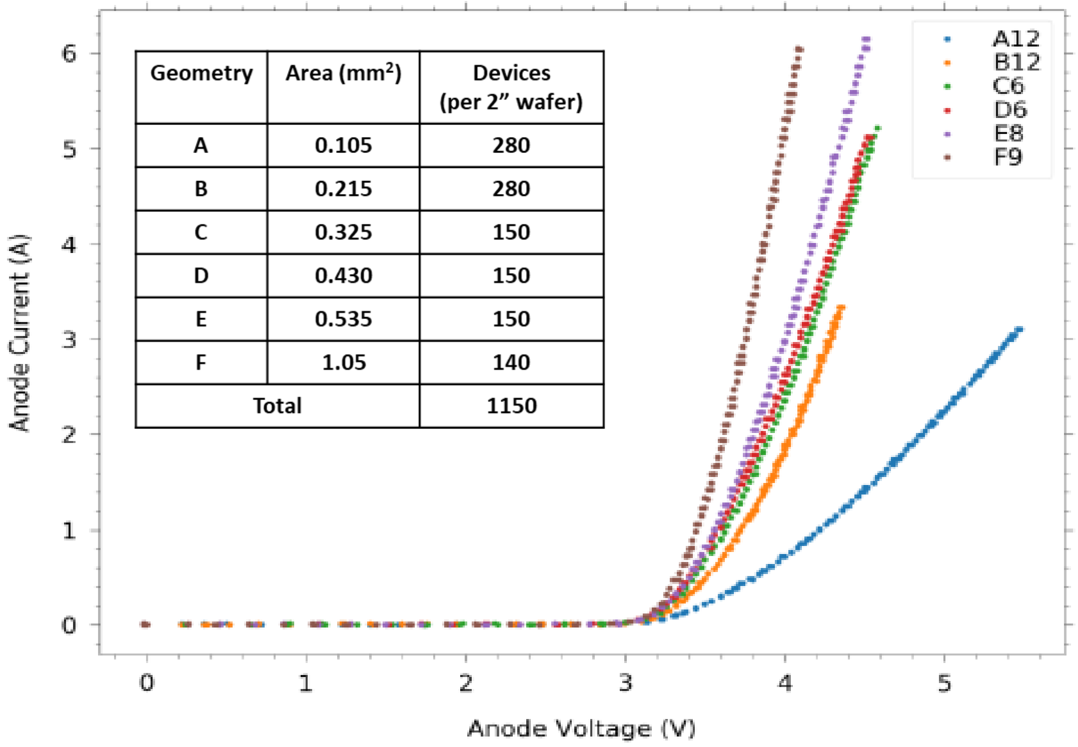
Foundry Electrical Testing

Typical foundry wafer



Wafer under test





Geometry	Area (mm²)	Devices (per 2" wafer)
A	0.105	280
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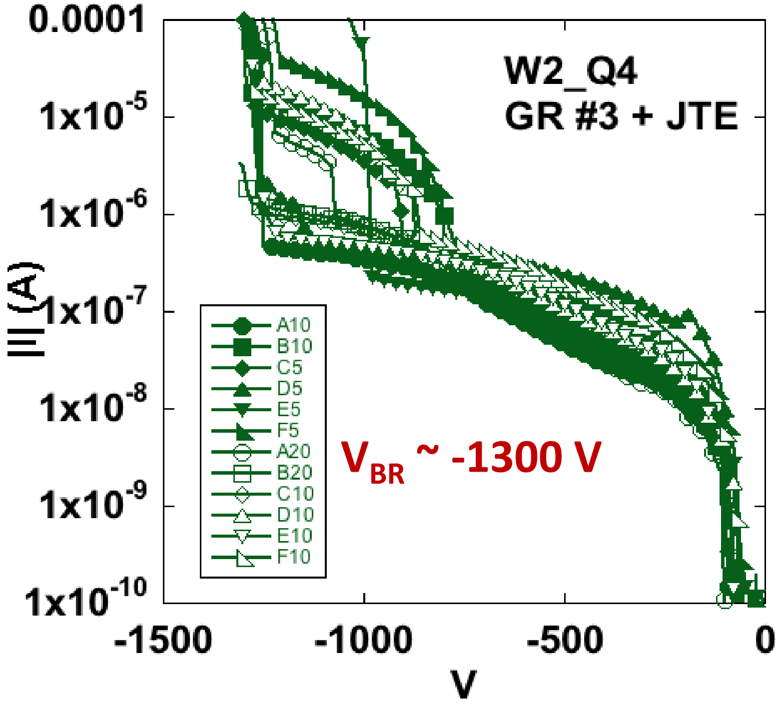
C	0.325	150
D	0.430	150
E	0.535	150
F	1.05	140
Total		1150

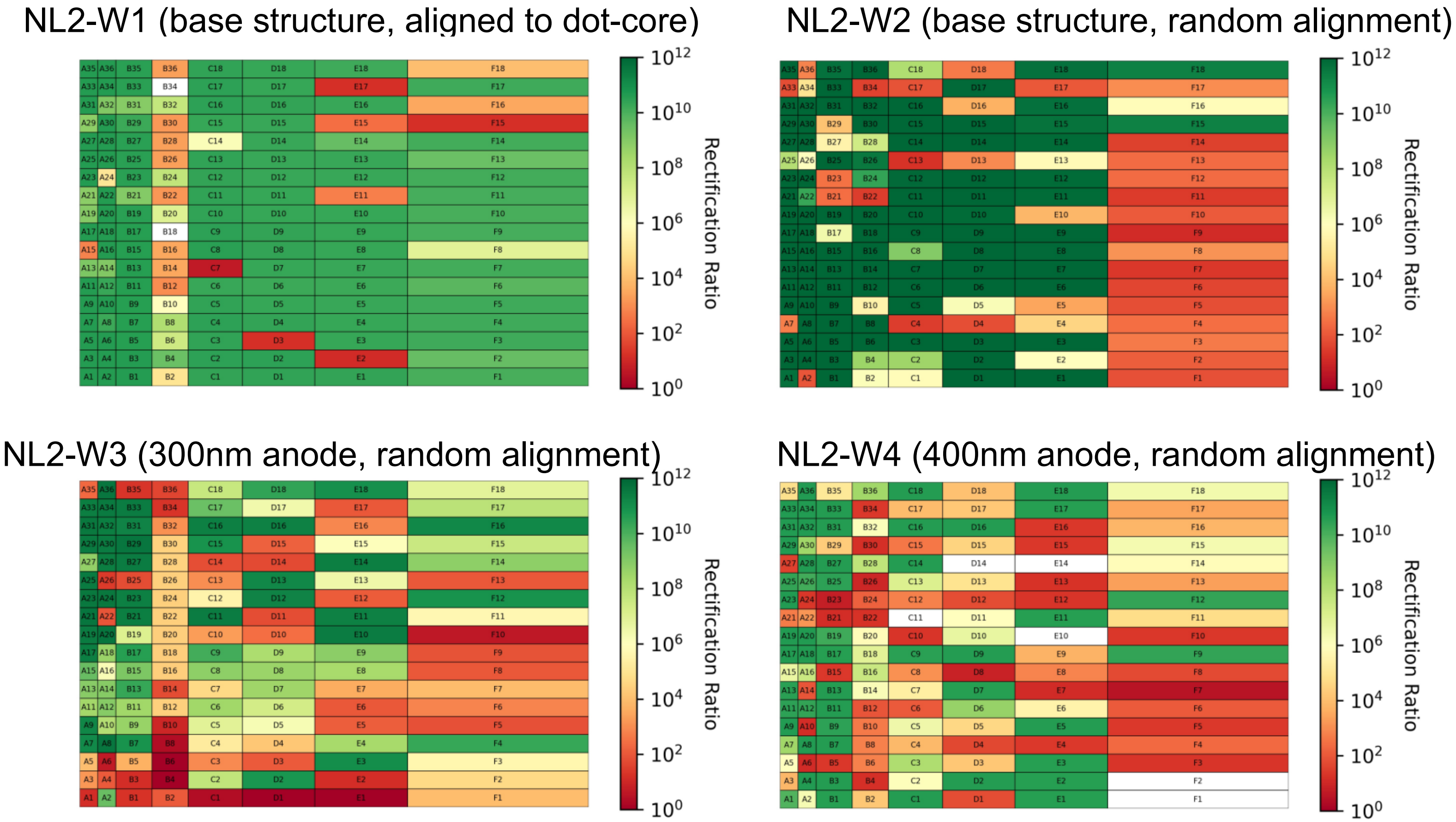
- **Representative forward I-V curves for device types A-F**
  - **Largest devices achieve ~6 A forward current**

T. Anderson, NRL

Foundry Yield Analysis



- Multiple devices achieve breakdown >1.3 kV, which is ~90% of the parallel-plane value



- ON/OFF ratio used for preliminary yield analysis – captures both devices that don't turn on OR don't turn off

T. Anderson, NRL

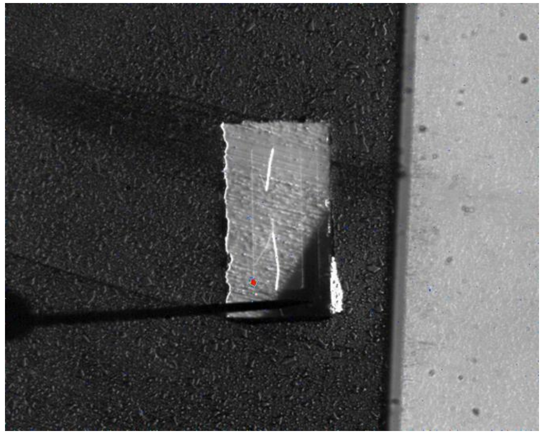
Reliability and Failure Analysis

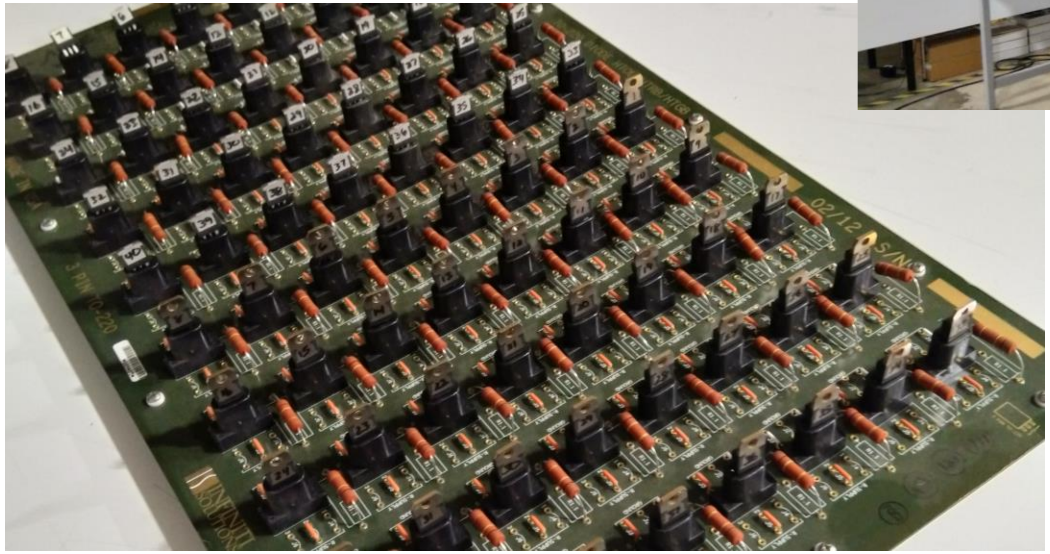
APS physics

- Extensive vertical GaN reliability and FA effort ongoing

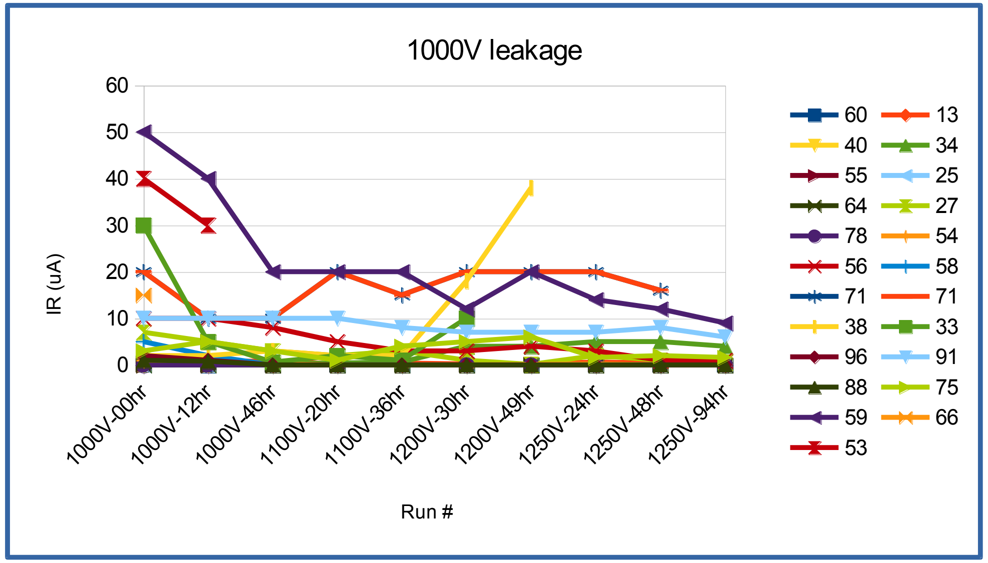
Reliability test ovens and power supplies

Failure Analysis: Emission Microscopy (EMMI)





Reliability test board



High Temperature Reverse Bias leakage current data

O. Aktas, EDYNX

Outline

- Overview of WBG Power Electronics
- Medium-Voltage Vertical GaN Devices
  - PN Diodes
- **Vertical GaN Devices for Electric Vehicles**
  - **JBS Diodes and MOSFETs**

DOE Targets for Electric Vehicle Drivetrains

APS physics

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy
VEHICLE TECHNOLOGIES OFFICE

- The Department of Energy has partnered with several automotive and energy companies to create a tentative roadmap for improvements to electric vehicle drives.
- "… EETT has a 2025 power density research target of **33 kW/L for a 100 kW peak system**. While achieving this target will require transformational technology changes to current materials and processes, it is essential for enabling widespread electrification across all light-duty vehicle platforms."
- 33 kW/L target is for motor plus power electronic drive; PE target is 100 kW/L for 100 kW system
- Reliability and cost targets are also specified

For more information about U.S. DRIVE, please see the U.S. DRIVE Partnership Plan at www.vehicles.energy.gov/about/partnerships/usdrive.html


USDRIVE
DRIVING RESEARCH AND INNOVATION FOR VEHICLE EFFICIENCY AND ENERGY SUSTAINABILITY

Electrical and Electronics Technical Team Roadmap

October 2017

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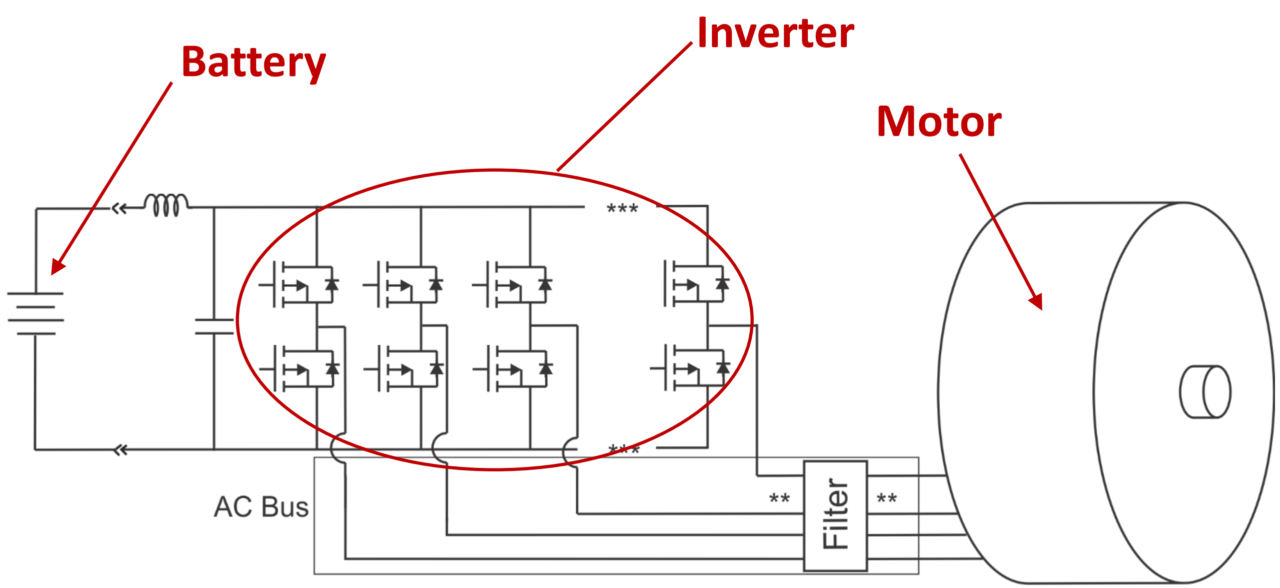
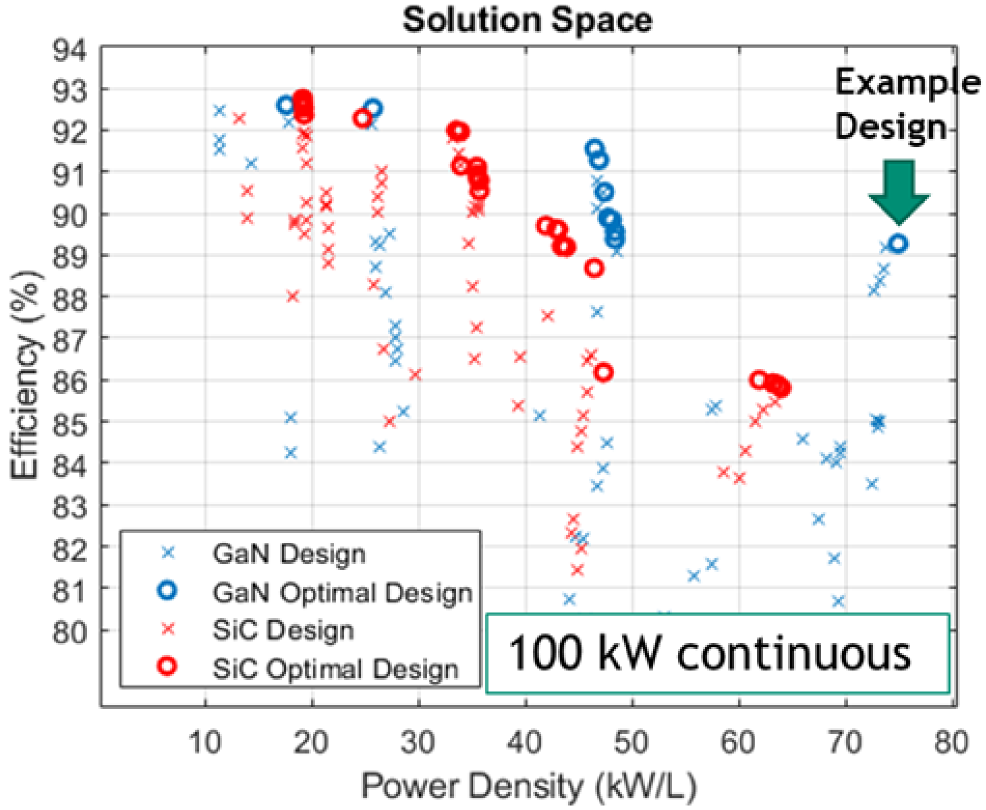
Advantages of Vertical GaN for Electric Vehicles

Electric Drivetrain Schematic





- Inverter and optional boost converter require switch-diode pairs (typical for switch-mode power conversion circuits)
- MOSFET and JBS diode are likely good choices (JBS diode combines best properties of Schottky and PN diodes)

- System-level genetic optimization indicates that vertical GaN diodes may out-perform SiC in terms of efficiency and power density

J. Neely, G. Pickrell, J. Flicker, L. Rashkin, and R. Kaplar, "The Case for Vertical Gallium Nitride Devices in Electric Vehicle Drives," *2020 IEEE Applied Power Electronics Conference* (APEC2020), Industry Session: Vehicle Electrification II (Virtual).

Vertical GaN JBS Diode Development

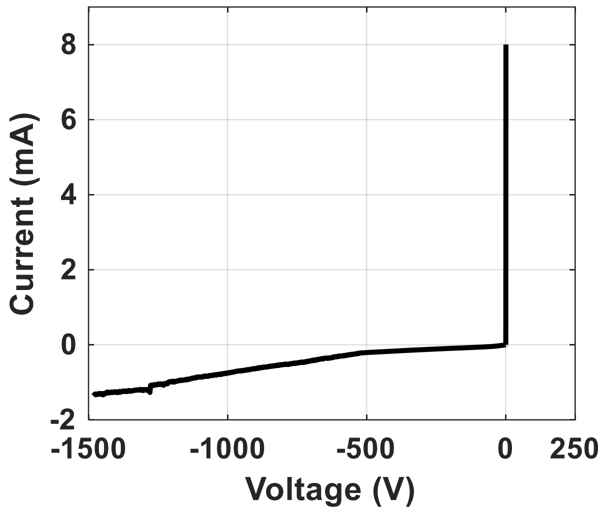
Fabrication of GaN JBS diodes:

- Etched-and-regrown JBS diode demonstrated
- 1500 V reverse holdoff voltage

Next Steps:

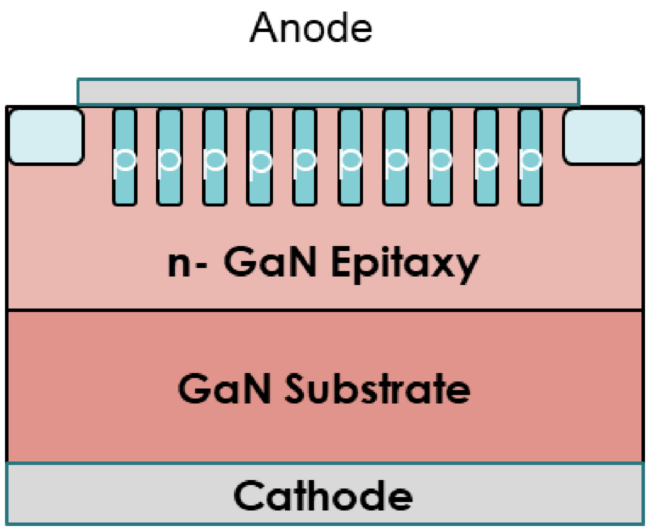
- Exploring regrowth surface pre-treatment strategies to reduce current leakage
- Added JTE to aid in field management and improve reverse breakdown

IV curve for gen 1 GaN JBS diode

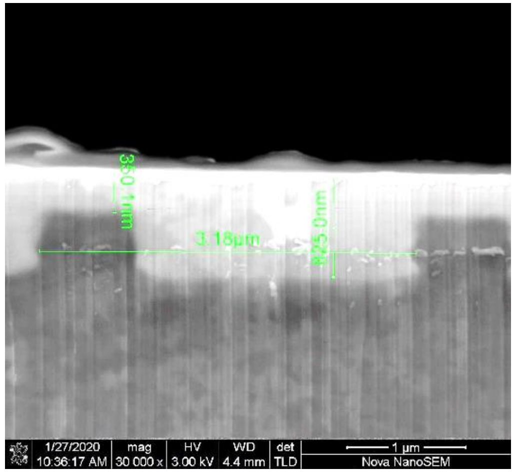


- Low turn-on voltage (consistent with Schottky)
- Low leakage current (consistent with PN junction)
- Confirms JBS operation

JBS Diode Schematic



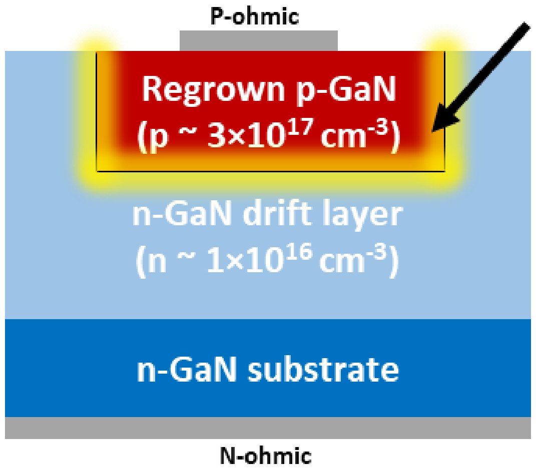
Cross-Sectional SEM of Regrown PN Junction



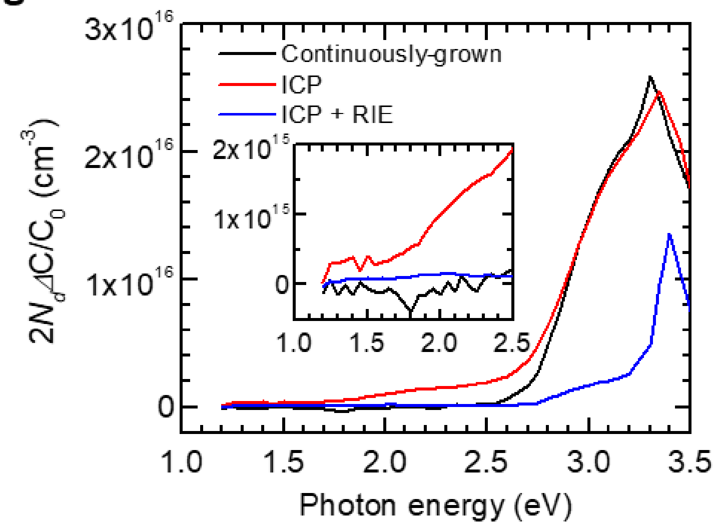
A. Binder, SNL

Etch and Regrowth Needed for JBS Diodes

Plasma etch damage



DLOS Spectra



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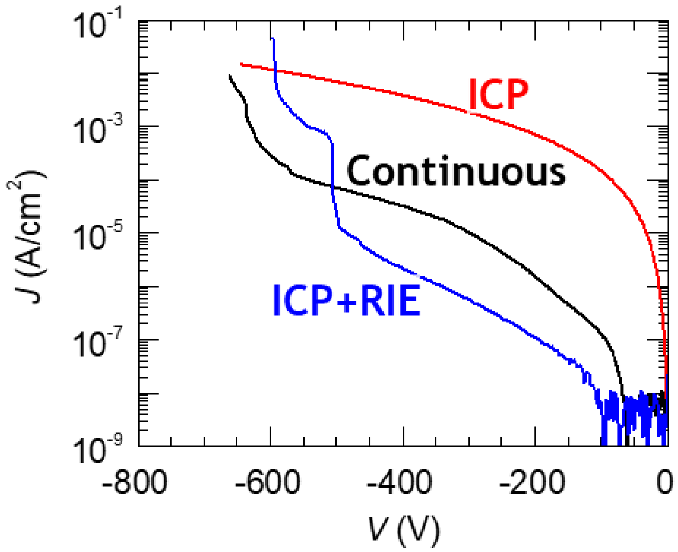
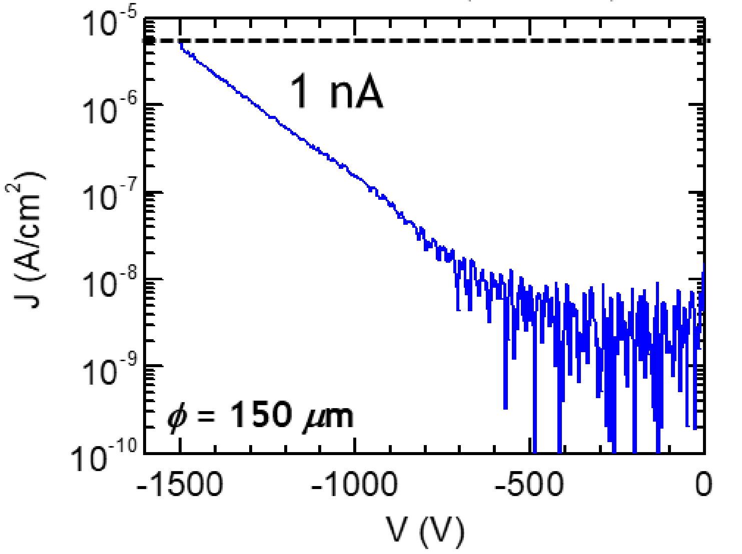
PNDIODES

Reverse *I*-*V* (No JTE)



Reverse *I*-*V* (w/ JTE)



- **Correlated E_c – 1.9 eV deep level with plasma damage and leakage**
- **Removed plasma damage with post-ICP RIE step**
- **Achieved etched-and-regrown diode > 1.5 kV and 1.4 mΩ.cm²**

A. Armstrong, SNL

Vertical GaN MOSFET Development

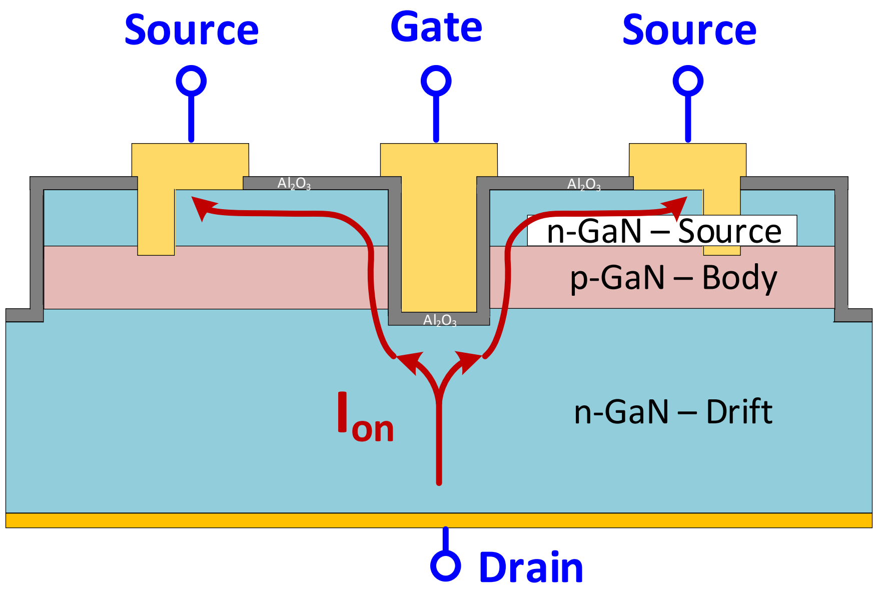
Trench MOSFET key features:

- Selective-area doping not needed for body and source
- Gate on vertical etched GaN sidewall
- High fields at bottom trench corner

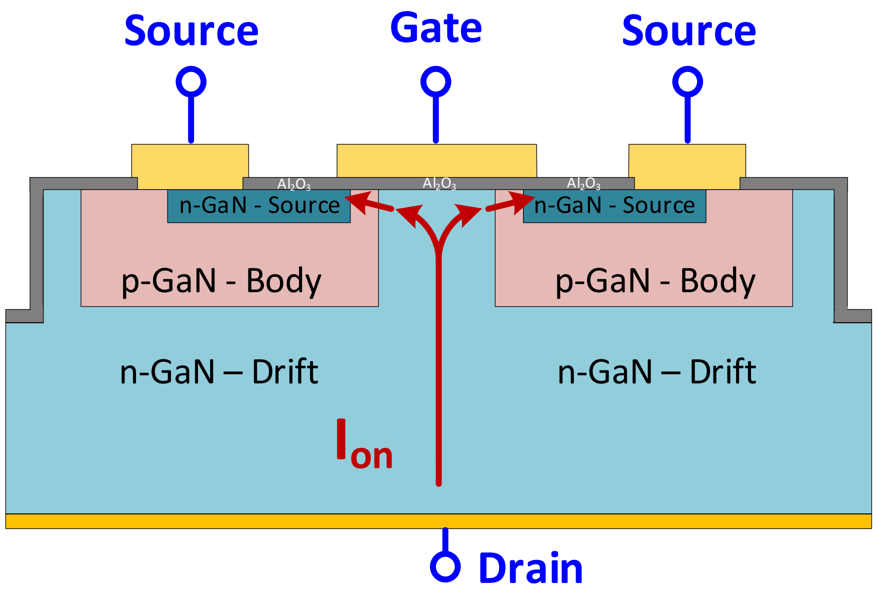
Double-well MOSFET key features:

- Selective-area doping required for body and source
- Gate on planar top surface
- JFET region engineering critical

Trench MOSFET

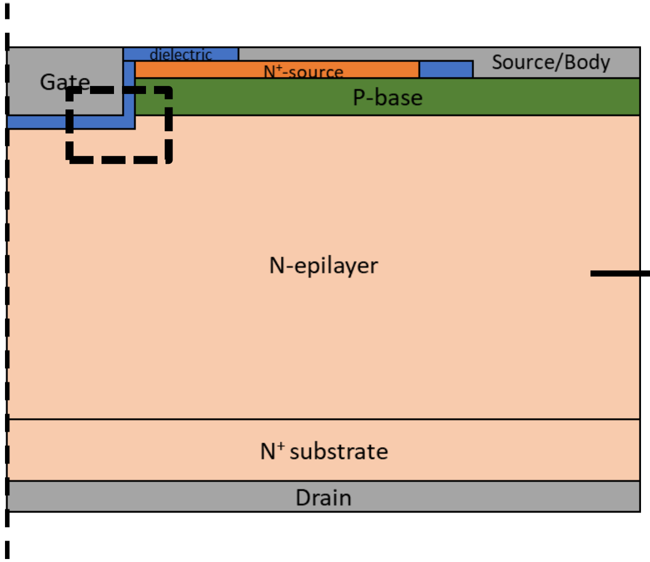


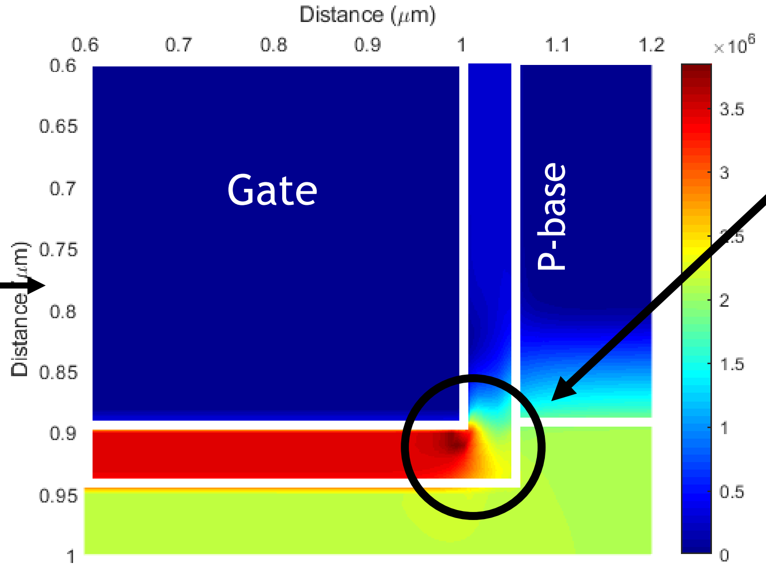
Double-well MOSFET



A. Binder, SNL

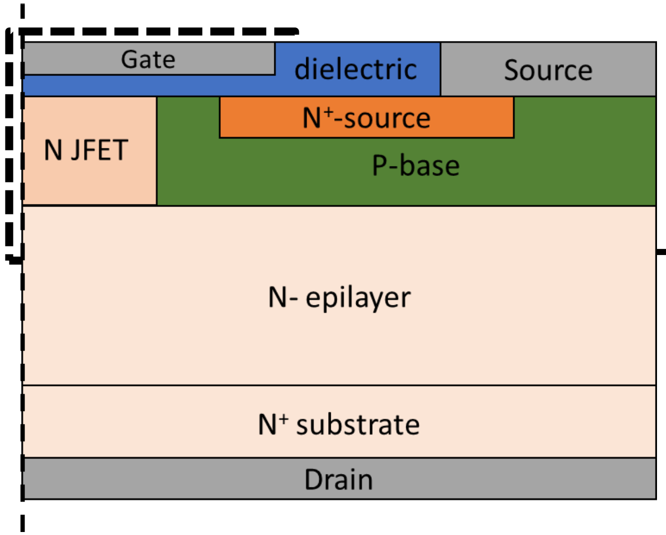
TCAD Simulation of T-MOSFET and D-MOSFET

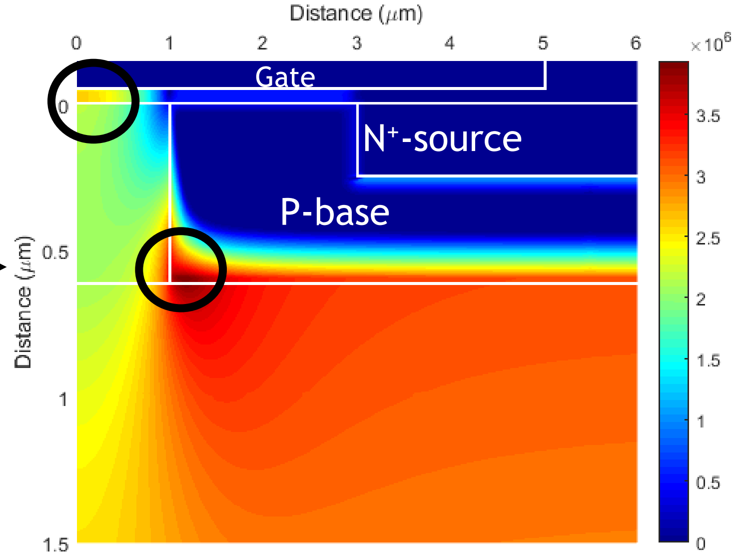




Field crowding at the corner of the gate elevates electric field in dielectric

Electric field taken at V_g=0 and V_{DS}=1200 V



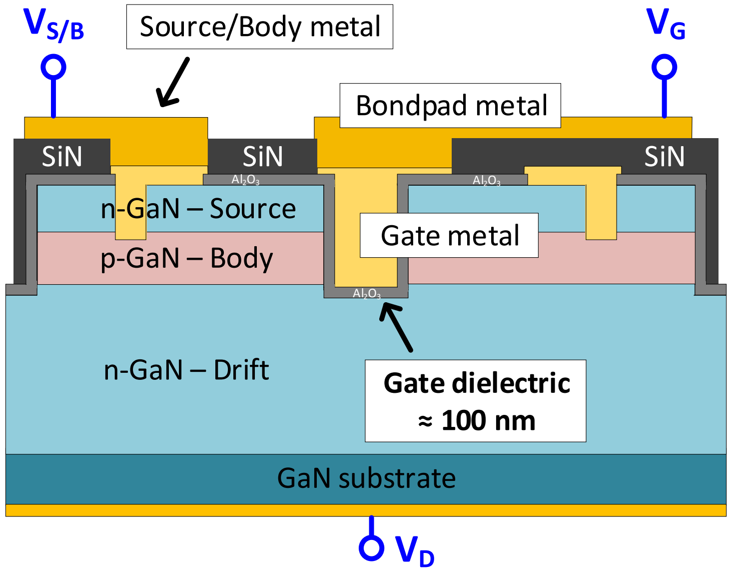


- **Large electric field occurs in GaN at corner of JFET region**
- **Largest dielectric E-field occurs under center of gate**

L. Yates, SNL

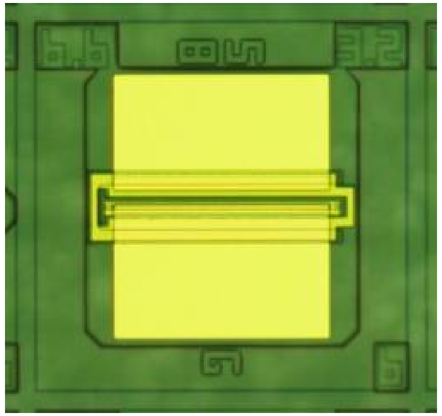
Initial Trench MOSFET Electrical Data

T-MOSFET Diagram

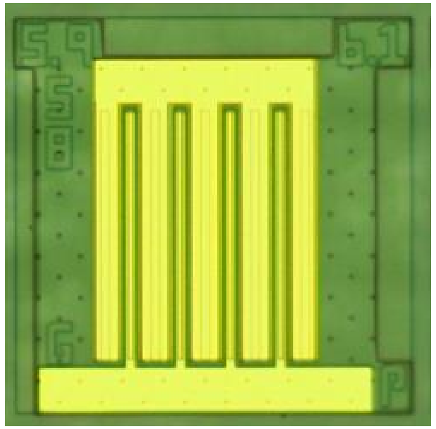


- **T-MOSFETs demonstrated**
- **Devices have a good on/off ratio, ~10^8**
- **Positive threshold voltage: ~8 V**
- **Current density ~400 mA/mm achieved**
  - **Single-finger and four-finger devices fabricated**

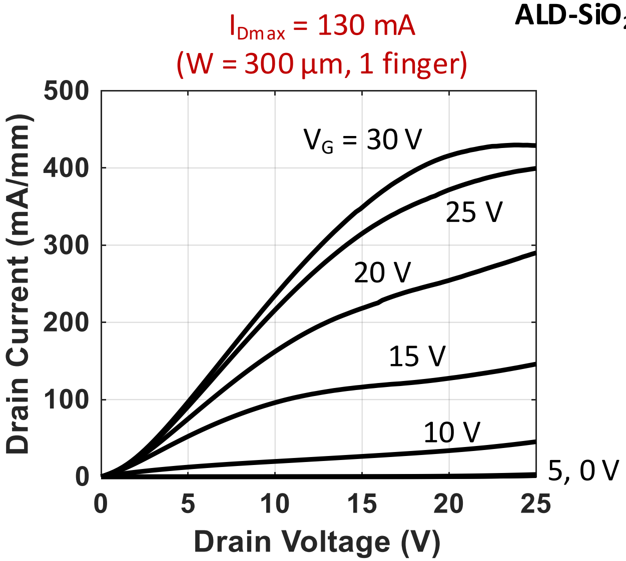
Single-finger



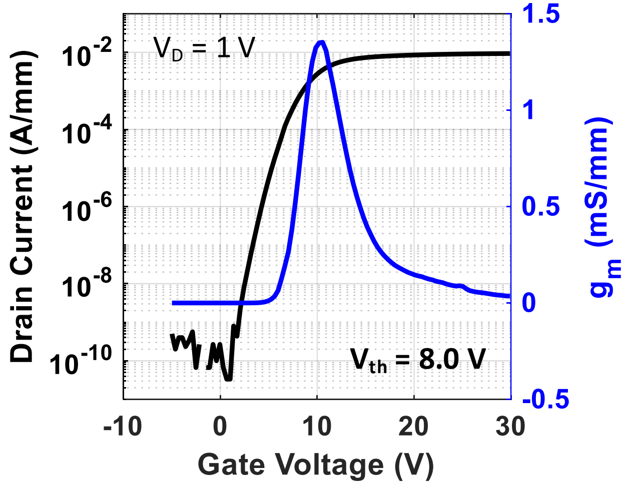
Four-finger



Lot 5: Single Finger MOSFET
ALD-SiO_2 gate



VNA7682C-D: 6.5-4.4



A. Binder, SNL

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  - JBS Diodes and MOSFETs

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Questions?

Bob Kaplar: rjkapla@sandia.gov

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