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# FAIR DEAL Grand Challenge Overview

**Team Members (alphabetized by last name):**
Chris Allemang, Evan Anderson, Andrew Baczewski, Ezra Bussmann, Robert Butera, DeAnna Campbell, Quinn Campbell, Steve Carr, Esther Frederick, Philip Gamache, Xujiao Gao, Albert Grine, Mark Gunter, Connor Halsey, Jeff Ivie, Aaron Katzenmeyer, Andrew Leenheer, Bill Lepkowski, Tzu-Ming Lu, Denis Mamaluy, Juan Mendez, Fabián Peña, Scott Schmucker, David Scrymgeour, Lisa Tracy, George Wang, Daniel Ward, and Steve Young

**Thrust Leads:**
Shashank Misra, Denis Mamaluy, Xujiao Gao, Daniel Ward, David Scrymgeour, and George Wang

**Lead Principal Investigator (PI)**: Shashank Misra

**Program Managers (PMs):** Robert Koudelka, Conrad James, Rick Muller and Paul Sharps

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico
87185 and Livermore,
California 94550

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## ABSTRACT

While it is likely practically a bad idea to shrink a transistor to the size of an atom, there is no arguing that it would be fantastic to have atomic-scale control over every aspect of a transistor – a kind of crystal ball to understand and evaluate new ideas. This project showed that it was possible to take a niche technique used to place dopants in silicon with atomic precision and apply it broadly to study opportunities and limitations in microelectronics. In addition, it laid the foundation to attaining atomic-scale control in semiconductor manufacturing more broadly.

## ACKNOWLEDGEMENTS

This project went from the principal investigator (PI) needing to be convinced that it was worth submitting an idea at 3 PM on the Friday before the submission deadline, to being the "riskiest Grand Challenge Sandia has ever funded", to one of the few projects I've been on that hit its big audacious goals. This was because of the genuine effort put forth by a lot of people.

To the core FAIR DEAL team - Scott Schmucker, Jeff Ivie, Evan Anderson, Fabian Pena, Ezra Bussmann, Aaron Katzenmeyer, DeAnna Campbell, Philip Gamache, Mark Gunter, Andrew Leenheer, Connor Halsey, David Scrymgeour, Tzu-Ming Lu, Lisa Tracy, Albert Grine, Chris Allemang, Xujiao "Suzey" Gao, Denis Mamaluy, Juan Mendez, Bill Lepkowski, Steve Young, Quinn Campbell, Andrew Baczewski, Esther Frederick, George Wang, Bob Butera, Igor Kolesnichenko, Andrew Teplyakov, Alexander Shestopalov, Kevin Jones, and Dan Ward – I truly enjoyed working with each of you, and remain in awe of everything you got done, even when faced with a global pandemic.

To the FAIR DEAL External Advisory Board (EAB) – Raj Apte (Chair), Sadas Shankar, Steven Goodnick, Duncan Dversdall, Tina Kaarsberg, John Pellerin, Gary Patton, Drew Wimmer and Pierre-Emmanuel Gaillardon – thanks for being a part of our team, and putting genuine care and thought into advising us on which directions to head in.

To the program and project management team – Robert Koudelka, Paul Sharps, Conrad James, Rick Muller, David White, Jim Hudgens, Lori Mann, Jennifer Woodrome, Randy Smith, Caitlin Friedman, Deanne Idar and Whitney Wenger – thanks for your careful guidance in constructing and reconstructing the program, organizing and executing five big events, and opening doors to new opportunities.

And finally, thanks to Greg Frye-Mason and Leigh Cunningham in the LDRD office for the foresight and fortitude to fund the FAIR DEAL GC project from FY2019 to FY2021.

## CONTENTS

# ACRONYMS AND DEFINITIONS

| Abbreviation | Definition |
|---|---|
| AMO | Advanced Manufacturing Office |
| ALD | Atomic layer deposition |
| ALE | Atomic layer etch |
| AP | Atomic precision |
| APAM | Atomic precision advanced manufacturing |
| $BCl_3$ | Boron trichloride |
| BEETS | Big Energy Efficient Transistors project |
| CMOS | Complementary metal-oxide semiconductor technology |
| DFT | Density functional theory |
| DOE | Department of Energy |
| EAB | External Advisory Board |
| FAIR DEAL | Far reaching applications, implications, and realization of digital electronics at the atomic limit |
| GC | Grand challenge |
| KMC | Kinetic Monte Carlo |
| LDRD | Laboratory directed research and development |
| Microfab | Micro fabrication facility |
| MOSFET | Metal-oxide semiconductor field effect transistor |
| $PH_3$ | Phosphine |
| PI | Principal investigator |
| PoP | Proof-of-principle |
| RT | Room temperature |
| S&T | Science and technology |
| SC | Office of Science |
| SET | Single electron transistor |
| Si | Silicon |
| SiFab | Silicon fabrication facility |
| STM | Scanning tunneling microscope/ microscopy |
| TCAD | Technology computer-aided design |
| TFET | Tunnel field effect transistor |

# 1. INTRODUCTION

The Far Reaching Applications, Implications, and Realization of Digital Electronics at the Atomic Limit (FAIR DEAL) Laboratory Directed Research and Development (LDRD) Grand Challenge (GC) sought to develop the science and technology (S&T) required to use atomic precision advanced manufacturing (APAM) to explore opportunities in digital microelectronics for Sandia's customers. APAM promises to establish an opportunity to directly manipulate device physics through control over the underlying atomic structure of a transistor, opening the door to deeper understanding both of current and new transistor technologies. Moreover, because the APAM *process* relies on chemistry to introduce a density of dopants that exceeds the solid solubility limit, transforming silicon (Si) into a material with fundamentally different optical and electrical characteristics, atomic resolution is not required for nearer-term impact. Two capstone goals of the project represent giant leaps forward in turning the promise of APAM in the microelectronics application space into a reality – the development of an APAM-based vertical tunnel field effect transistor (TFET), and the integration of an APAM wire into a conventional complementary metal-oxide semiconductor technology (CMOS) circuit.

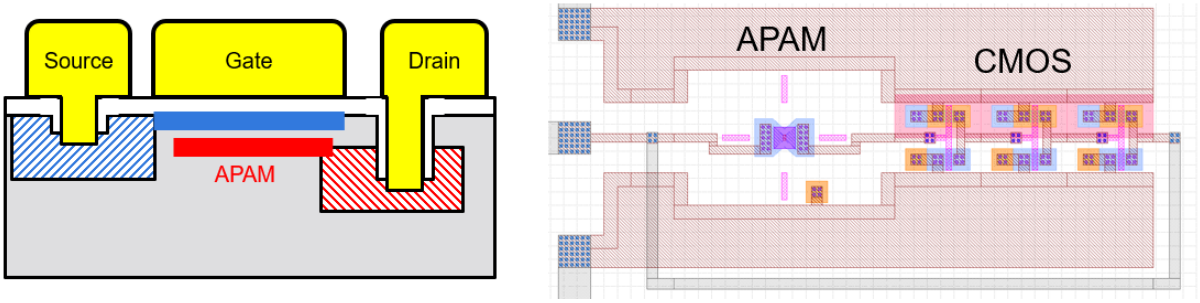


**Figure 1. FAIR DEAL Exemplars.** (Left) In the vertical TFET, a surface gate accumulates a layer of holes (blue) from a silicide contact (source). This turns on band-to-band tunneling to a buried APAM layer of phosphorus (red). (Right) Layout of an integrated circuit where three CMOS inverters are connected in a loop with an APAM device.

The project was organized into four thrusts (as follows) that sought to develop foundational capabilities, spanning APAM, microfabrication, characterization, and modeling, intended to better position Sandia to pursue opportunities in energy efficient computing with industry partners, and microelectronics trust and security with government partners.

- **Thrust #1 – APAM devices**: Expand the complexity of device structures that leverage the unique properties of APAM.
- **Thrust #2 – Modeling:** Develop a toolset connecting process, device, and circuit simulation to understand both APAM transistors and their inclusion in CMOS circuits.
- **Thrust #3 – CMOS Integration:** Discover new processing pathways that can be used to combine APAM and CMOS.
- **Thrust #4 – APAM Toolbox:** Expand the breadth of APAM pathways to functionalize Si and establish proof-of-principle (PoP) demonstrations on the path to scalable manufacturability.

This document is meant to be a high-level narrative of the project team's accomplishments, and a roadmap to our publications. A second document – the **FAIR DEAL Deep Dive** – will outline each of the thrusts and capabilities in significant detail and includes our current vision of follow-on

projects. That document includes complete references, and not just our publications. We will refer to specific sections in the **Deep Dive** in bold below, as a roadmap to that document.

## 2. BACKGROUND

For decades, the microelectronics ecosystem has been driven by a virtuous cycle to achieve increased microsystem functionality and reduced cost by shrinking the channel of the metal-oxide semiconductor field effect transistor (MOSFET). However, the exponential rise in the cost of research and infrastructure required to justify further shrinking the MOSFET has led to a significant decrease in the number of companies willing to continue the virtuous cycle to now just three worldwide. At the same time, MOSFETs have run into both challenging physical limits, such as the shrinking of gate oxides below 1 nm motivating a change in materials, and fundamental limits, such as the thermal energy at room temperature (RT) limiting Dennard scaling. In this context, it makes sense to relax the requirement for manufacturability to determine which paths to pursue, informed by physical and fundamental limits.

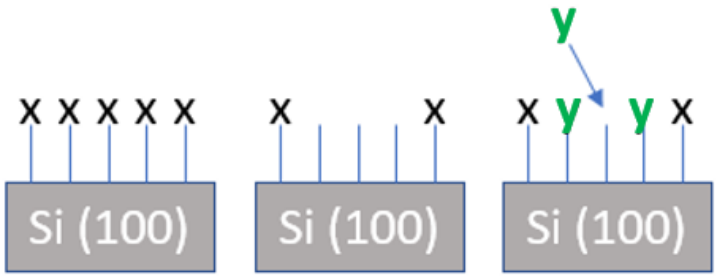


**Figure 2. The abstracted APAM process.** Molecule X is attached to the surface of silicon (left) and serves as a resist. It can be selectively removed, exposing reactive silicon dangling bonds (middle). Certain molecular precursors y will selectively bond to reactive sites. For conventional APAM, x is hydrogen, patterning is done with an STM, y is phosphine, and the entire patterned structure is capped with a thin film of silicon to preserve the planar device.

Understanding the wide-ranging opportunities created by APAM requires understanding its core technology - a novel surface chemistry-based approach to device fabrication that produces planar donor-based (i.e., electron-doped) devices in Si with atomic precision (AP). Masked ion implantation, one of the standard methods to deliver dopants into semiconductors, suffers from dopant straggle. Selective epitaxial deposition has gained favor, but still has a precision limited by top-down microfabrication. In both cases, the resulting dopant concentration is thermodynamically limited by the solubility of dopants in Si. The APAM process starts by passivating the chemically active surface of Si using a monolayer of hydrogen that resists adsorption of other species – an atomic "resist," borrowing from the term "photoresist" in photolithography ("x" in Figure 2). Carefully selected precursor molecules will only react with the parts of the surface where this atomic resist has been removed, re-exposing the chemically active surface. By using a scanning tunneling microscope (STM) to perform atomic-scale hydrogen depassivation (middle panel in Figure 2), and introducing phosphine ($PH_3$) exposure ("y"in Figure 2), electrically active phosphorus-based devices can easily be made to ±1 lattice-site accuracy. Moreover, APAM can deliver dopants to densities ten times higher than the solid solubility limit because it relies on chemistry to incorporate dopants and operates at temperatures low enough to keep them frozen in place.

The benefit of APAM is not limited to scaling transistors to single-atom dimensions. In the vertical TFET of Figure 1, the steepness of the turn-on current can be limited by the sharpness of the dopant profile for the buried donor layer. This in turn increases the lowest voltage needed to operate the vertical TFET device. An APAM TFET overcomes such limitations. The vertical geometry, made possible by the atomically-sharp buried APAM layer, produces planar tunneling and holds promise for dramatically exceeding the current density for conventional edge-tunneling TFET geometries. Nothing in this device concept requires advanced patterning capabilities – the device should work just as well at the 350-nm node as at the 3-nm node. The combined APAM and CMOS circuit in Figure 1 establishes a PoP for manufacturability. Pathways to integrate APAM with CMOS benefit from the flexibility of chemistry-based processing, and from significant changes to the electronic structure originating from a dopant density that far exceeds the solid solubility limit. A concrete example is a near-term application pursued by the project – the reduction of metal-

semiconductor contact resistance, which is a significant enough problem that the contacts are the single largest size element in advanced technologies.

Prior to 2019 (the start of the program) the idea that microelectronics problems can be pursued using APAM was simply laughable [1]. State-of-the-art APAM devices consisted only of dopants, and were only operated at cryogenic temperatures, meaning that any practical application was far out of reach. Despite using Si as a substrate, APAM had never been integrated with CMOS in a meaningful way. This meant there was no practical way to add an APAM-enabled device as the "special sauce" in a CMOS circuit. Even if these physical limitations could be overcome, sufficient modeling tools that incorporate APAM special features had yet to be developed. So projecting performance from a proposed design was impossible. Neither was there a process developed for acceptor doping, required for complementary transistors and modern circuits. And there was no pathway to a fab-scale approach, either for manufacturing or for rapid development.

Successfully addressing these types of research challenges requires spanning and integrating a broad range of disciplines from electrical engineering to chemistry across the full spectrum of discovery science to complex technology. And each research challenge is so fundamental that failure to make progress in any area leaves the ultimate goal just as far away, invariant of progress made in adjacent areas. By some measure, this is the definition of a grand challenge.

# 3. ACCOMPLISHMENTS

**At a high level, the answer to whether APAM can be reasonably applied to problems in microelectronics is yes, and without reservation.** We have shown it can be used to make complicated transistor devices, it is readily integrated with CMOS fabrication, there is a route to manufacturability, and complementary doping is at hand. The project exemplars – the APAM-enabled vertical TFET and APAM directly integrated with CMOS – is imminent in the case of the first and has already been accomplished in the case of the second.

Programmatically, establishing the S&T foundation for APAM in microelectronics has enabled connecting to other (existing) communities, and is starting to lead to commercial interest. This creates an environment where researchers have the tools needed to develop an application, potential examples of which we will discuss in greater detail in the next section.

In the following sections we provide a high-level overview of each of the thrust areas with the modeling thrust tasks interwoven into each of the other three thrust areas, given that in practice, all the work involved such close feedback and integration with the modeling thrust efforts.

## 3.1. APAM-enabled Devices

The primary technical difficulty with making complicated application-relevant devices that incorporate APAM stems from thermal budget considerations. Creating an atomically clean surface to prepare for APAM requires heating to high enough temperatures that most previously added chip features are destroyed. After APAM, the process to add features to the chip can involve heating to temperatures that activate dopant diffusion. The former problem is discussed in **Doping Profile Insanity**, and the solution in **Reduced Temperature Prep.** The latter problem convoluted different physical mechanisms that were smearing out the dopant layer, as discussed in the **STM Sprint,** in addition to post-processing thermal budget issues, as discussed in **Channel Engineering**. **Weak Localization** measurements were critical in determining the thickness of the dopant layer (colloquially, whether it was still "healthy"). A significant smearing mechanism is adatom-mediated during cap growth, and **Optical Profiling** was important in controlling the Si-capping layer growth rate. Less-involved techniques to assess different aspects of doped Si – including ellipsometry [2] and scanning microwave impedance microscopy [3] – were workhorses used throughout the project.

The solution to those problems has let us establish the two key missing components required of any practical APAM device – isolated contacts to enable **Room Temperature Operation**, and high-k/metal **Vertical Gate Stack** to enable high gain switching (Figure 1). While relatively standard structures were adopted, significant **Fabrication Development** was needed to ensure the room temperature platform functioned without leaking current, and significant process development was required for the gate stack to behave respectably [4, 5]. Most importantly, understanding the underlying principles has helped us incorporate features required by more complicated devices in record time. For example, the Department of Energy's (DOE's) Advanced Manufacturing Office (AMO)-funded project Big Energy Efficient Transistors (BEETS) has picked up creation of the APAM-enabled TFET in Figure 1, and was able to integrate a post-APAM hole-type surface silicide contact in a single quarter [5].

An absolutely critical aspect of designing devices and interpreting the data has been to model the APAM devices with **Semiclassical Simulation** [6,7], enabled by the addition of two general capabilities to Charon, Sandia's technology computer-aided design (TCAD) code –adding finite frequency response and **Cryogenic Transport**. Looking to an area of opportunity, leveraging quantum effects in practical applications, we have stablished a **Quantum Transport** modeling

capability, which has been used to make foundational predictions about conduction through nanowires [8] and tunnel junctions.

## 3.2. APAM – CMOS Integration

One of the GC team's crowning achievements was the demonstration that APAM can generally be used to enhance CMOS without detrimental effects (Figure 1). In practice, the problem of **Direct Integration** of APAM with CMOS is significantly more complicated than the related issue of making APAM devices. Specifically the wafer will have more structures on it at the point APAM is added, and will have more complicated processing done to it afterwards. **Fabrication Development** details our integration pathway not only with CMOS7 from Sandia's Microsystems Engineering, Science and Applications (MESA) Si fabrication facility (SiFab), but also our own custom transistor flow in Sandia's micro-fabrication facility (μFab), which can, in principle, be shared with external collaborators. To understand that our **Reduced Temperature Preps** were doing no harm to the parent CMOS, we did extensive forensic analysis of the failure modes of a **Ring Oscillator**, standalone transistors, and test structures. A key step was **Streamlined Simulation** connecting **Circuit Modeling** to **Semiclassical Simulation** and other materials modeling tools. We also looked at the question of the **Robustness** of APAM relative to CMOS and found that APAM survives longer in accelerated lifetime testing than CMOS [9].

The project team also discovered two applications where APAM can have near-term impact by enhancing CMOS. The first is through decreasing the contact resistance of MOSFETs at advanced nodes. Perhaps surprisingly, the largest physical feature of a modern transistor comes from the metal-semiconductor contacts. **Channel Engineering** has shown that the peak active carrier density achievable using APAM exceeds the state-of-the art by a factor of ten. We are in the process of working with Applied Materials to determine whether the anticipated concomitant reduction in contact resistance is realized. From the perspective of manufacturability, we have shown APAM can be templated wafer-scale, albeit at reduced resolution, using photolithography of hard masks that are in wide use in manufacturing now [10]. A scalable process will require the development of a tool to execute APAM chemistry at high throughput and requires buy-in from a tool maker like Applied Materials.

The second application discovered by the GC Team, leverages the **Optical Response** of APAM layers to make supply-chain assurance markers on the backside of Si chips. APAM-doped layers were found to have a high density of defects, which suppresses **Photoluminesence**. However, a high density of dopants, which produces a Drude-like response that extends into the mid-infrared [2], and **Optical Modeling** indicates that this is a consequence of the two-dimensional nature of the layer [11]. Building an optical metasurface on the backside of an off-the-shelf microchip will additionally require a **Reduced Temperature Prep** with a more diminutive thermal budget that preserves the metal layers of the chip. Several candidate solutions have been explored, however, integration with CMOS remains to be evaluated.

## 3.3. APAM Toolbox

The GC team's third headline achievement was laying the groundwork for a vast expansion of what can be done with atomic-scale processing (Figure 2). Microelectronics generally require both polarities of dopants – not just donors, but also acceptors – to realize complementary logic. While an acceptor dopant was discovered by another group, the precursor had unacceptable dimerization, which led to deactivation [12]. We engaged external collaborators to quickly screen acceptor precursors both through **Solution-Phase Doping** [13, 14] and **Vacuum Doping** [15, 16, 17].

Outside of the identification of a $PH_3$-like acceptor precursor, boron trichloride ($BCl_3$), this effort also produced a general framework to think about expansion of atomically precise area-selective surface chemistry to oxides, metals, and etches through interfacing with atomic layer deposition (**ALD**)/ atomic layer etch (**ALE**) techniques. A particularly potent pathway appears to be using **Alternative Resists**, where a hydrogen resist is patterned to nanometer precision and filled in with a halogen [18] in an APAM tool, creating a stable atomic-scale template that can be carried to an ALD or ALE reactor for further processing.

For all this work, a critical realization was that density functional theory + kinetic Monte Carlo **(DFT + KMC)** simulations can perform a critical pathfinding function for new chemistries, with KMC providing particularly compelling details. Another area where this kind of modeling had significant impact was for quantum applications needing atomically-placed single dopants to function as qubits, ranging from quantum computing [19, 20] to analog simulation [21, 22]. We have discovered a simple scheme to produce near-unity single dopant incorporation for both donors [23] and acceptors [24], opening the door to substantial improved yields in multi-dopant structures, where yields of even ten dopant structures are less than 10% under normal conditions.

While there are advantages to what atomic-scale processing produces, e.g., doping that exceeds the solid solubility limit, there may also be benefits to replace a macro-scale process with an atomic-scale one purely from a processing perspective. One specific example is having an atomically-perfect starting point for chemistry-based processing, as opposed to a range of possibilities that occurs when the surface is prepared using either solution-based chemistry or energetic (plasma-based) means [13, 16]. A second is the crystallinity of the resist, where, unlike traditional polymer resists, there is exactly one resist atom per site, with a very consistent threshold for activation. In using **Photolithography** to make donor-based devices [25, 26], we were also able to demonstrate that hydrogen is a competitive resist in terms of energy needed to pattern, a key factor in determining how fast wafers can be processed in production. In the future, as industrial processing runs into issues with shrinking into the nanoscale regime, joining photolithography-based patterning with perfect starting surfaces and ALD/ALE processing holds significant promise.

## 3.4. Workshop on the Atomic Scale

The APAM community is small, entailing approximately five laboratories worldwide, but atomic-scale control is the domain of many disciplines, approaches, technologies, and materials. In April 2021, the GC team hosted an online workshop intended to serve as a merging of different scientific communities to build a broader community of practice and as brainstorming sessions to discuss opportunities and challenges across three broad and inter-related areas: fabrication, characterization, and devices / applications [27]. In short, the workshop aimed to answer the question: What are promising future directions in atomic-scale fabrication and characterization, and for devices made with AP? The workshop was organized as three several-hour sessions as follows, each followed by a panel discussion led by moderators:

- **Session 1: Fabrication:** Challenges and opportunities for scaling down ALD and ALE to near-atomic resolution;
- **Session 2: Characterization:** Opportunities and challenges for building towards in-operando characterization at the atomic limit; and
- **Session 3: Devices and Applications:** Leveraging and evaluating atomic scale control for next-generation microelectronics.

# 4. IMPACT

Astonishingly, given the range of open science questions involved, the GC team hit each one of the major project-end goals that were identified in the original idea document, save for circuit polymorphism for hardware trust. Programmatically, the near-term future for microelectronics research looks promising, with significant new programs in this area anticipated in the next few years.

This section summarizes the smaller projects and ideas that are carrying the GC team forward, hopefully bridging to the larger programs that new funding in this area will bring.

- **BEETS**: This DOE AMO project seeks to establish the viability of an APAM enabled vertical TFET.
- **Co-designed improved neural foundations leveraging inherent physics stochasticity**: This DOE Office of Science (SC) project asks whether probabilistic computing is a useful paradigm, and leverages APAM to design tunnel diodes that may be used to generate random numbers at the same massive scales as found in the brain.
- **Room temperature single electron transistors (RT-SETs)**: SETs are spectacular electrometers and could have significant impact as transducers in traditional sensors. This project seeks to leverage APAM to create schemes that allow them to operate at RT.
- **Hot qubits**: This project seeks to measure the charge noise in APAM SETs to determine schemes where it can be intentionally suppressed. Charge noise and sensor instability are responsible for the requirement that semiconductor spin qubits be operated at dilution refrigerator temperatures.
- **APAM for hardware trust and security**: This project seeks to use APAM tunnel junctions as nonlinear circuit elements that enable circuit-level polymorphism – circuits having different logic functions at different supply voltages.
- **Ionic liquid gated APAM nanowires**: APAM nanowires provide confinement that is reminiscent of 2D materials, albeit with lower mobility and higher carrier density. This project seeks to make a transistor using an ionic gel dielectric, which may be capable of depleting the high carrier density, and an APAM nanowire channel.
- **Atomically precise ultra-High Performance 2D Micro Electronics**: This proposal, led by Zyvex Labs, seeks to make and model an APAM-based bipolar junction transistor. Enabling a small base dimension may improve the speed of these devices for analog applications.
- **Engineering 2D transition metal dichalcogenides through APAM**: This project seeks to determine whether general rules of thumb for APAM-based chemistry can be carried over to another material of wide interest – the transition metal dichalcogenides. Both high levels of doping and atomically precise defect placement have compelling device-based ramifications in these materials.
- **Superconducting semiconductors**: Extricating the sensitive Josephson junction in a superconducting qubit from material interfaces holds promise for improved coherence. This project looks at whether extreme levels of acceptor doping in 2D sheets may induce Si to superconduct, potentially opening the door to semiconductor nanostructure control over the qubit.

- **Discovering atomic limit electro-optical characteristics in silicon:** Impurity bands have historically been an underutilized way of manipulating semiconductor band structure. Various in-gap impurities hold great promise to create a direct band gap in silicon that enables efficient light absorption and emission.

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All references were partly funded by FAIR DEAL. Bolded references denote ones where most of the work was performed under FAIR DEAL.


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| Gao, Xujiao “Suzey” | 01355 | xngao@sandia.gov |
| Sharps, Paul | 01876 | psharps@sandia.gov |
| Wang, George | 01876 | gtwang@sandia.gov |
| Swartzentruber, Brian | 01882 | bsswart@sandia.gov |
| Cunningham, Leigh | 01910 | lcunnin@sandia.gov |
| James, Conrad | 05229 | cdjame@sandia.gov |
| Misra, Shashank | 05229 | smisra@sandia.gov |
| Schmucker, Scott | 05229 | swschmu@sandia.gov |
| White, David | 05600 | drwhite@sandia.gov |
| Koudelka, Robert | 05640 | rkoudel@sandia.gov |
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