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Manipulation of Hole Spin Transport in Germanium

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ABSTRACT

Downscaling of the silicon metal-oxide-semiconductor field-effect transistor technology is expected to reach a fundamental limit soon. A paradigm shift in computing is occurring. Spin field-effect transistors are considered a candidate architecture for next-generation microelectronics. Being able to leverage the existing infrastructure for silicon, a spin field-effect transistor technology based on group IV heterostructures will have unparalleled technical and economical advantages. For the same material platform reason, germanium hole quantum dots are also considered a competitive architecture for semiconductor-based quantum technology. In this project, we investigated several approaches to creating hole devices in germanium-based materials as well as injecting hole spins in such structures. We also explored the roles of hole injection in wet chemical etching of germanium. Our main results include the demonstration of germanium metal-oxide-semiconductor field-effect transistors operated at cryogenic temperatures, ohmic current-voltage characteristics in germanium/silicon-germanium heterostructures with ferromagnetic contacts at deep cryogenic temperatures and high magnetic fields, evaluation of the effects of surface preparation on carrier mobility in germanium/silicon-germanium heterostructures, and hole spin polarization through integrated permanent magnets. These results serve as essential components for fabricating next-generation germanium-based devices for microelectronics and quantum systems.

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ACRONYMS AND DEFINITIONS

Abbreviation	Definition
2D	Two-dimensional
ALD	Atomic layer deposition
BOE	Buffered oxide etch
DIP	Dual in-line package
EBL	Electron beam lithography
FET	Field-effect transistor
HFET	Heterostructure field-effect transistor
LDRD	Laboratory directed research and development
LSRL	Lawrence Semiconductor Research Laboratory
MACE	Metal-assisted chemical etching
MOS	Metal-oxide-semiconductor
RTA	Rapid thermal anneal; Rapid thermal annealer
SEM	Scanning electron microscope; Scanning electron microscopy

Abbreviation	Definition
SOC	Spin orbit coupling
TEM	Transmission electron microscope; Transmission electron microscopy
XRD	X-ray diffraction

1. INTRODUCTION

Downscaling the Si field-effect transistor (FET) technology to achieve higher transistor packing densities, faster computer speeds, and lower power consumption will soon reach a fundamental limit. A new device architecture and possibly a computing paradigm are required for meeting the ever-growing demand for more computing power with higher energy efficiency. Currently many paradigm-shifting proposals for future computers exist. While one or more of these novel schemes may be the ultimate solution for computing far in the future, most of them deviate from the existing silicon technology so much that the transition could be highly disruptive and present a roadblock toward adoption. A technology or device architecture that is more akin to current silicon transistors at the materials and fabrication levels has a smaller barrier toward technology maturation and is more likely to represent the near to mid term solution for the next two decades.

Ge is a material that is intrinsically compatible with Si and the associated technology. Ge can be epitaxially grown on Si wafers. The SiGe epitaxy technology has advanced rapidly in the past two decades, and device quality Ge layers with controlled strain can now be routinely grown. Due to the nature of the valence band of Ge, the mobility of Ge holes can be much higher than feasible in Si. The higher atomic number of Ge compared to Si also means stronger spin-orbit coupling (SOC), which is an additional degree of freedom that can be leveraged for devices. The advantages of compatibility with the Si industry, higher carrier mobility, and the potential of electric field control of spins make Ge holes a promising material platform for next-generation computing devices. In this project, we explore the feasibility of two types of devices for promising computing architectures in Ge-based systems: spin field-effect transistors (FETs) and quantum dots. We choose to work with holes, because of the demonstrated strong, gateable SOC and because of the band alignment of strained Ge in SiGe heterostructures. Nevertheless, many of the results acquired here for holes in principle can be extended to electrons in Ge.

Spin FETs have a device architecture that resembles conventional FETs [1][2]. Unlike in conventional FETs where information is encoded in the charge degree of freedom and therefore voltage and current, the spin degree of freedom is utilized in spin FETs. Spin-polarized ferromagnetic electrodes only allow aligned spins to pass through easily. A spin is injected into the channel from the injector electrode and moves toward the detector electrode. As the spin moves in the channel, the spin rotates because of the SOC intrinsic to the channel material. The rotation speed can be controlled by the magnitude of the electric field defined by the gate through the Rashba effect. The gate thus controls whether a spin aligns or anti-aligns with the detector. Since no actual charge current but only spin current is required, and a small change in gate voltage is sufficient for completely flipping the spin alignment, this architecture can be fast and energy efficient.

Two most important ingredients for spin FETs are (1) efficient spin injection and detection and (2) ballistic transport with strong, gate-controlled SOC. If the transport is diffusive, the alignment of spins is randomized as the spins move through the channel, negating the spin transistor operation. The most convincing operation of spin FETs was demonstrated in InAs [3], a III-V compound semiconductor with strong SOC and high electron mobility. The effect, however, is

weak and only present at low temperatures. More importantly, InAs is a material that is difficult to integrate into a silicon foundry. We reported in 2018 that two-dimensional (2D) holes in Ge/SiGe heterostructures possess strong, gate-controlled Rashba SOC [4]. The spin rotation length can be much shorter than the mean free path, suggesting that the aforementioned ingredient (2) can be satisfied and ballistic spin FETs are possible in this material. In this project, we investigated approaches to accomplish injection and manipulation of hole spins in Ge-based structures.

In addition to the spin FET approach, hole spins have also been considered for quantum computing and coherent operations have been demonstrated [5][6][7][8][9]. One complication of hole spins arises from the valence band nature. In many semiconductors, including Si and Ge, the valence band has a four-fold degeneracy at the zone center, two for spins and two for the heavy hole and light hole bands. This additional degeneracy can be lifted by strain and quantum confinement. For (100) oriented 2D hole systems, such as 2D holes in strained Ge/SiGe heterostructures or Ge metal-oxide-semiconductor (MOS) FETs, the two low energy bands are the heavy hole bands with spins $\pm 3/2$. Similar to qubits in electron spin systems, quantum information can be encoded in hole spins. To drive the transition between the two spin states, one can use electric fields at microwave frequencies to drive electric dipole spin resonance that is enabled by the strong SOC associated with the valence band in Ge. A synergistic laboratory directed research and development (LDRD) project “Leveraging Spin-Orbit Coupling in Ge/SiGe Heterostructures for Quantum Information Transfer” focused on coherent operation and quantum state transduction using Ge hole spin qubits in Ge/SiGe heterostructures. In this concurrent synergistic project, we explored the feasibility of fabricating Ge hole quantum dots in Ge MOSFETs, which in general have better tolerance against harsh processing conditions. SiGe heterostructures, especially on the Ge-rich end, are known to have low thermal budget due to the concerns of strain relaxation, diffusion of Si and Ge across the epitaxial interfaces, and generation of defects at high temperatures. The reactive Ge rich surfaces also make it difficult to keep the Ge/SiGe heterostructures intact during process.

As an extension to our study of hole injection, we also performed an exploratory investigation of metal-assisted chemical etching (MACE) of Ge, which could rely on hole injection from a metal contacting Ge as a catalytic mechanism for etching of Ge in a wet etchant. Several length scales were identified and intriguing surface morphology due to MACE was observed.

We summarize our work on Ge-based materials and devices in Section 2. Our investigation into methods of injecting and polarizing hole spins in Ge heterostructures are reported in Section 3. The exploratory study of MACE of Ge is presented in Section 4.

2. GE-BASED MATERIALS AND DEVICES

In this project, we considered and worked with two types of Ge-based materials for p-channel (hole) devices: Ge MOSFETs and Ge/SiGe heterostructures. The goals were to develop reliable process flows for fabricating FET devices and to establish the electrical behavior at cryogenic temperatures.

2.1. MOSFETs

Historically, Ge MOSFETs have been studied with a perspective of replacing Si MOSFETs in conventional integrated circuits because of the better material properties and the resulting better device performance, such as higher mobility. While many demonstrations of Ge MOSFETs have been presented in the literature [10][11][12][13][14][15], surprisingly there has been little work studying the operation of such devices at deep cryogenic temperatures. To consider to feasibility of using Ge MOSFETs as the platform for p-channel spin devices either for spin FETs or for quantum dots, we set out to first evaluate the performance of Ge p-channel MOSFETs at cryogenic temperatures.

We first developed a process flow for fabricating Ge p-channel MOSFETs. We used commercially available Ge wafers with a diameter of 2 inches. The wafer was nominally undoped with a resistivity of 50 $\Omega\cdot\text{cm}$. The material was patterned and implanted with boron for the source and drain regions. The dopants were activated by a rapid thermal anneal (RTA) at 350 °C. The gate insulator was 90 nm of Al_2O_3 deposited in an atomic-layer-deposition (ALD) system. Ti/Au stacks were used for Ohmic contacts to the source and drain regions as well as the top gate.

The MOSFET devices were characterized down to 0.3 K in a helium-3 cryostat. The carrier densities and mobilities were extracted from the transverse and longitudinal magneto-resistances. Figure 2-1 (a) and (b) show the carrier density as a function of gate voltage and carrier mobility as a function of carrier density, respectively. Both dependences are robust and repeatable upon multiple scans. P-channel operation is apparent, as the carrier density increases as the gate voltages is swept more negative. A strong hysteresis is observed in the density vs. voltage scan. As the gate is swept more negative, the density increases along the upper curve. When the gate is swept toward zero, the density follows the lower curve. This hysteretic behavior, typically absent or weak in Si MOSFETs, indicates that the ALD oxide and the oxide/Ge interface likely contain a high density of hole traps. When holes are pulled into the channel due the negative gate voltage, a portion of these induced holes are trapped and become immobilized. Upon reversal of the gate sweep direction, the trapped holes are not immediately released. The mobile carriers in the channel are depleted first, resulting in the observed strong hysteresis. The mobility shows a peak of $\sim 350 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ around $4\times 10^{12} \text{ cm}^{-2}$. A mobility peak at an intermediate density is commonly observed in MOSFET systems at cryogenic temperatures. On the low-density end, screening of disorder improves the mobility as the density increases. On the high-density end, interface roughness scattering becomes dominant and the mobility decreases with increasing density. The mobility-density dependence is not sensitive to the hysteresis.

The fabrication and device characteristics have been described in detail in a manuscript submitted for peer-reviewed publication.

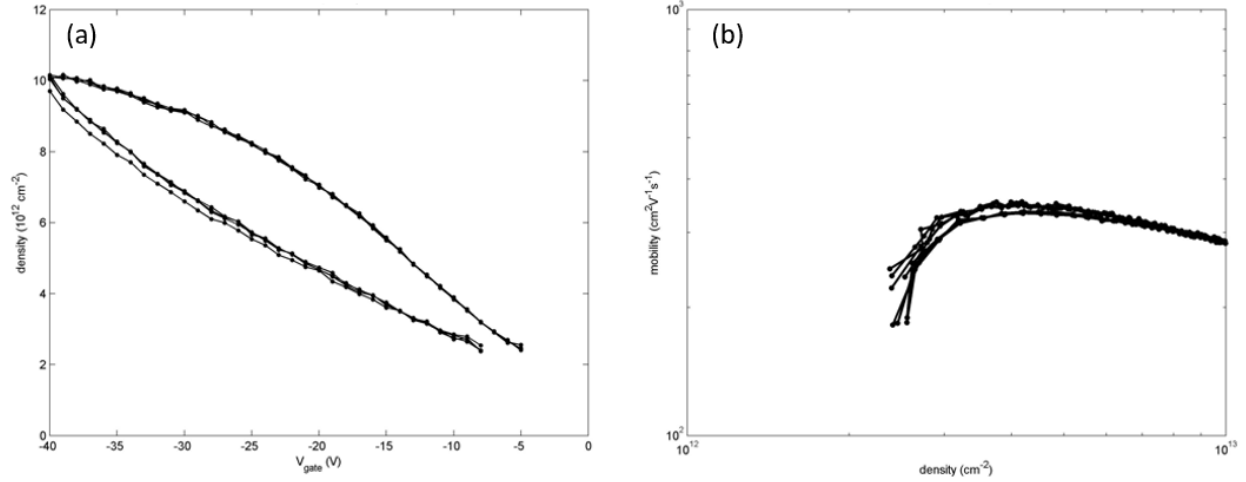


Figure 2-1. Electrical properties characterized by Hall effect measurements at 0.3 K. (a) Hall effect density as a function of gate voltage. (b) Mobility as a function of carrier density.

2.2. Ge hole MOS quantum dots

With a baseline fabrication process established and MOSFET device operation demonstrated, we proceeded with fabricating and demonstrating Ge hole MOS quantum dots. Such quantum dots may serve as the basis for semiconductor qubits, if single spins can be controllably isolated, manipulated, and read out.

Quantum dot device fabrication followed the process flow for Ge MOSFETs. After the implant activation and ALD oxide deposition, electron beam lithography (EBL) was performed on polymethyl methacrylate resist, followed by deposition and lift-off of a thin Ti/Pt stack. The cycle of ALD oxide deposition, EBL, and metal deposition and lift-off could be repeated up to three times depending on the quantum dot design. After the gates were defined, via holes for contacting the heavily implanted regions were etched through using buffered oxide etch (BOE). Ti/Au bond pads were then defined and deposited.

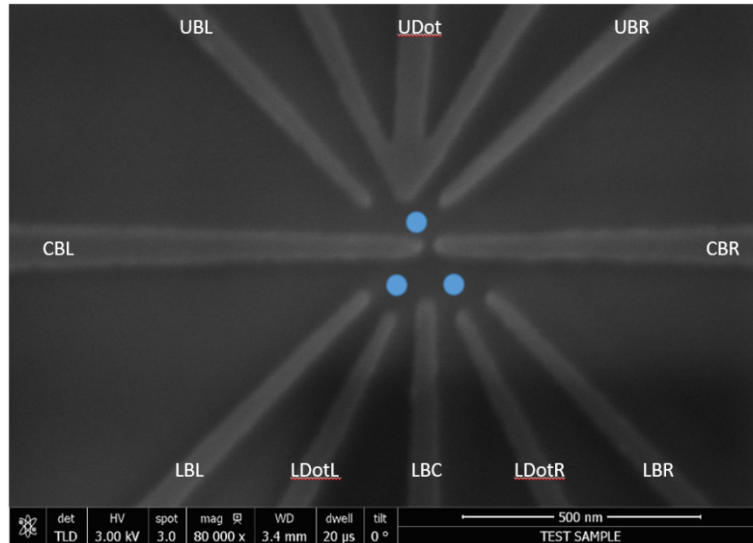


Figure 2-2. An SEM image of a two-metal-layer Ge MOS quantum dot device after the first round of nanoscale gate fabrication. The blue dots represent where quantum dots could form under appropriate voltage biases.

In this project we attempted two designs: a three-metal-layer design and a two-metal-layer design. These designs were also used for fabricating Ge/SiGe quantum dots in the synergistic LDRD project “Leveraging Spin-Orbit Coupling in Ge/SiGe Heterostructures for Quantum Information Transfer” with a different target application and slightly modified process flow. In the three-metal-layer design, three rounds of EBL were performed to define isolation gates, accumulation gates, and depletion gates in three different layers. This design requires accurate alignment at the second and third rounds of EBL. The yield was low, and the turnaround time was long. As our goal was to demonstrate quantum dot operation in a Ge MOSFET system and assess the feasibility of using such systems for quantum information science, we abandoned the three-metal-layer design and switched to the two-metal-layer design. In the new design, only one round of EBL was required for defining nanoscale depletion gates. A global top gate was used for accumulating holes, and alignment tolerance would not be an issue. The device yield and turnaround times were significantly improved. An SEM image of a two-metal-layer Ge MOS quantum dot device is shown in Figure 2-2 together with the gate names. By applying depletion voltages to the nanoscale gates shown in the image and a positive voltage to the global accumulation gate, it is possible to define three quantum dots – one in the upper channel and two in the lower channel – in the nanostructure region, as represented by the blue dots in Figure 2-2.

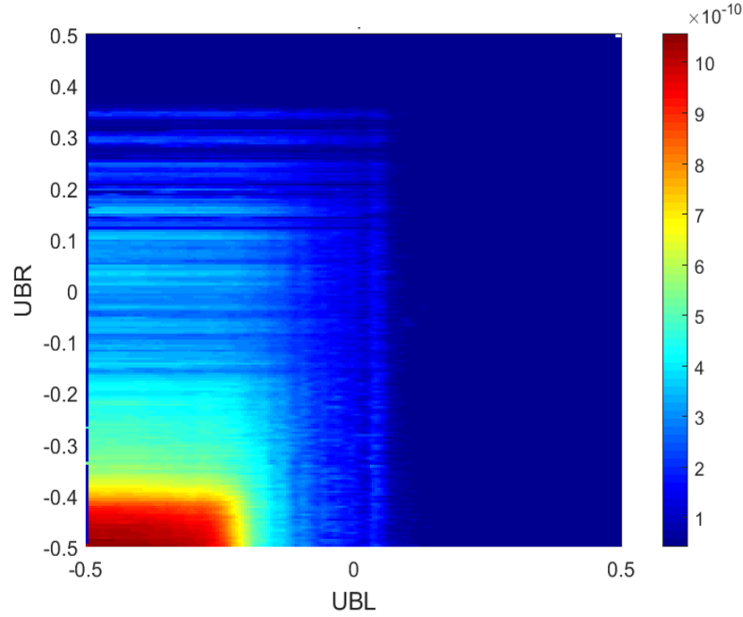


Figure 2-3. Device current as a function of the voltages at UBR and UBL.

In Figure 2-3 we show a representative scan of the device current in the upper channel as a function of the voltages at UBR and UBL. The other depletion gates were set at 0 V except that CBL and CBR were set at 3 V and UDot was set at -3 V. The accumulation gate voltage was also set at -3 V. This voltage configuration forced the current to go through the upper channel, and ideally we would be probing a single quantum dot in the upper channel. Our data shows that the Ge MOSFET architecture can indeed confine the device current through a constriction and potentially a quantum dot. However, while there are indeed current oscillations as a function of UBR and UBL voltages, there are two sets of oscillations and they are orthogonal to each other. Each set of oscillations is effectively only responsive to a particular gate. There is no oscillation that couples to both gates. The oscillations can be as due to local disorder near the respective depletion gates. This result implies that the disorder in Ge MOS systems can dominate the electrostatic potential, making lithographically defined quantum dots challenging to realize.

The details of Ge quantum dot fabrication and electrical characterization are to be reported in a manuscript as a peer-reviewed journal publication.

2.3. Strained Ge quantum wells in Ge/SiGe heterostructures

Ge/SiGe heterostructures have gained much interest since the breakthrough demonstration of high-mobility holes in such systems [16]. Later, enhancement-mode Ge/SiGe heterostructure FETs (HFETs) were demonstrated by Sandia and National Taiwan University [17]. These Ge/SiGe HFETs were used in several studies of low-density high-mobility Ge holes [18][19][20] and hole quantum dots [5][21]. These Ge/SiGe heterostructures typically consist of a virtual Ge substrate, a reverse graded SiGe buffer layer, a constant composition SiGe relaxed layer, a strained Ge quantum well, a top SiGe barrier layer, and an optional cap layer. The electrical performance of Spin FETs or quantum dots would be highly dependent on the quality of the starting material and the fabrication process flow.

In this project, we collaborated with Lawrence Semiconductor Research Laboratory (LSRL) to develop strained Ge quantum wells in SiGe heterostructures. We then used the material to develop a stable and reliable process flow for fabricating Ge/SiGe HFETs. The electrical properties of holes in these Ge/SiGe HFETs were correlated with processing conditions and nanostructures revealed by transmission electron microscopy (TEM). The Ge/SiGe material was developed synergistically with the LDRD project “Leveraging Spin-Orbit Coupling in Ge/SiGe Heterostructures for Quantum Information Transfer” which also needed high-quality starting material as well as a reliable process flow for Ge/SiGe HFETs.

The Ge/SiGe material was epitaxially grown by LSRL using their proprietary chemical vapor deposition process. Several iterations of growth were performed to calibrate the growth conditions. After the structures were delivered to Sandia, HFET devices were fabricated for electrical characterization. The process flow was similar to that used for Ge MOSFETs except for the surface clean step before the ALD oxide was deposited. Typically a dip in BOE was performed. We also investigated using H_2O_2 as the surface clean solution.

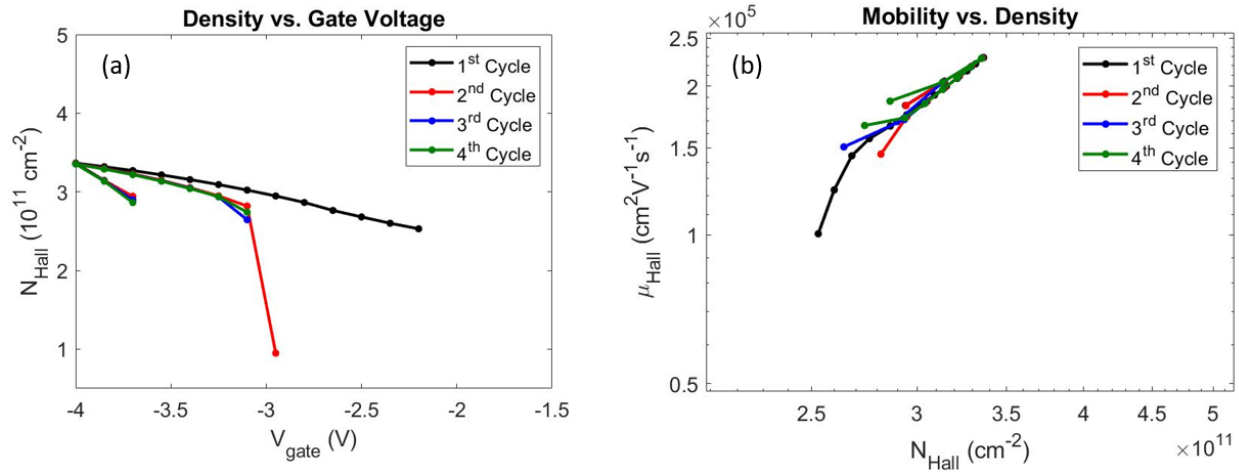


Figure 2-4. Electrical properties of holes in a Ge/SiGe heterostructure grown by LSRL. (a) Density vs gate voltage. (b) Mobility vs density.

Figure 2-4 shows the electrical properties obtained from Hall effect measurements at 4 Kelvin for a Ge/SiGe heterostructure grown by LSRL. The Si concentration in the SiGe barrier layer was 17 %, and the SiGe barrier layer was 30 nm, with a 1 nm Si cap on top. The HFET was not cleaned with H_2O_2 . The electrical properties – a peak mobility $> 2 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a saturation density $\sim 3.3 \times 10^{11} \text{ cm}^{-2}$ – are comparable to those demonstrated in material grown by leading academic groups [6][17][20].

Wet cleans of Si often contain H_2O_2 . A H_2O_2 dip combined with HCl dip was shown to result in clean Ge surfaces [22], which could improve the electrical properties. Using the LSRL-grown Ge/SiGe material, we investigated the effects of wet surface cleaning using H_2O_2 before the growth of the ALD Al_2O_3 gate insulator. A 7 % H_2O_2 solution was used to clean the surfaces of Ge/SiGe heterostructures for a variable time before the standard flow of device fabrication was continued.

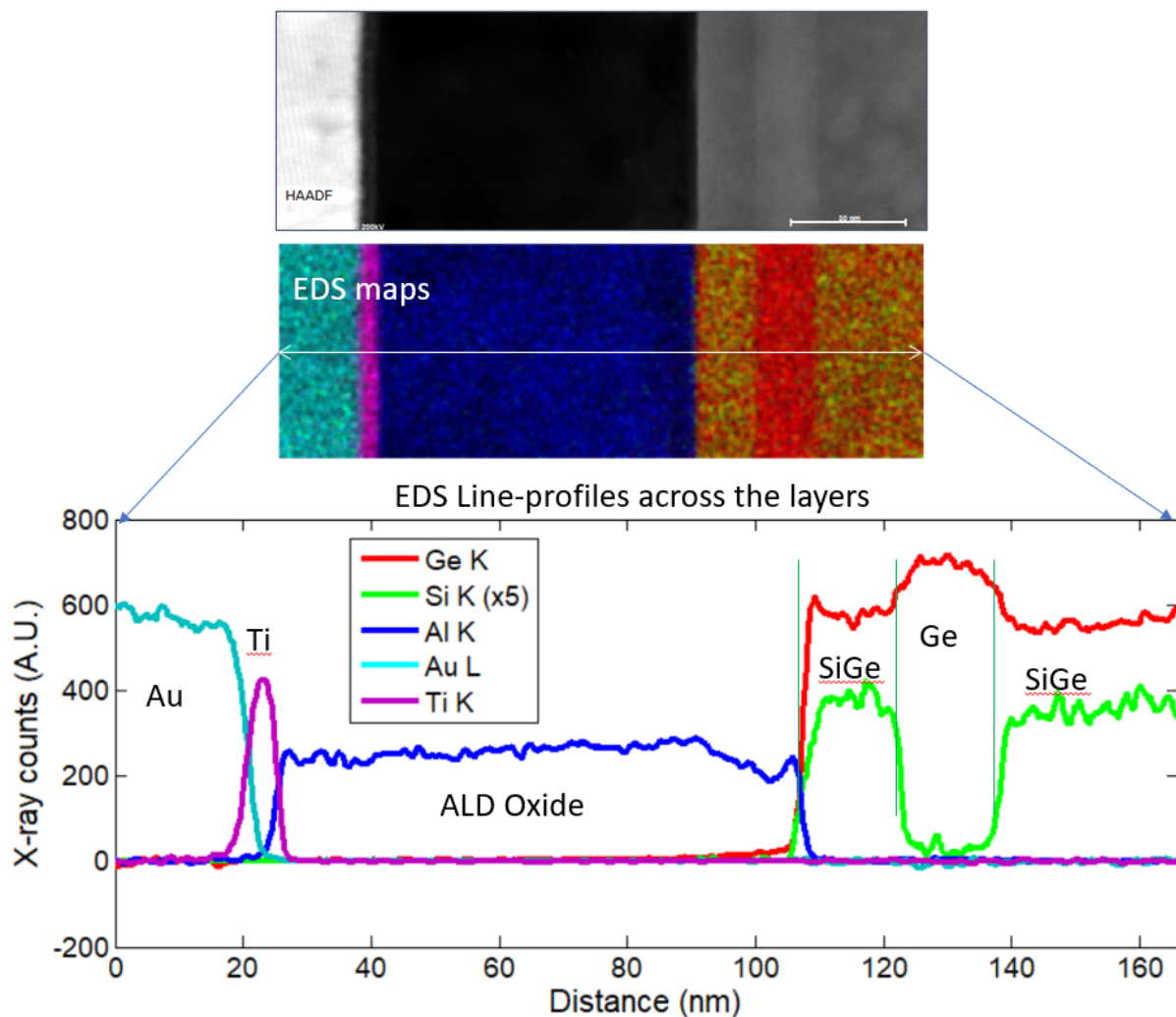


Figure 2-5. Cross-sectional TEM image and EDS maps of a metal-oxide-SiGe heterostructure stack.

Figure 2-5 shows the cross-sectional TEM image and energy dispersive spectroscopy (EDS) maps of a Ge/SiGe HFET stack. The Ge/SiGe heterostructure received a dip in 7 % H_2O_2 for 60 seconds before the growth of growth of ALD Al_2O_3 gate insulator. It can be seen that the H_2O_2 dip etched the material fairly aggressively. The SiGe barrier layer was reduced from 30 nm thick to 15 nm thick, as inferred from the TEM image and the EDS maps. The density-gate voltage dependence and mobility-density dependence are shown in Figure 2-6. With a much thinner SiGe barrier layer, the saturation density increases significantly, while the mobility drops by more than a factor of 2 at the same density. The result shows that using H_2O_2 to clean the surface of Ge/SiGe heterostructures needs to be performed carefully. An extended dip in H_2O_2 can result in significant loss of the SiGe barrier layer and change the electrical properties. On the other hand, a dip in H_2O_2 , when timed precisely, may be used to tune the thickness of the SiGe barrier layer, i.e., the depth of the Ge quantum well.

A manuscript is being prepared to report the development of Ge/SiGe heterostructures and the effects of surface preparation.

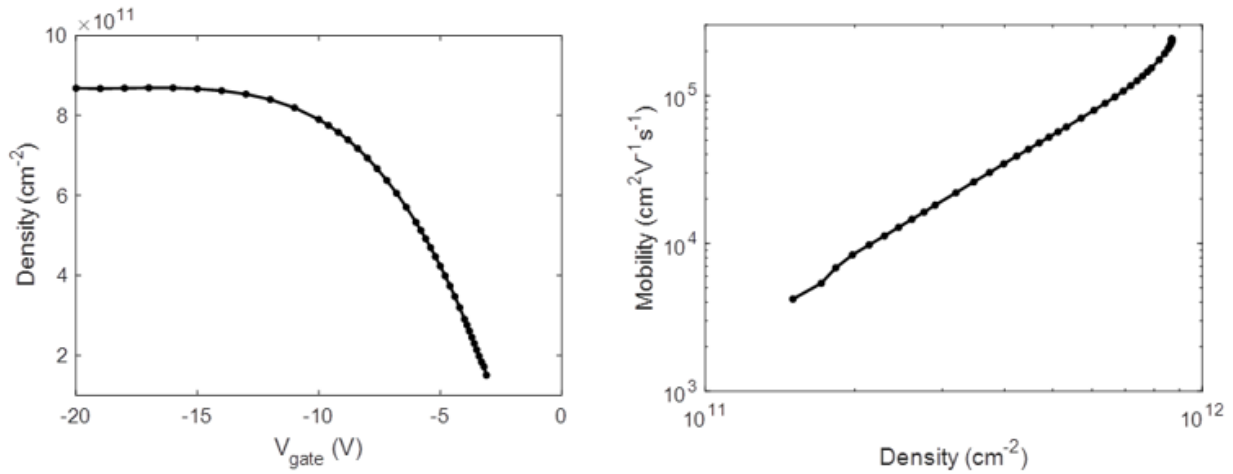


Figure 2-6. Electrical properties of holes in a Ge/SiGe HFET with a 60 second H_2O_2 clean. (a) Density vs gate voltage. (b) Mobility vs density.

2.4. Summary

We have developed baseline process flows for fabricating p-channel Ge MOSFET and Ge/SiGe HFET devices. Device operation at deep cryogenic temperatures was demonstrated in both systems. Ge MOS hole quantum dots were fabricated and tested in this project. Disorder in the MOS system can mask the behavior of lithographically defined quantum dots and make single hole operations challenging. We investigated the effects of surface preparation using H_2O_2 solutions on Ge/SiGe heterostructures and observed significant etching of the SiGe barrier layer. The structural change translates to the electrical properties. This etching effect needs to be taken into account when developing any Ge cleaning protocol involving H_2O_2 .

3. INJECTING SPINS

For spin FET operations, two important components are (1) efficient injection and extraction of spins and (2) manipulation of spins. Our previous demonstration of Ge holes in the ballistic regime where the mean free path is longer than the spin-orbit length [4] indicates that (2) is feasible. In this project, we investigate two approaches for spin injection for holes in Ge.

The first approach is to use ferromagnetic contacts to supply spin polarized carriers to the channel directly. This is the standard approach used for most spin FET investigations. For Ge, we attempted to form ferromagnetic contacts through solid-state reactions. By depositing appropriate metal on top of Ge structures and annealing the stack at elevated temperatures, we can form a ferromagnetic germanide phase in direct contact with the Ge channel.

The second approach is to use external rare-earth magnets to apply high magnetic fields to polarize the spins of holes. Because of the high g factor associated with heavy holes in Ge [18][19], hole spins can be polarized at fairly small magnetic fields. At sufficiently low carrier densities, the Zeeman energy at 1 T can be greater than the Fermi energy and the polarization can approach 100 %. By integrating microscale rare-earth magnets, high magnetic fields on the order of 1 T can be applied locally to regions of interest to selectively polarize spins near the contacts, constituting a new approach of injecting polarized spins into a hole channel. To investigate the feasibility, we used commercially available rare-earth magnets and Ge/SiGe HFETs to evaluate the field strengths and robustness of such schemes.

3.1. Ferromagnetic contacts for holes

With our Ge/SiGe quantum well heterostructures, Mn_5Ge_3 was the ferromagnetic germanide of choice because of its above room temperature Curie temperature [23]. Mn_5Ge_3 has been used to demonstrate spin injection in Ge nanowires [24] but has not been demonstrated in a planar Ge structure.

The first step in our study was to create a reliable process to produce the ferromagnetic phase of the Mn-Ge alloy, Mn_5Ge_3 . The Mn-Ge alloy system is quite complex as there are many phases that can occur. To make matters worse, Mn_5Ge_3 is limited to a small range of conditions under which it can form based on the phase diagram [23]. It is most commonly known to form around 250 °C [23][25]. However, it has been shown to form at temperatures up to 450 °C [24][26]. To ensure that we form the correct phase compatible with our fabrication process for undoped Ge/SiGe HFET devices, we annealed Mn thin films deposited on nominally undoped (100) Ge, with a resistivity around 50 $\Omega\cdot\text{cm}$, in the range of 200 – 500 °C in increments of 50 °C in order to determine a range of possible temperatures before preceding to the Ge/SiGe material.

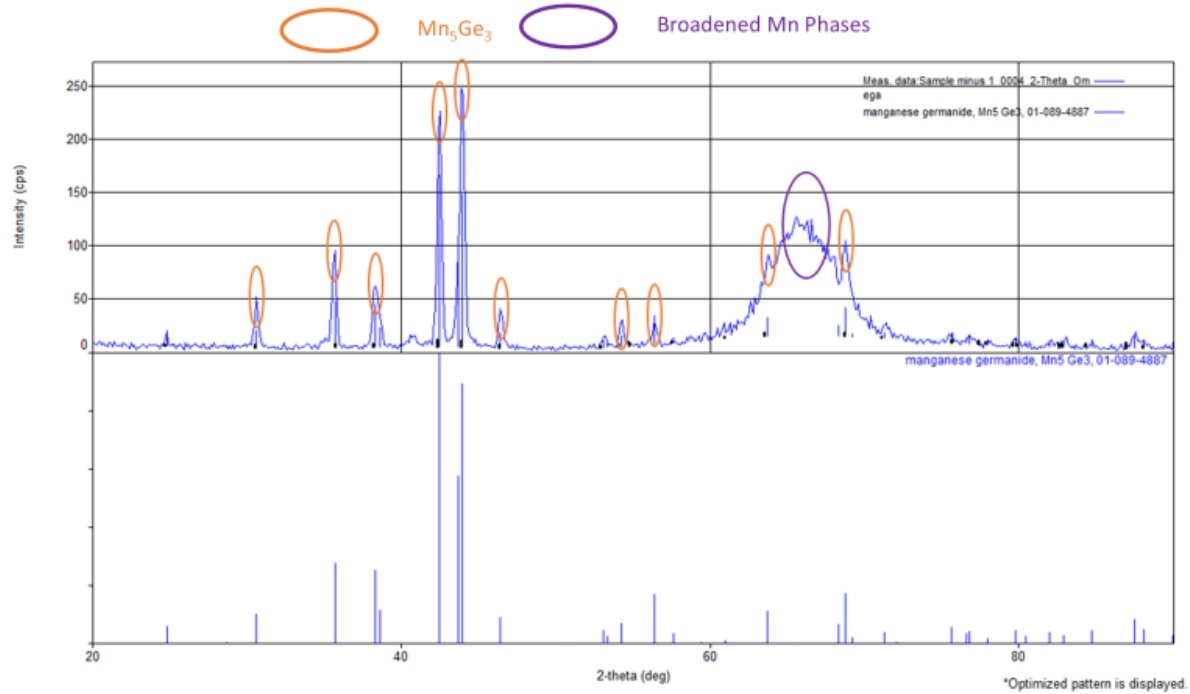


Figure 3-1. XRD of Mn thin film on Ge annealed at 350 °C

Our process for preparing the samples is as follows: standard solvent clean (acetone, methanol, isopropyl alcohol), oxygen plasma clean for 30 minutes, BOE dip for 30 seconds, rinse in deionized water for 30 seconds, thermal evaporation of Mn, and finally annealing in an RTA with 1000 sccm of argon for 30 minutes. Of all the samples prepared, only the sample annealed at 350 °C revealed signatures of Mn_5Ge_3 in the x-ray diffraction (XRD) spectra as shown by Figure 3-1. We observed unreacted Mn from 200 – 300 °C, Mn_5Ge_3 at 350 °C, followed by $\text{Mn}_{11}\text{Ge}_8$ from 400 – 500 °C. This transition of phases was consistent with what is expected [25] but occurred more abruptly and about 100 °C higher. With these results, we then proceeded to test the same process on the Ge/SiGe material but with the more narrowed range of 300 – 400 °C. Figure 3-2 shows the XRD results for the Mn thin film on Ge/SiGe annealed at 300 °C and 400 °C. Mn_5Ge_3 can be identified in both annealed stacks. We proceeded to adopt the 300 °C annealing temperature for our Ge/SiGe devices due to the increasing conversion of Mn_5Ge_3 into other phases. Figure 3-2 shows the increasing prevalence of Mn_3Ge from 300 to 400 °C.

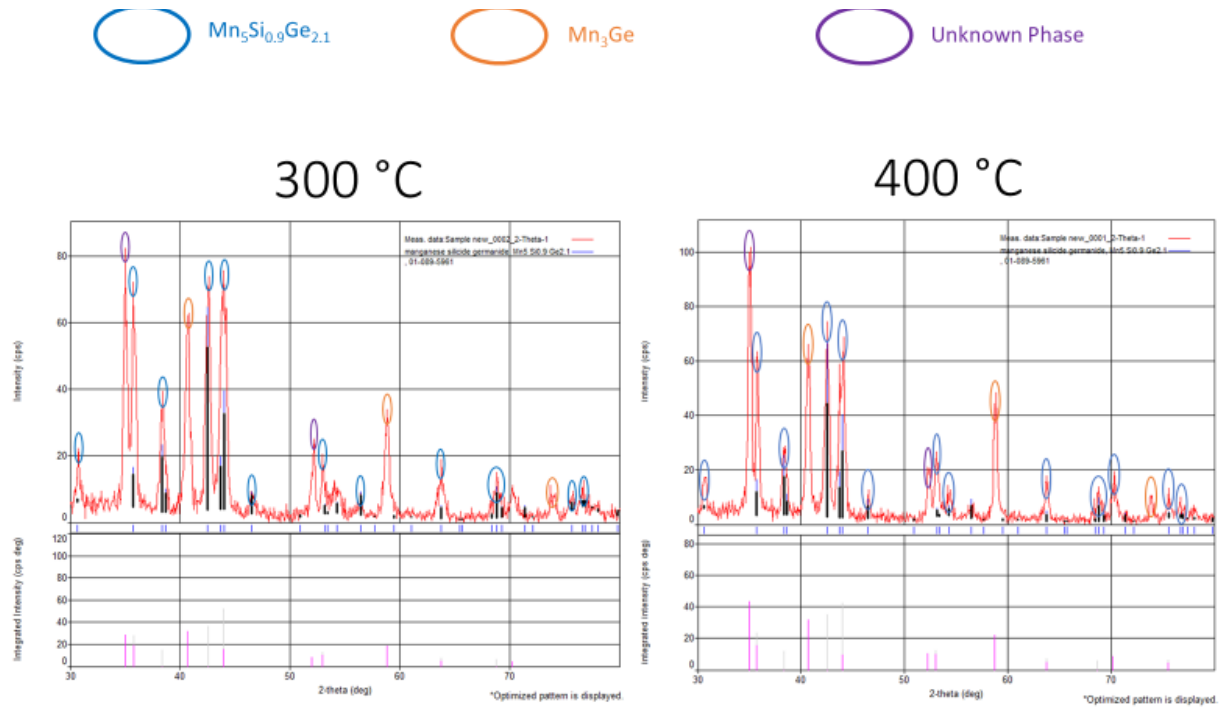


Figure 3-2. XRD spectra of Mn thin films on Ge/SiGe heterostructure annealed at 300 °C (left) and 400 °C (right).

The first series of devices we fabricated were to test the reliability of the ferromagnetic Mn_5Ge_3 contacts our process creates in comparison to nonmagnetic PtGe contacts, which are a reliable germanide-based contact for holes in Ge. The device schematic and corresponding measurement setup are shown in Figure 3-3. The inset of the device schematic highlights the naming convention for the four different sizes test. The convention is as follows: FM1 is a $2\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ contact, FM2 is a $10\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ contact, FM3 is a $20\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ contact, and FMM4 is a $50\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ contact. The number following the contact number is the group number corresponding to where the group is located on the device.

The results of the measurement are summarized in Figure 3-4. The left image shows that the device turns on as the gate voltage (V_{gate}) is swept negative. PtGe contacts reliably conduct around $V_{\text{gate}} = -4.5\text{ V}$. The center image confirms that conduction starts around -4.5 V for the Mn_5Ge_3 contacts as well, but they do so much less reliably. The right image shows the results for each contact averaged over the various groups. This highlights that there is a size dependence. Counterintuitively, the narrower contacts conduct better on average. Furthermore, the Mn_5Ge_3 contacts conduct much less than the PtGe contacts when the device is operated close to threshold.

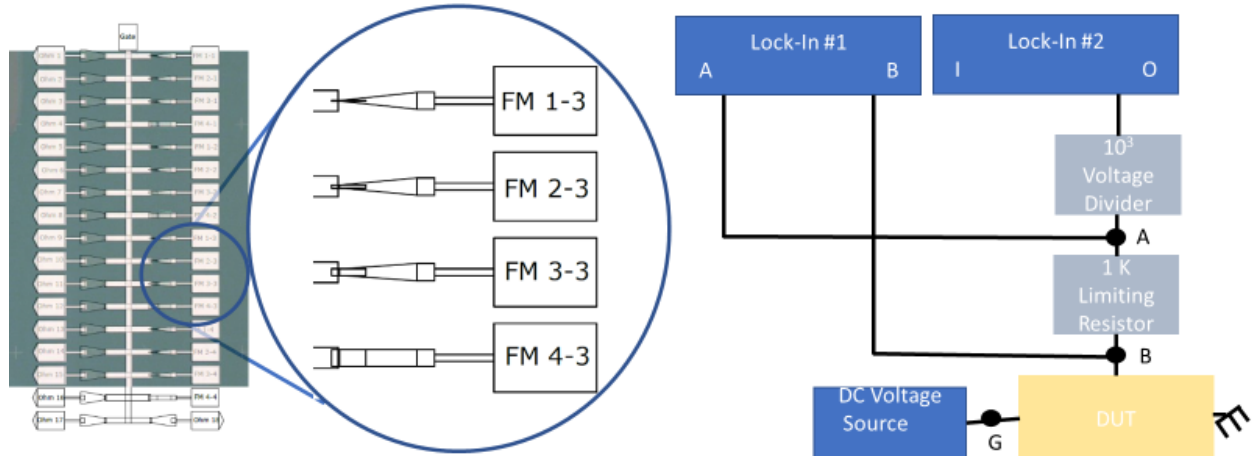


Figure 3-3. Contact metal comparison: (left) Device schematic used to compare the electrical performance of variously sized ferromagnetic contacts (FM) with non-magnetic contacts (NM). (right) Schematic of measurement setup.

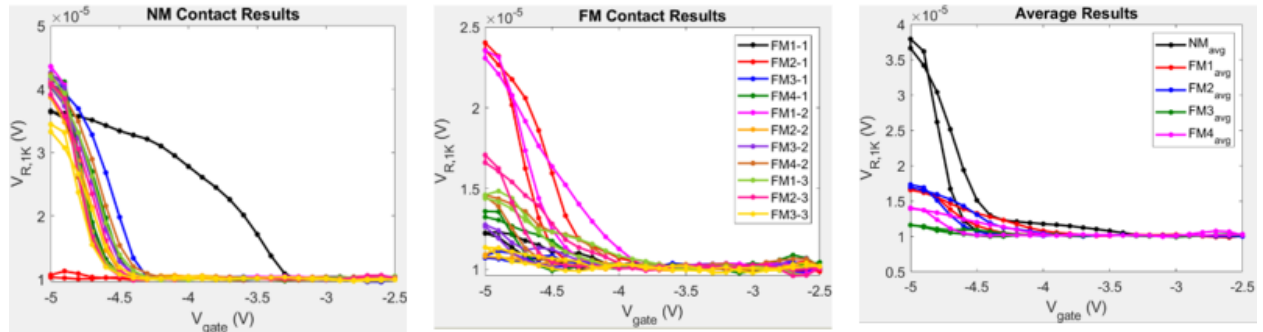


Figure 3-4. Results for contact metal comparison measurement.

In order to test spin injection/detection, we fabricated a set of lateral spin valve devices as shown by Figure 3-5. We were able to verify that the device turned on by testing the PtGe ohmic contacts at each end of the device. Unfortunately, we could not get any conduction from the Mn_5Ge_3 contacts. However, the Hall bar and transmission line devices also fabricated on the sample ended up working as expected.

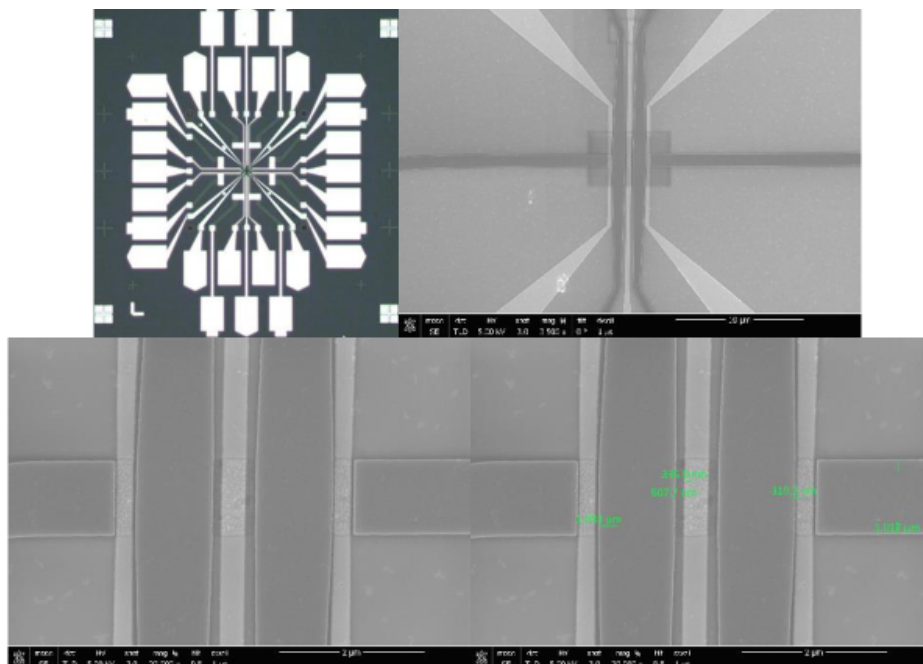


Figure 3-5. Images of a fabricated lateral spin valve device with a undoped Ge/SiGe HFET material stack.

The transmission line devices fabricated were of a standard design that used contacts of the same size separated by various distances: 50, 100, 325, 400, and 675 μm . Figure 3-6 shows the schematic for the measurement setup. While the Mn_5Ge_3 contacts were unreliable, similar to the previous contact testing device, we were able to extract a contact resistance on the order of 1 $\text{k}\Omega$.

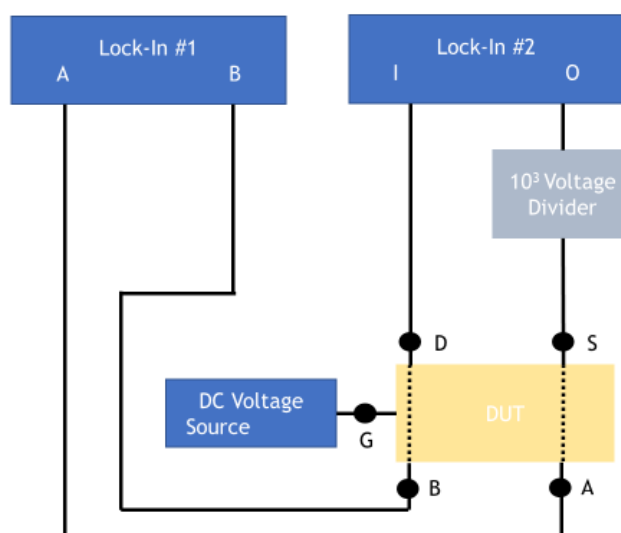


Figure 3-6. Schematic for the traditional transmission line measurement.

The Hall bar devices turned out to be the best devices tested. The Mn_5Ge_3 contacts all reliably provided excellent conduction at 0.3 K. We extracted a saturation density $\sim 7 \times 10^{11} \text{ cm}^{-2}$ with a peak mobility $\sim 2 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. We examined a cross section of the Hall bar devices using TEM and verified that the contacts were Mn_5Ge_3 using selective area electron diffraction. Afterwards, we fabricated Schottky diodes on (100) n-type Ge wafers with a resistivity of $1 - 10 \text{ } \Omega \cdot \text{cm}$. Like most of the previous devices, the Mn_5Ge_3 proved to be unreliable. However, after many trials, we were able to extract a Schottky barrier height of $\sim 0.58 \text{ eV}$ and nonideality factor of 1 for a Mn_5Ge_3 -n type Ge Schottky diode.

3.2. Polarizing hole spins using rare earth permanent magnets

In order to investigate our concept of integrating magnetized ferromagnetic gates near non-magnetic contacts for polarized spin injection, we decided to use commercial rare-earth magnets as our first step proof-of-concept. Previously, it was shown that a low-density 2D hole gas can be completely spin polarized in magnetic fields as low as 0.5 T [18]. Commercial rare-earth magnets can easily be obtained with field strengths upwards of $\sim 1 \text{ T}$ and thus are more than sufficient for our purpose. Furthermore, we were motivated by an experimental setup which used rare earth magnets, in a Helmholtz configuration, to generate a magnetic field of $\sim 1 \text{ T}$ in a dry ^3He fridge [27]. For our purposes, we chose an experimental setup designed around a existing liquid helium dipper probe for the ability to rapidly prototype and perform quick measurements.

Our dipper probe uses standard 2×8 dual-in-line-package (DIP) chip carriers, so we designed our mount to hold a 2×8 DIP chip carrier between two NdFeB magnets in a vertical Helmholtz configuration. This allows the samples to be moved from one measurement probe to another. The basis for the idea and our first design iteration are shown by Figure 3-7. Our initial design was square due to its easier print geometry for a 3D printer and was designed using SolidWorks. It was designed with a 1.25" diagonal to fit into He dewars. However, due to slightly different neck sizes amongst various dewars, we switched to a cylindrical design to be more accommodating despite the increased difficulty in printing. Nonetheless, the first prototype proved that everything fit well together.

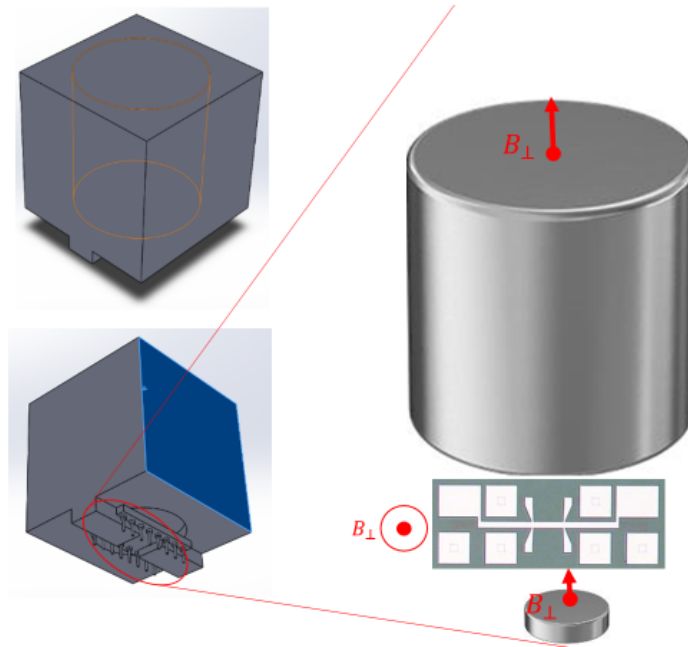


Figure 3-7. (a) Top view of insert with yellow outline indicating the hole for the large magnet. (b) Bottom view of insert showing the DIP chip carrier being held below large magnet. (c) Schematic indicating a Hall bar device in relation the Helmholtz magnet configuration.

Our design uses a 1" diameter, 1" thick NdFeB magnet with a remanence of 1.48 T to produce most of the field felt by the device and is held in place 0.1" above the surface of the device. A smaller 0.25" diameter, 0.625" thick NdFeB with a remanence of 1.48 T is placed underneath the chip carrier creating the Helmholtz configuration enhancing the field through the device. Both magnets were commercially off-the-shelf and purchased through McMaster-Carr. The custom insert that houses the magnets and the chip carrier was 3D printed using polylactic acid filaments due to its wide availability and cost effectiveness. Figure 3-8 shows the assembly of the final insert prototype. First, the insert is 3D printed in two halves. Next, the chip carrier is placed underneath the support tabs which then holds the insert together due to the tight fit. The large NdFeB magnet is then placed in the insert. A separately 3D printed cap is used to keep the large magnet secure from slipping backwards and properly up against the 0.1" spacer. The smaller magnet is then placed centered on the underside of the chip carrier. Finally, everything is held tightly together and anchored to the dip probe with polytetrafluoroethylene tape.

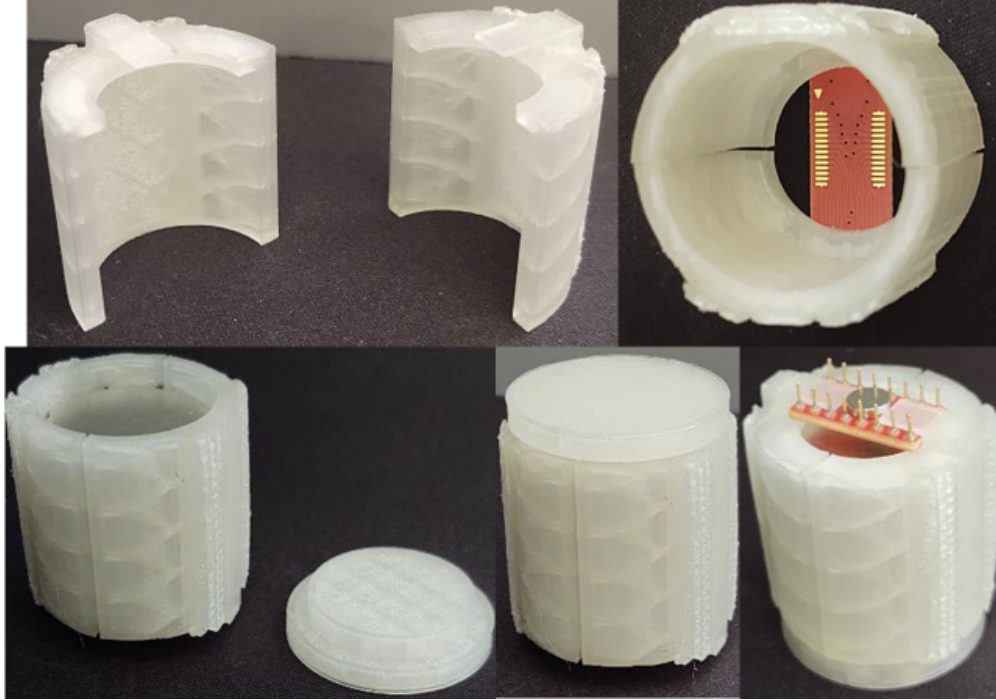


Figure 3-8. Final insert prototype assembly for magnetizing samples using rare-earth magnets.

To estimate the strength of the magnetic field felt by a device in our prototype, we used a calibrated Ge/SiGe HFET Hall bar device. The calibration was performed using another liquid helium dipper probe that uses a superconducting electromagnet to produce the magnetic field which serves as the reference for our permanent magnet probe. The experimental setup is visualized by Figure 3-9. The measurement utilized three SRS830 lock-in amplifiers operating at a frequency of 19.869 Hz. Lock-in amplifiers #1-2 operated in A-B mode to measure the respective transverse and longitudinal voltages, while lock-in #3 operated in I (10^6) mode to measure the current passing through the Hall bar. The sine out (O) of lock-on 3 was set to 0.1 V and was followed by a 10^3 voltage divider before connecting to the device to ensure a low-amplitude signal. Together, the measured current and voltages allow us to determine the transverse resistance R_{xy} and longitudinal resistance R_{xx} . The magnetic field was swept from 0 – 1 T at each gate voltage which were stepped from 0 to -10 V. The gate voltages were set by a Keithley 2400 source meter while the magnet was controlled by a KepCo power supply.

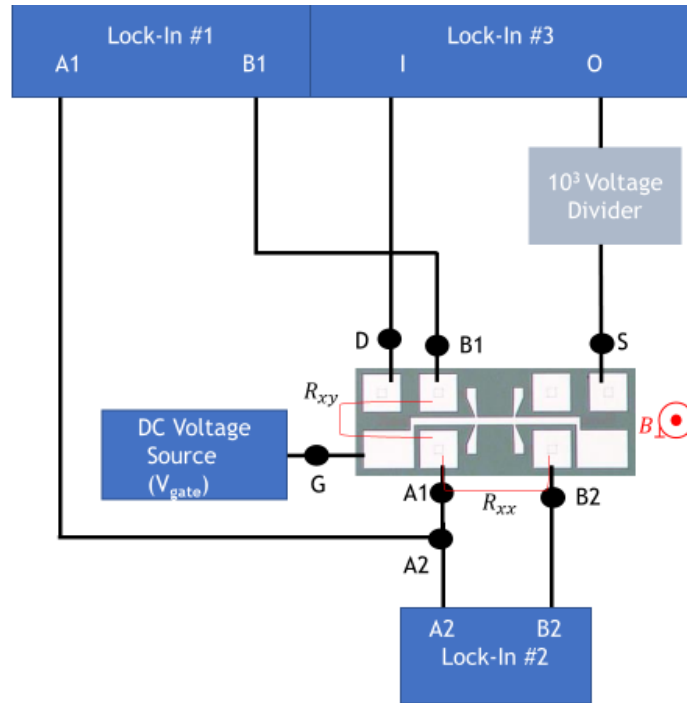


Figure 3-9. Schematic for Hall effect measurements. The magnetic field B is provided by an electromagnet or rare-earth permanent magnets.

The slope from the linear fit of R_{xy} , as a function of magnetic field, is the Hall coefficient. The Hall coefficient is measured as a function of gate voltage for the Hall bar device as shown in the left image of Figure 3-10. The Hall coefficient is used as the calibration for the measured magnetic field from the rare-earth magnets. We measured the effective magnetic field from both the single large magnet (black curve) and the Helmholtz configuration (red curve). The center and right images of Figure 3-10 show the I - V and R_{xy} vs. V respectively. To ensure an accurate and fair comparison of the effective magnetic fields, we use the values obtained at saturation ($V_{\text{gate}} = -7\text{V}$) where the measured current is the same. Therefore, the measured R_{xy} values differ purely from the magnetic field strength. At $V_{\text{gate}} = -7\text{ V}$, the Hall coefficient has a value of $2179\text{ }\Omega/\text{T}$ and R_{xy} has values of $846\text{ }\Omega$ and $1815\text{ }\Omega$ for the single and Helmholtz configurations respectively. The effective magnetic field is obtained by the ratio of R_{xy} to Hall coefficient yielding values of 0.39 T for the single magnet configuration and 0.86 T for the Helmholtz configuration.

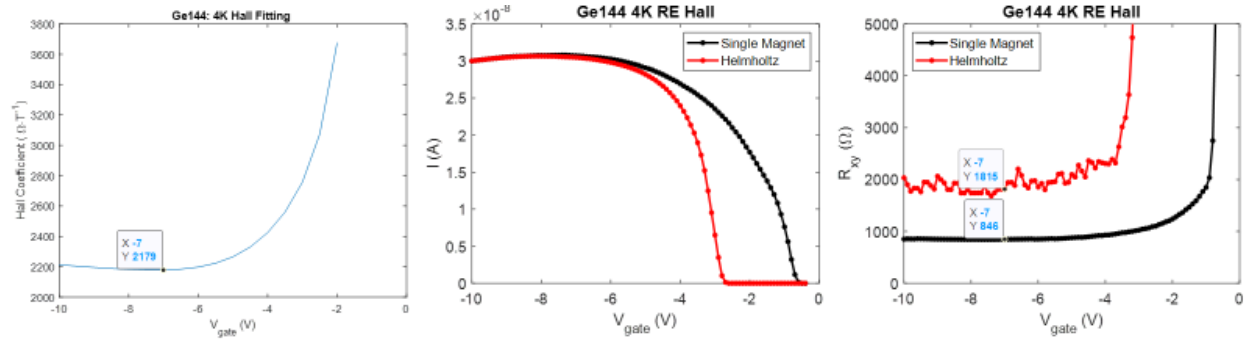


Figure 3-10. Rare-earth magnet Hall probe calibration results: (left) Hall bar device calibration curve, (center) I-V curve for the Hall bar device in the rare-earth magnet probe, (right) transverse resistance vs. gate voltage for Hall bar in rare-earth magnet probe.

With a measured effective magnetic field of 0.86 T, our rare-earth magnet Hall probe, in a Helmholtz configuration, can be used to fully polarize spins of a low-density 2D hole gas [18]. However, the prototype could use a few improvements. If the thickness of the 0.1" spacer is reduced, then the magnetic field will increase for both configurations. It may be possible to obtain a strong enough field with a single magnet. Also, if pin extension header is added to the chip carriers, then they would fit better and make a better electrical connection for the Helmholtz configuration. This would also open the opportunity for using a thicker bottom magnet to further increase the magnetic field.

3.3. Summary

We have tested and confirmed the formation of Mn_5Ge_3 after Mn/Ge and Mn/Ge/SiGe stacks were annealed in an RTA. The ferromagnetic contacts were used in electrical characterization of Ge/SiGe HFET devices. While the contact reliability needs further improvement, we obtained an estimate of the contact resistance between Mn_5Ge_3 and the Ge channel. These ferromagnetic contacts remained functional during high-field magneto-resistance measurements at 0.3 K. We assembled a probe using 3D printing and commercially available rare-earth magnets to apply high magnetic fields to Ge 2D holes to polarize the spins. Calibration based on electromagnets showed that a magnetic field as high as 0.86 T was obtained in a Helmholtz configuration. This magnetic field is sufficiently high to fully polarized the spins of a low-density 2D hole gas. Further miniaturization and on chip integration of rare earth nano-magnets could enable local polarization of hole spins, resulting in effective spin injection without the need for ferromagnetic contacts.

4. METAL-ASSISTED CHEMICAL ETCHING OF GE

MACE is a semiconductor processing technique that has been used to create large aspect ratio nanostructures like nano-pillars [28], nano-holes [29], and nano-fins [30]. These structures have been used in practical devices like low-reflection photodetectors and fin FETs. The accepted chemical mechanism for etching in the presence of metals is as follows: the noble metal donates holes to the semiconductor; the hole-rich semiconductor reacts with the etchant more easily than does the intrinsic semiconductor; the surface product of this reaction – sometimes but not always an oxide of the semiconductor – is dissolved into solution; the cycle starts again on the next layer of semiconductor exposed to solution [31][32]. Ge, which is more reactive than Si, is etched by H_2O_2 even in the absence of a metal catalyst [33][34][35][36][37][38].

Using dilute H_2O_2 as the etchant, Ge as the semiconductor, and Au structures as the metal catalyst, we investigate in this project the dependence of etch depth on etchant concentration and on proximity to Au.

4.1. Processing

The processing steps are shown in Figure 4-1. Undoped germanium in the $\langle 100 \rangle$ crystal orientation is soaked in 15% HCl, rinsed in de-ionized water, soaked in 7% H_2O_2 and rinsed. This sequence is repeated two more times. Since photoresist does not adhere well to Ge, initially 2 nm of Al_2O_3 is deposited by ALD at 250 °C, and then the wafer is removed and stripped in an oxygen plasma. The sample is heated at 110 °C for one minute before spinning AZ5214 photoresist, followed by another minute of heating. The resist is exposed and developed such that resist is everywhere, except for a ring of 2 nm thick Al_2O_3 . A quick dip (5 seconds) in BOE removes the exposed Al_2O_3 . After depositing 40 nm of gold, soaking in solvents, and lift-off, a gold ring on bare Ge remains, surrounded by a 2 nm film of Al_2O_3 on bare Ge.

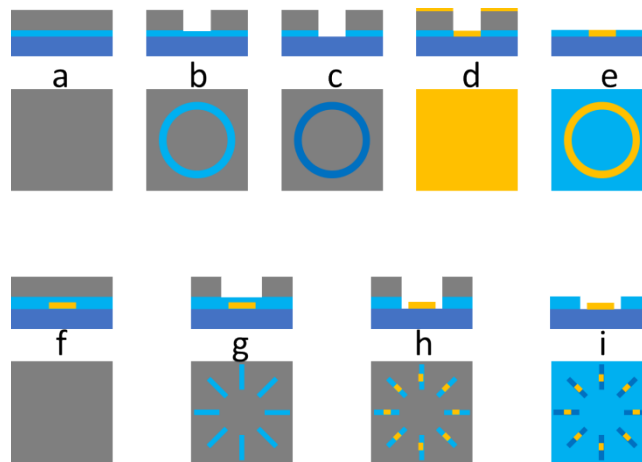


Figure 4-1. Process flow, showing sample cross section (smaller, layered images) and top view (larger squares) at each step. (a) Unpatterned germanium with first oxide layer and resist. (b) Resist pattern for gold deposition. (c) Oxide etch. (d) Gold deposition. (e) Liftoff. (f) Second oxide layer and resist. (g) Patterned resist. (h) Oxide etch. (i) Removal of resist.

A second layer of Al_2O_3 , of thickness 50 nm, is deposited by ALD at 250 °C, and then the wafer is removed and stripped in an oxygen plasma. A series of windows, like spokes concentric with the

gold ring, are photolithographically patterned. The exposed oxide is removed with BOE. Finally, the resist is removed, and we are left with rectangular strips of bare Ge, with a small area of Au in the middle. The strips are oriented at angles from 0° to 345°, in increments of 15° (Figure 4-2 left). In addition, a “control” sample is fabricated with the gold ring absent (Figure 4-2 right).

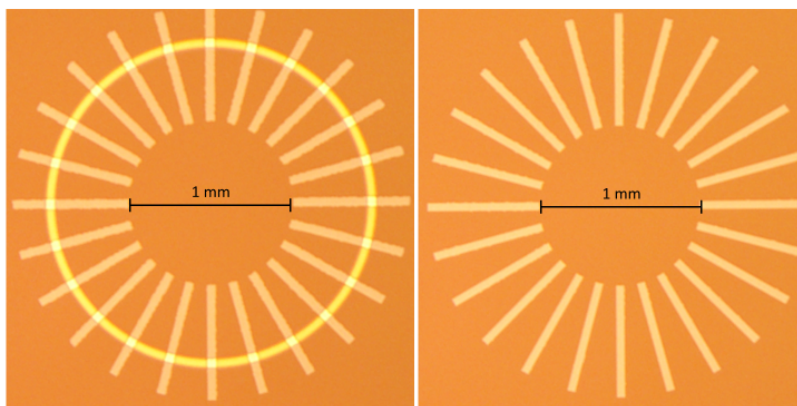


Figure 4-2. Left: Gold ring with “spokes” of bare germanium. Except for the gold and the spokes, the sample is coated with Al_2O_3 . Right: Control sample with no gold.

The samples are soaked in a mixture of stockroom H_2O_2 (30%) and de-ionized water, for one hour. The dilutions range from 1:20 to 1:500.

4.2. Surface profile resulting from MACE

At length scales on the order of a micron, the etch profile shows an angular dependence (Figure 4-3). At longer length scales, the etching is isotropic (Figure 4-4).

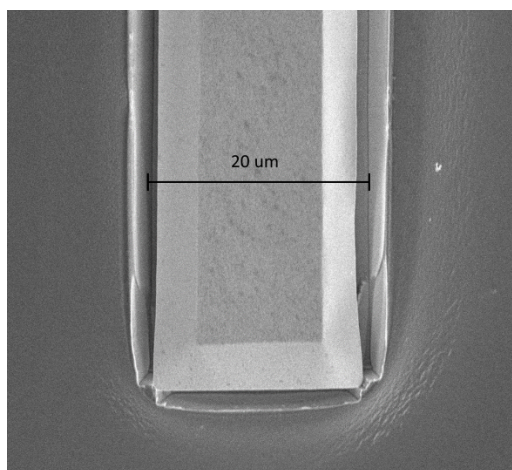


Figure 4-3. An SEM micrograph after etching. The indented corners at the bottom are evidence of unequal etch rates along different crystal axes.

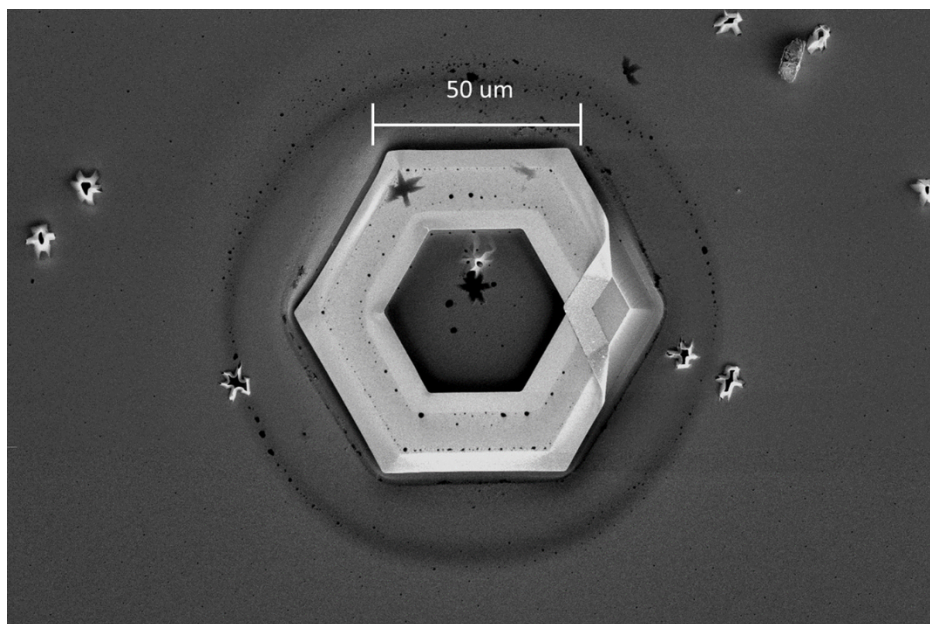


Figure 4-4. An SEM micrograph after etching. The Au hexagonal ring on the right has started to peel off. The bird-like particles are Al_2O_3 .

The wheel-and-spokes structures described in the processing section are useful for studying the dependence of etch depth upon H_2O_2 concentration, at length scales greater than a micron.

We measure the etch profile with a profilometer, as shown in Figure 4-5. The central plateau is Au. Most likely, etching has occurred beneath the gold, but it is not registered by the tip of the profilometer. In principle, gold could be easily removed with a aqueous solution of I_2 and KI [39], but the same solution also attacks Ge. The plateaus at the left and right are Al_2O_3 . We see dramatic enhancement of the etching near the Au strip. The different etch depths to the left and right may reflect the true topography, or they may be an artifact of the profilometer traversing an abrupt change in height. No effort was made to characterize the possibility of this artifact.

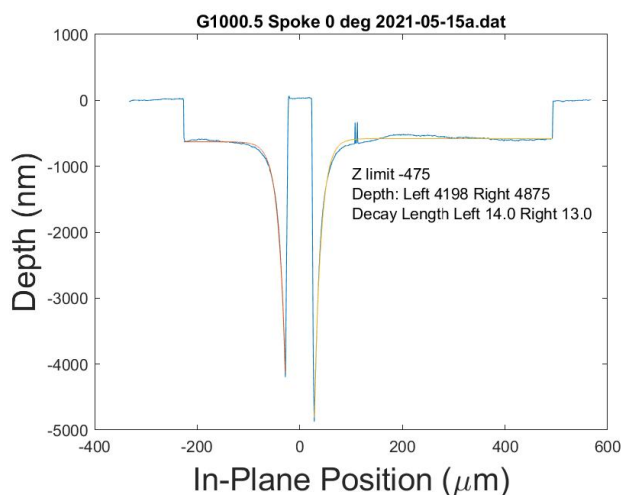


Figure 4-5. Profile of etch depth along a 0° spoke. The stock 30% H_2O_2 is diluted in water (H_2O_2 : H_2O = 1:100).

4.3. Summary

We have measured Au enhanced etch-depth profiles of intrinsic Ge. Based on the measurements, we have proposed an empirical formula of the etch profile. Etching enhancement is strongest close to the Au strip and decays exponentially with distance away from the Au strip. The decay length is independent of H_2O_2 concentration. The magnitude of the enhancement is proportional to the concentration raised to 0.2.

The measured etching decay length (d) is of the same order of magnitude of the Debye screening length for holes in Ge, which is a function of doping. To elucidate the mechanism of MACE, it would be interesting to repeat these experiments with n- and p-doped Ge.

We fit the etch profile, for a given side of the Au strip, as an exponential with an offset:

$$z = z_{\infty} - \Delta z e^{-x/d}$$

z_{∞} is the etch depth of Ge far from the Au strip, without enhancement. Δz , which we call the enhanced etch depth, is the difference between the etch depth next to the Au strip and the etch depth far from the Au strip. d is the exponential decay length with which the enhanced etch depth diminishes. The variation of the enhanced etch depth with the concentration of the etchant is fit to a power law:

$$\Delta z \propto \rho^{\xi}$$

where ρ is the concentration of H_2O_2 and ξ is approximately 1/5. We do not propose a physical reason for this empirical value of ξ . Earlier authors investigating the etching of Ge without the enhancement from Au as a function of H_2O_2 concentration have reported a power law with roughly the same value of ξ [33]. Unlike the etch depth, the decay length (roughly 15 μm) is independent of concentration. This decay length is of the same order of magnitude as the Debye screening length for holes in Ge.

5. CONCLUSION

In this project, we investigated several approaches to creating hole devices in germanium-based materials as well as injecting and manipulating hole spins in such structures. We also explored MACE of Ge with potentially a hole injection mechanism. Our main results include the demonstration of Ge MOSFETs operated at cryogenic temperatures, ohmic current-voltage characteristics in Ge/SiGe heterostructures with ferromagnetic contacts at deep cryogenic temperatures and high magnetic fields, evaluation of the effects of surface preparation on carrier mobility in Ge/SiGe heterostructures, and hole spin polarization through integrated permanent magnets. These results serve as essential components for fabricating next-generation germanium-based devices for microelectronics and quantum technology.

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