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ABSTRACT

Fully coupled randomly disordered recurrent superconducting networks with additional open-ended channels for inputs and outputs are considered the basis to introduce a new architecture to neuromorphic computing in this work. Various building blocks of such a network are designed around disordered array synaptic networks using superconducting devices and circuits as an example, while emphasizing that a similar architectural approach may be compatible with several other materials and devices. A multiply coupled (interconnected) disordered array of superconducting loops containing Josephson junctions [equivalent to superconducting quantum interference devices (SQUIDs)] forms the aforementioned collective synaptic network that forms a fully recurrent network together with compatible neuron-like elements and feedback loops, enabling unsupervised learning. This approach aims to take advantage of superior power efficiency, propagation speed, and synchronizability of a small world or a random network over an ordered/regular network. Additionally, it offers a significant factor of increase in scalability. A compatible leaky integrate-and-fire neuron made of superconducting loops with Josephson junctions is presented, along with circuit components for feedback loops as needed to complete the recurrent network. Several of these individual disordered array neural networks can further be coupled together in a similarly disordered way to form a hierarchical architecture of recurrent neural networks that is often suggested as similar to a biological brain.

I. INTRODUCTION

Neuromorphic computing has been gaining more and more interest recently due to several reasons such as (1) an approach for a power-efficient alternative to digital computing,[1,2] (2) a way to solve the problem of von Neumann bottleneck between the processor and memory,[3] or (3) in simulating aspects and gaining a better understanding of a biological brain,[4,5] etc. Depending upon the problem, different hardware approaches and models of the network elements in the neuron have been considered. For example, the Hodgkin–Huxley neuron model[6] is a popular and accurate representation of a biological neuron and is used in spiking neural networks[7] as well as mimicking biological behavior.[8] The McCulloch–Pitts neuron model[9] is popular with artificial neural networks that are used in convolutional neural networks.[10] Similarly, biologically inspired synapse models are compatible with spiking neural networks[11] and exhibit learning rules corresponding to spike timing-dependent plasticity.[12] Also, artificial synapses for largely feed-forward and non-spiking networks are also available.[13,14] In this article, we attempt to provide a novel approach to neuromorphic computing, which is not particularly designed to solve a specific problem in the existing computing paradigm, but to present a new architecture that may address several of the aforementioned aspects, while also attempting to provide an alternative perspective into the process of neuromorphic computing in general. Nevertheless, the superconducting network components considered here are compatible with spiking neural networks, and leaky integrate-and-fire neurons that may permit the development of a superconducting neural network can enable further exploration of the architecture.

There are two important aspects to consider when building a neural network. The first aspect involves identifying appropriate materials, devices, and circuits that closely emulate biological

aspects of elements such as neurons, synapses, and dendrites. Several such materials and devices are being studied and implemented with some degree of success,[15–27] particularly in studying memristive and phase-changing materials for synaptic connections and spiking behavior for neurons. The second aspect to consider involves scalability and power efficiency. A human brain comprises roughly 8.3×10^9 neurons with about 6.7×10^{13} synaptic connections between them[28,29] and consumes approximately 20 W of power.[30] Replicating this using artificial circuit elements to achieve similar power efficiency and connectivity currently presents some severe challenges, although rapid progress is being made in this area.[31–34]

The hardware challenges with respect to scalability can be addressed by increasing the density of processing power into smaller areas. A straightforward path to overcome this issue is by increasing the density of interconnections through further development of the IC fabrication techniques and also by decreasing the footprint of the individual elements used in the circuits. We present a collective synaptic network approach that could considerably improve the scalability factors of the already existing technologies by utilizing the exponential scaling of the memory capacity of disordered and coupled networks. In this example, all the neurons in a network are connected to each other through a disordered array of superconducting loops encompassing Josephson junctions, instead of establishing distinct synaptic connections between each pair of neurons. The details of the dynamics of such a network are discussed in Sec. II, using equivalent lumped-element circuit simulation results to demonstrate their operation. However, the idea is to replace a large number of individual interconnections between neurons with a system of a collective synaptic network that resembles or exceeds in complexity when compared to a traditional network, while any individual connection between neurons in such system exhibits synaptic behaviors in the form of spike timing and rate-dependency based learning rules. Watts and Strogatz[35] established that, in recurrent networks with fixed numbers of interconnections between them, small-world and random networks exhibit enhanced computational power, signal-propagation speed, and synchronizability compared to an ordered network. Therefore, introducing disorder to a highly interconnected network allows us to take advantage of lower computational power consumption and higher speed in addition to the specified increase in scalability by a significant margin. Furthermore, the tight coupling between all the interconnections causes the system to directly update its configuration with changing input and output signals of any neuron, instead of updating weight of each connection separately. This results in an exponential increase in the number of non-volatile memory configurations available (some more stable than others) with an increasing number of nodes in the network as shown in Sec. II. The dynamics guiding the emergent properties of such small-world or random network and the corresponding learning principles can be studied with the help of superconducting neural network elements introduced in Secs. II A–II D. Furthermore, such a network made of disordered arrays of superconducting loops can be used to construct a dense recurrent neural network even with the existing well-established technologies.[36–39]

In addition to the synaptic network, several other compatible network elements are presented, with circuit simulations, which together form a recurrent neural network with a hierarchical architecture, similar to a biological brain.[40] First, we introduce a design for a compatible leaky integrate-and-fire neuron with a dynamically updating threshold value. It is comprised of a large superconducting loop with a stack of Josephson junctions, with inputs occurring both in the form of direct spike trains from other neurons or as an equivalent continuous current signal corresponding to the incoming spike trains. The neuron circuit is described in detail in Sec. III.

Second, the feedback mechanism in this network is implemented through inductively/magnetically coupled circuits that are similar to that introduced by Shainline *et al.*[41] A large number of input spike trains can be fed into the neuron through a cascade of merger circuits[42] or through inductive/magnetic coupling into the current bias of the neuron if necessary. These various additional circuit elements are presented to underscore that a conceptually complete recurrent neural network can be built with the hierarchical architecture, using several disordered array networks, as detailed in Sec. V. The individual recurrent networks formed by neurons and a disordered array network are in turn connected to each other through a larger hierarchical disordered array, therefore representing self-similarity at the lower and higher levels, as often found in biological brains.[40] This approach can be followed to develop a more complex network with several additional disordered array structures at higher levels. A practical implementation of this network may require additional network components or modifications to the presented circuits for specific applications. But the emergent phenomenon of the disordered arrays and the principles governing their dynamics can be studied using the superconducting circuits presented in this paper.

II. DISORDERED ARRAY SYNAPTIC NETWORK

A. General overview

A disordered array of superconducting loops containing Josephson junctions in them is used as a collective synaptic network that can connect several neurons together. It forms a network where each neuron is connected to every other neuron as shown in Fig. 1(a), but with additional open-ended channels into it

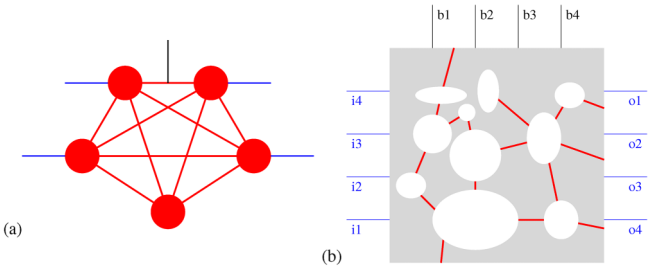

FIG. 1. (a) Fully recurrent neural network. Red circles represent neurons, and the respective red links represent synapses. Blue lines are input and output channels, while black lines are for feedback. (b) Disordered array synaptic network using superconducting loops. The gray area represents superconducting material, and the red lines signify positions of weak links that form Josephson junctions.

to connect to input/output neurons and to make feedback/feed-forward loop connections to synapses. Together with the feedback loops, the network is fully recurrent. A schematic of a disordered array of superconducting loops with Josephson junctions is shown in Fig. 1(b). The signal propagation in these networks occurs in the form of single-flux quantum voltage pulses/spikes generated at the Josephson junctions when the current through them exceeds a critical current.[42] The flux quanta are stored in the superconducting loops in the form of persistent loop currents. The number of flux quanta (and the corresponding persistent current) that each loop can store depends on the material and physical dimensions of the loop and therefore the resulting geometrical inductance, along with the Josephson junction parameters such as its critical current. The disordered array shown in Fig. 1(b) can be resolved into an equivalent lumped element circuit model for analysis as discussed in detail below. This results in dynamically changing current paths between any two nodes in the disordered array, as different junctions switch to produce single-flux quantum spikes. The stable loop currents of each state represent the memory configuration of the system.

The input and output signals, shown in Fig. 1(b) as "$i1, i2, \ldots$" and "$o1, o2, \ldots$," respectively, are spiking voltage pulses while the biasing signals "$b1, b2, \ldots$" are continuous but time-varying current inputs. The output voltage spikes are measured across Josephson junctions. The synaptic weight of an individual connection between any two neurons in the array is a characterization of the total current between the two corresponding nodes, which is the cumulative current from various dynamically changing paths between those two nodes. Therefore, the corresponding output spike generation across a junction depends on the input signals as well as the configuration of various loop currents from the previous state of the network. Therefore, the synaptic weight between any two nodes of the network can be calculated as shown in Eq. (1). The memory configuration of the network is sensitive to output signals when the output spike train is coupled to biasing currents in the form of a feedback loop. The feedback mechanism is discussed in Sec. III. Note that the feedback/feed-forward can also occur from another synaptic network from a different hierarchical level, as discussed in Sec. V. Changing the bias currents can change the memory/loop current configuration of the network and, therefore, the individual weights between any two neurons. While the feedback/feed-forward coupling to the biasing channels can enable unsupervised learning processes, the bias currents can also be updated manually to initialize the weights, or to update them when they are saturated. Further investigation is needed to develop specific programming methods to update the bias manually to interact with the emergent dynamics of the disordered system.

The dynamically changing synaptic weight between any two neurons in the network can be calculated using

$$\textit{Synaptic weight} = \frac{\textit{Number of spikes at the output neuron}}{\textit{Number of spikes at the input neuron}}. \quad (1)$$

If each of the loops in the array can be designed to satisfy $LI_C/\Phi_0 > 1$, where L is the inductance of the loop, I_C is the critical current of the junction, and Φ_0 is the magnetic flux quantum, then the loop can at least allow a circulating current corresponding to at least one flux quantum Φ_0 in the loop before the junction in it generates a spiking voltage pulse. More specifically, in the case of $\Phi_0 < LI_C < 2\Phi_0$, each loop can at least be in one of the three configurations corresponding to $+\Phi_0$, $-\Phi_0$, and 0 of clockwise, anticlockwise, and zero loop currents, respectively. Therefore, a disordered array with n different loops can have at least 3^n different memory configurations resulting in an exponential scaling of

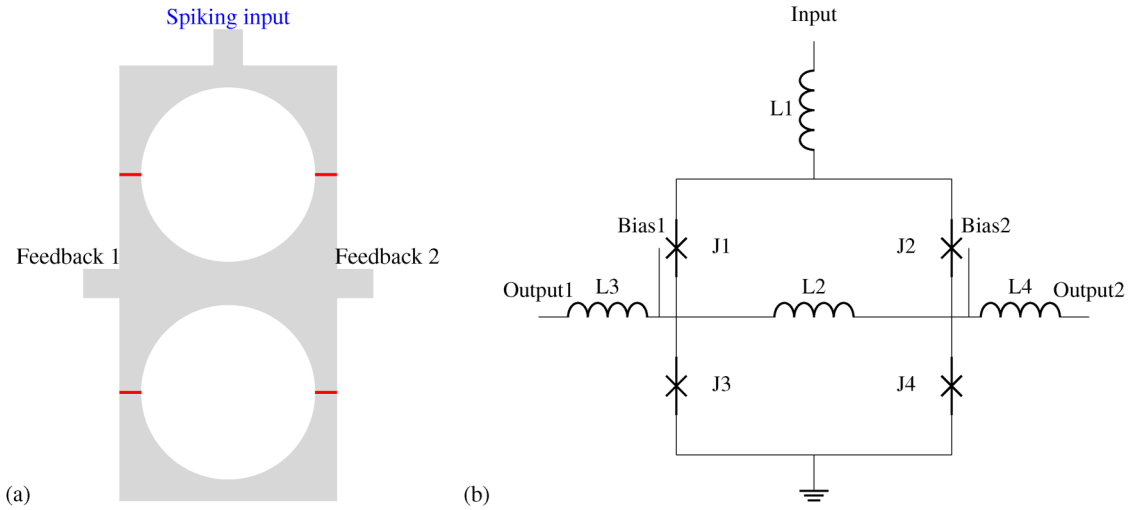

FIG. 2. (a) Three-state synaptic network formed using two loops with one input, two outputs, and two bias current channels. Josephson junction barriers are shown in red, while the gray area represents the superconducting material. (b) Equivalent lumped-element circuit model with junctions and inductors. Outputs are voltage spikes measured across J3 and J4 as shown.

memory capacity with increasing number of loops. This number can be even higher if some of the loops are larger and can accommodate more than a single Φ_0 in them (i.e., $LI_C/\Phi_0 > 2$). However, any degree of symmetry in the array will result in some redundant (degenerate) configurations, where the resultant weights between the nodes are identical between them. A maximum number of configurations for a given array can be achieved when the disorder is highest, with no degree of symmetry representing a random network, while any degree of symmetry represents a small-world network.

Establishing mathematical principles that guide the circuit dynamics can help understand the emergent properties of the disordered network. Such studies could also provide insight into whether specific application-related algorithms can be programmed in the form of particular small-world network array patterns. However, certain spike-timing and rate-dependency aspects of the synaptic weights in disordered networks can be demonstrated using a simpler and easier method to analyze arrays comprising two and three loops with arbitrarily chosen parameters. While a larger array may be more difficult to predict, various aspects of signal dynamics that occur in the simpler subset of two or three loops in the array can be understood from the following examples.

An example of an array larger than two or three loops is shown in Fig. 1(b), that is based on the planar YBCO-based Josephson junction process developed by Cybart *et al.*[39,43] We note that it is possible to manufacture such an array with several other existing popular Josephson junction circuit processes.[36–39]

B. A symmetric array 1 × 2 three-state synaptic network example

A "simple" synaptic network is designed to connect to one input neuron and two output neurons as shown in Fig. 2(a). The network also has two current bias channels that can be connected to feedback. The simplest form of this system is symmetric, with identical Josephson junction pairs $J1$, $J2$ and $J3$, $J4$. The inductance of the loops is assumed to be symmetrically distributed and, therefore, can be characterized using lumped element inductors as shown in Fig. 2(b). The Josephson junctions are shown as red lines that define the barrier in Fig. 2(a) along with the superconducting material characterized by inductances. The circuit equivalent used for simulations is shown in Fig. 2(b). The input excitations are chosen to represent an incoming spike train from an adjacent neuron, and the bias inputs are chosen to represent continuous current inputs from the feedback mechanism discussed in Sec. IV. The corresponding simulation results are shown in Fig. 4. The frequency of the input spike train is fixed and both the bias signals are current ramps with constant slopes as shown in Figs. 4(a), 4(b), and 4(e), respectively. Therefore, these excitations together represent a short time duration of the operation of the array, whereas the input and the biasing signals are expected to follow significantly complex dynamics at longer time scales. Note that the actual time scales used, i.e., the input time period of a few hundred picoseconds and the bias ramp rates of several micro-amperes per nanosecond, are not important for the operation of the circuit. However, the relative time scales such as the bias ramp rates with respect to the input frequency along with their respective magnitudes determine the synaptic weight as demonstrated in Figs. 4(i) and 4(j).

While two loops designed to satisfy $1 < LI_C/\Phi_0 < 2$ can have $3^n = 9$ configurations for the two loops ($n = 2$), the symmetry in the circuit restricts the total number of distinct configurations to four, while strong coupling between the outputs makes them almost identical. The various current paths and loop current components between input node and output junctions for four distinct configurations are shown in Fig. 3. Note that the currents in the opposite directions that can generate negative voltage spikes are also possible, but the circuit operation corresponding to them is identical to these four configurations. The circuit is simulated and the results of input, output, and bias signals as a function of time are shown in Fig. 4.

The circuit operation is similar to that of a T flip-flop or a frequency divider,[44] with additional, dynamically varying bias current signals that result in four different loop current states specified. Therefore, the input voltage spikes drive the incoming current through the junctions. The actual parameters and conditions used for circuit simulation are provided in the supplementary material for all the simulation results presented in this article. However, as the circuits are disordered arrays, the choice of parameters is not critical to understand the operation of the synaptic network. Different choices of parameters produce different emergent loop configuration dynamics. But practically plausible physical parameter values are chosen for simulations shown in Fig. 4 to demonstrate features of a spiking neural network.

When the bias currents are zero, the incoming spikes are insufficient to exceed critical currents of either of the junctions to generate an output voltage spike resulting in configuration 1 in

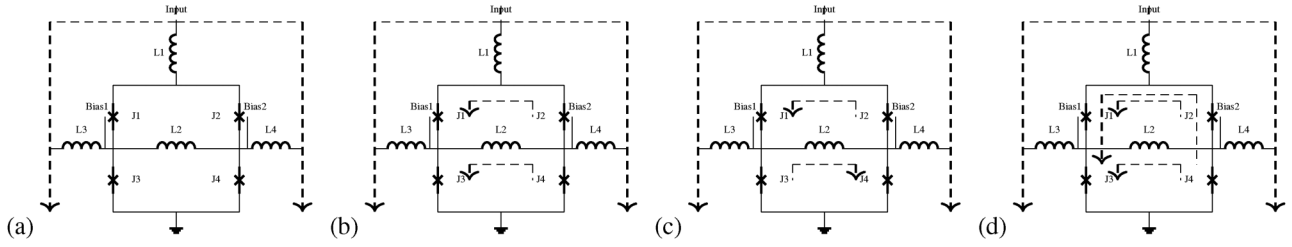

FIG. 3. Relative current directions corresponding to four different configurations/synaptic weights possible in the symmetric 1 × 2 three-state synaptic network shown in Fig. 2.

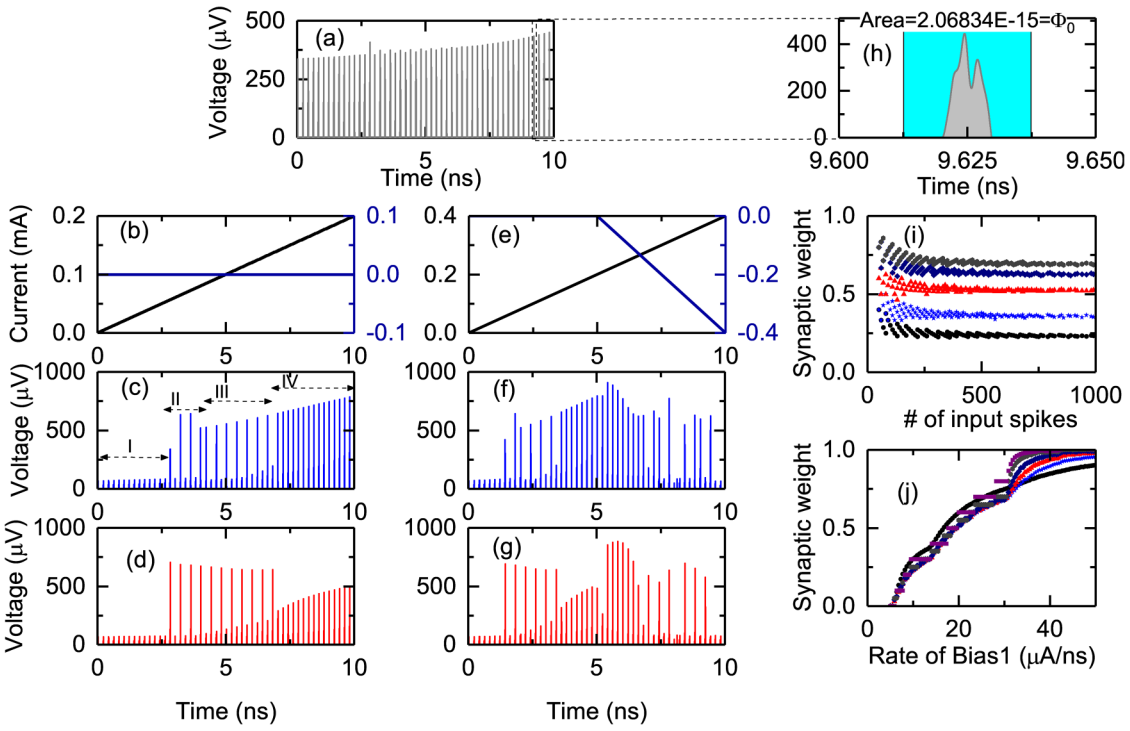

FIG. 4. Simulation results of the three-state synaptic network shown in Fig. 2. (a) Input spike train with constant frequency and magnitude. [(b) and (e)] Bias current signals. Black curve represents current through bias 1, and the blue curve represents current through bias 2. [(c) and (f)] Output spike trains measured across junction J3 of Fig. 2 (i.e., output 1), The four different configurations corresponding to different synaptic weights are highlighted in (c). [(d) and (g)] Output spike trains measured across junction J4 of Fig. 2. (h) Magnified view of a single spike demonstrating a single-flux quantum voltage pulse. (i) Synaptic weight, defined as the ratio of a number of output spikes to number of input spikes, plotted as a function of the number of input spikes in 10 ns, for different values of bias current slopes. Bias current slopes: ●-10 μA/ns, ★-15 μA/ns, ▲-20 μA/ns, ♦-25 μA/ns, and ⬢-30 μA/ns. (j) Synaptic weight, defined as the ratio of the number of output spikes to the number of input spikes in 10 ns, plotted as a function of slope of the bias current, for different numbers of input spikes. Number of input spikes : ●-1000, ★-200, ▲-100, ♦-50, ⬢-20, and ■-10.

Fig. 3(a), and no spikes are generated at the output. This corresponds to a synaptic weight of zero. As a ramp current input with a certain slope is applied to one of the bias inputs while the other bias input is zero, the circuit cycles through its four configurations at different bias current values. Both the outputs start to generate identical spike trains as the current from constant frequency input spikes and the bias current together are sufficient to switch junctions $J3$ and $J4$ to a dynamical state generating voltage spikes. At certain current biases, as the junctions $J3$ and $J4$ together exceed their respective critical currents with each incoming spike, the output spike frequency is half that of the input frequency resulting in a synaptic weight of 0.5. This operation corresponds to the second configuration as shown in Fig. 3(b) and occurs between 2.5 ns and 4 ns in Figs. 4(b)–4(d). The circuit transitions into the third configuration at a higher bias current value where the output frequency is unchanged, but the spike generation oscillates between both the outputs as observed between 4 ns and 7 ns in Figs. 4(b)–4(d), corresponding to junctions $J3$ and $J4$ switching alternatively as the loop current in $J3 - L2 - J4$ cycles between $+\Phi_0$ and $-\Phi_0$. As the current bias further increases, both the output spike trains are identical, but a higher current bias can generate voltage spikes across both junctions $J3$ and $J4$ simultaneously with every input spike. The weight between input and both the outputs are 1 in this state as observed after 7 ns in Figs. 4(b)–4(d). Both the outputs are identical due to the symmetry of the system and strong coupling between the output junctions. Although there are four configurations available, there are only three useful states corresponding to weights of 0, 0.5, and 1, making it a three-state synapse.

When both the current biases are active, the system cycles through the same four memory states but the transitions occur at different times and at different current values as shown in Figs. 4(e)–4(g). The weight/configuration of this network, therefore, depends on the input spike timing and/or frequency, the number of input spikes, and the slopes of the bias currents. The slopes can be either positive or negative as illustrated in Fig. 4(e), corresponding to either positive or negative feedback coupling.

Therefore, the memory configuration of the array is a function of two variables that are dependent on each other: the number/rate of the input spikes and the rate of change of the bias currents (i.e., the slope of the bias current signal). However, as the output signal is coupled to the bias current signal through a feedback loop as

discussed in Sec. IV, the slope of the bias current signal is proportional to the frequency of output spikes. Therefore, the synaptic weights between any two neurons are dependent on the relative timing and the rate of spikes of the input and the output signals. Figure 4(i) shows the dependence between the synaptic weight calculated using Eq. (1) as the ratio between the number of output spikes measured across $J3$ of Fig. 2 and the number of input spikes in a fixed time period of 10 ns. The input frequency is kept constant, while the bias current is linearly varied during this time period. The simulation results are shown for different bias current increase rates (slopes) in Fig. 4(i). As evident in the results, for a fixed output frequency (or bias current slope), the synaptic weight converges to a fixed value after 500 input spikes. The number of input spikes required for convergence changes with changing input frequency. Furthermore, different choices of bias current slope result in different convergent synaptic weight, indicating that the weight can be varied between 0 and 1 with the choice of bias current slopes. This is also evident in Fig. 4(j). Figure 4(j) shows the dependence between synaptic weight and the slope of the bias current (equivalent to output frequency). The results for different numbers of input spikes during the fixed time interval of 10 ns (equivalent to different input frequencies) are shown. Increasing the bias current slope increases the synaptic weight non-linearly. For the given set of input frequencies seen in Fig. 4(j), thresholds appear at certain bias current frequencies, such as at 15 μA/ns and 30 μA/ns where the synaptic weight appears to saturate as constant frequency input spikes are applied. The input frequency determines the resolution of weights that can be accessed between 0 and 1. Together, Figs. 4(i)–4(j) highlight the spike-timing and rate dependencies of input and output signals on the synaptic weight.

C. 3-loop 1 × 2 synaptic network example

The three-state synaptic network introduced in Sec. II B describing two loops is a highly constrained and symmetric (degenerate) system and was chosen to demonstrate the basic dynamics of a disordered array even though the symmetry resulted in degenerate memory configurations. Even this three loop geometry offers more options and complexities. Introducing some disorder in the system in the form of asymmetric geometry exponentially increases the number of configurations/states available, thereby transforming it to a complex system, while exhibiting similar time and rate-dependent dynamics with respect to input signals and output signals through feedback. A complex 3-loop disordered array system is chosen to demonstrate the dynamics of a network with 1 input and 2 outputs as shown in Fig. 5(a). In the equivalent circuit shown in Fig. 5(b), we allow no two junctions to be identical to each other. Furthermore, the inductance is asymmetrically distributed around loops. The inductor values and Josephson junction parameters are arbitrarily chosen, with a restriction to only allow up to 1 single-flux quantum in each of the loops. The actual parameters used in the simulation results are provided in the supplementary material. The circuit can be in up to $3^3 = 27$ different configurations, each of them resulting in different weights between the input and either of the two output neurons, which range from 0 to 1. The weight dynamically changes with changing input frequency or the rate of change of any of the bias currents (equivalent to the feedback corresponding to respective output frequencies).

Two different cases with different combinations of bias signals (i.e., different ramp rates) are simulated to demonstrate this aspect. The input spike frequency is kept constant, and the results of output spikes are presented in Fig. 6. The resulting output spike trains demonstrate voltage spikes with the timing between them varying according to the bias current signals. A constant frequency spike train shown in Fig. 6(a) is applied to the input terminal. The two output spike trains are plotted for two different biasing conditions in Figs. 6(b) and 6(c) and 6(e) and 6(f), respectively. The output spike trains are significantly more complex for the given deterministic input spike train and, therefore, are a result of the disordered coupling as well as the biasing conditions. Note that an inhibitory output can generate a decreasing or a negative bias current. As the physical parameters of the circuit remain unchanged, a correlated set of relations can be drawn between the

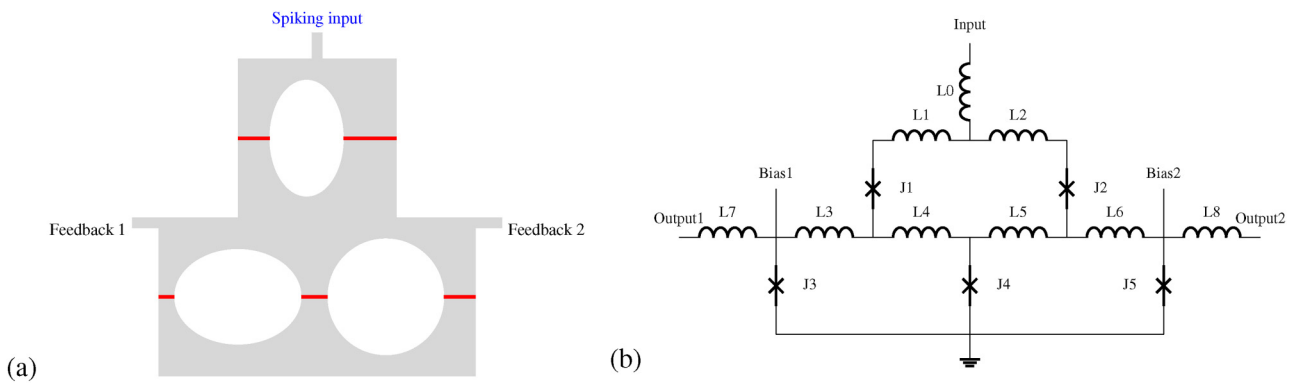

FIG. 5. (a) 1 × 2 three-loop disordered array synaptic network with two feedback terminals. Josephson junction barriers are shown in red, while the gray area represents the superconducting material. (b) Equivalent lumped-element circuit model with junctions and inductors. The output voltage spikes are measured across junctions J3 and J5. The circuit is completely disordered with no two junctions or inductors identical to each other.

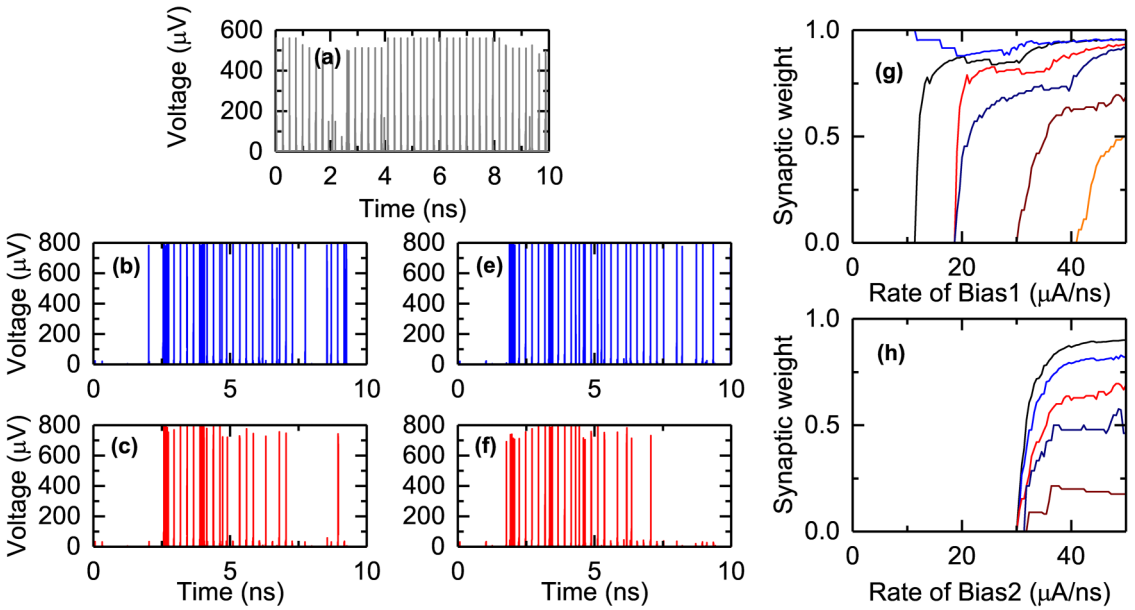

FIG. 6. Simulation results of the synaptic network shown in Fig. 5. (a) Constant frequency spiking input from an adjacent neuron. (b) Output spikes measured across an outer junction of the first output loop with feedback slopes of 20 μA/s and 0 μA/s. (c) Output spikes measured across an outer junction of the second output loop with a feedback slope of 20 μA/s and 0 μA/s. (e) Output spikes measured across an outer junction of the first output loop with feedback slopes of 20 μA/s and -10 μA/s. (f) Output spikes measured across an outer junction of the second output loop with a feedback slope of 20 μA/s and -10 μA/s. (g) Synaptic weight between output 1 and input with constant input frequency as a function of rate of change of feedback 1 at different values of rate of change of feedback 2. (h) Synaptic weight between output 1 and input at different input frequencies as a function of rate of change of feedback 1 at a constant rate of change of feedback 2.

synaptic weight and the input/output signals. To illustrate this, the synaptic weights are plotted as a function of slope of the bias current with constant input frequencies in Figs. 6(g) and 6(h). Different curves in the plot represent different input frequencies. Bias 1/feedback 1 is varied with bias 2 constant in Fig. 6(g) while bias 2/feedback 2 is varied with Bias1 constant in Fig. 6(h). Similar to the results observed in the three-state synaptic network in Fig. 4, the weight is zero below a threshold value of bias current slope. This threshold is dependent on the input frequency as evident in Figs. 6(g) and 6(h). Above the threshold, the weight changes with changing current slopes until a saturation value is reached, which is also dependent on the input frequency. While the actual dynamics are significantly complex to understand in detail, the emergent phenomenon exhibits spike timing and rate dependency of input and output (through feedback) on the synaptic weight. Additionally, the resulting synaptic weights are dependent on the previous state of the system. Note that the assumption here is that the parameters are chosen to satisfy $1 < LI_C/\Phi_0 < 2$. Relaxing those conditions would result in more than 27 configurations.

D. Large disordered array synaptic network

The number of configurations available increases exponentially with an increasing number of loops. Therefore, it is difficult and not too instructive to determine the behavior of such systems with a similar circuit analysis performed for smaller arrays as presented in Secs. II A–II C. Nevertheless, the circuit dynamics established so far can be expanded to understand interactions between any two adjacent loops that are part of a larger array. Two different variations of coupling can occur between any two such adjacent loops as shown in Fig. 7. In the first case, the loops are coupled through an inductor as shown in Fig. 7(a), whereas in the second case, the loops are coupled through a Josephson junction as shown in Fig. 7(b). In both cases, the configuration of the network (i.e., synaptic weight between any two nodes) changes when the loop currents change. Changes in loop currents occur when one or more of the junctions switch to a dynamic state, generating a single-flux quantum voltage pulse, following the current through them exceeding their respective critical currents. In other words, any current path between the neurons changes when one of the junctions in the path switches, resulting in a change in weight. Output spikes are produced when the current across the output junctions exceeds its critical current. Therefore, the interaction between the loops can be understood through the loop currents as a function of time and their transitions as the output frequency changes.

When two adjacent loops have an inductor in common as shown in Fig. 7(a), the circuit operates similar to that of a three-state synaptic network of Fig. 2. The simulation results of loop currents along with the output voltage spike train measured across junction $J4$ as a function of time are shown in Figs. 8(a)–8(d) for the specified bias current signals. The circuit operates in the mode that is identical

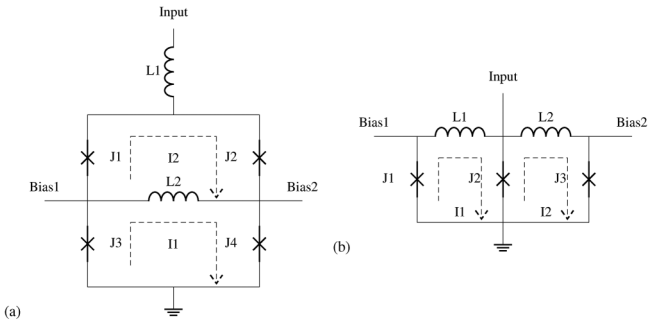

FIG. 7. Schematics representing two different types of loop interactions that can occur in a large disordered array. (a) Two loops coupled to each other through an inductive element. (b) Two loops coupled to each other through a Josephson junction.

to that shown in Fig. 3(a). Transient spiking currents are observed at regular intervals corresponding to each input voltage spike because the simulations performed are using transient circuit analysis. However, the steady-state currents between these spikes are indicative of the memory configuration of the array. Figures 8(b) and 8(c) are the loop currents corresponding to loops $J1 - L1 - L2 - J2$ and $J3 - L3 - J4$, respectively. Note that the current on one of the biasing terminals is steadily increasing, resulting in a corresponding increase in the steady-state loop currents. The circuit is subjected to the same four different configurations as that of Figs. 4(c) and 4(d). The loop currents are subjected to different interactions during these four configurations as they interact through the common inductor $L3$. When the output voltage is zero, the loop currents steadily increase or decrease until the loop current is sufficient to switch one of the junctions $J3$ or $J4$. As the bias current increases further, the output voltage generates a spike at every alternative input spike. The loop currents in $J1 - L1 - L2 - J2$ and $J3 - L3 - J4$ cycle between $+\Phi_0$ and $-\Phi_0$. The voltages across each of the junctions in these four states are shown in the supplementary material to further support the analysis. Initially, the loop currents are opposite to each other, acting together at $L3$. At a higher bias current, the loop currents are identical, therefore acting against each other through $L3$ as seen in Fig. 8(b) and 8(c) between 2.5 ns and 7 ns. In an asymmetric circuit, these two different configurations result in two different sets of weights. The cycling between states stops as the bias current increases further resulting in switching of all four junctions. Any further increase in bias current will result in a higher output frequency irrespective of the input signal. Therefore, when loops are coupled through an inductor, the relative cycling of individual loop currents between $+\Phi_0$ and $-\Phi_0$ can result in different weights, while switching of the junctions changes the number of flux quanta Φ_0 in the array.

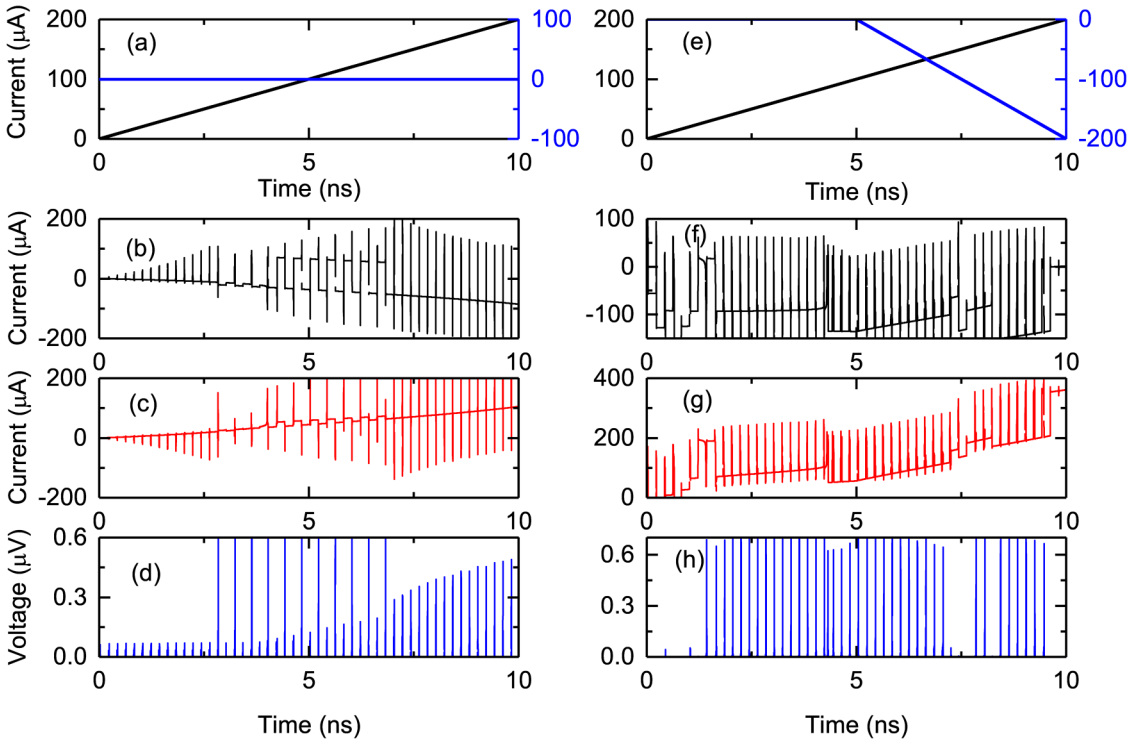

FIG. 8. Simulation results of the two loop circuits shown in Fig. 7. (a) and (e) Bias currents applied to the circuits from Figs. 7(a) and 7(b), respectively. Black curve represents current through bias 1, and the blue curve represents current through bias 2.

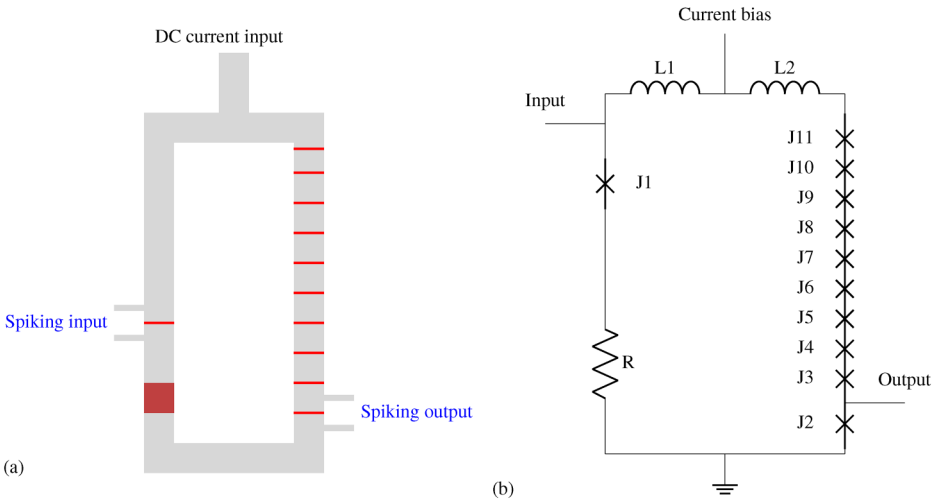

FIG. 9. Leaky integrate-and-fire neuron circuit schematic. Input signal represents spike trains received from other neurons/disordered arrays. Current bias represents integrated feedback and/or feed-forward signals. Output spike train is measured across junction J2.

The second type of coupling between the loops can occur through a Josephson junction as shown in Fig. 7(b). The simulation results of loop currents and the output voltage are shown in Figs. 8(e)–8(h) as a function of time for the given bias currents. In this array, the loop currents do not cycle between states with each input voltage spike, but abruptly switch to different values as one of the junctions switch. Switching of either $J1$ or $J3$ can add or remove a flux quantum Φ_0 to the array, while switching of $J2$ results in a change in weight by changing the interaction between the loop currents in both the loops. The corresponding voltages between each of the junctions in this configuration are provided in the supplementary material.

Therefore, the parameters of a large disordered array network can be described as shown in Eq. (2), with the relation between any two neurons in the network defined by the input $i1, i2, \ldots$ and output signals $o1, o2, \ldots$, along with the physical parameters $c1, c2, \ldots$ that are dependent on the coupling inductors and junctions between any two loops. Such a relationship can be used to characterize synaptic weights to physical parameters $c1, c2, \ldots$ for given inputs and outputs.

$$\begin{bmatrix} i1 \\ i2 \\ \ldots \end{bmatrix} \begin{bmatrix} c1 & c2 & \ldots \\ c3 & c4 & \ldots \\ \ldots & \ldots & \ldots \end{bmatrix} = \begin{bmatrix} o1 \\ o2 \\ \ldots \end{bmatrix}. \tag{2}$$

Identifying the coupling constants as shown in Eq. (2) does not imply that the weights can be programmed in a deterministic way. This is because the inputs $i1, i2, \ldots$ and outputs $o1, o2, \ldots$ are coupled to each other through feedback, and therefore their values are dependent on the previous memory state of the system. Furthermore, in the two and three loop synaptic array examples discussed in Figs. 3 and 7, it is clear that there is an upper limit to bias current, above which all the junctions in the circuit will be in the normal state (not shown in the simulation results). The feedback mechanism discussed in Sec. IV can be designed appropriately to only allow bias currents below this upper limit.

III. LEAKY INTEGRATE-AND-FIRE NEURON MODEL

In Secs. II A–II D, a collective synaptic network system was established that responds to spiking input and generates a spiking output. A compatible integrate and fire neuron is presented in this section that can be used to construct a recurrent neural network described in Sec. V. We describe a design that can react to incoming spikes from several other neurons through the synaptic network and generate a spiking output when the integrated signal overcomes a threshold. It comprises a superconducting loop with a stack of Josephson junctions as shown in Fig. 9(a) with *spiking input* for incoming spikes from several other neurons, or the *DC current input* that can be connected to feedback loops. The resulting spike train is applied across the input Josephson junction as shown in Fig. 10(a). The superconducting loop is designed to have a large inductance. Therefore, with each incoming spike switching the input junction $J1$ to a normal state, the current in the loop increases. The number of spikes that can enter the integration loop that can be referred to as the threshold, is determined by $\frac{LI_C}{\Phi_0}$, where L is the inductance of the loop [i.e., $L = L1 + L2$ in Fig. 9(b)], I_C is the critical current of the junctions in the identical junction stack, and Phi_0 is the magnetic flux quantum given by 2.5×10^{-15} Wb. When the loop current reaches a threshold, the junctions in the stack develop single-flux quantum voltage spikes. Therefore, the output spike train can be measured across one of the junctions in the stack as shown. Switching all the junctions in the stack results in a decrease in the persistent current in the integration loop to a resting potential u_{rest}. The simulation results of the incoming spikes of constant frequency, output spikes, and the loop current are shown in Figs. 10(a)–10(c), respectively. A small resistor R is added to the superconducting loop to allow the loop current to decay with a time constant of $\tau = \frac{L}{R}$, therefore exhibiting a leaky integrate-and-fire aspect. The resistor, therefore, allows us to decrease the time constants of the current loop to the time scale of the input signals. As shown in Figs. 10(a)–10(c), the circuit produces a spiking output when the loop current reaches a threshold value when a constant bias current as a constant frequency input spiking signal is applied. The operation of this design closely

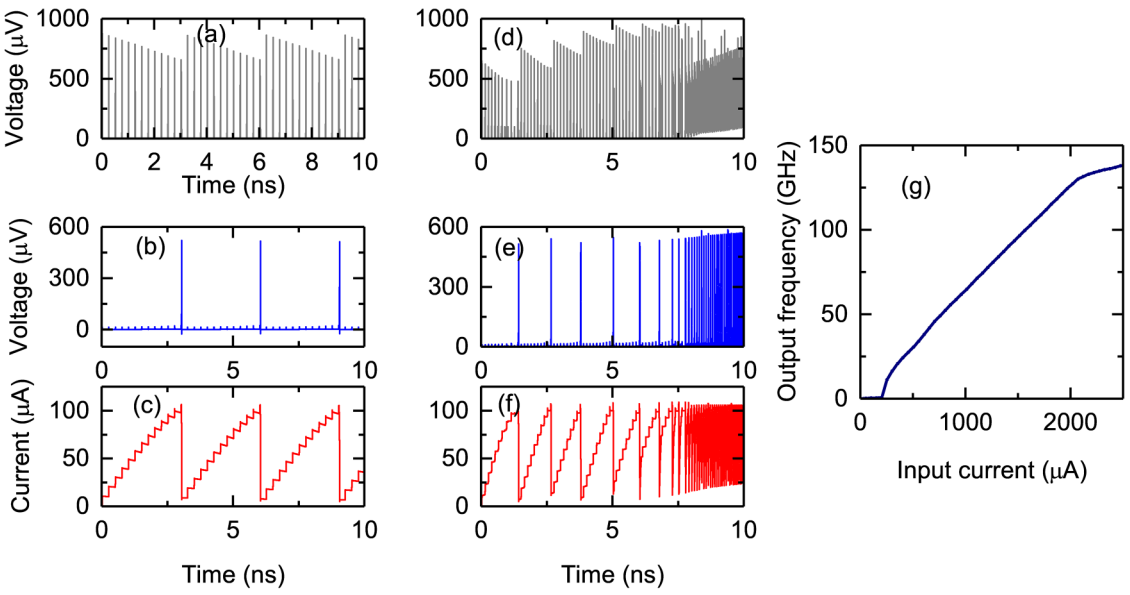

FIG. 10. (a) Input spike train with constant magnitude and frequency. (b) Output spike firing after the input signal reaches a threshold, for a given constant current bias. The current bias value defines the threshold. (c) Loop current representing the total signal accumulated in the neuron. The currents reset to a "rest" value after the neuron reaches the threshold and fires. (d) Varying frequency input signal obtained by applying a ramp current of a constant slope to the current bias. (e) Output spike train corresponding to input as in (d). (f) Loop current accumulated in the neuron showing dependency on input frequency. (g) Input current bias vs output frequency. The threshold varies with circuit parameters.

emulates a leaky integrate-and-fire model, which is described by

$$\tau \frac{d}{dt} u = -(u - u_{rest}) + RI(t). \tag{3}$$

The neuron fires and resets to resting potential when $u(t) = v$, where $u(t)$ is the loop current and v is the threshold defined by $\frac{LI_C}{\Phi_0}$.

The threshold, i.e., the number of incoming spikes needed for the neuron to fire, can be varied through a bias current/feedback loop as shown in Figs. 10(d)–10(f). A linearly ramping current is applied to the bias without a spiking input. Figure 10(e) shows that the threshold and the resting potential decrease as the current bias is increased, resulting in fewer input spikes required to fire the neuron. Therefore, when the bias current terminal is coupled to a positive feedback signal from the disordered array network, the neuron can be made to fire more readily and vice versa. The actual dynamics of the feedback/feed-forward signals can be a result of immediate output signals or signals from a different hierarchical level of the neural network through a feedback mechanism explained in Sec. V, similar to the mechanism for the synaptic network. Additionally, the current bias channel can also be used to integrate spike trains from a large number of neurons/synaptic networks through a similar mechanism as that of feedback shown in Sec. IV. Furthermore, the loop current magnitude (i.e., either resulting from the spiking input or the bias current) vs the output frequency resembles that of the ideal leaky integrate-and-fire model described by Eq. (3). The simulated input current vs output frequency is shown in Fig. 10(g). Therefore, this model circuit demonstrates the operation of a leaky integrate-and-fire model that is compatible with the disordered array synaptic network.

IV. FEEDBACK MECHANISM

One of the important aspects of the various circuits introduced in Secs. I–III is the feedback mechanism. Continuous and

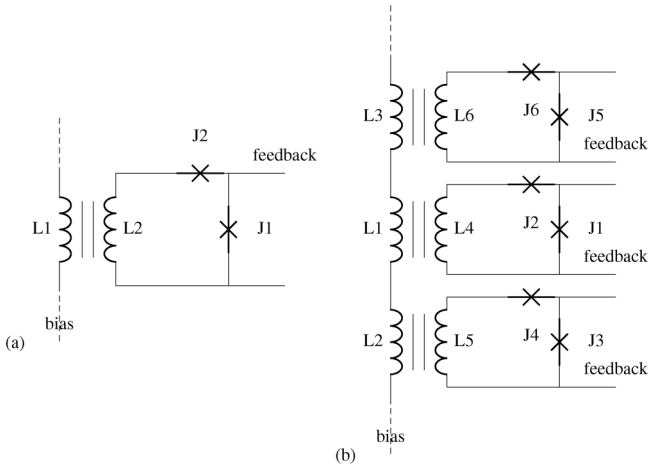

FIG. 11. (a) Feedback circuit to convert single-flux quantum pulses into current bias with a similar mechanism as introduced by Shainline *et al.*[41] (b) Several feedback connections can be made to a single bias line.

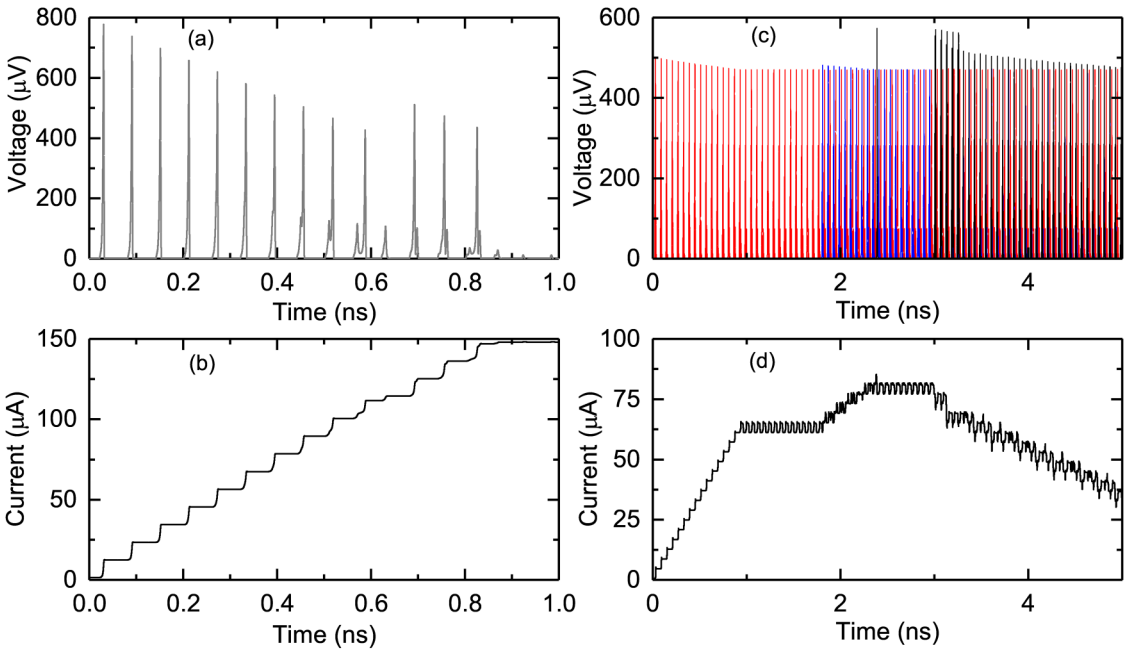

FIG. 12. Simulation results of feedback circuits shown in Fig. 10. (a) Spike train from output applied to J1 in Fig. 11(a). (b) Current bias through L1 in Fig. 11(a) that can be applied to the disordered array. (c) Spike trains applied to different hierarchical feedback loops through *J*1, *J*3, and *J*5, respectively. Red spikes represent signal applied at *J*1, blue represents signal applied at *J*3, and black represents signal applied at *J*5. (d) Total accumulated current on the bias line through inductors *L*1, *L*2, and *L*3 due to signals applied as shown in (c).

linearly increasing or decreasing ramp currents are chosen to emulate a simplified response from these feedback connections. In this section, the mechanism to convert an output spike train into a continuous bias current is presented. A variation of this mechanism is introduced by Shainline *et al.*[41] for use as a feedback mechanism for superconducting opto-electronic loop neural networks. Nevertheless, this circuit is suitable to convert an output spike train into a continuous current signal, the slope of which is proportional to the frequency of the spike train. The circuit for feedback is shown in Fig. 11. When a spiking input of constant frequency is applied across junction $J1$ of Fig. 11(a), a circulating current is added to the loop comprising $J1 - J2 - L2$. This current loop is inductively coupled to the larger current loop that goes through the bias current terminal and into the disordered array network. As the circulating current in the loop $J1 - J2 - L2$ increases, the current through the inductor $L1$ and, therefore, the bias current terminal increases. An upper limit to the bias current exists in this mechanism that is set by the inductor $L2$ at which the bias current

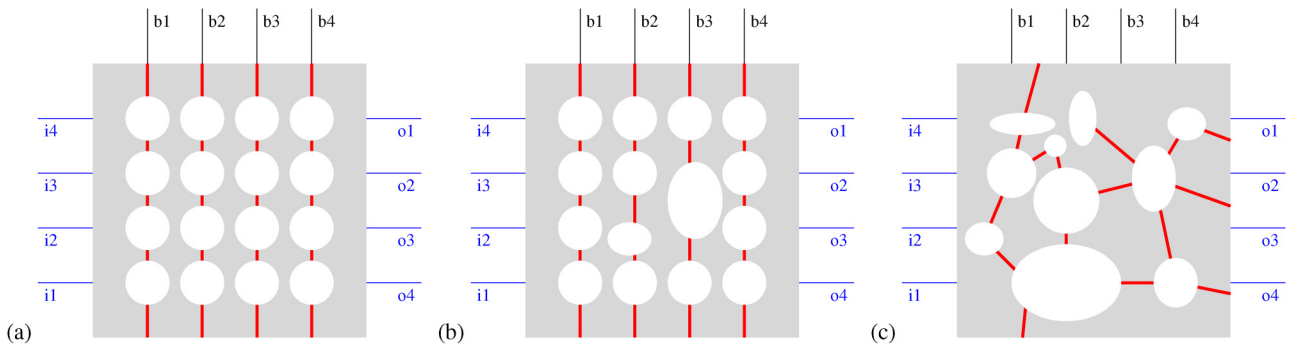

FIG. 13. Illustration of (a) regular, (b) small-world, and (c) random disordered array synaptic networks.

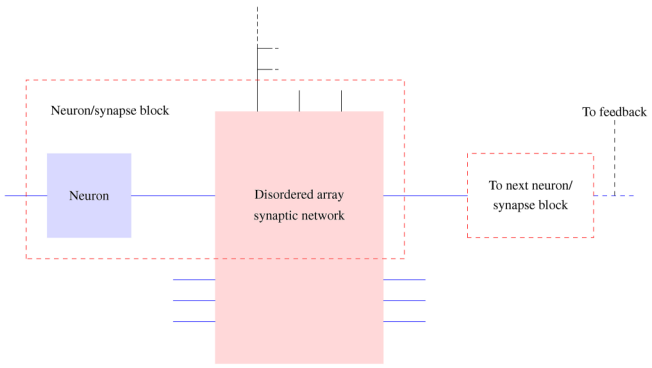

FIG. 14. Neural network schematic illustrating feedback connections for the hierarchical architecture. Blue lines represent connections from/to neurons, and black lines represent feedback connections. Feedback from multiple hierarchical levels can be coupled to each bias line on disordered arrays.

saturates. The corresponding simulation results are shown in Figs. 12(a) and 12(b). The inductive coupling to the bias line can either be positive or negative, representing an excitatory or inhibitory input, respectively. As evident from the synaptic network simulations, the bias currents can only be increased up to a certain value before reaching the maximum synaptic weight of 1. Increasing the bias currents beyond a certain value results in all the Josephson junctions in the array switching into the normal state without further evolution of the memory configurations. Therefore, the saturation values of the feedback current loops must be designed to limit bias currents from driving the disordered array into a saturated state.

A single bias line can be used to integrate feedback inputs from a large number of spike trains incoming from various channels in the network from different hierarchical levels of the recurrent neural network. The schematic of this aspect is demonstrated in Fig. 11(b) and the corresponding simulations results are shown in Figs. 12(c) and 12(d). Three different spike trains are applied to feedback loops across $J1$, $J2$, and $J3$, respectively as shown in Fig. 12(c). The inductive coupling to the inductor $L3$ in the biasing loop is in the opposite direction to that of the other two inductors resulting in the negative bias current. Initially, only one of the feedback spike trains (across $L1$) is active causing the total bias current to linearly increase until it reached saturation at 2 ns. When the second spike train (across $L2$) is active, the bias current further increases until it reaches a new saturation value. Note that the spike train across $L1$ is active during this period. Adding a negatively coupled spike train to this bias loop through $L3$ allows the bias current to decrease resulting in a complex mechanism to update the total bias current as shown in Fig. 12(d). The bias currents can also be updated manually by injecting current through a separate inductor in order to update the weights.

V. HIERARCHICAL ARCHITECTURE OF RECURRENT NEURAL NETWORKS

As mentioned in Secs. I–IV, the disordered array synaptic networks and the building blocks developed around them can be integrated together in a way to design fully connected and recurrent neural networks with hierarchical architecture for unsupervised learning. Any degree of symmetry in the disordered array results in degenerate memory configurations resembling a small-world network. The disorder can be varied to obtain small-world and random networks to take advantage of the collective emergent

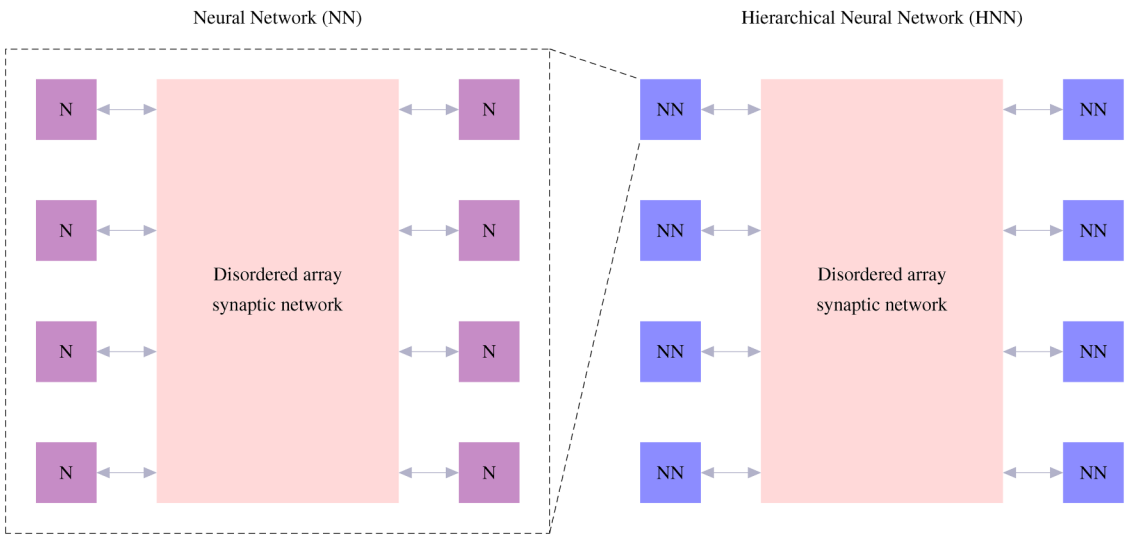

FIG. 15. Neural network schematic for the hierarchical architecture. The schematic on the left represents individual neurons connected to each other through a disordered array. The schematic on the right represents individual networks (may be viewed as corresponding to different functions) on the left connected to each other through a hierarchical disordered array.

properties,[35] as shown in Fig. 13. The schematic of a fully recurrent neural network at the lowest level is shown in Fig. 14. The input nodes to the disordered array can be connected to the loop neurons as shown in Sec. III, while the outputs can be coupled to the bias current terminals of the array through a feedback mechanism. The additional input and output nodes are open-ended that can be connected to other recurrent networks. Therefore, several of these neural networks can be combined together through a hierarchical disordered array with additional feedback connections arising from that array coupled to bias terminals of the lower level disordered arrays as shown in Fig. 15. Additionally, this architecture allows scaling the recurrent neural networks with self-similarity at the lowest and highest levels similar to that of a biological brain.[40] However, the emergent dynamics of such a network must be further investigated to determine the programming methods to update the weights as well as to design specific disordered patterns optimized for particular applications.

The organization of biological brain networks can be classified into structural and functional motifs,[45] where Sporns[28] identified that the brain networks develop by maximizing the functional motifs available for a small repertoire of structural motifs as allowed by evolutionary rules. Furthermore, the structural motifs are predominantly small-world networks[45] that support a large number of complex metastable states. The disordered array networks, therefore, allow flexibility to represent structural motifs that are designed for specific functionality. Several such distinct recurrent networks can be combined together in a hierarchical network to achieve a higher level functional motif operation.

Together, this system represents a recurrent network with an architecture of a hierarchy of loops, ranging from individual loop currents in a disordered array to a large loop current through the feedback network. The integration of information across a wide range of spatial and temporal scales can be constructed using disordered array networks as summarized in Figs. 14 and 15. Such a highly scalable network can be used to develop a complex system that can reconfigure itself in response to the inputs analogous to a biological brain network.[40]

VI. CONCLUSION

In this article, we have proposed a new approach to neuromorphic computing architecture using collective synaptic networks implementing disordered arrays. We have used superconducting disordered array loops to demonstrate the architecture. Equivalent lumped-element circuit simulations are used to illustrate complex dynamics of individual elements of such networks. The simulation results are shown for a short time duration of operation of the network with simplified excitation conditions, as the actual operation of these networks is significantly more complex. Additionally, we have introduced components such as leaky integrate-and-fire neuron and feedback that can be used to construct a recurrent neural network together with disordered arrays. Finally, we have shown that a large complex neural network with the hierarchical architecture that is similar to a biological brain can be constructed from the individual recurrent networks. However, we would like to suggest that this architecture is not unique to superconducting loops and that this disordered array approach can also be used with other hardware mechanisms of various materials that emulate neuron and synapse-like behavior. This can be achieved by creating a disordered array of coupled synapses in the network to create a complex dynamical system with a significantly larger number of states than individual synaptic connections between neurons. However, the introduced superconducting circuits can be used to develop the mathematical basis to further understand emergent phenomena to aid development of networks for practical applications.

This approach can significantly improve scalability of a neural network by replacing a large number of separate interconnections between neurons with a considerably smaller disordered array. Additionally, this high degree of inter-connectivity through a small-world network increases the synchronizability,[35] therefore enabling faster learning. Additionally, these circuits can naturally emulate spiking features of biological brains at high operating speeds up to hundreds of GHz (Ref. 47) while dissipating energies of the order of a few aJ/spike.[46]

SUPPLEMENTARY MATERIAL

See the supplementary material for the details of actual circuit parameters used in calculations/simulations that are discussed in the manuscript.

ACKNOWLEDGMENTS

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DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

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