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Executive Summary: The overall objective of this program is to achieve ~23% bifacial n-type cell efficiencies by developing and implementing optimized homogeneous or selective boron (B) emitter on front and tunnel oxide passivated contact (TOPCon) on rear side, in combination with advanced fine-line screen-printing metallization with floating busbars. During this research project, first we developed a technology roadmap to drive the 21% n-PERT cell efficiency from 21% to 23% by transforming the cell design to n-TOPCon and establishing the requirements for each layer, including B emitter, rear n-TOPCon, n-base Si and screen-printed contacts. Next, consistent with our roadmap, we developed advanced homogeneous implanted B emitter (150-180 Ω/□) passivated with ALD Al_2O_3 layer capped with PECVD SiN_x/SiO_x double-layer antireflection coating This gave a very low recombination current density of 10-15 fA/cm^2 prior to metallization. In addition, we demonstrated metallized recombination current density of ~31 fA/cm^2 for this advanced homogeneous B emitter with industrial screen-printed, fire-through contacts with 40 µm wide grid lines, floating busbars and implementation of an advanced Ag-Al paste which resulted in local or reduced area metal-Si contact under the grid lines with virtually no emitter surface etching. This paste reduced the full area metallized $J_{oe,metal}$ from >1100 fA/cm^2 to ~700 fA/cm^2. We also developed novel processes for the formation of p^+/p^{++} selective B emitter by a) single B diffusion with selective etch back and b) two-steps diffusion with implanted B in field region and APCVD B diffusion under the metal grid. We achieved very low un-metallized recombination current density (J_0) of ~18 fA/cm^2 for the selective $p^{++}p^+$ emitters (30/150 Ω/□) and metallized J_0 of ~28 fA/cm^2 with ~3% screen-printed metal contact to p^{++} regions. Next, we developed the technology for n-TOPCon by growing phosphorus-doped LPCVD and PECVD poly-Si on top of ~ 15Å chemically grown (NAO) tunnel oxide. After an optimized anneal at 875 °C for 30 min, passivated n-TOPCon have unmetallized J_0 of ~ 5 fA/cm^2 which went down further to ~ 1 fA/cm^2 after a 700 Å SiN_x capping layer and simulated contact firing cycle at 770 °C. After screen-printed fire-through metallization on this n-TOPCon with ~13% metal coverage, metallized J_0 value increased to only ~5 fA/cm^2 which is among the lowest reported value to the best of our knowledge for screen-printed metallization. Finally, we integrated all the above technology innovations and enhancements and demonstrated low-cost manufacturable screen-printed n-TOPCon bifacial Si solar cell with ~23% efficiencies.

Based on the experimental and theoretical understanding developed in this project, we have developed a new technology roadmap that shows that implementation of busbarless contacts, 10-20 ms bulk lifetime Si, and selective B emitter or selective TOPCon on the front can drive ~23% efficient cells achieved in this research to ~25% at low-cost.

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Background: Si solar cell is the dominant PV technology with a market share >90%. Therefore, it is critical to address the key issues facing Si PV to attain the DOE long-term goals. It is estimated that the Si modules need to be 23-25% efficient in combination with low manufacturing cost ($\leq ¢25/W$) to achieve ¢2-3/kWh long-term DOE target. To produce modules with such high efficiency and low cost, development and adoption of improved cell designs, technology innovations with high-throughput and reliable fabrication methods, and enhanced materials are crucial. These challenges are addressed in this project.

It is widely accepted that poly-Si based passivated contacts cells, also known as tunnel oxide passivated contact (TOPCon) cells, serve as newly emerging generation of advanced crystalline Si solar cells and have the potential to replace conventional full Al back and passivated emitter and rear cell (PERC) technology which currently dominates the photovoltaics (PV) industry [1]. Several groups have reported efficiencies approaching and exceeding 25% on laboratory-scale cells that employ FZ-Si and single side poly-Si based passivated contacts using non-commercial methods for front and/or back metallization [2, 3]. Poly-Si based passivated contact technology offers an ingenious solution to reducing diffusion- and metal-Si contact-induced recombination losses in bulk Si, therefore, it has primarily been confined to the rear of the cell because of high parasitic absorption losses in poly-Si [4]. An n-type TOPCon (n-TOPCon) is composed of a very thin tunnel oxide (SiO_x) capped with phosphorus-doped n^+ poly-Si. However, to adapt TOPCon technology for industrial production of large-area Si solar cells, several challenges need to be overcome, including development of tunnel oxide, screen-printing induced shunting and degradation of J_0 of n-TOPCon, parasitic absorption in the doped poly-Si, single-side deposition of poly-Si, and throughput [5]. The poly-Si thickness needs to be adequate to prevent the penetration of the fire-through metal paste into the thin oxide and oxide/Si interface. This is essential for achieving the lowest metallized J_0 for the TOPCon layer. With development of very low J_0 n-TOPCon, the recombination current densities in the bulk Si and passivated and metallized regions of B emitter are expected to become the limiting factor for higher efficiency single-side n-TOPCon cells. Therefore, higher bulk lifetime Si and carefully designed homogeneous B emitter with advanced screen-printed metallization or a selective B emitter (p^{++}/p^+) where highly-doped areas beneath the metal contacts reduce $J_{0,metal}$ passivated in between provide lower $J_{0,pass}$ due to lower doping, better surface passivation, reduced heavy doping effects. However, selective B emitter adds cost and process complexity that may negate the benefit of efficiency enhancement for industrial solar cells. Metallized J_0 can also be reduced by fine-line printing with floating busbars and by utilizing the paste and firing schemes that can give local area contacts under the grid without etching into the emitter. All these concepts are investigated and implemented in this research.

At the start of this program, we developed Sentaurus and Quakka 2D modeling capabilities and established a technology roadmap to ~23% efficiency n-TOPCon cell structure with quantitative requirements and metrics for each layer. Next, we developed individual technology enhancement features, such as low J_{ob}, poly-Si/SiO_2 (n-TOPCon), homogeneous and selective B emitters with low metallized J_{0e}, high bulk lifetime in Si, cofiring of screen-printed fire-through contacts to n-TOPCon and B emitter to minimize degradation in J_0 without compromising contact quality. We also investigated advanced screen printing with finer gridlines in combination with floating busbars as well as laser-

induced opening of grid pattern in combination with plating to reduce shading and metal-Si contact area fraction. Finally, we developed a process sequence by integrating all the best technologies developed in this program and demonstrated manufacturable large area high-efficiency (~23%) fully screen-printed bifacial n-type solar cells. Based on the experimental and theoretical understanding developed in this program, we developed a new technology roadmap to ~25% efficiency TOPCon cells through device modeling.

Introduction: Efficiency of current front junction *n*-type silicon solar cells is largely limited by the recombination in the heavily doped regions in the absorber and at the metal/silicon contacts. Carrier selective passivated contacts are a promising candidate for next-generation high-efficiency Si solar cells because they can eliminate high recombination at the metal/Si contacts and bypass the need for heavily diffused regions inside the absorber. In traditional cells, diffused and metallized regions in the absorber are utilized for separation, collection, and extraction of light-generated carriers in the absorber. Carrier selective passivating contacts provide an opportunity to displace these regions outside the absorber but still utilize their positive attributes. Because of high parasitic absorption in heavily doped poly-Si layers, we used TOPCon only on the rear side in this project and implemented advanced B emitter on the front side to minimize recombination on the front side. We employed ion implantation to form homogeneous as well selective B emitters because, besides time and temperature, it provides additional controls like implantation energy and dose for profile engineering and management. Ion implantation also provides opportunities for higher cell efficiency because of better areal uniformity, more precise control of doping profile, and excellent chemical purity of the beam. In addition to profile optimization and emitter passivation, we investigated different screen-printing metal pastes and firing schemes to minimize $J_{0e,metal}$, in conjunction with advanced screen printing with fine grid and floating busbars. A technology roadmap was developed for 23% cells by 2D simulations to guide the development of each layer.

The overall objective of this program is to achieve ~23% bifacial cell efficiencies by implementing optimized homogeneous or selective B emitter and rear side n-TOPCon, in combination with fine-line metallization and floating busbars. At the start of the program, we produced approximately ~21% efficient traditional n-PERT cells with diffused B emitter and P-doped BSF with a total J_0 value of ~315 fA/cm^2. Next, we developed 2D Sentaurus and Quakka modeling capabilities to develop a technology roadmap which revealed that a total J_0 of less than 50 fA/cm^2 is required to obtain high open-circuit voltages and achieve ~23% efficient cells. The recombination current J_0 has three main components including emitter (J_{0e}), bulk ($J_{0b\text{-}bulk}$), and n-TOPCon ($J_{0b'}$). Both J_{0e} and $J_{0b'}$ are composed of metallized and passivated regions. Through modeling and design we established practically achievable specific targets for metallized J_{0e} below 25 fA/cm^2 and $J_{0b'}$ below 5 fA/cm^2, while maintaining bulk lifetime of >1ms which should reduce $J_{ob\text{-}bulk}$ below 20 fA/cm^2.

Proposed J_0 and cell efficiency targets were achieved by a combination of fundamental understanding, device modeling, process development and implementation of front B homogeneous as well as selective emitter, rear n-TOPCon and fine-line advanced metallization. The project plan was divided into five tasks: 1) Device modeling to establish a technology roadmap to ~23% n-TOPCon cell including doping profiles and contact requirements. 2) Technology development and formation of advanced

homogeneous and selective B emitters 3) Technology development and formation of low J_0 screen-printed rear n-TOPCon 4) Advanced screen-printed and plated fine line metallization with floating busbars 5) Fabrication and demonstration of ~23% n-TOPCon bifacial cells by integration of advanced technologies.

TASK #1:

TECHNOLOGY ROADMAP DEVELOPMENT INCLUDING DOPING PROFILES, RECOMBINATION CURRENT AND CONTACT OPTIMIZATION BY DEVICE MODELING.

Task Summary: In this task, we performed 2D device modeling with Sentaurus and Quokka simulation tools to achieve 23% TOPCon cells through optimization of B emitter, n-TOPCon, and screen-printed contacts. A technology roadmap was developed to quantify the required unmetallized and metallized J_0 values and material parameters in each layer to achieve the target efficiency. This involved theoretical calculations of doping profiles, sheet resistance and contact parameters for lightly and heavily doped regions of the device, Sentaurus Device model was used to first generate J_0 vs SRV curves from the simulated and measured doping profiles. Then, from the knowledge of SRV on top of the doped profiles and at the metal-Si interface (~10^7 cm/s), J_0 contributions from doped and metallized regions were extracted for different profiles, and their sum was used to obtain the metallized J_0 value. We started with the fabrication of 21% n-PERT cell in our lab with total J_0 value of ~315 fA/cm^2 and 55 µm wide screen-printed lines with bulk lifetime of ~ 1ms. Our technology roadmap revealed that the total J_0 allowed for 23 % cell is only 50 fA/cm^2 so we set the practically achievable target of 30 fA/cm^2 for metallized homogeneous or selective B emitter, metallized J_0 target of 5 fA/cm^2 for the rear n-TOPCon and bulk lifetime of 1-2 ms, corresponding to $J_{0,bulk}$ of <20 fA/cm^2. In addition to the target J_0 values for each layer, we established contact and shading parameters to achieve 23% efficiency. We validated the model by applying it to match the cell parameters of the initially fabricated n-PERT and TOPCon cells using measured material, device and contact parameters.

Milestone - Develop a technology roadmap for >23% screen-printed cells using optimized doping profiles and screen-printed B emitter and rear side n-TOPCon (BP1, Q4- Achieved)

TASK #2:

TECHNOLOGY DEVELOPMENT AND FORMATION OF OPTIMIZED HOMOGENEOUS AND SELECTIVE P^{++}-P^{+} B EMITTERS

Task Summary: Since the target for metallized J_{0e} was ~ 25 fA/cm^2, task 2 dealt with experimental development of homogeneous B emitter with unmetallized J_0 of <15 fA/cm^2 and unmetallized $J_0 \leq 20$ fA/cm^2 for B selective emitter consistent with the guidelines from the roadmap in task 1. The objective was to find the manufacturable and cost-effective approach to forming B emitter that can meet the J_0 requirements. Implanted and APCVD emitters were investigated. We fabricated 90-200 Ω/□ homogeneous implanted B emitters as well as selective B emitters formed by a combination of implanted field region (>150 Ω/□) and APCVD B diffused p^{++} region (<50 Ω/□). Various dielectric passivation schemes (ALD/APCVD Al_2O_3 with PECVD SiN_x/SiO_x capping) were tested and qualified to optimize passivation quality and achieve the unmetallized J_0 targets. For the formation of B selective emitter, several different technologies (laser doping, etch-back, and double diffusion) were investigated. We succeeded in fabricating 170 Ω/□ implanted homogeneous emitter with unmetallized J_0 of ~ 10 fA/cm^2 and a 150/45 Ω/□ implanted/APCVD diffused selective B emitter with passivated J_{0e} ~18 fA/cm^2. After

metallization homogeneous B emitter gave total metallized J_{0e} of 30 fA/cm^2 with contact resistivity of 3-5 mΩ-cm^2 and selective emitter resulted in metallized J_{0e} of 25 fA/cm^2 and contact resistivity of ~1 mΩ-cm^2. These values are consistent with target values set by our roadmap for 23 % cells.

Milestone – Demonstrate $J_{0e,pass}$ ≤15 fA/cm^2 for passivated /unmetallized homogeneous emitter and $J_{0e,pass}$ ≤25 fA/cm^2 for unmetallized /passivated p^{++}-p^{+} selective emitter (BP2, Q4- Achieved)

Task #3:

Technology development and formation of n-TOPCon

Task Summary: At the beginning of the project, we started experimental development of phosphorus diffused selective BSF to achieve < 25 fA/cm^2. This was found to be more challenging and process intensive. Therefore, we changed the direction of this task from selective P BSF to n-TOPCon because n-TOPCon started to look very promising for minimizing low metallized rear J_0 due to superior carrier selectivity and excellent passivation quality (BP1, Q4). We investigated both PECVD and LPCVD tools to grow phosphorus-doped poly-Si on top of chemically grown ~15 Å tunnel oxide to fabricate poly-Si/SiO_2 passivated contacts. Post poly-Si deposition anneal was optimized and 875 °C was found to be the optimum for our TOPCon structure which gave the lowest J_0 and highest implied V_{oc}. We achieved excellent passivation quality from PECVD grown thin (10-40 nm) poly-Si and LPCVD grown thick (100-200 nm) poly-Si with unmetallized J_0 of ~3 fA/cm^2, which reduced to ~1 fA/cm^2 after ~700 Å thick SiN_x deposition. Due to the fire through screen-printed metallization at high temperature (~770°C) and lower quality of thicker PECVD films in our tool, we chose the LPCVD process for growing the thick n-TOPCon, which was subsequently coated with SiN_x for contact firing. We also studied the effect of screen-printed fire-through contacts on J_0 for different pastes and poly-Si thickness. Appropriate paste and optimized firing resulted in metallized J_0 of 5 fA/cm^2 with ~10% metal coverage on the rear TOPCon to maintain bi-faciality. In addition, contact resistivity for 200 nm thick poly was found to be ~ 2 mΩ-cm^2. This is entirely consistent with the roadmap and the required metallized $J_{0b'}$ for achieving 23% efficiency.

Milestone – Demonstrate J_0 ≤5 fA/cm^2 for metallized n-TOPCon (BP2, Q4- Achieved)

Task #4:

Advanced screen-printed and plated fine line metallization with floating busbars.

Task Summary: Task 4 involved advanced metallization to form contacts to B emitters with reduced shading and metal-Si contact area, without compromising the contact and series resistance (Rs). Target Rs value in the roadmap was set at ~ 0.5 ohm-cm^2 for the 23% bifacial cell. This was a challenge for the 170 Ω/□ homogeneous emitter and required experimenting with different pastes and firing schemes. In the case of selective emitter, the challenge was to align the contacts in the heavily diffused tracks while keeping the contact coverage and metal/Si contact to a minimum. Consistent with our technology roadmap, the metallized J_0, J_{sc} and series resistance targets were achieved by pushing the limit of screen-printing technology to achieve ~40 µm wide grid lines after contact firing in combination with co-fired floating busbars. At the start of the program, our grid line widths were ~ 55 µm with fire-through contacts and no floating busbars. Finer grid lines reduced shading and the floating bus bars reduced metal/Si contact area and J_0. This was accomplished by experimenting with advanced screens with appropriate

emulsion thickness and narrow openings in combination with pastes that do not spread appreciably upon firing.

The second fine line metallization approach involved fabricating ~30 µm wide Ni-Cu plated self-aligned contacts to heavily doped emitter regions. This was achieved by laser opening of narrow grid lines (~10 µm) followed by damage removal and electroless plating of Ni-Cu. This approach gave enhancement in J_{sc} due to narrower grid lines (~25-30 µm) but the residual laser damage on the emitter surface resulted in slightly lower V_{oc}. Therefore 40 µm screen printed lines with floating busbars were used in final cell fabrication process which resulted in >0.3% enhancement in cell efficiency. We briefly attempted the use of busbarless /muti-wire contact in the final budget period to enhance cell performance.

Milestone – Demonstrate screen printed <50 µm wide grid lines with floating busbars and good alignment with 150 µm wide heavily diffused selective tracks (BP2, Q7- Achieved)

Milestone - Demonstrate <40 µm self-aligned plated contacts with contact resistance below 5 mΩ-cm^2 (BP3, Q2 - Achieved)

TASK #5:

FABRICATION OF HIGH-EFFICIENCY N-TOPCON CELLS BY PROCESS DEVELOPMENT AND INTEGRATION OF ADVANCED TECHNOLOGIES

Task Summary: Task 5 involved integration of all the promising advanced technologies into a process sequence to fabricate screen printed 23% commercial size bifacial solar cells. In this task we achieved screen printed 239 cm^2 n-TOPCon bifacial cells with efficiency of 22.6%. Modeling and analysis showed slightly higher n-factor (~1.1) due to edge leakage effects which lowered the FF. To eliminate the edge effects, we fabricated 10x10 cm cell size within the 6-inch pseudo square wafer by laser isolation and modified the grid design with three busbars for 100 cm^2 cell. This resulted in 22.9% efficiency, consistent with our technology roadmap. Finally, we demonstrated fully screen-printed 239 cm^2 ~23% efficient bifacial n-TOPCon cells with chemical edge isolation process. These cells were fabricated with homogeneous B emitters. Based on the experimental and theoretical understanding developed in this program, we have established a new roadmap to ~25% cell efficiency n-TOPCon cells which involves busbarless contacts, much higher bulk lifetime and selective emitter.

Milestone – Demonstrate n-TOPCon cell efficiency >22.5% (BP3, Q2- Achieved)
Go/No-Go – Cell efficiency >22.0% (BP3, Q2- Achieved)
Final Deliverable – Screen printed, large area n-TOPCon bifacial cells with efficiency >22.5% (Achieved)

Project Results and Discussion:

Task #1: Technology roadmap development including doping profiles, recombination current and contact optimization by device modeling.

Key Achievements: In Task 1, we implemented several models including, 2D Sentaurus [6] and Quokka 2 [7] models for device simulation, Sentaurus Process model for implanted profile simulation, Sentaurus Device model for J_0 vs SRV curve for each profile and antireflection coating, in-house grid model for grid design, contacts and floating busbar optimization. These models were used throughout the project to analyze the fabricated cells and understand the loss mechanisms in them. At the start we fabricated and modeled 21% traditional n-PERT cell and then applied Sentaurus and Quokka 2

models to establish a roadmap by identifying and quantifying the practically achievable properties and required enhancements in B emitter, n-TOPCon region, bulk lifetime, optical properties and contact parameters that can get us to 23% n-TOPCon cell efficiency. It was found that a metallized J_0 of 30 fA/cm^2 in B emitter and 5 fA/cm^2 in rear TOPCon in combination with 1-2 ms bulk lifetime, 40 µm grid lines and floating busbars can get us to our efficiency target. The cell efficiency roadmap was utilized to guide the experimental work and validate the technology development. Each layer of the device was investigated and optimized individually and then integrated to achieve the target efficiency. Finally, a new roadmap was developed for ~25% TOPCon cells.

Results and Discussion in Task 1

We started the program with the fabrication of traditional n-PERT cells and used them to validate the 2D device modeling capabilities (Sentaurus and Quokka) and extend the simulations to establish a technology roadmap to achieve target cell efficiency. Analysis of our ~21% PERT cells showed that based on our starting material quality and processing, we can maintain bulk lifetimes in the range of 1-2 ms in the finished cells. Therefore, we created a roadmap with a bulk lifetime of 1.5 ms.

Figure 1 shows our technology roadmap to > 23% efficiency, starting with our 21.2% N-PERT cell fabricated at the start of this project. This cell had total J_0 = 304 fA/cm^2, V_{OC} = 661 mV and J_{SC} = 39.2 mA/cm^2. This modeling was performed using 2D Quokka 2 simulator. In Figure 1 we have also quantified the individual contributions to

Efficiency	21.1%	21.4%	22.3%	22.8%	23.1%	23.5%
Total J_0 (fA/cm²)	304	206	84	56	44	39
Voc (mV)	661	672	695	706	712	715
Jsc (mA/cm²)	39.2	39.5	39.5	40.4	40.4	40.4
FF (%)	81.2	80.5	81.0	79.9	80.1	81.3

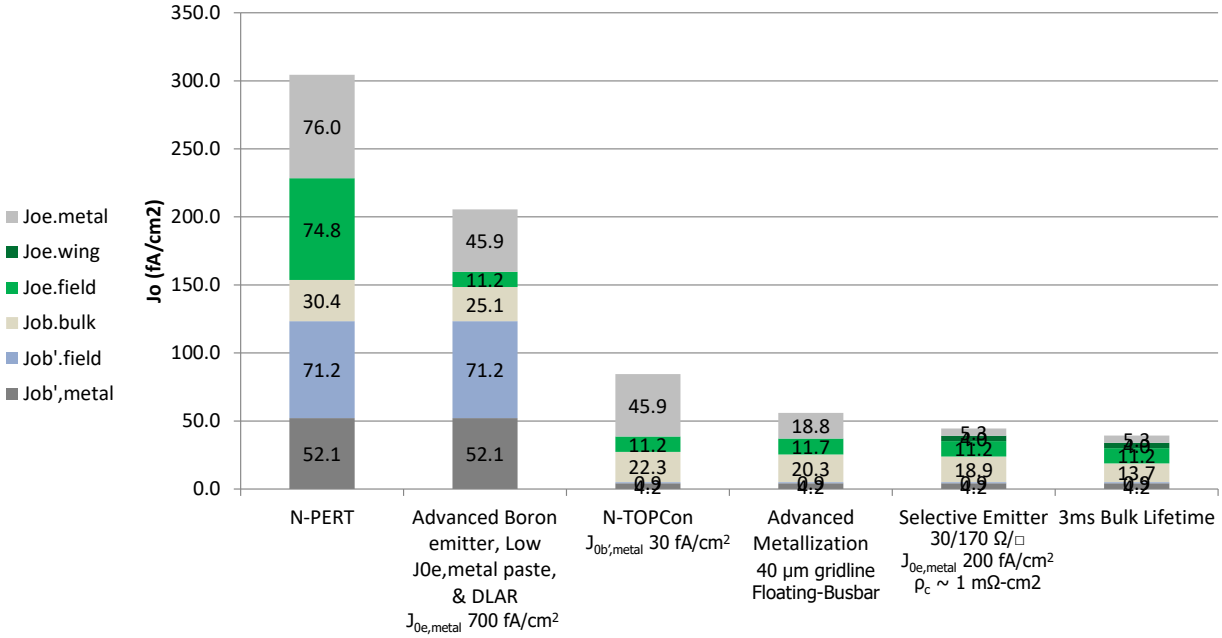


Figure 1 Technology roadmap for >23% n-TOPCon cells, start with our 21.0% n-PERT cell

total J_0 from the front and back metallized regions, B emitter, back surface field and the

bulk. This helps in identifying which regions are limiting the cell performance. Table 1 shows the detailed input and output parameters for each case or bar on the roadmap. Notice that in our PERT cell B emitter was 95 Ω/□ with single-layer AR coating, metal grid coverage of 6.5% and fire-through busbars. This resulted in metallized J_{0e} of ~150 fA/cm^2 from B emitter. Full area P diffused BSF with screen-printed contact resulted in metallized $J_{0b'}$ of 123 fA/cm^2. The bulk contribution to J_0 was 30.4 fA/cm^2 which was extracted from the difference between total J_0 of 304 fA/cm^2, obtained from Voc and Jsc of the cell, and the known metallized J_{0e} and $J_{0b'}$ numbers.

Since total J_0 to achieve 23% efficient cell be only about 50 fA/cm^2 (bars 4 and 5 in Fig 1), we had to design each layer of the n-PERT cell to minimize J_0. The second bar shows that if we can reduce the metallized J_{0e} of the B emitter from 150 to 57 fA/cm^2 by raising its sheet resistance from 95 to 170 Ω/□ and using advanced screen-printed paste that can reduce full area $J_{oe,metal}$ from 1160 fA/cm^2 to 700 fA/cm^2 (Table 1), we can get 21.4% efficient cells. At this point cell performance gets limited by the regions below the emitter. The third bar in the roadmap shows that we need to develop a carrier selective n-TOPCon to replace the n^+ BSF and lower the metallized J_0 from 123 fA/cm^2 to 5 fA/cm^2 with 13% metal coverage (Table 1). This is a challenging task but achievable because in n-TOPCon both diffused and metallized regions are displaced outside the absorber. In addition, modeling shows that we also need to tailor the thickness and doping in rear poly to achieve contact resistivity of < 2 mΩ-cm^2 and good FF. This enhancement should raise the efficiency to 22.3%. The fourth bar in the technology roadmap in Fig 1 shows that we also need to improve our screen-printing to reduce the line width from 55 to ~40 μm, busbar width from 900 to 600um and incorporate floating busbars to reduce shading as well as metal-induced recombination on the front side. This will raise the efficiency to 22.8% (Table 1). With the above changes in screen-printing parameters, we had re-optimize the grid design to maintain low contact and series resistance. This was done by using our in-house grid model. The fifth bar in the roadmap shows that implementation of a p^+/p^{++} selective emitter (170/30 Ω/□ with metallized J_0 of < 25 fA/cm^2 and contact resistivity of ~ 1 mΩ-cm^2, instead of 30 fA/cm^2 and 3-5 mΩ-cm^2 for the homogeneous emitter, will bump the cell efficiency to 23%. Last bar shows the importance of bulk lifetime at this point because J_{0b} starts to play a big role in limiting the cell efficiency. If we can have a bulk lifetime of 3 ms, this efficiency will climb to 23.5%. To highlight the importance of bulk resistivity and lifetime (material quality) we performed additional modeling to quantify the impact of bulk lifetime alone as well as the combined effect lifetime and resistivity on the efficiency of our cell design (Figs 2 and 3). Figure 2 shows that, with a higher than 2 ms SRH lifetime, our n-TOPCon cell can achieve > 23% efficiency with a homogeneous B emitter on the front. The efficiency contour map as a function of bulk resistivity and mid-gap SRH lifetime is generated in Figure 3. The white dashed line shows the optimum bulk resistivity that results in maximum efficiency at each SRH lifetime. The optimum resistivity increases with increasing SRH lifetime, and when $\tau_{n0} = \tau_{p0} > \sim 4\ ms$, the optimum resistivity increases to > 20 Ω-cm bulk resistivity. This is because the benefit of higher τ_{bulk} from lowly doped bulk outweighs the lateral transport benefit from highly doped bulk material.

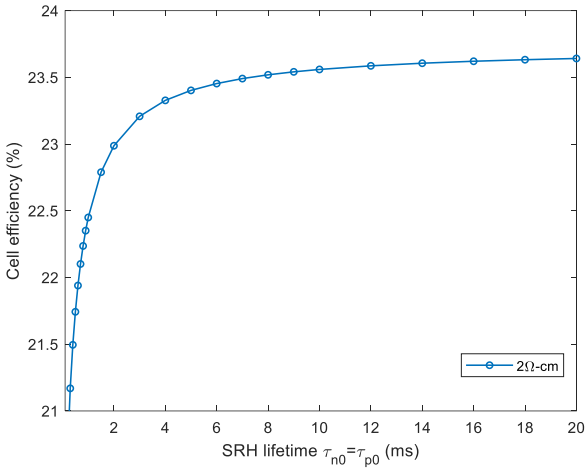


Figure 2 Efficiency vs mid-gap SRH lifetime of n-TOPCon cells with advanced metallization (bar 4 in Figure 1). It shows 23% efficiency can be achieved with 2 ms lifetime without selective emitter, and 23.2% efficiency can be achieved with 3 ms lifetime.

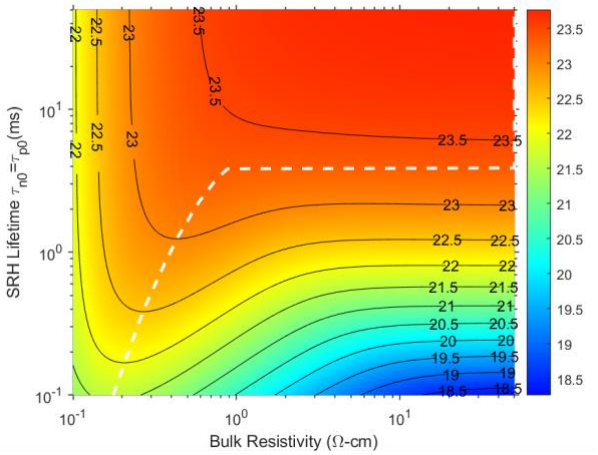


Figure 3 Efficiency contour map of n-TOPCon cells with advanced metallization (bar 4 in Figure 1) as a function of bulk resistivity and mid-gap SRH lifetimes. The white dashed line corresponds to the optimum bulk resistivity that results in maximum efficiency at each SRH lifetime

Table 1 Quokka 2 modeling results and input parameters for the n-PERT and n-TOPCon cells

	N-PERT	**Advanced Boron emitter, Low $J_{0e,metal}$ paste, & DLAR**	**N-TOPCon**	**Advanced Metallization**	**Selective Emitter**	**3ms Bulk Lifetime**
Efficiency	**21.1%**	**21.4%**	**22.3%**	**22.8%**	**23.1%**	**23.5%**
Total J_0 (fA/cm^2)	**304**	**206**	**84**	**56**	**44**	**39**
Voc (mV)	**661**	**672**	**695**	**706**	**712**	**715**
Jsc (mA/cm^2)	**39.2**	**39.5**	**39.5**	**40.4**	**40.4**	**40.4**
FF (%)	**81.2**	**80.5**	**81.0**	**79.9**	**80.1**	**81.3**
Cell size (cm^2)	239	239	239	239	239	239
Anti-Reflection Layer	Single Layer	Double Layers	Double Layers	Double Layers	Double Layers	Double Layers
Front finger width W_f (μm)	55	55	55	40	40	40
Front shading coverage	6.55%	6.55%	6.55%	4.59%	4.59%	4.59%
Front metal contact coverage	6.55%	6.55%	6.55%	2.67%	2.67%	2.67%
Busbar number / width (μm)	5 / 900	5 / 900	5 / 900	5/600	5/600	5/600

Floating or Fire-through BB	Fire-through BB	Fire-through BB	Fire-through BB	Floating BB	Floating BB	Floating BB
Wafer Thickness (μm)	180	180	180	180	180	180
Front Contact Resistivity (mΩ-cm^2)	1	3	3	3	1	1
Selective emitter sheet resistance (Ω/□)	NA	NA	NA	NA	30	30
Selective emitter junction width (μm)	NA	NA	NA	NA	100	100
Wing J_0 (fA/cm^2)	NA	NA	NA	NA	100	100
Front passivated J_0 (fA/cm^2)	80	12	12	12	12	12
Front contact $J_{0,metal}$ (fA/cm^2)	1160	700	700	700	200	200
Front emitter sheet resistance (Ω/□)	95	170	170	170	170	170
Substrate resistivity (Ω-cm)	2	2	2	2	2	2
mid-gap SRH Lifetimes (τ_n=τ_p) (ms)	1.5	1.5	1.5	1.5	1.5	3
Back Contact Resistivity (mΩ-cm^2)	1	1	2	2	2	2
Rear passivated J_0 (fA/cm^2)	72	72	1	1	1	1
Rear contact $J_{0,metal}$ (fA/cm^2)	4600	4600	30	30	30	30
Rear contact percentage	1.13%	1.13%	13%	13%	13%	13%

Task #2: Technology development and formation of optimized homogeneous and selective B emitter

Key Achievements: In task 2, we investigated an experimental development of advanced homogeneous B emitter as well B selective emitters to achieve metallized J_0 of ~25 fA/cm^2. We developed a homogeneous implanted B emitter with the passivated J_0 ~ 10 fA/cm^2 and metallized J_0 ~30 fA/cm^2 using high sheet resistance (170-180 Ω/□) emitter in combination with advanced metallization involving low $J_{0,metal}$ paste, fine line printing and floating busbars. This resulted in reduced shading, metal-Si contact area and 3-5 mΩ-cm^2 contact resistivity. We also developed a new process for selective B emitter with ~ 150 Ω/□ implanted B in the field area and ~ 45 Ω/□ APCVD B glass diffusion in the contact area. Consistent with the roadmap, this resulted in unmetallized J_0 of~18 fA/cm^2 and metallized J_{0e} <30 fA/cm^2.

Results and Discussion in Task 2

Task 2.1 Development of advanced homogeneous implanted B emitter

In this project, we investigated the effect of profile and sheet resistance of ion-implanted homogeneous B emitter on the efficiency of bifacial n-TOPCon cells by a combination of modeling, technology development and cell fabrication. It is well known that the screen-printed Ag/Al contacts to B emitters can be made with much lower surface concentration (<2×10^{19} cm^{-3}) compared to the screen-printed Ag contacts to phosphorus (P) doped n-type emitters (~1×10^{20} cm^{-3}). This provides an opportunity to lower $J_{0e,pass}$ by reducing B doping without sacrificing contact quality. However, this makes the metal-induced recombination much worse because lightly doped emitters are more transparent and sensitive to surface recombination velocity. Due to these tradeoffs, it is challenging to tailor the doping profile of a homogeneous B emitter to achieve low J_{0e} values in the passivated as well as metallized regions simultaneously, while maintaining good ohmic contact and acceptable sheet resistance for high FF. This problem can be mitigated by driving the B emitter profile or junction deep to decouple the metallized surface from metal, optimizing screen-printed contacts to lower $J_{0e,metal}$, and reducing the direct metal-Si contact area. In this study, we have employed ion implantation to form B emitters because, besides time and temperature, it provides additional controls like implantation energy and dose for profile engineering and management. Ion implantation also provides opportunities for higher cell efficiency because of better areal uniformity, more precise control of doping profile, and excellent chemical purity of the beam. Efficiency improvement and lower recombination current density with B and P implanted regions have been published by several groups [8-15] with screen-printed cell efficiencies approaching 21%.

In addition to profile optimization, we investigated different screen-printing metal pastes and firing schemes to minimize $J_{0e,metal}$ and quantify contact resistivity, and then use that information in Sentaurus 2D device simulations to understand the tradeoffs to select the optimum B emitter profile. Experimental values of $J_{0e,metal}$ were determined for selected screen-printed fire-through metal pastes to demonstrate that $J_{0e,metal}$ can increase or decrease depending on the aggressiveness of the glass frit, and its interaction with emitter surface as well as passivating dielectric underneath the grid. According to our technology roadmap in Task 1, final goal of this task was to achieve a metallized J_{0e} of ~ 30 fA/cm^2 with a homogeneous B emitter so that ~23% n-type cells can be achieved with n-TOPCon rear contact.

Ion-implanted B emitters in the sheet resistance range of 48-200 Ω/□ were fabricated and characterized in terms of sheet resistance, doping profiles, specific contact

resistivity, $J_{0e,pass}$ and $J_{0e,metal}$. To quantify the emitter recombination current density (J_{0e}), symmetric $p^+/n/p^+$ test structures were prepared by B implantation and annealing on 200 µm thick 20 Ω-cm 6-inch pseudo square high bulk lifetime n-type monocrystalline Czochralski (Cz) wafers. After saw damage etching and texturing followed by a standard RCA clean process, wafers received B implantation at 10 keV with doses ranging from 1×10^{15} cm^{-2} to 5×10^{15} cm^{-2} on both sides. All samples were annealed at 1050 ℃ for 1 hour in N_2 ambient followed by an in-situ oxidation for 30 minutes in O_2 ambient to remove implanted damage, activate dopants and drive the junction deep. After etching the thermal oxide in a dilute HF solution, the sheet resistance of implanted B emitters (R_{sheet}) was measured by a four-point probe. After a standard RCA clean, ~100 Å thick aluminum oxide (Al_2O_3) layer was deposited for surface passivation by plasma-assisted atomic layer deposition (ALD) on both sides, followed by plasma-enhanced chemical vapor deposition (PECVD) of SiN_x/SiO_2 stack on top of the Al_2O_3 for both passivation and antireflection coating. Next, samples were subjected to a firing cycle without any metal paste to simulate the effect of screen-printed contact firing on passivation quality of the unmetallized portion of the emitter. Finally, $J_{0e,pass}$ was measured under high-level injection using the photo-conductance decay (PCD) method proposed by Kane and Swanson [16]. In order to quantify the recombination current density contribution due to metallized portion of the B emitter ($J_{0e,metal}$), 40 µm wide metal gridlines with varying pitch and metal fraction (f_{metal}) were screen-printed only on rear side of the symmetric structure. Several different pastes were investigated but only two most pertinent ones (A&B) are reported. To evaluate the effect of pastes A and B on $J_{0e,metal}$, the two commercial Ag/Al pastes were applied on 170 Ω/□ symmetric $p^+/n/p^+$ test samples implanted with 1.2×10^{15} cm^{-2} B dose. After firing, the Ag/Al bulk electrode was etched away in $HCl:H_2O_2:H_2O$ =1:1:1 solution, leaving only the thin glass layer on Si surface with embedded metal crystallites into the emitter. $J_{0e,metal}$ for the two pastes was then determined by fitting the measured total J_0 of etched samples as a function of the f_{metal}. Since J_0 for the symmetric test structure with metal contacts on one side can be expressed as:

$$Measured\ total\ J_0 = J_{0e,front,metal} \times f_{metal} + J_{0e,front,pass} \times (1 - f_{metal}) + J_{0e,rear,pass}$$

$$Slope\ of\ J_0\ vs\ f_{metal} = J_{0e,front,metal} - J_{0e,front,pass} = J_{0e,metal} - J_{0e,pass}$$

With $Intercept = J_{0e,front,pass} + J_{0e,rear,pass} = 2 \times J_{0e,pass}$,

therefore, $J_{0e,pass} = \frac{Intercept}{2}$ and $J_{0e,metal} = Slope + J_{0e,pass}$

Thus both $J_{0e,metal}$ and $J_{0e,pass}$ can be obtained from the slope and intercept of the linear plot. In addition, the specific contact resistivity between screen-printed Ag/Al contact and the implanted B emitters for the two pastes was measured by transfer length method (TLM), using separate test samples prepared with unequally spaced screen-printed lines. Finally, the profile of the170 Ω/□ emitter was measured by electrochemical capacitance-voltage measurement (ECV) to match and validate the Sentaurus Process model used to generate various implanted profiles.

2.1.1 Characterization of unmetallized ion-implanted B emitters as a function of implantation dose

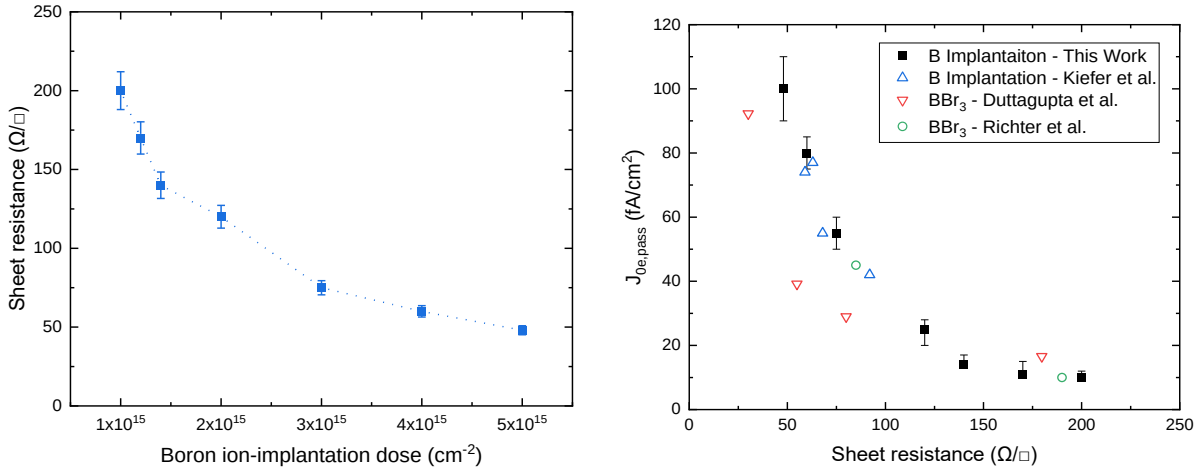


Figure 4. Boron emitter sheet resistance as a function of boron ion-implantation doses for 10 keV implantation energy and 1050 ℃ post-implantation anneal (left) Experimentally measured $J_{0e,pass}$ in this study (solid symbols) and selected literature data (open symbols) [17-19] as a function of boron emitter sheet resistance on textured surface (right)

Figure 4a shows the sheet resistance (R_{sheet}) of the ion-implanted B emitters fabricated in this study as a function of B ion-implantation dose using 10 keV implantation energy and the above mentioned 1050 ℃ anneal. As expected R_{sheet} decreases from 200 Ω/□ to 48 Ω/□, as the B implantation dose increases from 1×10^{15} cm^{-2} to 5×10^{15} cm^{-2}. Figure 4 (right) shows the measured $J_{0e,pass}$ for the ion-implanted textured B emitters fabricated in this study as a function of B emitter sheet resistance. The solid squares show our results and the open symbols show literature data from [17-19] for comparison. Notice, very low $J_{0e,pass}$ < 15 fA/cm^2 were achieved for R_{sheet} > 140 Ω/□. Figure 5 shows the measured contact resistivity as a function of B emitter sheet resistance. Contact resistivity of less than 5 mΩ-cm^2 was achieved for both pastes A and B for ≤170 Ω/□ implanted emitters with surface concentration of 6 × 10^{18}/cm^3, which is acceptable for high-efficiency cells. Next step was to determine the metallized J_{0e} which is composed of passivated region between the gridlines as well as metallized emitter portion under the grid. In order to quantify and explain the difference between the metallized J_0 for the two pastes, we first simulated their profiles and established a baseline or reference value of $J_{oe,metal}$

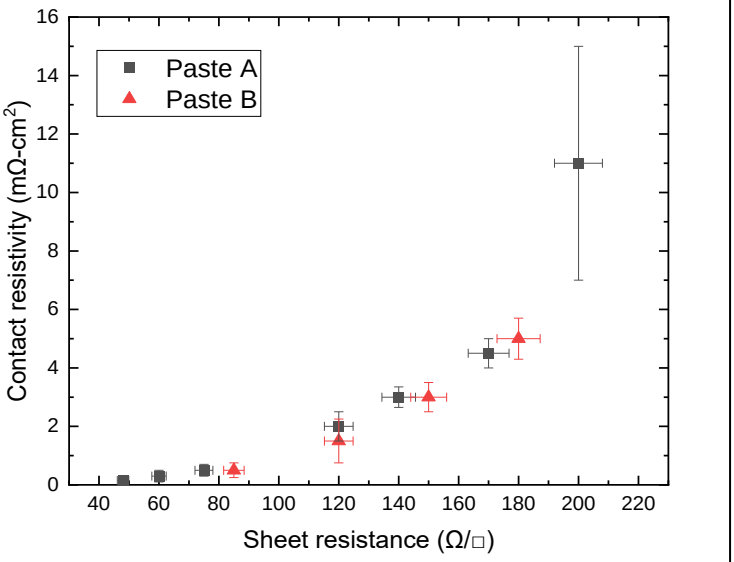


Figure 5 Measured contact resistivity as a function of boron emitter sheet resistance for paste A and B

assuming an ideal or uniform full area metal-Si contact interface. This is described in the next section.

2.1.2 Modeling to establish a baseline metallized $J_{0e,metal}$ value for implanted B emitters assuming uniform metal contact interface with surface recombination velocity (*SRV*) = 10^7 cm/s

Sentaurus Process model was used to simulate the implanted B profiles in this study.

In this model we selected 'Monte Carlo model' for simulating distribution of implanted B and 'Boron-interstitial clusters' (BIC) model for simulation of dopant activation and clustering. This was validated by direct ECV measurements of couple of profiles. Figure 6 shows we obtained a reasonably good match between the measured B profile by ECV and the simulated profile for the 170 Ω/□ emitter. The small deviations between simulation and measurement are attributed to the actual diffusion mechanism and assumed oxidation enhanced diffusion model. This validation provided a good basis for simulating B emitter profiles implanted with different doses, as shown in Figure 7. These profiles were then fed into the Sentaurus Device model to generate J_0 vs *SRV* curves for the simulated profiles by varying *SRV*. Full area baseline $J_{0e,metal}$ value for each emitter was extracted assuming a uniform 100% metal-Si contact area with *SRV* = 10^7 cm/s. This baseline $J_{0e,metal}$ value will be used as a reference to compare the quality of different screen-printed contacts. It is important to recognize that actual screen-printed contact interface is highly non-uniform and can have $J_{0e,metal}$ greater

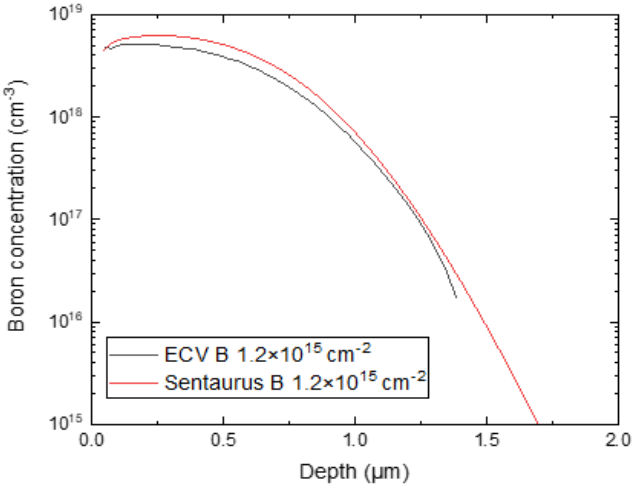
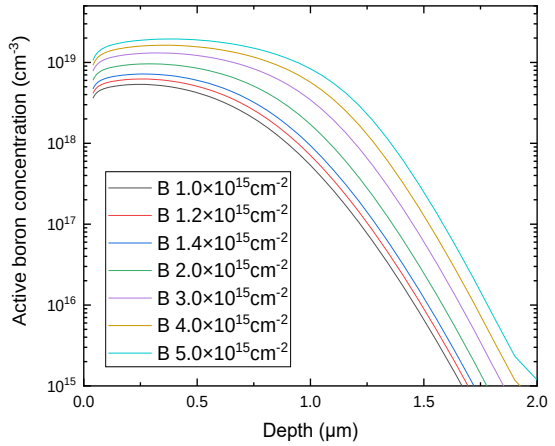


Figure 6. Comparison between the ECV measurement and the Sentaurus Process simulation for B emitter profile with implanted dose of 1.2 × 10^{15} cm^{-2}



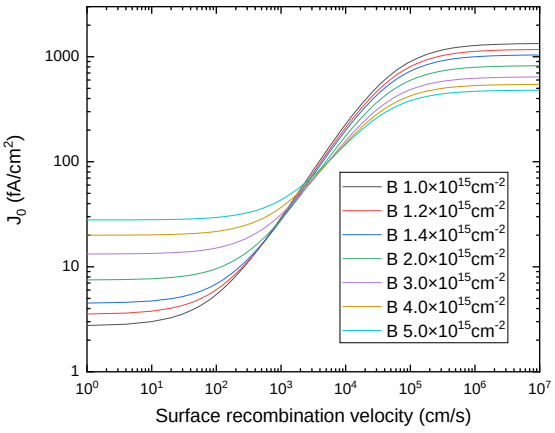


Figure 7. Simulated boron profiles with different implanted boron doses with Sentaurus Process simulation (left) and calculated J_{0e} as functions of surface recombination velocity with different boron implant doses (right)

or less than the baseline case depending on the paste and firing conditions. Figure 8 shows a schematic of a typical screen-printed interface [20]. If there are metal crystallites embedded into the emitter in conjunction with over-etching of the passivation layer by glass frit (resulting in partial truncation of the emitter profile), then $J_{0e,metal}$ could be higher than the baseline case. On the other hand, if there are some unetched passivating SiN islands under the metal grid (resulting in local contacts), then $J_{0e,metal}$ can be lower than the baseline $J_{0e,metal}$ value.

2.1.3 Modeling and quantitative understanding of the significant difference in the $J_{0e,metal}$ for pastes A and B

Formation of screen-printed contacts involves firing-induced etching or dissolution of passivation and antireflection coatings by molten glass frit, followed by solidification of a very thin glass layer between the Si emitter surface and bulk Ag/Al electrode [21-23]. Some Ag crystallites are also formed at the Si surface and get partially embedded into the Si emitter surface to form either direct contact to the top metal electrode or indirect contact through the glass layer above it (Figure 8), which can conduct by tunneling or hopping through the suspended fine Ag particles in it [23, 24]. Any appreciable etching of the emitter surface layer is known to increase sheet resistance and $J_{0e,metal}$ and lower implied FF because contacts are made deeper into the emitter [20, 25, 26]. On the other hand, if the frit is not very aggressive, entire dielectric layer underneath the metal electrode may not dissolve, resulting in the formation of non-uniformly distributed dielectric islands underneath the grid [20]. This will reduce $J_{0e,metal}$ value due to local contacts through the dielectric layer relative to the full area baseline contact. That is why we first established the baseline $J_{0e,metal}$ value for reference.

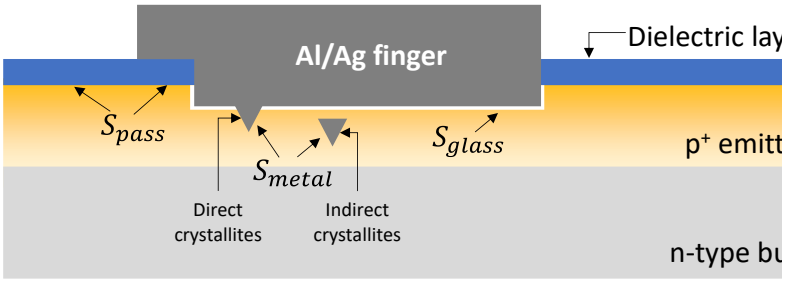


Figure 8. Schematic diagram of the features of metal-Si contact formation after firing.

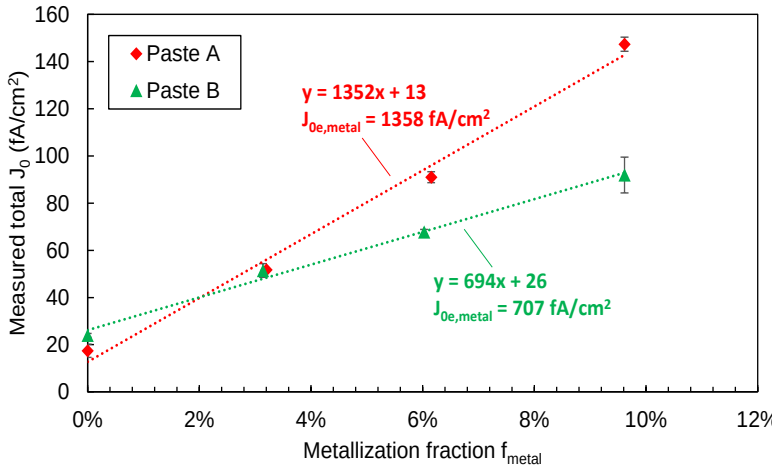
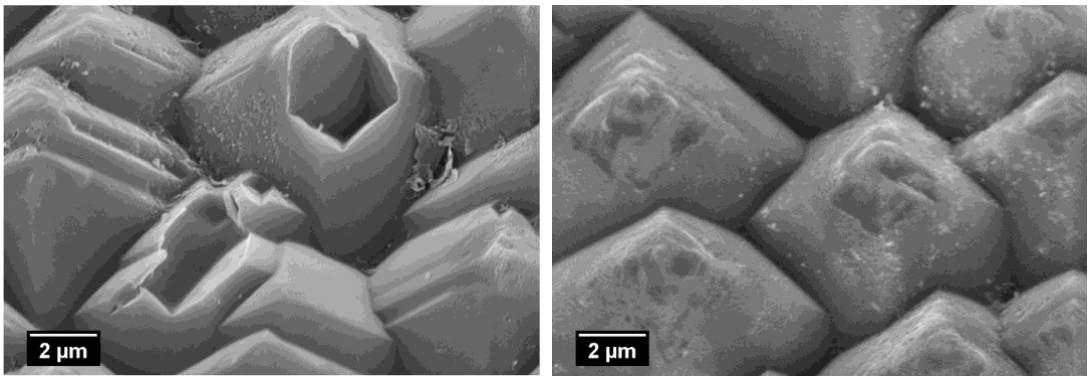


Figure 9. Plot of measured total J_0 as a function of metallization fraction f_{metal} with metal paste A and paste B

In the previous section we defined baseline contact as a contact with uniform interface and 100% metal-Si contact with $SRV = 10^7$ cm/s. Baseline $J_{0e,metal}$ was found to be 1172 fA/cm^2 for our 170 Ω/□ emitter. However linear plots of total J_0 as a function of

f_{metal} for pastes A and paste B on 170 Ω/□ emitter in Figure 9 reveal very different $J_{0e,metal}$ values. For both pastes A and B, the intercept ($2 \times J_{0e,pass}$) gave $J_{0e,pass}$ value of ~ 11 fA/cm^2, but the slope ($J_{0e,metal} - J_{0e,pass}$) gave $J_{0e,metal}$ = 1358 fA/cm^2 for paste A, which is 15% higher than the simulated baseline value. On the contrary, $J_{0e,metal}$ for paste B was found to be 707 fA/cm^2 , which is 40% lower than the baseline contact. To understand the reason for this significant difference, the silicon surfaces under the metal contacts were analyzed by SEM after first removing the bulk metal gridline in HCl:H_2O_2:H_2O 1:1:1 solution and then etching the glass layer in dilute HF solution. The SEM pictures for the two pastes are shown in Figure 10.

Figure 10(a) shows that in the case of paste A, the edges of pyramids are rounded with sporadic deep holes and virtually no cloudy regions on the faces of the pyramids. Deep holes are indicative of penetrating metal crystallites which came off during removal of metal and glass layers. Rounding indicates the possibility of etching of the emitter surface, and lack of cloudy regions suggests the absence of unetched dielectric islands.



(a) Paste A (b) Paste B

Figure 10. SEM images of silicon surfaces under metal contacts after removal of the fired screen-printed metal gridline and glass from fired metal gridlines with paste A and paste B.

This suggests that frit chemistry and firing of paste A is more aggressive than desired. This is consistent with the observed increase in $J_{0e,metal}$ over the baseline contact because both embedded metal crystallites and over-etching of dielectric layer will increase $J_{0e,metal}$ because metal contact is made below the original emitter surface. To estimate the average emitter depth removal, we applied Daniel Inns' [25] and Koduvelikulathu's [27] methodology, which involves using truncated profile after removing a slice of the emitter near the surface, generating a plot of J_{0e} vs *SRV* curve, and then determining full area $J_{0e,metal}$ at *SRV*=10^7 cm/s. Figure 11 shows a graph of $J_{0e,metal}$ vs emitter etch depth for paste A, which reveals an effective metal penetration depth of 130 nm at which $J_{0e,metal}$ matches the measured value of 1358 fA/cm^2.

Contrary to paste A, measured J0e,metal for paste B was found to be much lower (707 fA/cm2) than the simulated baseline J0e,metal = 1172 fA/cm2. Figure 10(b) shows that unlike paste A, the pyramids after firing with paste B do not show voids. Only minimal damage or imprints on the silicon surface are observed after the removal of metal and glass layer. This suggests no appreciable metal penetration or over etching of the emitter. However appreciable fraction of cloudy regions on the sides of the pyramids are observed, suggesting the presence of unetched dielectric islands under the metal grid lines which

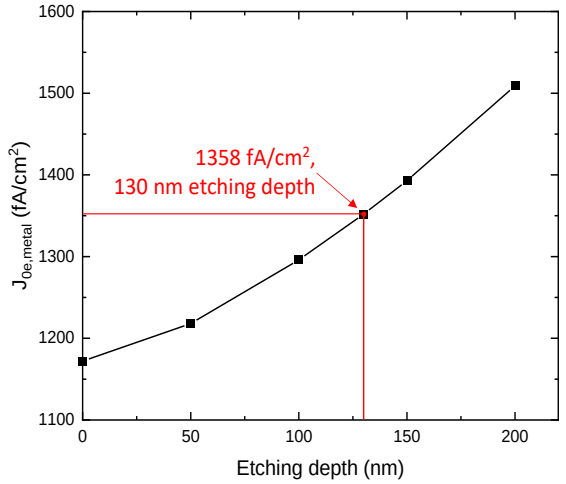


Figure 11. Simulated paste A $J_{0e,metal}$ with varied metal etching depth for 170 Ω/□ B emitter. With an uniform 130 nm etching, the simulated $J_{0e,metal}$ matches with the experimental measurement (1358 fA/cm^2).

were not completely removed during etching of the metal and glass layers. The presence of unetched dielectric layers has been reported by several investigators [20, 21] for the Ag/Al pastes and, as discussed earlier, may lower the $J_{0e,metal}$ by reducing the effective metal-Si contact due to local contacts.

To obtain a quantitative understanding of this effect, we calculated $J_{0e,metal}$ by assuming no emitter surface etching and variable metal-Si contact area fraction under the grid due to dielectric islands. Total $J_{0e,metal}$ was calculated as a function of unetched dielectric area fraction ($f_{dielectric}$) according to $J_{0e,metal}$ = 11 $f_{dielectric}$ + 1172 × (1-$f_{dielectric}$) where 1172 fA/cm^2 represents the calculated full area baseline metal contact for this profile and 11 fA/cm^2 corresponds to the measured full area the $Al_2O_3/SiN_x/SiO_2$ passivated emitter. Figure 12 shows the calculated $J_{0e,metal}$ as a function of dielectric layers area fraction, which reveals that paste B contact interface has ~40% unetched dielectric islands at which calculated $J_{0e,metal}$ matches the measured value of 707 fA/cm^2.

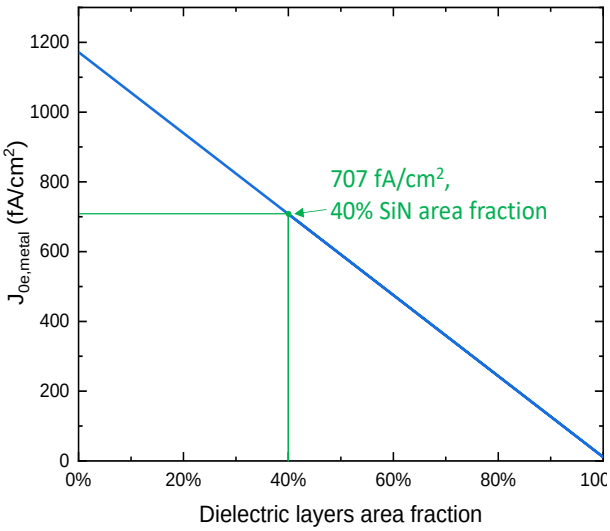


Figure 12. Simulated paste B $J_{0e,metal}$ with varied dielectric layers area fraction for 170 Ω/□ B emitter.

Next we performed model calculations to estimate full area J0e,metal for all the B emitter profiles or sheet resistances fabricated in this study for the two pastes assuming emitter etch depth of 130 nm for paste A and unetched dielectric area fraction of 40% for paste B. These values were then used in device modeling to predict the cell efficiency and select the optimum emitter since J0e,pass and J0e,metal show opposite trends. For efficiency calculations, the number of grid lines was optimized for each sheet resistance. After establishing full area J_{opass} =11 fA/cm^2 and J_{ometal} = 707 fA/cm^2 (Fig. 9) for our 170 Ω/□ implanted homogeneous emitter, we estimated the total metallized J_{0e} using the metal-Si contact area fraction of 2.7% for our 40 µm wide grid lines and floating busbars according to :

$$J_{0e,metal} = 11 \times f_{dielectric} + 707 \times (1-f_{dielectric}) = 11x0.973 + 707x0.027 = 29.8 \text{ fA/cm}^2$$

This is very close to our target value of ~30 fA/cm^2 for the 23% efficient cell (Fig 1). In addition, this emitter has 3-5 mΩ-cm^2 contact resistance (Figure 5) which is also consistent with the requirement of the technology roadmap, therefore, we decided to use 170 Ω/□ homogeneous emitter for our 23% efficiency target.

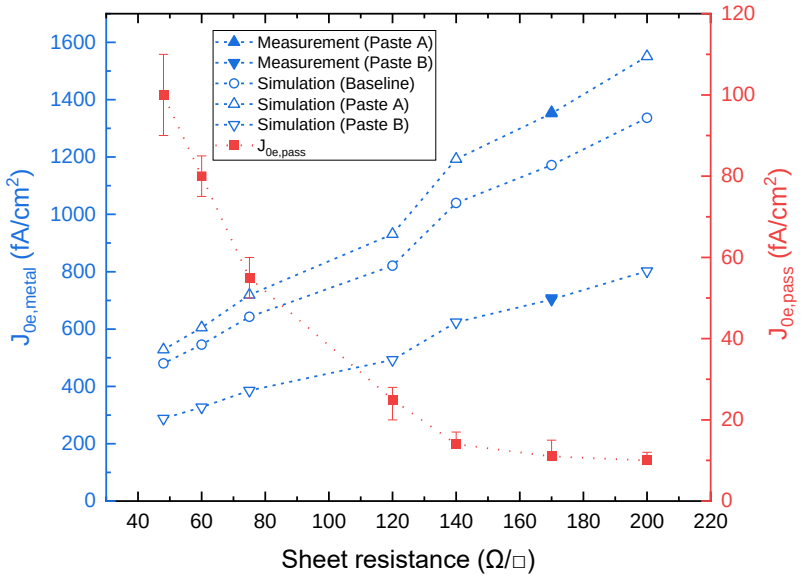


Figure 13. Measured $J_{0e,metal}$ at 170 Ω/□ boron emitter, and simulated $J_{0e,metal}$ for baseline, paste A (assuming emitter etch depth of 130 nm) and paste B (assuming unetched dielectric layers area fraction of 40%) as a function of boron sheet resistance from Sentaurus simulation

2.2 Development of selective boron emitter Selective Emitter Process A: Single boron diffusion and etch back process

Our wet chemical etch-back process involves growing a porous Si layer on the heavily doped boron emitter regions (p^{++}) by immersing the wafers into an etching solution and then removing this porous layer to form lightly doped field regions (p^{+}), while the selective regions for screen-printed metal contacts are masked with a screen-printed acid resist material to protect the initially diffused p^{++} region. It was found that an appropriate wet chemical solution is crucial to obtain uniform etching and controlled etch rate to meet the requirement of the field emitter sheet resistance target. In this study, we developed an acidic solution composed of hydrofluoric acid (HF), nitric acid (HNO_3), and deionized (DI) water to process spontaneous electroless etching of the p^{++} boron emitter in order to obtain high etching homogeneity in combination with controllable etch rate. This is similar to stain etching proposed by Turner in 1960s, in which a porous Si film is formed by surface reaction involving electron transfer. It was proposed that stain etching is an electrochemical reaction involving anodic and cathodic sites on the Si surface with local cell current flowing between them according to the following reactions:

Anode: $Si+2H_2O+mh^+ \rightarrow SiO2+4H^+ +(4-m)e^-$ (1)

$SiO_2+6HF \rightarrow H_2SiF_6+2H_2O$ (2)

Cathode: $HNO_3+3H^+ \rightarrow NO+2H_2O+3h^+,$ (3)

where m is the average number of holes required to dissociate one Si atom. When Si dissolves into etching solution at the anodic sites, the oxidant is reduced at the cathodic sites. When some sites are anodic much more than they are cathodic, etch pits will form. Then, quantum confinement effects shield these pore walls and etching proceeds only at the bottom of pores towards unconfined bulk Si, which results in porous Si formation. This formation is initiated by the valence band holes on the Si surface, which is the product of reaction (3), and the key roles of the oxidant is to inject h+ into the valence band. It is also found that the addition of trace amount of NO_2- from a compound such as sodium nitrite ($NaNO_2$) can catalyze the reactions by eliminating the induction period and greatly accelerating the etching rate. Furthermore, the free hole density of the valence band in the boron doped p+ layer is much higher compared to phosphorus doped n+ layers. As a result, in order to form porous Si, the HNO_3 content in the boron emitter etch-back solution is lower than that of etching-back n+ layers. It is also noteworthy that porous Si is not stable in OH^- aqueous solution and is fairly efficiently removed by it. Therefore, we used potassium hydroxide (KOH) solution to remove porous Si.

In this study, after industrial alkaline texturing of n-type ~2.2 Ω cm Cz Si wafers, a borosilicate glass (BSG) layer was deposited in an atmospheric pressure chemical vapor deposited (APCVD) tool, followed by annealing at 1000 °C for 1 h in N_2 and O_2 ambient. The sheet resistance of the resulting boron-doped emitter was measured by 4-point probe method on 5 spots (center and 4 corners) and obtained from the average value. Then, four different solutions containing different volume ratios of concentrated HF, HNO3, and DI water were used to study the wet chemical etch-back property of the homogeneous p^{++} emitter. Fig. 14 shows that there was no evidence of porous Si growth in solution (d), since the oxidant HNO_3 is not available to inject h^+ into the valence band to initiate the porous Si formation (Eq. (3)). When a small amount of HNO_3 is added, solution (c), a very slow emitter etching take places due to the weak oxidizing power of low HNO_3 concentration that results in a very long induction period of

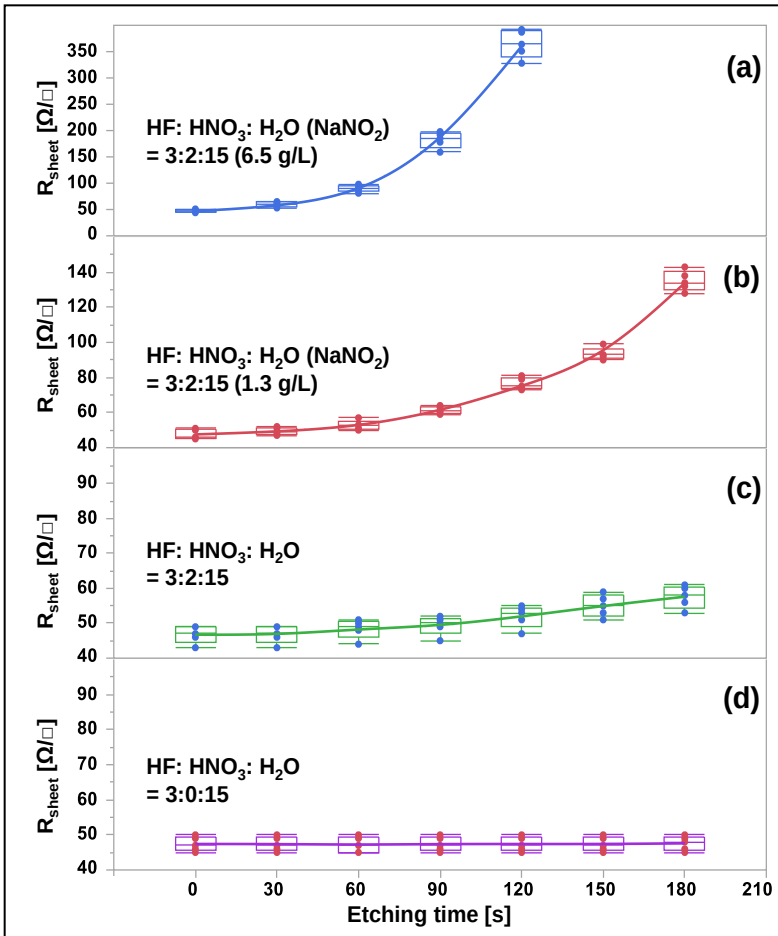


Figure 14. Sheet resistance of etch-backed boron emitter R_{sheet} as a function of etching time in four solution

porous Si formation. Even after 180 s of etching, the sheet resistance increases from 47 to 58 (±5) Ω/□. When $NaNO_2$ catalyst is added (1.3 g/l concentration), solution (b), the sheet resistance increases with etching time and reaches 135 (±10) Ω/□ after 180 s etching. This is because the NO_2^- ions from $NaNO_2$ react with proton (H^+) to form nitrous acid (HNO_2). Then, the HNO_2 reacts with HNO_3 to produce the NO_2 that oxidizes the Si surface by injecting a hole, which accelerates the etching rate. Hence, solution (b) has a higher etching rate than (c), even though they have the same $HF/HNO_3/H_2O$ volume ratio (3:2:15). This controlled etching rate in solution (b) is suitable for manufacturing in terms of process time and etching homogeneity (≤10% on sheet resistance variation). However, if the $NaNO_2$ concentration increases to 6.5 g/l, solution (a), the chemical reaction is dramatically intensified, leading to a less controllable rapid etching rate. The sheet resistance quickly reaches 360 (±40) Ω/□ after etching just 120 s. This is because the oversupply of NaNO2 catalyst makes the porous Si growth too rapid and difficult to control. Therefore, only solution (b) was found to be appropriate and was used for the selective emitter and cell fabrication in this work.

The effect of emitter etch-back on the passivation quality is shown in Fig. 15. Fig. 15 shows the Auger-corrected inverse effective lifetimes for symmetric structures with various emitters passivated by Al_2O_3/SiN_x on high bulk lifetime (≥2 ms) Cz wafers. Al_2O_3 was deposited by plasma-assisted atomic layer deposition (ALD) at a temperature of 150 °C for 100 cycles, followed by a 70 nm SiNx layer deposited by plasma-assisted chemical vapor deposition (PECVD) at 400 °C to activate the Al_2O_3 charge and serve as an antireflection coating layer. Note that the 47 Ω/□ emitter is obtained just after boron diffusion anneal, which increases to 65, 120, 150, and 180 Ω/□ after etching in solution (b) for 0, 150, 165, and 180 s, respectively, respectively, followed by porous Si removal in 1% diluted KOH for 120 s and a high temperature thermal oxidation above 1000 °C. J_{0e} drops significantly from 85 to 32 fA/cm^2 for the p^{++} emitter due to lower surface recombination velocity, while its sheet resistance increases from 47 to 65 Ω/□. In addition, after the wet chemical etch-back and thermal oxidation, J_{0e} decreases further to 21, 14, and 9 fA/cm^2 due to the reduced Auger recombination in the etched-back shallow emitters with sheet resistances of 120, 150, and 180 Ω/□, respectively.

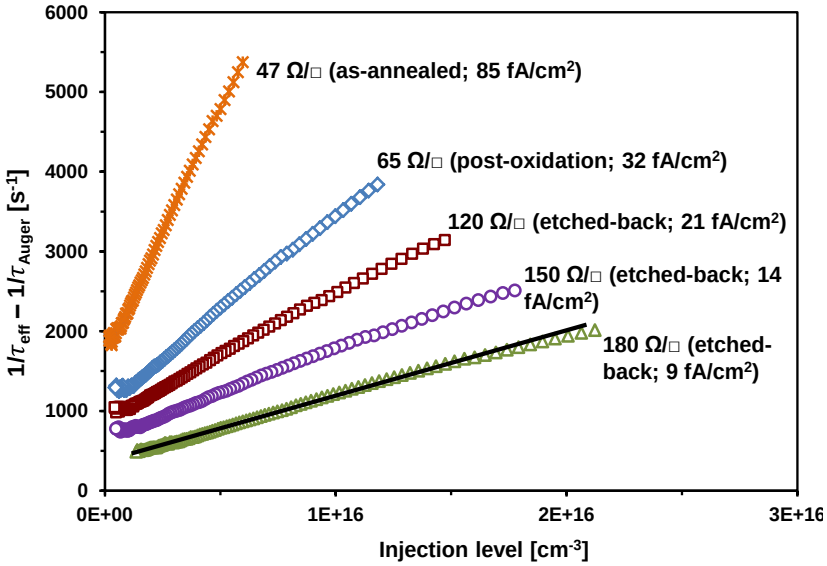


Figure 15. Measured Auger corrected inverse effective lifetime as a function of the injection level for Joe samples with various sheet resistance.

To confirm etch process, we fabricated n-TOPCon cell with selective emitter fabricated by etch back process. After the initial boron diffusion, an acid resist mask was screen-printed. Next, the Si wafers were immersed in solution (b) to grow porous Si for 180s, followed by porous Si and resist mask removal. Then, the oxidation was performed above 1000 °C, which increases the sheet resistance of p^{++} region to 65 Ω/□, in combination with 180 Ω/□, for the etched-back field region (p^{+}). The optical microscope image in Fig. 16 (a) clearly shows that the p^{++} region is about 220 µm wide (pitch of 1.56 mm), which is suitable for aligning the screen-printed Al/Ag gridline. The next step involves tunnel oxide passivated back contact (TOPCon) formation on the rear as shown by the transmission electron microscopy (TEM) image in Fig. 16(b). This carrier selective TOPCON scheme provides excellent surface passivation by allowing efficient transport of majority carriers (electrons) while effectively blocking minority carriers (holes). Al_2O_3/SiN_x was deposited on the front selective boron emitter for passivation and antireflection coating. Then, Al/Ag gridlines were aligned and screen-printed within 220 µm wide p^{++} tracks, followed by a high temperature (>700 °C) firing in an industrial-style belt furnace to obtain good ohmic contacts on the front. The resulting Al/Ag gridline width is 65 µm (Fig.16(a)). Finally, Ag was evaporated on top of the poly-Si of the entire rear side to form the back contact. As a result, the 21.04% efficient selective emitter cells in this study gave only ~ 0.2% higher absolute efficiency over the homogeneous cell as shown in table 2.

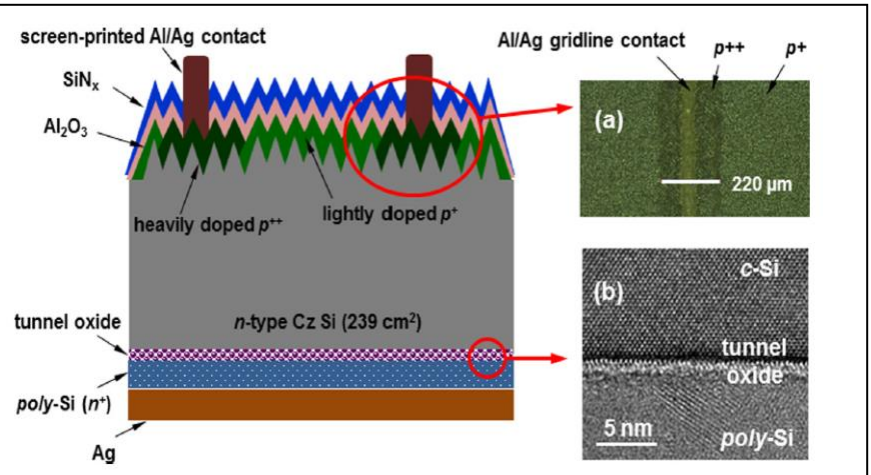


Figure 16. Schematic of solar cells with selective boron emitter fabricated etch back process

In summary, a high V_{oc} of 682.8mV and efficiency of 21.04% for front-junction n-type Si solar cell with APCVD deposited selective boron emitter formed by wet chemical etch-back has been reported in this task. This study demonstrates excellent performance of our etch-back process on heavily boron doped emitter by growing porous Si in a proper

Table 2. Light I-V results of n-type solar cells featuring homogeneous or selective B emitter

Emitter structure		V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)	R_s (Ω cm^2)
Homogeneous (65 Ω/□)	Average	673.5 ± 2.4	39.2 ± 0.2	78.3 ± 0.4	20.6 ± 0.2	0.51 ± 0.06
	Best	676.6	39.3	78.4	20.83	0.52
Selective (65/180 Ω/□)	Average	679.2 ± 3.5	39.5 ± 0.2	77.7 ± 0.3	20.8 ± 0.2	0.62 ± 0.04
	Best	682.8	39.6	77.9	21.04	0.63

chemical solution with $NaNO_2$ catalyst and subsequently removing it, which results in J_{0e} of 9 fA/cm^2 on the etched back p$^+$ region (~180 Ω/).

Selective Emitter Process B: Two step boron diffusion to achieve metallized J_{0e} of ~25 fA/cm^2

Various investigators have tried boron selective emitter formation by different methods, such as etch-back, laser doping and in some cases 2-step diffusion using expensive photolithography. Each of the above-mentioned methods have their drawbacks. In the case of etch-back process, emitter etching may be difficult to control, may modify the texturing and decrease the J_{sc}. In addition, oxidation may be needed after etch-back to improve the J_{0e}. The laser doping method relies on excess B dopant in the B glass after the formation of the lightly doped area. The desired 120-150 Ω/□ field emitter may or may not have enough dopant to accomplish this compared to a 65-90 Ω/□ emitter. In addition, laser doping can cause some damage to the silicon surface and to the lightly doped emitter underneath and may require an additional high temperature anneal to recover laser damage.

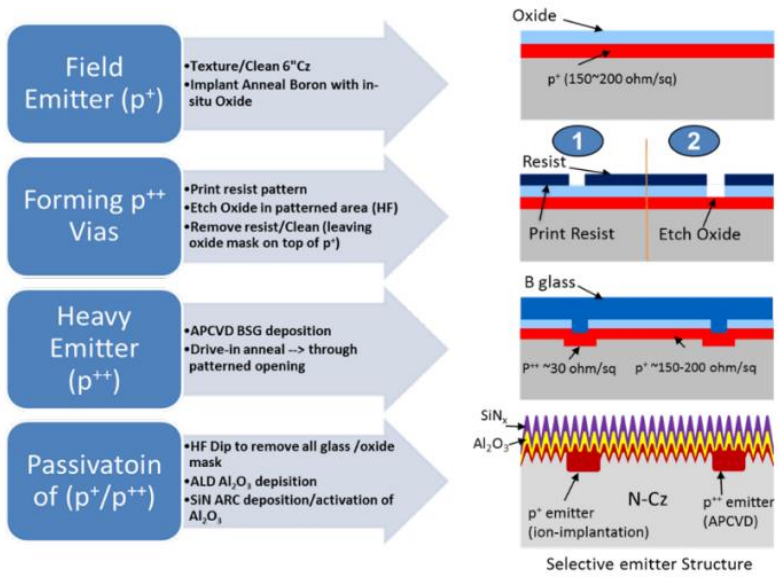


Figure 17. Process flow to fabricate boron selective emitter using two-step emitter approach

A two-step emitter approach can control the p$^+$ and p^{++} profiles independently, however in the past only

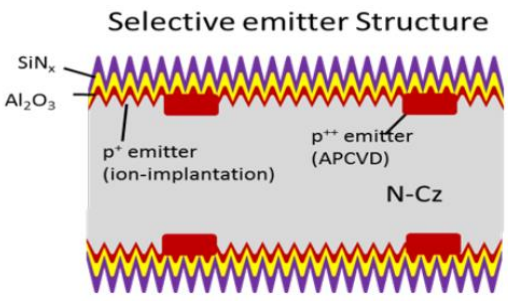


Figure 18. Fabricated symmetric p+p++ Jo test structure

small area cells have been attempted using a time-consuming and expensive photolithography approach, which cannot be applied to large-area commercial cells. In this section, we report on the development of a manufacturable selective emitter with screen-printed contacts that can result in very low J_{0e} for commercial size solar cells. Figure 17 shows our process sequence for forming a high-quality boron selective emitter. At first, symmetric p^+p^{++} test structures were fabricated to confirm the passivation quality of unmetallized boron selective emitter. Textured Cz wafers with resistivity of ~20 Ω-cm and high bulk lifetime (> 3 ms) were used in this study to form symmetric structures as shown in Figure 18. The Cz wafers were annealed at 1050°C in N_2 and O_2 after homogeneous ion-implantation on both sides with various doses to achieve sheet resistance in the range of 120-200 Ω/□. Screen-printed negative resist patterns were printed on both sides based on optimized and modeled grid design and sheet resistance. As shown in Figure 17, these wafers were then dipped in dilute HF solution to get ~130 µm wide openings through the 500 Å oxide mask. Screen-printed resist was then removed in solvents. After cleaning the wafers with patterned oxide mask, APCVD boron-doped glass with a suitable concentration was deposited on the entire wafer on both sides, followed by optimized anneal to drive in the heavy boron diffusion (p^{++}) in the open grid. The boron glass and oxide mask were then removed, and the wafers were passivated on both sides by ALD Al_2O_3 and SiN capping layer, followed by simulated contact firing in a belt furnace without any metal contacts. Very low J_{0e} of 13 fA/cm^2 for 200/30 Ω/□ and 18 fA/cm^2 for 150/30 Ω/□ unmetallized p^+/p^{++} selective emitters were achieved on symmetric structures.

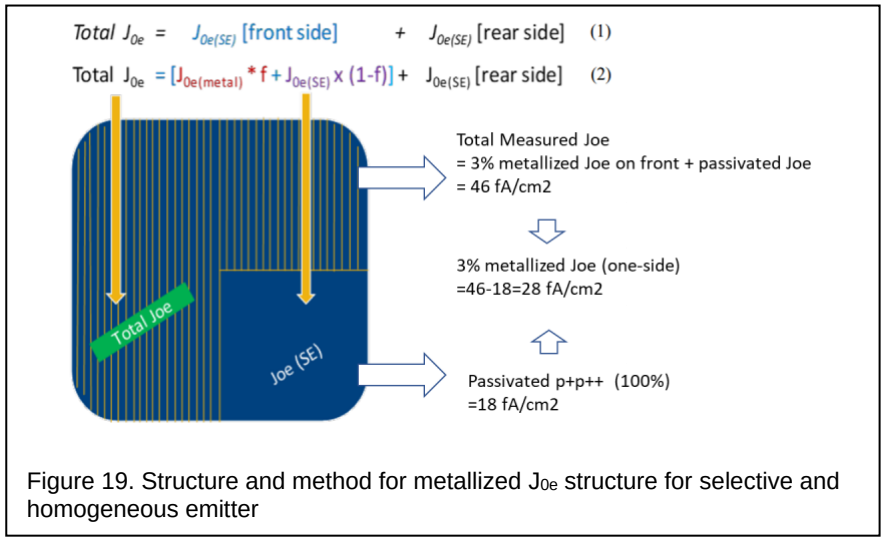


Figure 19. Structure and method for metallized J_{0e} structure for selective and homogeneous emitter

In order to study the effect of screen-printed metal on the heavily doped emitter, symmetric (textured and passivated) test structures were prepared with 150 Ω/□ and 30 Ω/□ homogeneous emitters as well as the 150/30 Ω/□ selective emitter. Then metal was screen printed on one side with different spacing and fired. Excess metal was then removed in HCl to extract the metallized J_{0e} using the QSSPC measurement technique. Figure 19 shows the metal grid printed within the selective emitter pattern leaving a quarter of the wafer unprinted to extract the total J_{0e} of metallized selective emitter as well as

Emitter	Sheet Rho Field – Contact (Ω/□)	J_{0e} passivated, p^+ (fA/cm^2)	J_{0e} passivated, p^{++} (fA/cm^2)	Calculated J_{0e} 100% metal (fA/cm^2)	Total J_{0e} (3% metal + 5% p^{++} passivated + 92% p^+ passivated)
SE (p^+–p^{++})	150 – 30	18	86	210	27

Table 3. Metallized J_{0e} for p^+p^{++} selective boron emitter

unmetallized emitter. As shown in Fig. 19, the first equation represents the total J_{0e} including the front and the rear selective emitters. Since only the front side of the wafer was metallized, J_{0e} from the front side can be broken down into metallized + unmetallized regions as shown by the second equation in Fig. 19. Since the metal fraction, f, is measured, we can calculate the total metallized J_{0e} of the selective emitter as shown in Table 3. Table 3 shows that for a metal fraction of 3%, which is achievable by floating busbars, a total metallized J_{0e} of 27 fA/cm^2 was achieved for this selective emitter. A 1 cm strip was cut from the same sample shown in Fig. 19 to perform TLM measurement, which gave a specific contact resistance of 10.74 mΩ-cm^2 and 2.25 mΩ-cm^2 for the 150 Ω/□ homogeneous and the 150/30 Ω/□ selective emitter, respectively. This selective emitter was first tested on a traditional n-PERT cell with full $POCl_3$ BSF, which gave 6 mV higher V_{oc}, 0.4 mA/cm^2 increase in J_{sc} and 0.4% higher efficiency compared to the counterpart n-PERT with homogeneous emitter. This quantitatively validates the superiority of the newly developed selective emitter and its metallized J_{0e} of 28 fA/cm^2 is consistent with the requirement of 23% n-TOPCon cell (Fig. 1). We have had some issues with the n-factor or junction shunting in the TOPCon cells with selective emitter. This is currently under investigation. Table 4 shows that recently when we introduced a chemical edge isolation step it reduced the junction shunting appreciably and resulted in 22.3% large area selective emitter cell.

Table 4 Light I-V measurement results of n-TOPCon solar cells with ~140/30 Ω/□ selective B emitters with and without edge isolation

Edge Isolation	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	Eff [%]	n-factor	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]
No	692	39.7	77.3	21.3	1.29	0.64	1545
Yes	703	40.1	79.0	22.3	1.13	0.55	566219

Key Achievements: In task 3, we demonstrated the development and implementation of screen-printed carrier-selective tunnel oxide passivated poly-Si/SiO2 rear contact for high-efficiency front junction crystalline Si solar cells. Using a 15Å thick tunnel oxide grown in nitric acid at 100°C and capped with 100-200 nm LPCVD grown n$^+$ poly-Si, we were able to achieve excellent rear contact passivation even after the formation of screen-printed contacts. We achieved very low J_0 of 1-2 fA/cm^2 from LPCVD grown n-TOPCon after SiN_x capping and contact simulated firing process. We also demonstrated metallized n-TOPCon J_0 of ~5 fA/cm^2 with 13% metal coverage after firing the screen-printed Ag contacts through the SiN_x capping layer on top of poly-Si. This is consistent and sufficient for 23% cells according to our technology roadmap.

Results and Discussion in Task 3

Development of LPCVD n-TOPCon Process

Efficiency of current front junction *n*-type silicon solar cells is largely limited by the recombination in the heavily doped regions in the absorber and at the metal/silicon contacts. Carrier selective passivated contacts are a promising candidate for next-generation high-efficiency Si solar cells because they can eliminate high recombination

at the metal/Si contacts and also bypass the need for heavily diffused regions inside the absorber. V_{oc} can approach Auger limit with carrier selective passivated contacts because V_{oc} becomes independent of doping induced Fermi levels and dependent on the Quasi Fermi levels dictated by the bulk lifetime and injection level in the base. In traditional cells, diffused and metallized regions in the absorber are utilized for separation, collection, and extraction of light-generated carriers in the absorber. Carrier selective passivating contacts provide an opportunity to displace these regions outside the absorber but still utilize their positive attributes.

3.1 Understanding and Operating Principle of Carrier Selective Tunnel Oxide Passivating Contact

Figure 20 shows the schematic band diagram of the electron selective tunnel oxide passivated contact involving *n*-type substrate, tunnel oxide, and n^+ polysilicon layer. Metal contact is formed on top of the polysilicon layer. The band diagram in Fig. 20(B) shows that there are four parallel mechanisms that contribute to carrier selectivity: (1) heavily doped n^+ polycrystalline silicon creates an accumulation layer at the absorber/tunnel oxide interface due to the work function difference between the n^+ polycrystalline silicon and the *n*-silicon absorber. This band bending induced accumulation layer provides a barrier for minority carrier holes to get to the tunnel oxide while assisting majority carrier electrons to migrate toward the oxide/Si interface. (2) Tunnel oxide provides the second level of carrier selectivity because it presents 4.5 eV barrier for holes to tunnel through relative to 3.1 eV barrier for electrons. (3) Large number of available states in the conduction band of the poly-Si layer in combination with large number of electrons at the absorber/oxide interface increases tunneling probability and allows electrons to easily tunnel through the oxide, however, holes near valence band edge of absorber may not be able to tunnel through because of fewer holes and very few or no available states in the forbidden gap of n^+ poly-Si. (4) Even if a hole is somehow able to tunnel through the oxide into the n^+ poly-Si, it encounters much higher barrier or resistance compared to electrons to get to the metal contact for recombination. Thus, the recombination of the minority carrier holes significantly reduced at the metal contact and in the heavily diffused poly-Si region due to high carrier selectivity. In addition, induced field effect increases electron concentration (accumulation layer) and reduces hole concentration significantly at the absorber-poly silicon interface, reducing defect induced SRH recombination at the interface, further lowering the J_0 value associated with this TOPCon structure. Finally,

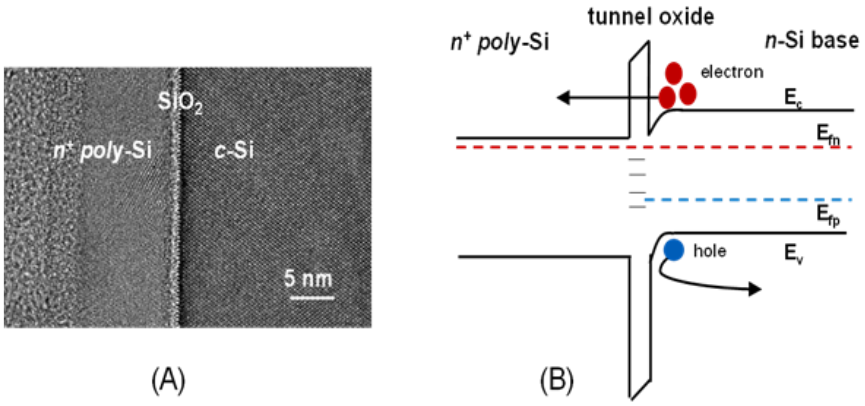


Figure.20 Transmission electron microscopy image (A) and schematic band diagram (B) of tunnel oxide passivated contact structure

there is generally a very modest/shallow phosphorus diffusion into the absorber through the tunnel oxide during the polysilicon anneal which partially shields the tunnel oxide/Si interface recombination without appreciably introducing Auger recombination.

HIT cell, which has produced the world's highest V_{oc} and cell efficiency, is a great example of carrier selective passivated contact where an intrinsic and doped a-Si layers are deposited on both sides of Si wafer to achieve carrier selectivity and interface passivation. However, this leads to some loss in J_{SC} due to absorption in a-Si layers. In addition, there is high cost associated with ITO deposition low-temperature metallization. Therefore, we decided to develop TOPCon which uses poly-Si/SiO_2 contacts to minimize absorption compared to a-Si and allows the use of traditional low-cost screen printing for contact formation. This was done by first developing the technology for TOPCon and then optimizing it to achieve the target metallized Jo value of ~ 5 fA/cm^2. This is described in the next section.

3.2 Experimental Development and Characterization of nTOPCon using Chemically Grown Oxide and LPCVD Polysilicon

In this section we report on the development of n-TOPCon by chemical growth of tunnel oxide followed by LPCVD deposition of phosphorus-doped polysilicon anneal with the goal of achieving metallized $J_{0b'}$ of ~ 5 fA/cm^2. Figure 21 shows the symmetric structure used to study the effect of various tunnel oxides and polysilicon layers on the $J_{ob'}$ and implied open-circuit voltage (iV_{oc}).

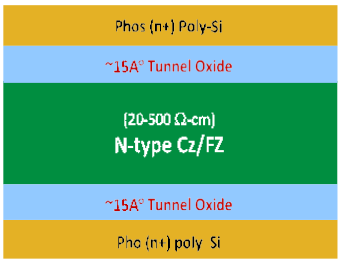


Figure 21. Symmetric structure to study $J_{ob'}$ and iV_{oc}

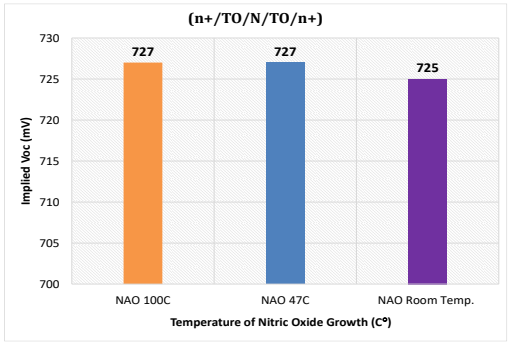


Figure 22. Effect of NAO temperature on iV_{oc}.

A high lifetime wafer was used for this study so that the variation in J_0 primarily reflects the change in surface passivation quality of TOPCon. Lightly doped Cz and/or FZ wafers with resistivity of 20-500 Ω-cm and high bulk lifetime (>3ms) were used in this study. The iV_{OC} and J_0 were measured at an injection level of ~1-3E15/cm^3 using the Sinton PCD tester and the method proposed by Kane and Swanson [16]. A thick thermal oxide was grown as reference while thin tunnel oxides (~15Å) were grown chemically in sulfuric acid (H_2SO_4) and nitric acid (HNO_3) at room temperature. After growing the tunnel oxides, a phosphorous-doped polysilicon layer was deposited on both sides of the wafer in a LPCVD furnace at a temperature of

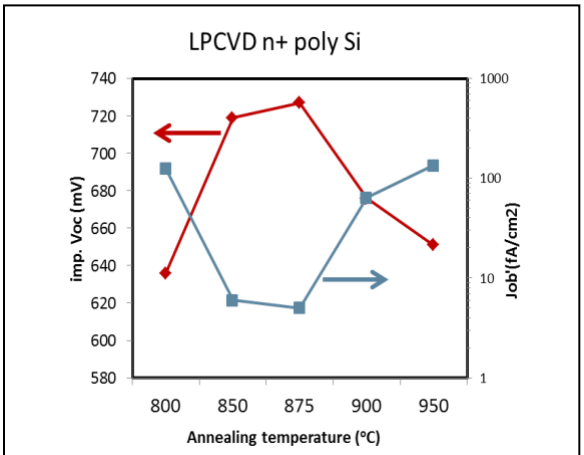


Figure 23 Implied V_{oc} as a function of anneal temperature of n-TOPCon with chemically grown tunnel oxide and LPCVD poly-Si

~600°C with SiH_4 and PH_3 gases. Since the deposited poly layer at 600°C was found to be a mixture of amorphous and crystalline silicon, a crystallization anneal was performed to improve the properties of this layer and activate the dopants. After a crystallization anneal above 800°C in N_2 ambient, the implied open circuit was measured using the Sinton PCD tester. As expected, the 230Å thick thermal oxide reference gave higher iV_{oc} (707mV) but is not suitable for tunneling due to its thickness. The oxide grown in nitric acid (695mV) gave better iV_{OC} than the sulfuric acid (675mV), however the iV_{OC} in both cases was below the target value of 725mV to achieve 23% efficient cells.

Since chemically grown oxide at room temperature is generally inferior due to high interface state density, a study was conducted to optimize its quality by Nitric Acid Oxide (NAO) growth at different temperatures (25-100°C). Identical conditions were used for the n^+ polysilicon deposition and anneal (875°C). Symmetric structures n^{+poly}/TO/N/TO/n^{+poly} were fabricated for this study. Figure 22 shows that the iV_{oc} for NAO grown at elevated temperature (100°C) is only marginally higher than the room temperature. Figure 22 shows that optimization of tunnel oxide and deposition/anneal of nTOPCon resulted in iV_{OC} of ~730 mV and unmetallized J_0 of ~6 fA/cm^2. For the best results, we decided to use 100°C temperature for NAO and 875°C anneal for poly in this study.

3.3 Detailed characterization of LPCVD polysilicon and poly-Si/oxide interface

In order to understand and explain the effect of crystallization temperature on iV_{oc} and J_0 in Figure 23, we first performed SIMS (Secondary Ion Mass Spectrometry) analysis on mirror-polished wafers to study the phosphorous activation and diffusion into Si as a function of polysilicon anneal temperature through the tunnel oxide. Figure 24 shows the SIMS profile of the phosphorous doped polysilicon in the as-deposited state as well as a function of annealing temperature. In these type of SIMS measurements Argon sputtering can cause some phosphorous to diffuse into the silicon (black curve in Figure 24). Figure 24 reveals that phosphorous diffuses deeper (>120nm) as the anneal temperature is increased from 800°C to 930°C. Low P content can improve iV_{oc} by shielding the interface defects, like in a BSF. However excessive P diffusion can induce Auger recombination and bandgap narrowing and degrade iV_{oc} and J_0.

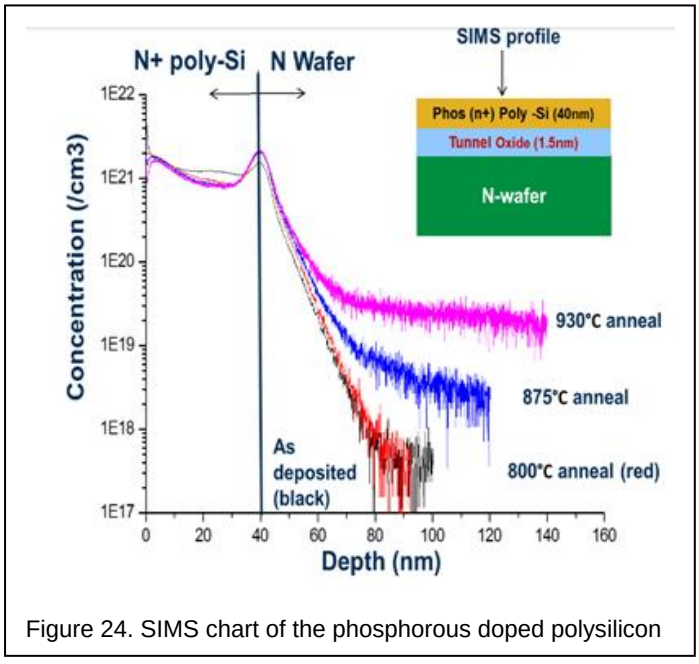


Figure 24. SIMS chart of the phosphorous doped polysilicon

To further understand the degradation in iV_{oc} at higher anneal temperatures (>900°C), HREM (High-resolution transmission electron microscopy) was performed. HREM is an imaging mode of the transmission electron microscope (TEM) that allows for direct imaging of the atomic structure of the sample. Figure 25 shows that the thin ~1.5nm

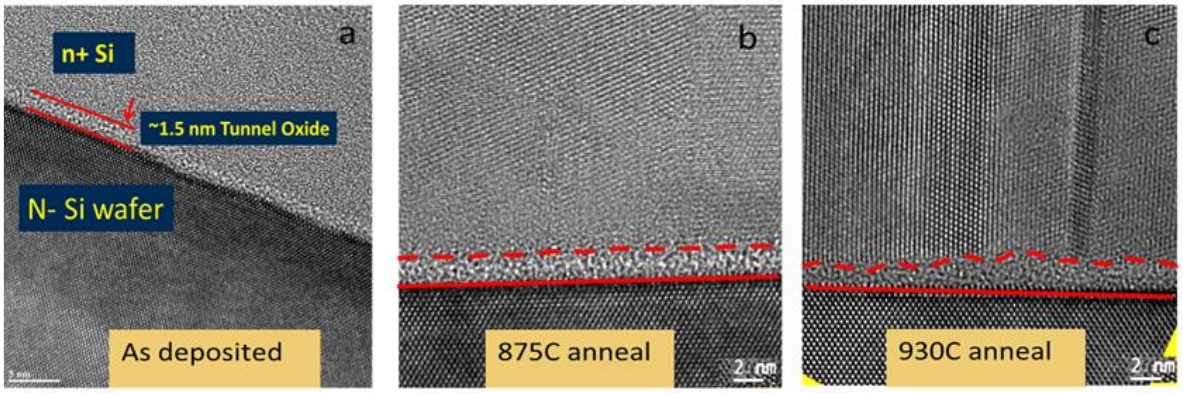


Figure 25 HREM images: a) As deposited, b) Annealed at 875°C, c) Annealed at 930°C

chemical oxide can withstand moderate to high (900°C) anneal temperatures since we did not observe any disruption or breakdown. However, after the 930°C anneal the tunnel oxide is somewhat deformed as indicated by the arbitrary dashed red line in image. Figure 25 c, which shows larger poly-crystalline grains causing the tunnel oxide to thin in some regions which may locally disrupt oxide in extreme case. This could enhance undesirable tunneling of holes from the bulk into the n+ region and reduce the carrier-selectivity, accounting for lower the iV_{oc}. We believe a combination of interface disruption and excess P diffusion is the reason for degradation at higher anneal temperatures (.875°C). At lower temperatures (>750°C) iVoc increases gradually because of more dopant activation, crystallization and modest P diffusion into Si.

3.4 Investigation of the impact of metal contact on saturation current density ($J_{0b'}$) of TOPCon structures

Symmetrical test structures of n-TOPCon were prepared to quantify their passivation properties as well as the impact of screen-printed metallization (Figure 26). The symmetric LPCVD grown n-TOPCon structures were prepared on planar Si wafers capped with SiN_x for the J_0 measurements. In order to quantify the effect of screen-printed fire-through metallization on recombination current density of rear

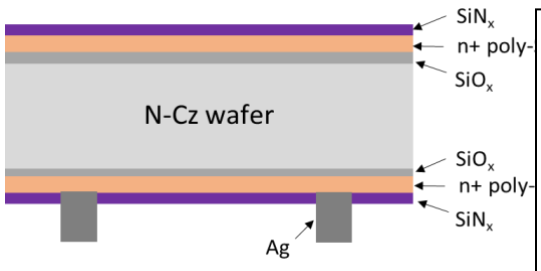
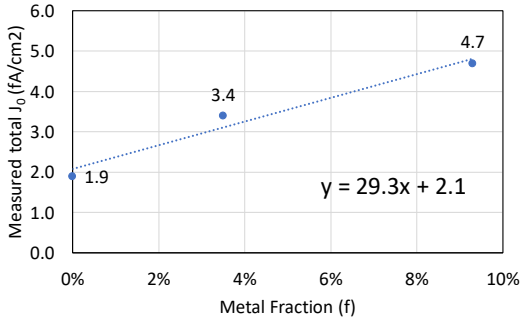


Figure 26. Schematic of n-TOPCon and to investig
the impact of screen-printed metallization on J_0

$$Total\ J_0 = (J_{0\_TOPCon,metal} - J_{0\_TOPCon,pass}) \times f + 2\,J_{0\_TOPCon,pass}$$



n-TOPCon symmetric test structure

$J_{0\_TOPCon,pass}$ ~ 1 fA/cm^2

$J_{0\_TOPCon,metal}$ ~ 30 fA/cm^2

Figure 27 Measured recombination current density (J_0) from n-TOPCon and as a function of metal fraction on one side

n-TOPCon (J_{0_TOPCon}), gridlines with different metal coverage were screen-printed only on one side of the symmetric structures. After the simulated contact firing, the excess printed metal was etched away in $HCl:H_2O_2:H_2O$ =1:1:1 solution, leaving only the embedded metal contact/crystallites on the surface for the metallized J_0 measurements.

For the quantitative study, the total J_0 of the above test structures with different metal fraction on one side were measured by the PCD tester, with the light flashing on the no-metal side to avoid any shading effect. In addition, specific contact resistance was measured using TLM pattern on the same samples, resulting in 2 mΩ-cm^2 values for the n-TOPCon. Figure 27 shows the measured total J_0 from the n-TOPCon test structures as a function of metal fraction on one side. The total measured J_0 of the test structures with different metal fractions (f) on one side can be expressed as

$$\begin{aligned} Total\, J_0 &= J_{0\_TOPCon(no\ metal)} + J_{0\_TOPCon(with\ metal\ fraction\ f)} \\ &= J_{0\_TOPCon,pass} + [J_{0\_TOPCon,pass} \times (1-f) + J_{0\_TOPCon,metal} \times f] \\ &= (J_{0\_TOPCon,metal} - J_{0\_TOPCon,pass}) \times f + 2\, J_{0\_TOPCon,pass} \end{aligned}$$

where $J_{0\_TOPCon,pass}$ and $J_{0\_TOPCon,metal}$ are the full area J_0 values for the un-metallized and metallized regions of n-TOPCon.

Figure 27 shows that without any metal, intercept or total J_0 (=2 × $J_{0\_TOPCon,pass}$) of ~ 2 fA/cm^2 was achieved, which corresponds to a $J_{0\_TOPCon,pass}$ of ~ 1 fA/cm^2, indicating excellent passivation quality of our SiN_x capped LPCVD grown unmetallized n-TOPCon after simulated contact firing. Note that SiN deposition lowered the unmetallized $J_{0\_TOPCon,pass}$ from ~ 6 to ~ 1 fA/cm^2. However, total J_{0_TOPCon} did show a slight increase with increased metal fraction (Figure 27). From the intercept and slope of the linear fit to the experimental data in Figure 27 (a) (y = 29.3 x + 2.1), we obtained a full area $J_{0\_TOPCon,metal}$ ~30 fA/cm^2 and $J_{0\_TOPCon,pass}$ ~ 1.05 fA/cm^2 for the metallized and unmetallized n-TOPCon regions. This corresponds to a total metallized J_{0_TOPCon} of 5 fA/cm^2 (= 30 × 13.5% + 1 × 86.5%) for 13.5% metal coverage on the back used in this study. This is entirely consistent with our roadmap which calls for development of metallized Job' of ~5fA/cm^2 in combination with contact resistivity of < 3 mΩ-cm^2.

3.5 Investigation of the impact of LPCVD poly thickness on J_0 and contact resistivity of n-TOPCon

For the screen-printed fire through-contacts on n-TOPCon structure, in this section thickness of poly-Si was optimized to achieve with good passivation quality without compromising the contact resistivity. This is because if poly-Si is too thick, efficiency will be reduced by the parasitic absorption losses. However, if it is too thin, the passivation quality may be degraded by screen-printed metallization and HF etching involved in the fabrication process.

Therefore, we investigated the quality and performance of different LPCVD poly-Si thicknesses by fabricating symmetric structures with tunnel oxide and LPCVD poly on both sides, and then measuring the $J_{0b'}$ after (a) poly-Si anneal (b) SiN_x deposition, and (c) contact firing cycle. Figure 28 shows the change in $J_{0b'}$ for 100 nm & 200 nm thick poly-Si. Note that unmetallized $J_{0b'}$ gets better both after SiN_x deposition and simulation firing possibly due to hydrogenation of the interface defects. This resulted in excellent unmetallized $J_{0b'}$<2 fA/cm^2 for both 100 nm and 200 nm thick poly-Si, which is at least as good or superior to the values reported in the literature [28, 29].

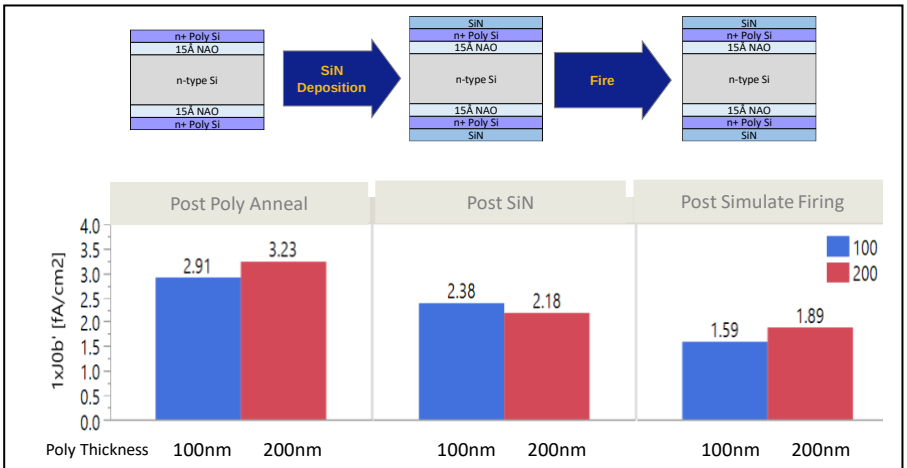


Figure 28. $J_{0b'}$ with different LPCVD poly-Si thickness at different stages

Next we investigated the impact of metallization and found that screen-printing metal pastes and firing conditions play an important role in metallized J_0 value. Optimized paste and firing condition can achieve good metal contact resistivity without sacrificing the passivation quality. The impact of metallization on J_0 was investigated with the help of symmetric LPCVD TOPCon structures screen-printed with different silver metal pastes only on one side (Fig 26). After firing, the metal was removed by HCl/H_2O_2 solution. Figure 29 demonstrates the extracted full area $J_{0,poly}$ with different metal coverage (0-12%) using the optimized firing condition. It shows that we were able to achieve excellent $J_{0b'}$ of around 5 fA/cm^2 with ~9% metal coverage on both 100 nm & 200 nm poly with Dupont 17S paste. It also shows that selecting the optimized metal

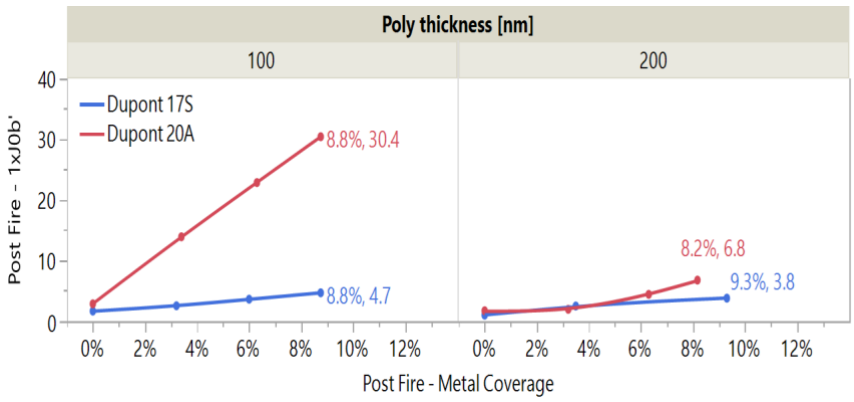


Figure 29. Full area $J_{0,poly}$ with different metal coverage (fired at 780C). The left column is with 100nm poly-Si, and the right column is with 200 nm poly-Si.

paste is more important for thinner poly (100 nm) because for paste 20 A this value increases rapidly to 30 fA/cm^2 for thinner poly.. Table 5 shows that we can also get good contact resistivity and sheet resistance with both 100 & 200 nm poly thickness. Thus proper choice of screen-printing metal paste, firing and thickness of LPCVD TOPCon we were able to achieve metallized $J_{0b'}$ of 5 fA/cm^2 with ~ 10 % metal coverage, in combination with contact resistivity of < 2 mΩ-cm^2. This is entirely consistent with our technology roadmap requirement for 23% cells.

Task #4: Advanced screen-printed and plated fine-line metallization

100nm Poly Paste	Contact resistivity - R_c [mΩ-cm^2]	LPCVD Poly sheet resistance - R_{sh} [Ω/□]
Dupont 17S	7.0	64 Ω/□
Dupont 20A	4.4	

200nm Poly Paste	Contact resistivity - R_c [mΩ-cm^2]	LPCVD Poly sheet resistance - R_{sh} [Ω/□]
Dupont 17S	1.8	37 Ω/□
Dupont 20A	0.6	

Table 5. Contact resistivity of different silver paste (fired at 780C) on LPCVD poly and the poly sheet resistance with 100 nm (left) and 200 nm (right) thick

Key achievements : In task 4, we investigated various metallization schemes to achieve good ohmic contact with reduced shading and reduced metal-Si contact fraction. We attempted a) laser ablation to define grid pattern followed by electroless Ni-Cu plating process as well as b) screen-printing process with advanced pastes and screens with appropriate emulsion and narrow openings. For plated contacts we tested various laser conditions to open the grid lines through the passivation layers and used different electrolytes for plating the openings. We achieved ~30 µm wide uniform plated grid lines with only 10 -15 µm metal-Si contact width. This increased Jsc but showed small degradation in V_{oc}, in spite of reduced metal-Si contact area, due to laser-induced residual damage of the emitter surface. Our second approach involved advanced screen-printing where we investigated various pastes and screens from different suppliers to print narrow grid in combination with floating busbars to reduce the metal/Si contact area and metallized J_0. Consistent with our roadmap for 23% cells, we were able to advance screen printing technology to reduce line width from 55 to <40 µm in combination with floating busbars to reduce the metal-Si contact area below 3%, while maintaining good contact and series resistance ohms/sq.

Results and Discussion in Task 4

4.1 Laser ablation and plating process to reduce line width and shading.

Ni/Cu/Ag plating is an industrially feasible metallization technology for solar cells. In this study the front side passivation/anti-reflection coating (ARC) was locally removed by UV-ps laser ablation. Subsequent to the laser processing a stack of Ni/Cu/Ag was plated onto the ablated areas. Photoluminescence imaging (PLI) was used which allows local characterization of the implied open-circuit voltage (iVoc) and implied fill factor (iFF). PLI was used as quality control of the solar cell precursor and to

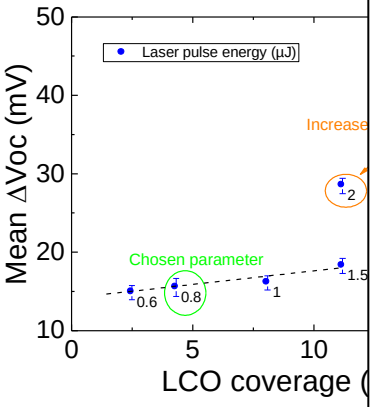


Figure 30. Measured mean Voc drop ar

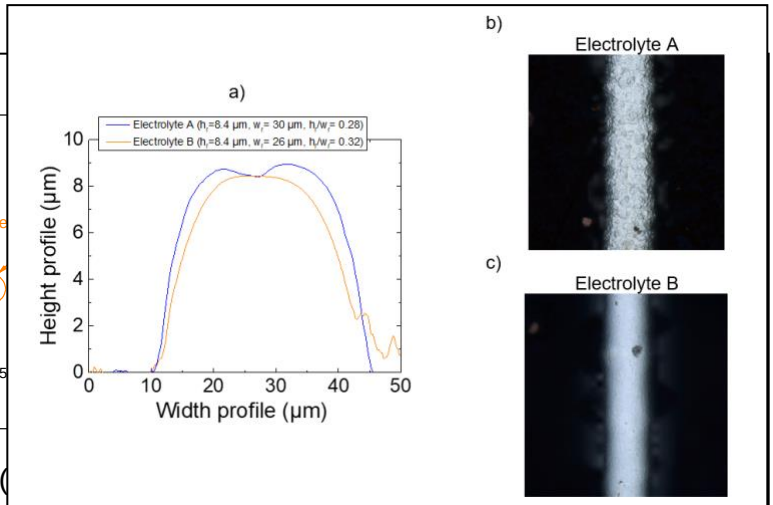


Figure 31. Confocal microscope measurements of the profile (a) and top view images (b,c) of Ni/Cu/Ag plated finger

evaluate iV_{oc} and iFF degradation due to laser ablation. Figure 30 shows the measured V_{oc} and iFF degradation after laser ablation on the emitter as function of laser contact opening (LCO) coverage. Laser condition (0.8µJ) was chosen to open the dielectric layer on the emitter with <10% LCO coverage before plating.

For the plating, the evaluation included two commercial Cu electrolytes A and B. Furthermore, a variation of plating rate within the specifications of the electrolytes was performed. The most significant impact on aspect ratio and optical appearance was the choice of the electrolyte. The variations of plating rate did not show a significant impact on finger geometry and appearance. Figure 31 shows finger cross sections and microscopic top view images of two exemplary fingers for electrolytes A and B. Electrolyte B demonstrates larger aspect ratio of 0.32 compared to electrolyte A (0.28). Overall the optical appearance of the finger is smoother. The smoother finger surface and the steeper finger edges can increase reflections from the finger onto the active solar cell surface which will reduce the effective finger shading width. The laser ablation with optimized Cu electrolyte technology was implemented in n-TOPCon cells, resulting in 0.2-0.3% efficiency enhancement with Jsc increase of 0.4-0.6 mA/cm^2. However, the increase in Voc was slightly limited by the UV laser-induced damage during the opening of dielectric.

4.2 Fine line screen-printing technology

4.2.1 Advanced screen printing with < 40 µm grid lines in combination with floating to reduce shading and metal-induced recombination

In addition to the plating technology, we also investigated various pastes and screens to reduce screen-printed grid width below 40um after firing. Figure 32 shows the microscopic images of fingers printed from different metal pastes and screens. Our

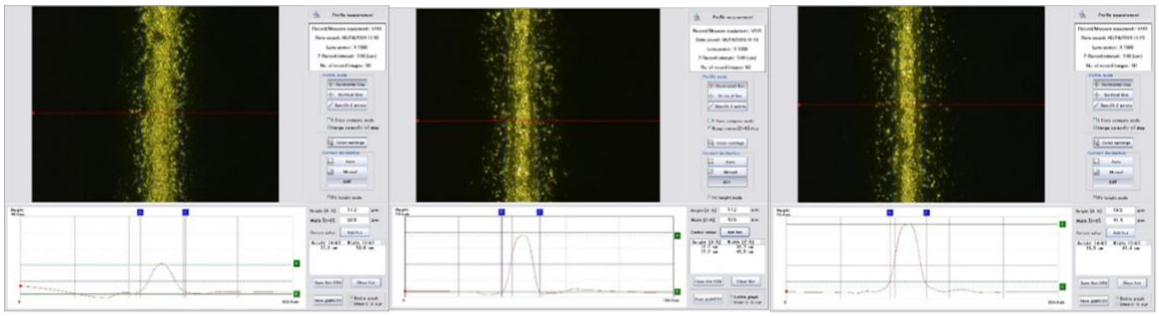


Figure 32. 2D microscope images from baseline D paste and two different H pastes

starting baseline Ag-Al paste (D paste) gave ~50 µm grid width and ~17 µm height after simulated firing. However, using the more advanced screen from Murakami with narrow openings reduced the line width to 45 and then implantation of a paste from Hereaus reduced it further to ~40 µm with 20 µm height. Reduced grid width (50 to 40 µm) improved J_{sc} (~0.4 mA/cm^2) less shading higher V_{oc} due to reduced metal-Si contact area.

In addition to narrow line width, we also investigated floating busbar technology to reduce the metal-Si contact area further. We found that our baseline paste D for grid did not form good contact with the floating busbar paste due to chemical mismatch and reduced FF. Therefore, we tested other pastes and finally found an Heraeus paste for narrow grid contacts which also worked very well for the ohmic contact with floating busbar. However, the new H paste did not fire-through our standard 7-10 nm Al_2O_3 layer on boron emitter, resulting in unacceptably high contact resistance (>10 mΩ-cm^2) and total Rs (>1 Ω-cm^2). Therefore, we had to investigate the use of thinner Al_2O_3 layers for the new H paste to implement floating busbars. Table 6 shows the LIV data for n-PERT cell with thin Al_2O_3 (3~5 nm)/SiN_x stack on front n-PERT cells with total Rs ~0.68, which is still little higher but acceptable.

Table 6. LIV data from n-PERT cell with screen-printed contact using baseline and two new pastes with and without floating BB.

New paste	Al2O3	Device ID	Voc [V]	Isc [A]	Jsc	FF [%]	Eff [%]	n-factor	RSERIES [Ω-cm2]	RSHUNT [Ω-cm2]
Baseline	7 nm	Non Floating	0.663	9.63	40.3	78.3	20.9	1.09	0.77	3710
H1660	3~5 nm	Non Floating	0.665	9.62	40.2	78.1	20.9	1.15	0.68	2050
		Floating	0.673	9.64	40.3	77.6	21.1	1.16	0.81	2380
H1616	3~5 nm	Non Floating	0.668	9.66	40.4	78.0	21.1	1.12	0.77	2425
		Floating	0.670	9.65	40.4	77.8	21.0	1.13	0.82	3665

TASK #5: FABRICATION OF HIGH-EFFICIENCY N-TOPCON CELLS BY PROCESS DEVELOPMENT AND INTEGRATION OF ADVANCED TECHNOLOGIES

Key achievements: Task 5 involved the integration of all the promising advanced technologies developed in the previous tasks into a process sequence to fabricate commercial ready n-TOPCon cells with efficiency ≥22.5 %. In this task we were able to demonstrate a low-cost commercial ready screen-printed n-type bifacial Si solar cells with 22.6% efficiency and 702 mV open-circuit voltage (cell size: 239 cm^2) and 22.9% efficiency n TOPCon cells with optimized B sheet resistance and improved edge isolation (cell size: 100 cm^2). These cells were achieved with homogeneous implanted emitters with metallized J_{0e} of ~30 fA/cm^2 and rear TOPCon metallized $J_{0b'}$ of 5 fA/cm^2 in conjunction with 40 µm wide grid lines, floating busbars and bulk lifetime of ~ 1ms.

5.1 Fabrication of 239 cm^2 screen-printed bifacial n-TOPCon cell with homogeneous B emitter

After developing all the individual technology enhancements, consistent with the technology roadmap, we developed a process sequence in our lab to fabricate commercial size screen-printed n-TOPCon cells. Figure 33 shows the process flow and structure of the large-area (239 cm^2) n-type bifacial cells fabricated with an implanted B emitter on front and LPCVD grown n-TOPCon on rear side of 2 Ω-cm n-type Cz wafers. Since LPCVD grows poly-Si on both sides of the wafer, we had to implement a masking process to etch poly-Si from front side since we did not have the single side etching tool widely used in industry. This added couple of extra steps. After standard saw damage etching, texturing and cleaning, the wafers received B ion implantation on the front side with a dose of 1.2e15/cm^2 at 10 KeV ion energy followed by an annealing and oxidation process at high temperature (~1050 °C), which resulted in sheet resistance of 170-180 Ω/□. After the removal of thermally grown oxide during implant anneal, a PECVD SiN_x was deposited on the front

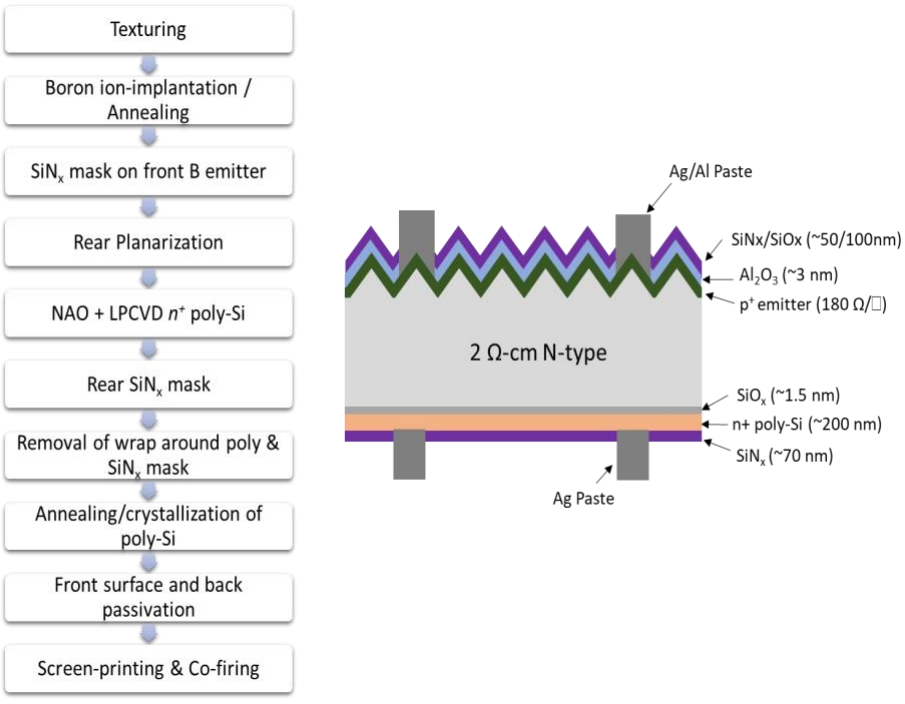


Figure 33 Process sequence and structure of the screen-printed bifacial N-type Si solar cell with front implanted boron emitter and rear tunnel oxide passivated contact

side as a mask to protect the emitter during back planarization and front poly-Si etching. A heated KOH treatment was used to planarize the back. After an acid clean and HF dip, a ~15 Å tunnel oxide layer was grown by nitric acid oxidation (NAO) at 100 °C for ~10 minutes, followed by 200 nm LPCVD n^+ poly-Si deposition at 580 °C with in-situ phosphorus doping. Next, a PECVD SiN_x masking layer was deposited on back poly-Si, and then the front poly-Si was removed by wet etching in KOH solution. After that, both front and back SiN_x masks were removed by HF treatment. The samples were then annealed at 855 °C for poly-Si crystallization and dopant activation. The B emitter was then passivated by atomic layer deposition (ALD) of Al_2O_3 and PECVD SiN_x/SiO_x stack while the back poly-Si was capped with ~700 Å thick PECVD SiN_x layer. For cells with non-floating busbars, 40 µm wide 104 grid lines in combination with 600 µm wide 5 busbars were screen-printed on B emitter using a fire through Ag/Al paste and single print. Front side metallization with floating busbars (FB) was done using dual-print, where the grid fingers were screen-printed first using the fire-through Ag/Al paste first and then a fritless non-fire-through Ag paste was used to print the busbars. Next, 60 µm wide 300 grid lines/600 µm wide 5 busbars were screen-printed on the rear n-TOPCon using fire-through Ag paste and single print. Finally, all samples were co-fired in an industrial-style belt furnace with peak firing temperature of 770 °C. The two SiN_x masking steps employed in our cell fabrication process can be eliminated by the single side etching tool used in industrial setting.

Table 7 shows the cell parameters from light I-V measurements when the cell is illuminated from the front side. Cells were measured using the Fraunhofer ISE certificated reference cell. The cell with fire-through busbars showed ~22% efficiency with V_{oc} of 687 mV, J_{sc} of 40.1 mA/cm^2, and *FF* of 79.7%. However, the cells with floating busbars showed ~15 mV higher V_{oc}, resulting in a V_{oc} of 702 mV and efficiency of ~22.6%. To the best of our knowledge, this is among the highest cell V_{oc} on the large area (≥ 239 cm^2) TOPCon cell with homogeneous B emitter on n-type Cz wafer with industrial screen-printed fire-through metallization on both sides. Note that cells with and without the floating busbars gave similar *FF* (79.7%) even though floating busbar cell gave higher Rs due to reduced metal-Si contact, which was compensated by slightly higher *pFF* (Table 7). Both cells showed high J_{SC} (> 40 mA/cm^2) due to high EQE, reduced reflectance from narrow lines, and SiO_2/SiN_x two-layer AR coating on front.

Table 7 Measured I-V results of screen-printed, large-area n-TOPCon bifacial cells with non-floating and floating busbars

Busbar	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]	n-factor	Rs [Ω-cm^2]	Rsh [Ω-cm^2]	pFF [%]
nFB	687	40.1	79.7	22.0	1.15	0.49	5520	82.0
FB	702	40.3	79.7	22.6	1.12	0.59	12800	82.7

5.2 Fabrication of 100 cm^2 ~23% n-TOPCon cells with homogeneous B emitter

With homogeneous B emitter and full area n-TOPCon on the rear, we achieved 22.6% efficiency. However, we found the n-factor was high (n=1.12) due to the edge leakage current as shown by Electroluminescence and reverse bias measurement below (Fig 34). This could result from our wafer holder or some non-uniformity in deposition systems. Since, this reduces cell efficiency, we decided to fabricate a smaller cell on the fullsize wafer in an attempt to eliminate the edge effects (Fig. 34).

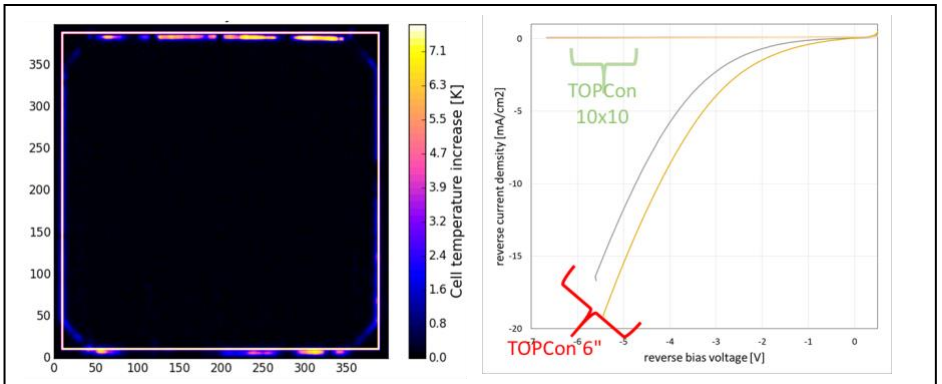


Figure 34. EL image of full area 239 cm^2 under reverse bias (left) and comparison of reverse leakage current of laser isolated 100 cm^2 cell and full area 239 cm^2 cell (right)

In order to validate the above hypothesis, we fabricated 10 cm ×10 cm bifacial n-TOPCon cells with 120 Ω/□ and 170 Ω/□ ion-implanted B emitters on front and carrier-selective n-TOPCon contacts on the back of 2 Ω-cm ~200 µm thick 239 cm^2 n-type Cz wafers. After standard saw damage etching, texturing and cleaning, the wafers received 10 keV B ion-implantation on the front side with a dose of 1.2×10^{15}/cm^2 or 2.0×10^{15}/cm^2 followed by annealing at 1050 ℃ for 1 hour in N_2 ambient and 30 min oxidation, which resulted in sheet resistances of 120 Ω/□ and 170 Ω/□, respectively. Next, 10 cm × 10 cm regions were laser isolated, but not removed from 6-inch pseudo square wafers to form 100 cm^2 cells. The laser damage was removed by a 60 ℃ 10 minutes KOH treatment during which the emitter was protected by the thermal oxide grown during the post-implant anneal. After the removal of thermal oxide, an n-TOPCon structure was fabricated on the rear side by growing a 15 Å thick chemical oxide in HNO_3 solution followed by LPCVD growth of ~80 Ω/□ ~200 nm n^+ poly-Si. The B emitter was then passivated by atomic layer deposition (ALD) of Al_2O_3 and PECVD SiN_x/SiO_2 stack while the back poly-Si was capped with ~700 Å thick PECVD SiN_x layer. Next, 40 µm wide 70

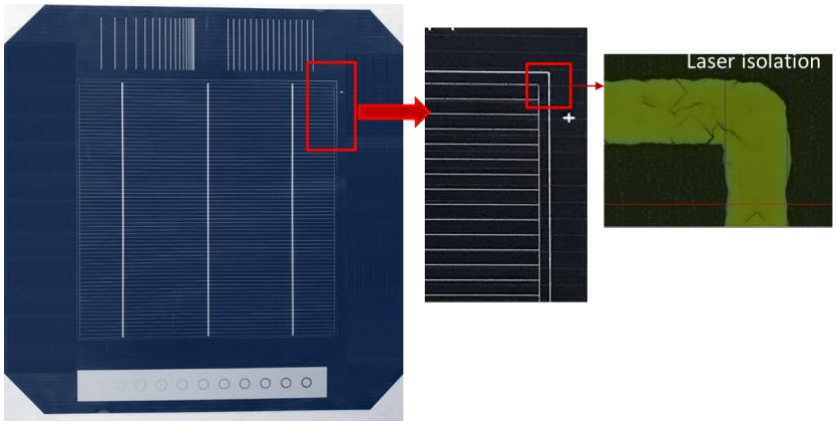


Figure 35. Cell image of 10x10 cm on 6 inch wafer with laser isolated edge

metal gridlines with three busbars (total metal coverage ~ 3.8%) were screen-printed on the emitter and 200 grid lines with three busbars (total metal coverage ~13%) were printed on the rear side (Fig. 35). Samples were then co-fired with peak firing temperature of 770 ℃ and tested under AM 1.5G illumination. Cell images of laser isolated 10x10cm on 6 inch wafer is shown in Fig. 35. Table 8 shows the n-TOPCon solar cells fabricated with 120 and 170 Ω/□ homogeneous Boron emitters. Consistent with the roadmap and model calculations (Table 9, Figure 1), 22.9% efficient fully screen-printed cells were achieved with both 120 and 170 homogeneous emitters.

Table 8 Light I-V measurement results of n-TOPCon solar cells with 170 Ω/□ and 120 Ω/□ implanted B emitters

Boron emitter R_{sheet}	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	Eff [%]	n-factor	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]
170 Ω/□	693	40.9	80.7	22.9	1.04	0.47	7590
120 Ω/□	694	40.9	80.6	22.9	1.09	0.43	13900

Above cells were fabricated with homogeneous emitters, In an attempt to quantify the efficiency gain from selective emitter on these cells, first we characterized and modeled our 22.9% cell and then extended model calculations to predict the efficiency enhancement by replacing the homogeneous emitter with 48/170 Ω/□ implanted p^{++}/p^{+} B selective emitter cell (Table 9). This was done with Sentaurus device model. Fig 34 shows the unit cell configuration for both homogeneous and selective emitters used in this model. Note that Contact resistivity, $J_{0e,pass}$ and $J_{0e,metal}$ values for the implanted heavily-doped 48 Ω/□ emitter (p^{++} region) were taken from task 2 (Fig. 2). All the relevant input parameters used in modeling of the selective emitter cell are highlighted in Table 9, which revealed a gain of ~ 0.2% in efficiency over the homogeneous emitter cell.

Since our selective emitter gave a metallized J_0 of ~25 fA/cm^2 and showed an efficiency gain of ~0.4% on n-PERT cells (Task 2.2) and modeling shows ~0.2% for TOPCon cells, an attempt was made to implement our implanted/APCVD selective emitter with TOPCon back to fabricate full area 239 cm^2 cells to realize the potential efficiency gain. Current full size TOPCon cells with selective emitter show some edge shunting issues with high n-factor (> 1.1). We are in the process of resolving this issue to demonstrate even higher efficiency.

Table 9 Sentaurus Device modeling results and input parameters for the TOPCon cells with homogeneous 170 Ω/□ B emitter and selective B emitter

Parameters	170 Ω/□ homogeneous boron emitter with Paste B	48 / 170 Ω/□ Selective boron emitter with Paste B
Voc [mV]	698	700
Jsc [mA/cm^2]	40.9	40.8
FF [%]	79.9	80.7
Efficiency [%]	22.8	23.0
Cell size (cm^2)	100	100
Front finger width W_f (μm)	40	40

Front shading/metal contact coverage	3.7%	3.7%
Busbar number / width (μm)	3 / 300	3 / 300
Wafer Thickness (μm)	180	180
Front Contact Resistivity (mΩ-cm^2)	5	0.1
Selective emitter sheet resistance (Ω/□)	N/A	48
Selective emitter junction width (μm)	N/A	200
Substrate resistivity (Ω-cm)	2	2
Substrate doping (cm^{-3})	2.38×10^{15}	2.38×10^{15}
Front passivated FSRV (cm/s)	297	297
Wing FSRV (cm/s)	NA	5366
Front contact FSRV (cm/s)	10^7	10^7
Lifetime (ms)	1	1
Back Contact Resistivity (mΩ-cm^2)	2	2
Back contact hole SRV at *n*+ Si/tunnel oxide interface (cm/s)	328	328

Table 10 Comparison of measured and Sentaurus device modeled results of n-TOPCon solar cells.

Boron emitter R_{sheet}		V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	Eff [%]
170 Ω/□	Experiment	693	40.9	80.7	22.9
	Model	698	40.9	79.9	22.8
120 Ω/□	Experiment	694	40.9	80.6	22.9
	Model	695	40.8	80.6	22.9

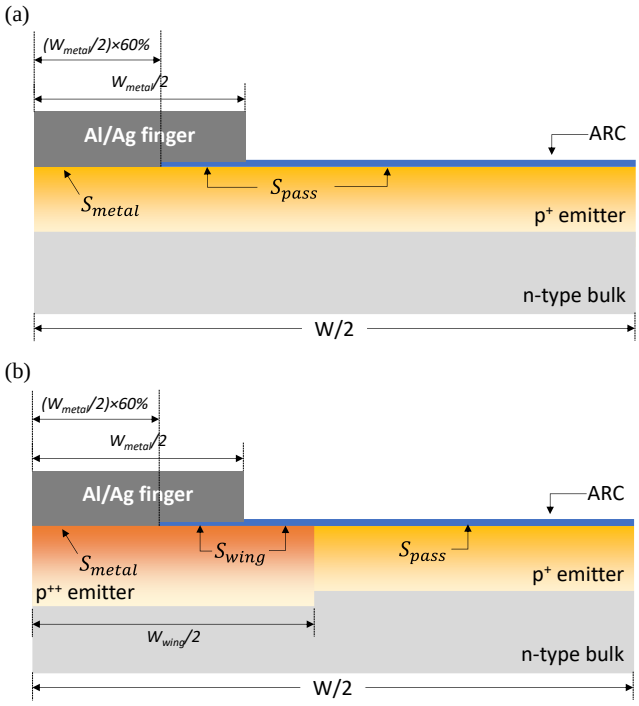


Figure 36. Unit cells in Sentaurus Device modeling for (a) Homogeneous emitter with paste B (b) Selective B emitter with Paste B

5.3 Fabrication of 239 cm^2 ~23% n-TOPCon cells with homogeneous B emitter

Based on our above investigation and finding that our large area (239 cm2) cells suffer from slight edge leakage effect which reduced the efficiency by ~0.3% compared to 100 cm^2 cells fabricated inside large area wafer, we developed and introduced a chemical edge isolation step in an attempt to eliminate the edge leakage. Table 11 shows that finally we succeeded in achieving fully screen-printed 239 cm^2 ~23% efficient bifacial n-TOPCon cells with implanted homogeneous B emitter (~140 Ω/□) on the front and n-TOPCon on the back of a 2 Ω-cm n-type Cz Si.

Table 11. Light I-V measurement results of n-TOPCon solar cells with 135 Ω/□ implanted B emitters

Emitter R_{sheet}	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	Eff [%]	n-factor	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]
135 Ω/□	708	40.3	80.3	22.9	1.04	0.55	71534
	706	40.2	79.8	22.7	1.08	0.52	566219

Conclusions: We demonstrated low-cost commercial size industrial screen-printed n-type bifacial n-TOPCon Si solar cell with 22.6-22.9% efficiency by a combination of device modeling and design, development and integration of several advanced technology

features including low-J_0 implanted B emitters, n-TOPCon on the rear and fine line screen printing with floating busbars.

In Task 1, we performed 2D device modeling to optimize the design of B emitter and n-TOPCon. This task provided guidelines to minimize the number of experiments required to achieve the J_0 targets. We set-up 2D Sentaurus and Quokka 2 modeling capabilities for n-TOPCon cells and validated that by matching our fabricated n-TOPCon cells. This model was then used to establish a technology roadmap to ~23 % n-TOPCon cells with specific guidelines for required J_0 in each layer, bulk lifetime and contact parameters. This roadmap was used to guide the experimental work and the models were used frequently to extract key parameters from the fabricated cells to understand the loss mechanisms. In task 2, we developed advanced homogeneous and selective B emitters to achieve metallized J_{0e} of 25-30 fA/cm^2 using the guidelines from modeling task 1. Consistent with our roadmap, we succeeded in developing a 170 Ω/□ homogeneous implanted B emitter with unmetallized or passivated J_0 ~ 10 fA/cm^2 and metallized J_0 ~30 fA/cm^2 for with 3-5 mΩ-cm^2 contact resistivity. We also developed a process to fabricate selective B emitter using implanted 150 Ω/□ B in the field area and ~ 45 Ω/□ APCVD B diffusion in the contact area. We demonstrated metallized J_{0e} of ~ 25 fA/cm^2 from this selective B emitter. In task 3, we developed carrier-selective tunnel oxide passivated rear n-poly-Si/SiO2 contact with excellent $J_{0b'}$. This was achieved by first growing a 15Å thick tunnel oxide grown in nitric acid at 100°C and then capping it with 100-200 nm LPCVD grown n^+ poly-Si. We were able to maintain excellent rear contact passivation even after the formation of screen-printed contacts. We achieved unmetallized J_0 of 1-2 fA/cm^2 for LPCVD grown n-TOPCon capped with SiN_x after simulated contact firing process. More importantly, we achieved metallized $J_{0b'}$ of ~ 5fA/cm^2 with 9% metal coverage on n-TOPCon which is consistent with the roadmap and is among the best reported value in the literature for screen printed contacts. In task 4, we investigated various metallization schemes to reduce metal shading and contact recombination. We first investigated laser ablated and Ni-Cu plated contacts. We tested various laser power conditions to open the passivation layers to first define the grid pattern and then use appropriate electrolyte to plate the openings. This resulted in 10-15 µm wide metal-Si contact regions and 30 µm wide plated lines after plating in conjunction with very good ohmic contact (< 1 mΩ-cm^2). This approach resulted in ~ 0.4 mA/cm^2 increase in Jsc and ~ 0.2% higher efficiency. However, V_{oc} increase was somewhat limited by the laser induced damage of the emitter during laser ablation of the dielectric., In addition to the plating approach, we also investigated various advanced screens, pastes and firing schemes to obtain narrow screen-printed grid lines in combination with floating busbars to minimize metal-Si contact area and shading. We collaborated with different screen and paste suppliers. Consistent with our technology roadmap, we succeeded in printing < 40 µm wide grid lines and developed printing and cofiring of floating busbars to achieve ~0.2% efficiency increase from this technology development. it was also found that paste chemistry and firing cycle affects the emitter surface etching and percentage of unetched dielectric islands under the metal contacts. This has a significant impact on the $J_{0,metal}$. For example, we found Paste A increased the $J_{0e,metal}$ from ~ 1172 to 1358 fA/cm^2 or by 16% due to 0.13 µm etching of emitter surface while paste B resulted in 40 % reduction in $J_{0e,metal}$ down to 708 fA/cm^2 due to virtually no surface etching and presence of significant fraction (40%) of unetched or undissolved dielectric islands under the grid. This results in the formation of

local contacts. Task 5 involved the integration of all the promising advanced technologies in the previous tasks into a process sequence to fabricate commercial ready n-TOPCon cells with efficiency ≥22.5 %.

Fully screen-printed large area ~22.6% efficient bifacial n-type Si solar cells were fabricated with implanted lightly doped homogeneous B emitter (170 Ω/□) on the front and n-TOPCon on the back of a 2 Ω-cm n-type Cz Si. SiN_x capped LPCVD grown 200 nm n^+ poly-Si on ~15Å tunnel oxide produced unmetallized J_0 value of ~1 fA/cm^2 and metallized J_0 of ~5 fA/cm^2 with 13.5% metal coverage. Advanced B emitter and n-TOPCon each contributed to >0.6 % increase in cell efficiency while fine line printing and floating busbars on the front emitter gave ~14 mV increase in V_{OC} with 0.3-0.5% efficiency enhancement due to reduced front metal/Si contact area on the lightly doped B emitter. Detailed analysis was performed to determine the J_0 component and interface recombination velocity of each region, which indicated metallized J_{0e} = ~31 fA/cm^2 the for the lightly doped B emitter, $J_{0b'}$ = 5 fA/cm^2 for the rear TOPCon and J_{0_bulk} = 22 fA/cm^2 corresponding to a bulk lifetime of ~1.2 ms. Detailed analysis of these cells indicated that the ideality factor n was little higher (1.12 instead of ~1.05) in 22.6% cells due to modest edge leakage effect. Therefore, we fabricated a 10cm x10cm cell within the 239 cm^2 6-inch pseudo square wafer with the help of laser isolation to eliminate edge leakage. This resulted in 22.9% efficient 100 cm^2 cells with n factor of 1.04. Finally, we demonstrated fully screen-printed 239 cm^2 ~23% efficient bifacial n-TOPCon cells with chemical edge isolation process.

We also applied 2D device modeling to understand and explain the loss mechanisms in these cells and developed a new technology roadmap for achieving ~25% efficient TOPCon cells which involves implementation of busbarless contacts, implementation of selective emitter and much higher bulk lifetimes (10-20 ms).

PATH FORWARD: Based on the fabrication and modeling of 22.5%-23% efficient cells, fundamental understanding developed in this study, and available data in the literature, we have developed a new technology roadmap (Figure 37) to ~25% efficient bifacial screen-printed single side n-TOPCon cells. This involves three technology enhancements (contacts, lifetime, and selective emitter) that currently exist in the literature. According to Figure 37, if we implement 30 µm wide screen-printed grid lines [30] in combination with busbarless contacts (a new industry standard used by several research institutes, which ignores shading from external busbars [31-34]), our 22.6% cell efficiency will rise to 23.5%. This is because of reduced shading, metal-Si contact area, and reduced busbar to busbar spacing or resistance. Next technology enhancement requires 15-20 ms bulk lifetime in n-base material, compared to ~1ms in our current cells.

This has been also reported by few investigators in finished cells [35] and materials [36, 37]. This modification will raise the efficiency to 24.6%. Finally by replacing our homogeneous B emitter with a p^+-p^{++} selective emitter with full area $J_{0,metal}$ = 210 fA/cm^2 with contact resistivity ~ 1 mΩ-cm^2,(compared to 706 fA/cm^2 and 3 mΩ-cm^2 in our current homogeneous emitter cell) will raise the cell efficiency to 25.0%. This selective emitter requirement is similar to the selective emitter developed in this project (Task 2). Table 12 shows all the relevant inputs to this model and roadmap.

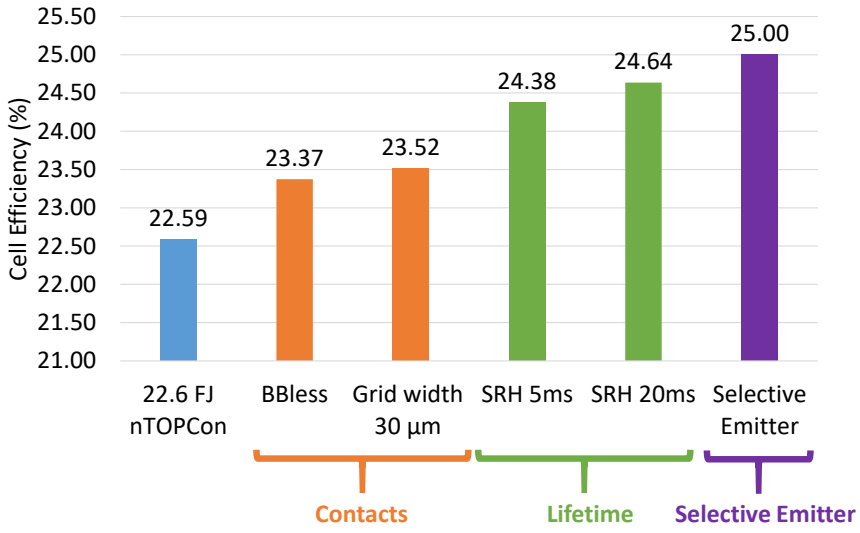


Figure 37. Roadmap to 24.9% efficiency with single-side TOPCon on rear side

Table 12 Quokka 2 modeling results and input parameters for the roadmap from 22.6% to 24.9%

Parameters	22.6% n-TOPCon	Busbar-less	Grid width 30 µm	SRH 5ms	SRH 20 ms	Selective emitter
Voc [mV]	704	705	708	713	715	719
Jsc [mA/cm^2]	40.3	41.2	41.4	41.5	41.5	41.5
FF [%]	79.4	80.4	80.0	82.2	82.9	83.7
Efficiency [%]	22.59	23.37	23.52	24.38	24.64	25.00
Cell size (cm^2)	239	239	239	239	239	239
Front finger width W_f (µm)	40	40	30	30	30	30
Front shading coverage	4.49%	2.56%	1.92%	1.92%	1.92%	1.92%
Front metal contact coverage	2.56%	2.56%	1.92%	1.92%	1.92%	1.92%
Busbar number / width (µm)	5/600	0/0	0/0	0/0	0/0	0/0
Wafer Thickness (µm)	170	170	170	170	170	170
Front Contact Resistivity (mΩ-cm^2)	3	3	3	3	3	0.8
Selective emitter sheet resistance (Ω/□)	NA	NA	NA	NA	NA	30
Selective emitter junction width (µm)	NA	NA	NA	NA	NA	100
Substrate resistivity (Ω-cm)	2	2	2	2	2	2
Front passivated J_0 (fA/cm^2)	12	12	12	12	12	12
Wing J_0 (fA/cm^2)	NA	NA	NA	NA	NA	90

Front contact $J_{0,metal}$ (fA/cm^2)	706	706	706	706	706	210
Bulk SRH Lifetime (ms)	1.2	1.2	1.2	5	20	20
Back Contact Resistivity ($m\Omega$-cm^2)	2	2	2	2	2	2
Rear passivated J_0 (fA/cm^2)	1	1	1	1	1	1
Rear contact $J_{0,metal}$ (fA/cm^2)	30	30	30	30	30	30
Rear contact percentage	13.5%	13.5%	13.5%	13.5%	13.5%	13.5%

Budget and Schedule:

The initial award amount was $1,250,000, of which $125,004 was awardee cost share and the remainder was the federal share. The initial budget period was from 8/1/2016-7/1/2019. Additional funds and time were granted which extended the award until 7/1/2020 and provided an additional $333,334. A final extension was granted at no cost which shifted the end date to 1/31/2021. The end balance of the award is $28,160, all of which is in the federal share. Cost share was fully met by the institute and subcontractor. The remaining balance is due to unspent funds designated for a second subcontractor who was unable to meet their obligation. The majority of funds set aside for this subcontractor were diverted to personnel costs (+ fringe & overhead) for prime award.

Publications Resulting from this Work:

1. Ajeet Rohatgi, Kai Zhu, Jinhui Tong, Dong Hoe Kim, Elsa Reichmanis, Brian Rounsaville, Vivek Prakash, Young-Woo Ok, “26.7% Efficient 4-Terminal Perovskite-Silicon Tandem Solar Cell Composed of a High-Performance Semi-transparent Perovskite Cell and a Doped Poly-Si/SiOx Passivating Contact Silicon Cell”, IEEE Journal of Photovoltaics, vol. 10, no. 2, pp. 417-422, March 2020.

2. Ying-Yuan Huang, Keeya Madani, Wookjin Choi, Ajay D Upadhyaya, Vijaykumar D Upadhyaya, Ajeet Rohatgi, Young-Woo Ok, “Fully Screen-Printed Bifacial Large Area 22.6% N-type Si Soar Cell with Lightly Doped Ion-Implanted Boron Emitter and Tunnel Oxide Passivated Rear Contact”, Solar Energy Materials and Solar Cells, vol. 214, n119585, 2020

3. George C. Wilkes, Ajay D. Upadhyaya, Ajeet Rohatgi, and Mool C. Gupta, “Laser Crystallization and Dopant Activation of a-Si:H Carrier-Selective Layer in TOPCon Si Soar Cells”, IEEE Journal of 10 (5), p1283-1289, 2020

4. Keeya Madani, Ajeet Rohatgi, Kwan Hong Min, Hee-eun Song, Ying-Yuan Huang, Ajay D. Upadhyaya, Vijaykumar Upadhyaya, Brian Rounsaville, and Young-Woo Ok. "Comparison of passivation properties of plasma-assisted ALD and APCVD deposited Al2O3 with SiNx capping." Solar Energy Materials and Solar Cells 218 (2020): 110718

5. Woojun Yoon, David Scheiman, Young-Woo Ok, Zhaoning Song, Glenn Jernigan, Ajeet Rohatgi, Yanfa Yan and Phillip Jenkins, “Sputtered Indium Tin Oxide as a Recombination Layer Formed on the Tunnel Oxide/Poly-Si Passivating Contact enabling Efficient Monolithic Perovskite/Si Tandem Solar Cells”, Solar Energy Materials and Solar Cells, vol. 210, n110482, 2020,

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8. Ajay D Upadhyaya, Keeya Madani, Vijaykumar Upadhyaya, Brian Rounsaville, and Ajeet Rohatgi, “Boron Selective Emitter formation with un-metallized Joe of 13 fA/cm^2 for Silicon Solar Cells Application”, 47th IEEE PVSC 2020

9. Ying-Yuan Huang, Young-Woo Ok, Ajay D Upadhyaya, Vijaykumar D Upadhyaya, Keeya Madani, Ajeet Rohatgi, “Large Area 21.6% Efficiency Front Junction N-type Cell with Screen Printed Tunnel Oxide Passivated Poly-Si Rear Contact”, 46th IEEE PVSC , 2019

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Patent

Ajay Upadhyaya, Ajeet Rohatgi et. al "Selective Boron Emitter Formation for Commercial Solar Cells" U.S. Patent Application No. 62/725,284, Filed: August 31, 2018, GTRC Reference No.: 7991, Our Reference No.: GTRC7991PRV

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Appendix (published key papers-#3)

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