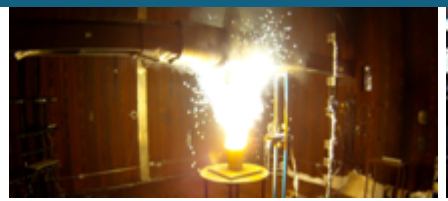
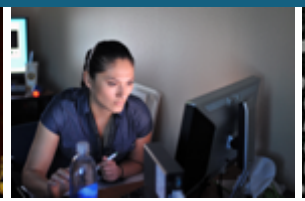
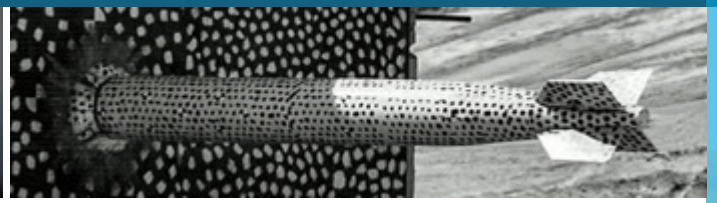
SAND2020-13172C

Sandia National Laboratories

Room Temperature Operation of Donor-Based Atomically Precise Devices







Jeffrey A. Ivie*, Lisa A. Tracy, Juan P. Mendez, Suzy Gao, Evan M. Anderson, Scott W. Schmucker, DeAnna M. Campbell, David Scrymgeour, Aaron M. Katzenmeyer, Dan R. Ward, Tzu-Ming Lu, Shashank Misra

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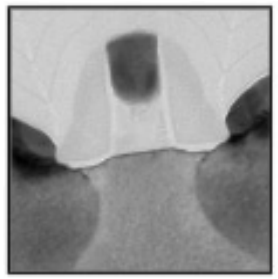
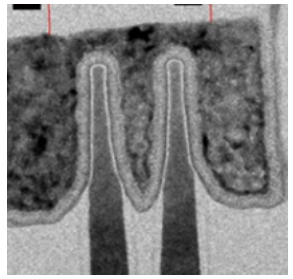
Issues with Modern CMOS Process Development



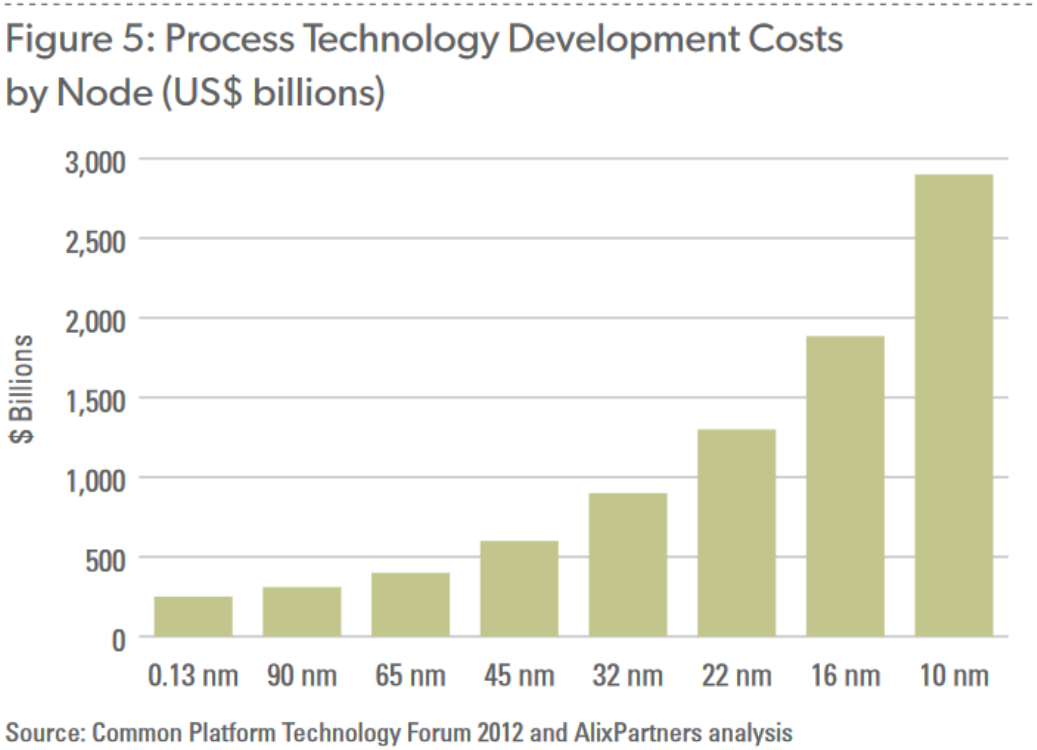
65 nm



10 nm

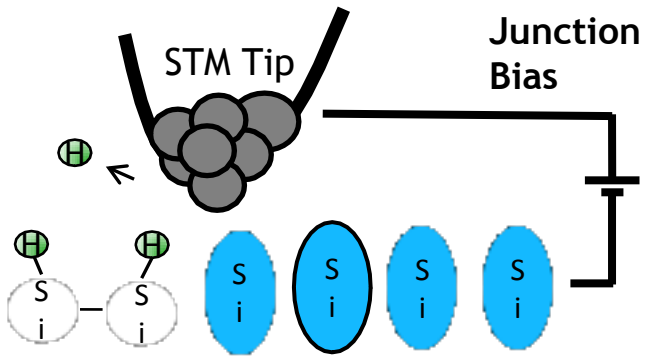
?

3-5 nm

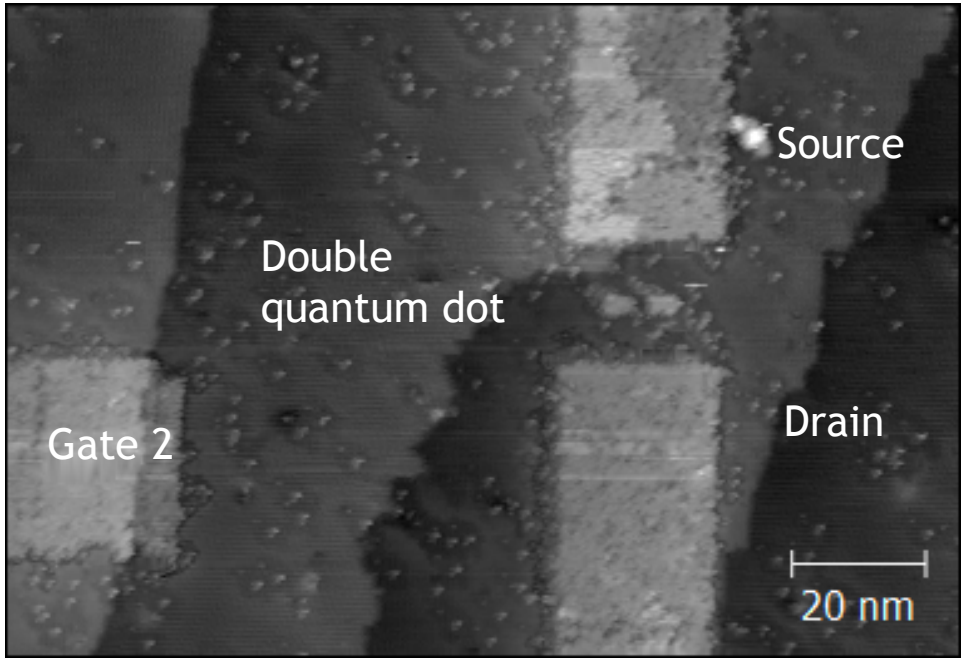


Need for New Pathfinding Science!

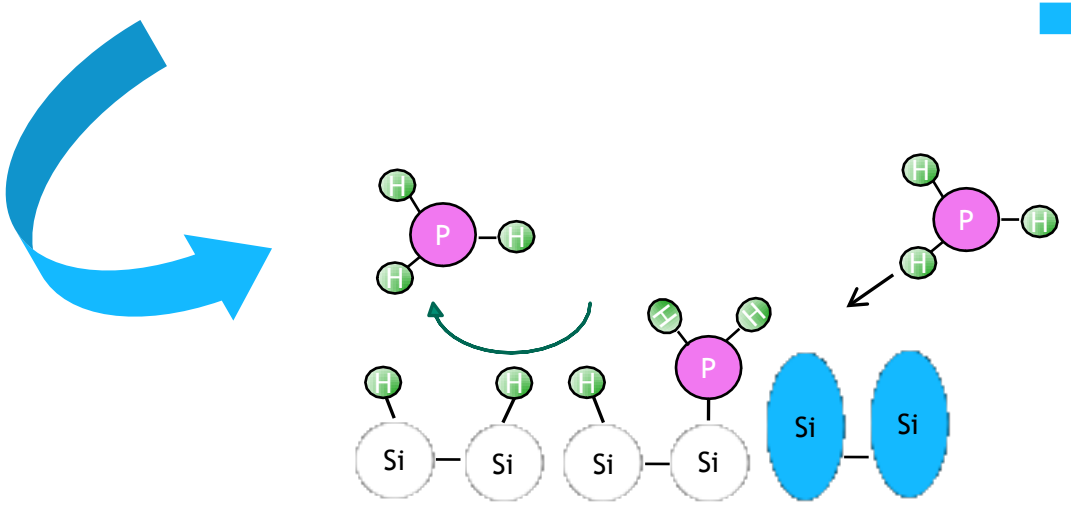
Atomic Precision Advanced Manufacturing (APAM): Ultra High Doping



- Atomic precision achieved through hydrogen desorption with scanning tunneling microscope (STM)



STM



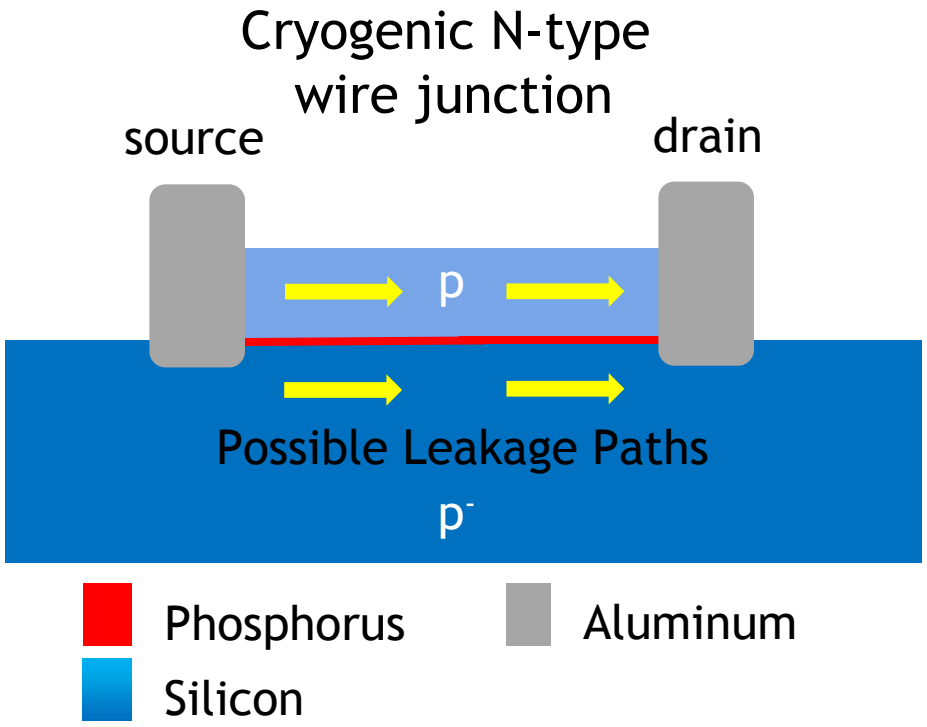
- Expose to PH_3 precursor, which **only** bind to exposed reactive sites
- Generate dopant concentrations **above solubility limit** (~$1x10^{20}$ atoms/cm^3)

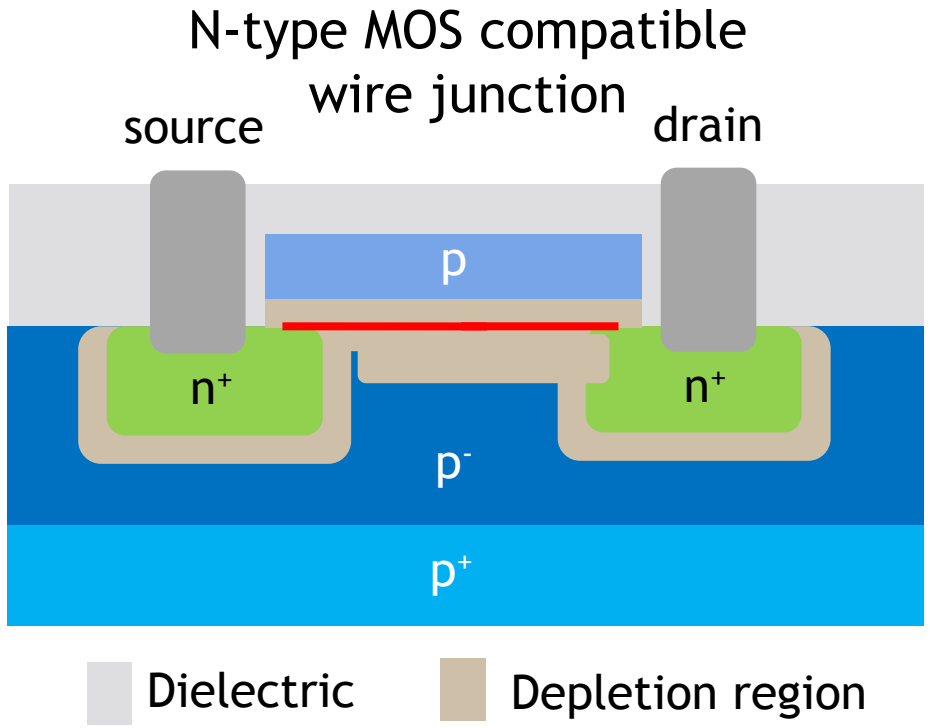
Result: Atomic Precision Quantum Devices

Ward, *et. al. Elec. Dev. Fail. Anal.*, **22**, 1, 4-

APAM + MOS: Need Room Temperature Operation

- **Problem:** Quantum devices **only** operate at 4K or lower.
  - Leakage currents become major issue at higher T
- **Solution!** Adapt MOS-like doping schemes

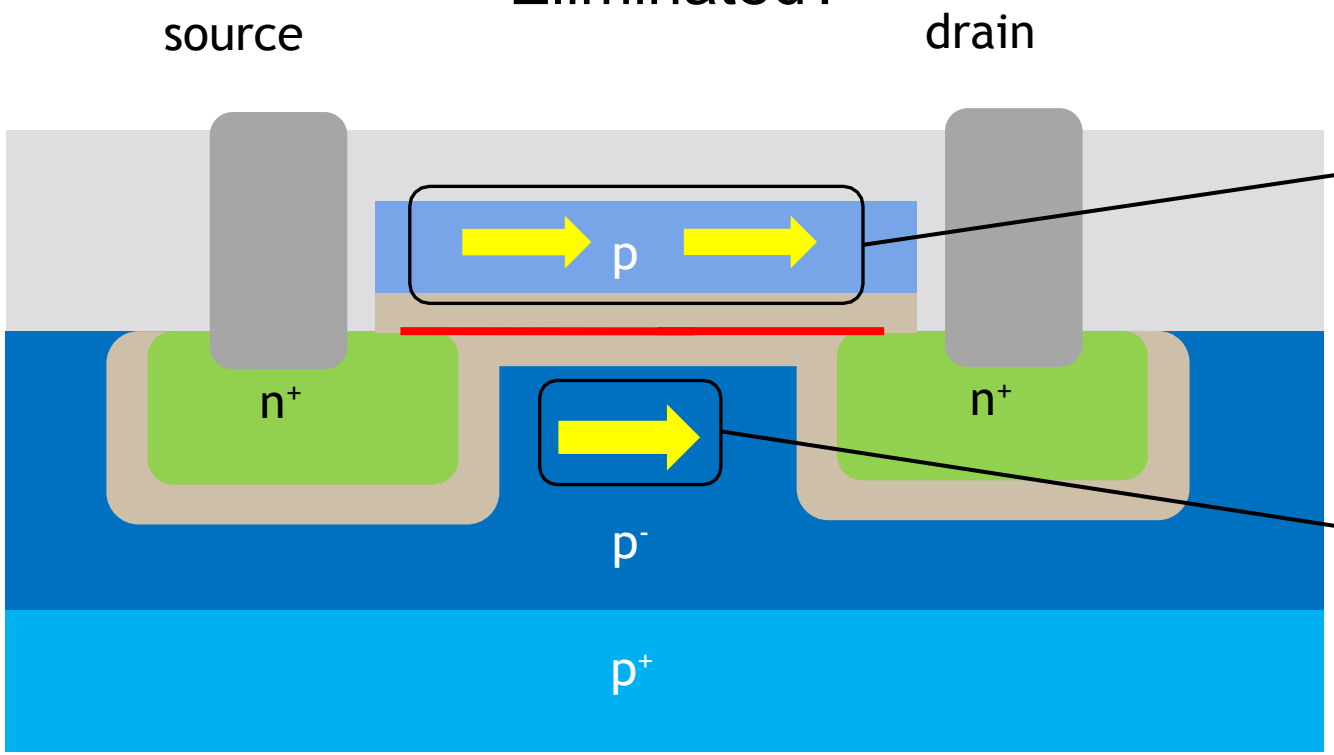




Can Room Temperature (RT) Operation Be

RT APAM: Addressing Leakage

Question: Have Leakage Pathways Been Eliminated?

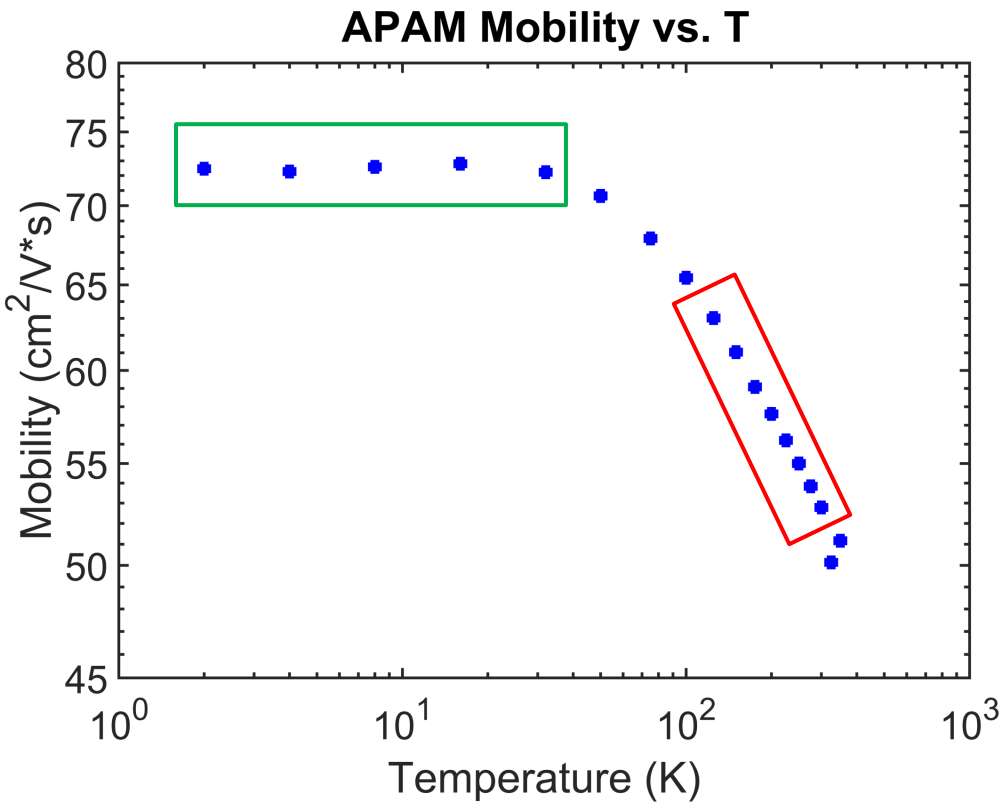


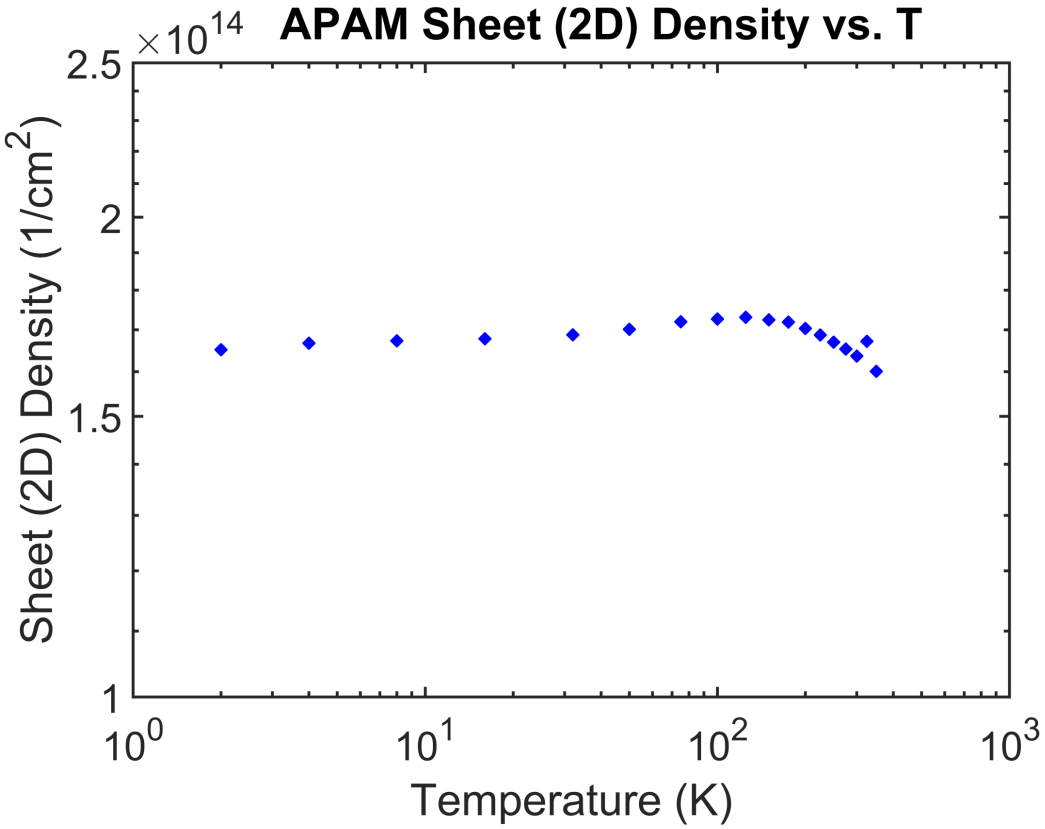
- Leakage comparable to P δ-layer
- Consequence of diffused δ-layer during Si growth

- Well isolated relative to P δ-layer (9 kΩ for P δ-layer, 6 MΩ to p^+ handle)

Answer: Outside of Diffused P δ-layer, Yes!

RT APAM: Temperature Dependent Electrical Properties



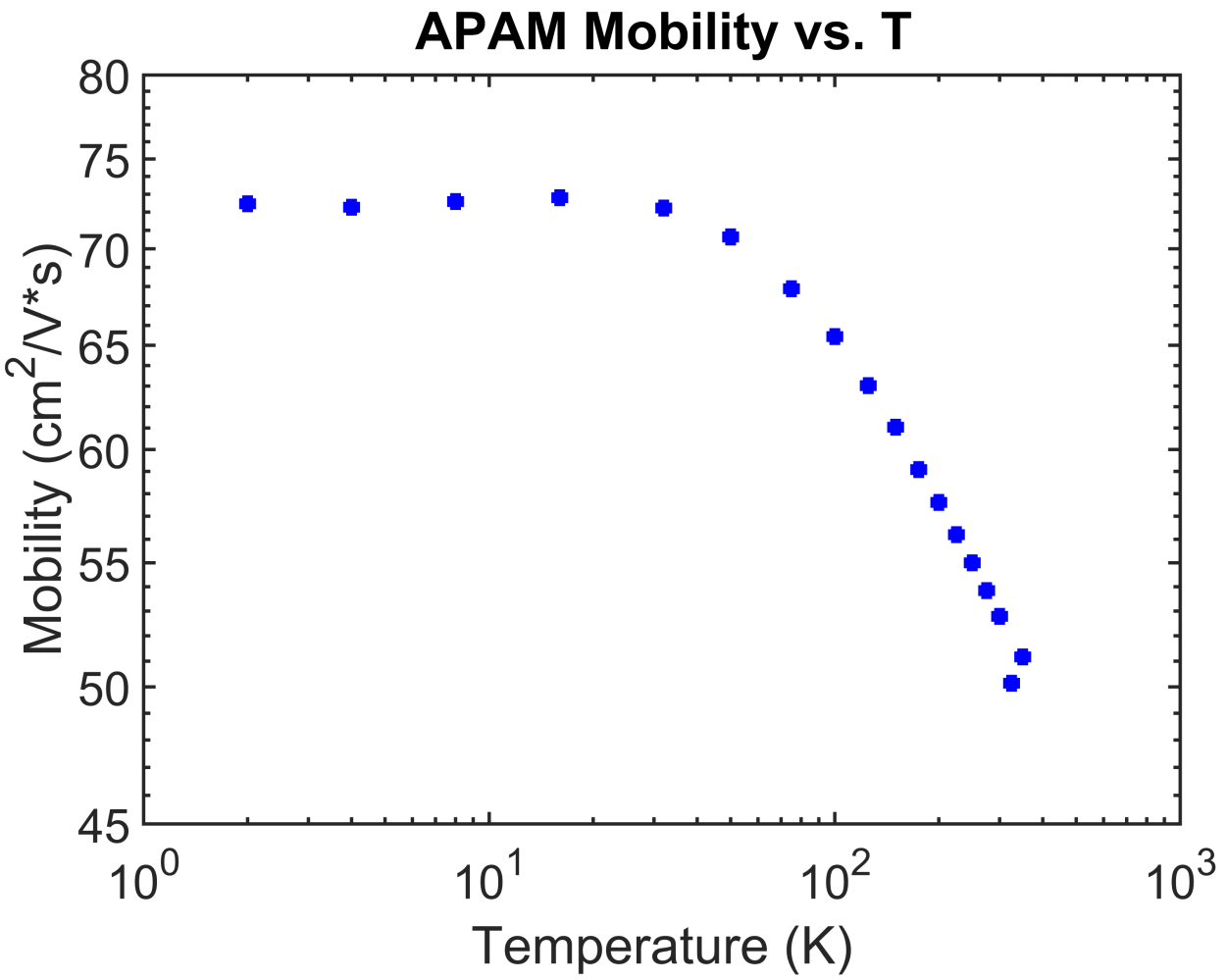


- Temperature dependent mobility (μ(T)) exhibits regions found in other 2D systems
- Sheet (2D) Density independent of temperature as expected

P δ-layer Behaves as Expected Across Different Temperatures

Ando, *et. al. Rev. Mod. Phys*, **54**, 2, 437-672

Prospectus



Use of MOS capability counter-doping scheme enables RT operation of P δ-layer

Leakage pathways mostly eliminated, with reduction of Si growth temperature eliminating P δ-layer diffusion and remaining leakage pathway

Variable temperature electrical properties were assessed to be as expected for a 2D system.

Next step includes the integration of low thermal budget Al_2O_3 gate stack for transistor development

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