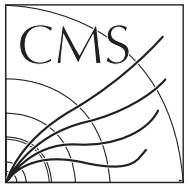
Available on CMS information server

CMS CR -2016/453



The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

14 December 2016

Development of Flexible, Scalable, Low Cost Readout for Beam Tests of High Granularity Calorimeter for the CMS Endcap

Paul Michael Rubinov for the CMS Collaboration

Abstract

As part of the development of the High Granularity Calorimeter for the CMS Endcap at HL-LHC, The CMS collaboration is conducting a comprehensive series of beam tests. The first beam test, with a single HGC module was carried out in March of 2016 at the Fermilab Test Beam Facility, continuing to a 16 module test in July of 2016. We describe here the development of a low cost readout system that is simple to implement and is able to grow with the system under test. The system is based on the low cost Zynq SoC that allows simple DAQ development in a Linux environment. For this application we used the Digilent ZedBoard, which allows high speed LVDS links and Linux software development on a single commercial board. A small custom FPGA board designed to comply with the VITA 57 Field Programmable Mezzanine Card standard implements the interface to the readout ASIC mounted on the HGC sensor modules and provides the LVDS links to the ZedBoard, either directly over the FMC connector or via a custom carrier card. This architecture provides scalability, ease of development and low cost.

Presented at *IEEE-NSS-MIC-2016 IEEE Nuclear Science Symposium and Medical Imaging Conference*

Development of Flexible, Scalable, Low Cost Readout for Beam Tests of the High Granularity Calorimeter for the CMS Endcap

P. Rubinov[1] on behalf of the CMS collaboration

***Abstract*—As part of the development of the High Granularity Calorimeter for the CMS Endcap at HL-LHC, The CMS collaboration is conducting a comprehensive series of beam tests. The first beam test, with a single HGC module was carried out in March of 2016 at the Fermilab Test Beam Facility, continuing to a 16 module test in July of 2016. We describe here the development of a low cost readout system that is simple to implement and is able to grow with the system under test. The system is based on the low cost Zynq SoC that allows simple DAQ development in a Linux environment. For this application we used the Digilent ZedBoard, which allows high speed LVDS links and Linux software development on a single commercial board. A small custom FPGA board designed to comply with the VITA 57 Field Programmable Mezzanine Card standard implements the interface to the readout ASIC mounted on the HGC sensor modules and provides the LVDS links to the ZedBoard, either directly over the FMC connector or via a custom carrier card. This architecture provides scalability, ease of development and low cost.**

***Index Terms*—Data acquisition, beam test, CMS, High-Granularity Calorimeter.**

I. Introduction

The upgrade of the CMS Endcap Calorimeters for operation at the HL-LHC is required due the expected levels of radiation (up to a fluence of 1E16 n/cm^2 and an integrated dose of 150 Mrads at a pseudo-rapidity of around 3) and the high number of interactions occurring within the same bunch crossing, or 'pileup', which could be as high as 200. The CMS collaboration has chosen to replace the currently-installed endcap calorimeters with a new, high-granularity calorimeter (HGCAL). The main active media of this calorimeter is large-area silicon sensors. This has become feasible due to improvements in our understanding of the radiation properties of silicon, a significant reduction in the cost of silicon sensors and the availability of low-power radiation-resistant electronics[1]. The design adopted by CMS is similar to calorimeters under development by the CALICE collaboration for use at linear colliders[2], but modified significantly to account for the operational differences at the HL-LHC. A more detailed discussion of the HGCAL can be found in Ref. [3].

In order to address issues inherent in this new technology, the HGCAL group undertook an aggressive campaign of building and operating a small portion of the proposed HGCAL in test beams at Fermilab and CERN. This paper describes the architecture and operation of the data acquisition used in the 2016 campaign.

As the 2016 campaign was the first test of many aspects of the HGCAL - sensors, module construction, readout - the system being described was designed to accommodate small test stands with a single sensor but is able to scale up to 28 sensors.

II. Hardware description

A. Sensor module

The novel hexagonal sensors used in the 2016 test beam originated from six-inch (150mm) wafers from Hamamatsu, with 128 channels per sensor, each channel approximately 1cm^2 in area. A majority of the cells were hexagonal, with some half-hexagons and other shapes at the sensor edges. Whilst the physical thickness of the sensors was 300 microns, the effective depletion depth for these sensors was approximately 200 microns. A schematic view of the sensor is shown in Figure 1. The sensors are assembled into "bare modules", with a 25%:75% copper-tungsten plate as a base, metalized Kapton film to provide back-side bias, then the silicon sensor and a PCB on top. There are holes in the module PCB to make connections to the sensor with wire bonds. The PCB routes the signals from the silicon to two small connectors, which allow the signals to be read out by front-end ASICs. A photo of a bare module appears in Figure 2.

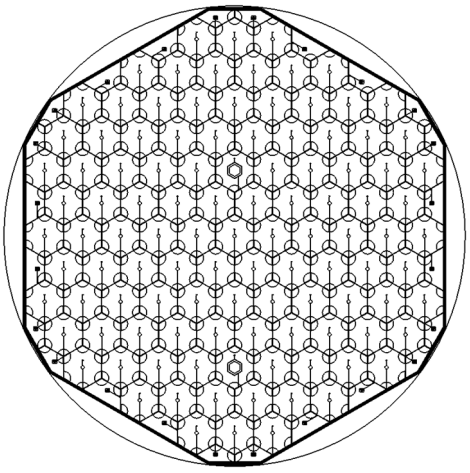


Figure 1. Diagram view of a hexagonal sensor used in the 2016 HGCAL beam tests. The sensor is divided (mostly) into hexagonal cells with an area of about 1cm^2

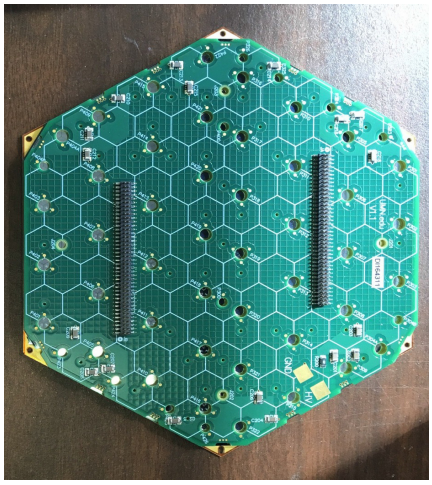


Figure 2. A photo of the assembled sensor module showing the PCB with connectors and holes for wire bonds. The Kapton layer is visible at the corners, where there are also holes through the module to enable it to be attached to a support (cooling) plate.

B. *Readout board and ASIC*

The system used in the 2016 test beam is based on the SKIROC2 ASIC, designed by the Omega group [4]. This is a complex, high performance ASIC, and our system uses only some of the available functionality. Each SKIROC has 64 channels, with each channel having a preamplifier and two separate slow shapers. The SKIROC2 has many functions such as a fast shaper, self-trigger, fifteen cell pipeline and so on, that were not used in our system. Only the slow shapers are used in our system as we utilized an external trigger (the fast shaper is used for self-trigger). The two shapers have a fixed gain ratio of 10:1, providing low and high gain amplification and hence a large dynamic range with, at the same time, good accuracy for small signals from single particles. For every trigger received, both high and low gain signals were read out for every channel. A very simplified schematic of the SKIROC2 is shown in Figure 3. The SKIROC2 also has very powerful multiplexing capabilities for internal signals - both analog and digital.

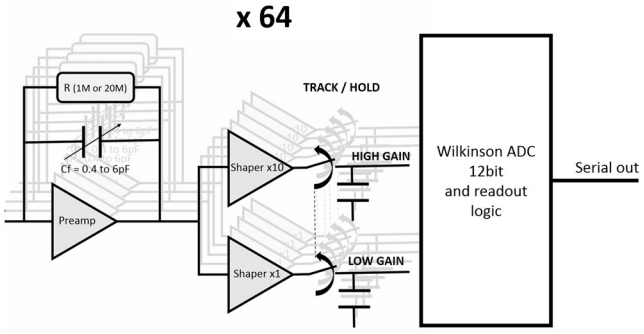


Figure 3. A simplified schematic of the SKIROC2 showing only the sections used in the TB2016 DAQ.

The SKIROC2 ASIC is mounted on a "Readout Board" designed by E. Frahm at the University of Minnesota. The board layout is such that it can accommodate both bare die and quad flat pack (QFP) packaged chips. This is clearly visible in the photograph shown in Figure 4. The connection to the rest of the system is made through the use of Hirose FH26-39S-0.3SHW connectors and Molex FFC, part number 0150150239; both easily available from electronic component distributors. These cables supply power, control signals and carry the digital data during readout.

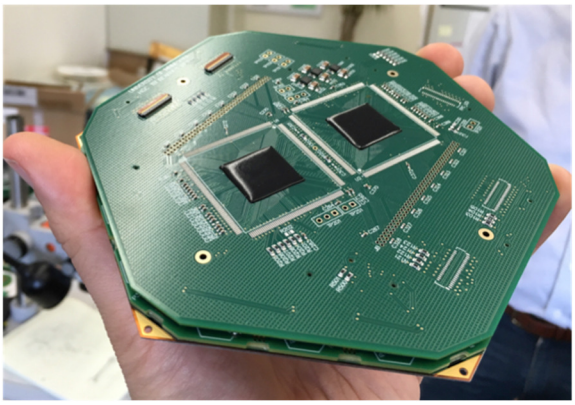


Figure 4. Photo of the complete HGCAL module, with the readout board with two SKIROC2 bare die chips wire-bonded (under protective black potting material).

C. *Mechanics*

The signals from the SKIROC2s (digital data, since the ADC is incorporated into the ASIC itself) are carried by the flex cable to another PCB, a passive adapter called the "elbow board". There is another short flex cable of the same type that carries the signals to FPGA cards sitting in a passive 6U crate.

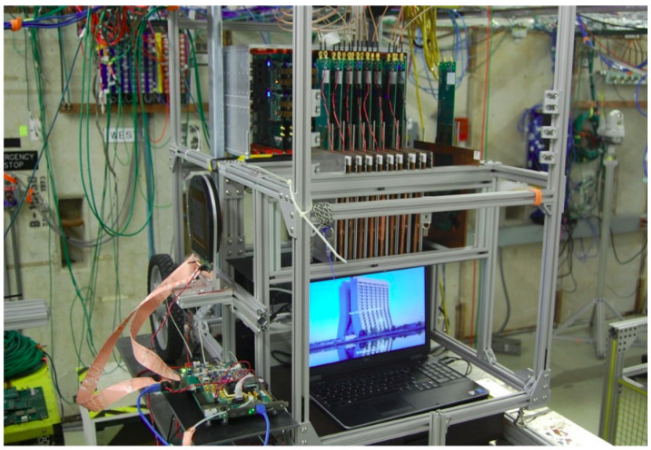


Figure 5. A photo of the test beam setup at Fermilab in July of 2016. There are 16 modules in a hanging folder arrangement.

D. *Readout electronics*

Most modern DAQ systems will have a number of common elements - the front end ASIC is connected to an FPGA, which collects and buffers the data and is, in turn, connected to a Linux workstation. Our system follows this model. The key aspects of flexibility, scalability and affordability depend on the details of how these elements are arranged. One of the key requirements of the HGCAL test beam DAQ was that it will be able to grow as modules were built and added to the system, while also being able to accommodate small, single module test stands. This goal was met by placing the control FPGA on a small FMC (VITA

57) [5] compliant mezzanine module. This card is called the "FMC_IO" and is pictured in Figure 6. The FPGA we chose was the Xilinx XC7A100T "Artix" device. This FMC board is mated to an FMC carrier card (CC). In the case of a single module, the carrier is the commercially-available "Zedboard" (see "zedboard.org" website for details).

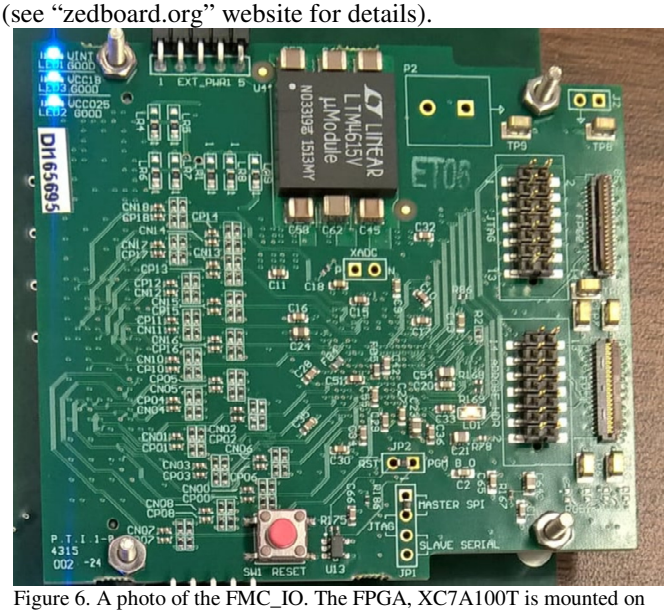


Figure 6. A photo of the FMC_IO. The FPGA, XC7A100T is mounted on the back side and is not visible in this photo.

The Zedboard is equipped with the Xilinx XC7Z020 "Zynq" device. This is an SOC (System On Chip) that combines a dual core Arm processor and an "Artix" type FPGA in the same device. The Zedboard is a fully fledged embedded Linux system, with 500Mbytes of RAM, gigabit Ethernet and other peripherals. The details of how this system works are described in the next section. In this section we note that for the test beam application, we designed two additional cards. A simple FMC module, called the ZedIO which was used to break out the signals from the Zedboard FMC connector, and route them to 14 full-size HDMI connectors. These HDMI connectors carry serialized data and clock to another card, a 6U carrier for the FMC_IO, called the DDC. The DDC in turn routes the signals to the FMC_IO. The important point is that the DDC and ZedIO are relatively simple cards with only buffers and connectors - no FPGAs. This allows flexibility, since one Zedboard can control many FMC_IO, rather than just one, thus reducing the cost and complexity of the system. A photo of the complete system is shown in Figure 7. The FMC_IO are connected via two flex cables to an elbow board, which is in turn connected to the SKIROC2 on the hexagonal module. The use of LVDS links running over the HDMI cables gives the system great flexibility as one Zedboard is able to connect to up to fourteen DDC cards, each of which carries two FMC_IO. Each FMC_IO in turn connects to two SKIROC2 chips. In total then, a single Zedboard is able to read 14 x 2 x 2 = 56 SKIROC2, or 14 x 2 x 2 x 64 = 3564 channels. In fact, the FMC_IOs are able to read up to four SKIROC2 chips each, and the Zedboards have features that allow up to five of them to be synchronized into a single DAQ system, with a common clock and trigger. Thus, the theoretical maximum for the system is 560 SKIROC2 chips, or approximately 36k channels. However, the maximum number we actually operated in the test beam was one Zedboard, eight DDC, and sixteen FMC_IO, for a total of 1024 channels. A block diagram of the connections is shown in Figure 8.

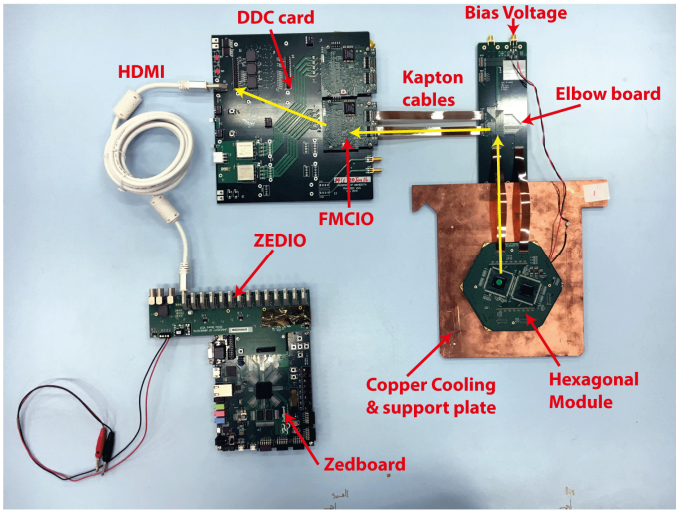


Figure 7. A photo of the system with two modules being exercised on a bench. The yellow arrows represent the data path from the module.

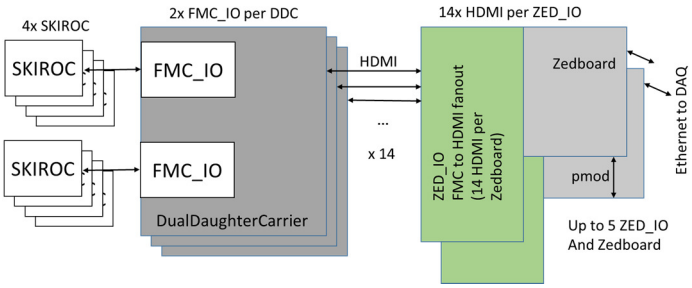


Figure 8. A block diagram showing the system connectivity.

III. Firmware Description

The functioning of a modern system cannot be understood without some analysis of the firmware and software. Our test beam DAQ system is driven primarily by the software running as a Linux executable on the Zedboard. This software communicates with the external world via ethernet. A series of simple commands is used to control the software. These commands can be issued by other software, running on another computer, or they can actually be entered by an operator directly via telnet. The basic sequence of operations is as follows:

1. The software is made aware of the hardware configuration - how many and which particular HDMI connectors are in use. This step also establishes the LVDS link and checks it - it is checked by reading the firmware version register from the FMC_IO.
2. The source of the trigger is defined. This can be an external trigger, or it can be software generated, with optional delay.
3. The "run" is defined – name and length are set.
4. The software is instructed to start the DAQ run.

At this point, the system is able to acquire data. Once a trigger is received on the Zedboard (normally from scintillators upstream of our test system), a timestamp is recorded and the

trigger is broadcast to all the FMC_IOs and further triggers are vetoed. Each FMC_IO, upon receipt of the trigger, cycles the readout of the finite state machine that controls the readout of the SKIROC2 through the appropriate states and stores the data that are returned by the SKIROC2 in local memory on the FMC_IO FPGA. It also appends the timestamp and trigger number to the data record. The processor checks if all the FMC_IOs have completed storing the data corresponding to the given trigger to local memory. Once a positive response is received from the FMC_IO, the trigger veto is removed and the system is able to acquire the next event. This continues for a predetermined number of triggers (typically about a hundred, but with a maximum of 500 – which is the maximum that can be stored in the FMC_IO). This is referred to as a "spill", and corresponds to the presence of the beam. At Fermilab, the spill lasts for 4 seconds, and is repeated every 60 seconds. At CERN, the beam lasts for about 5 seconds and repeats every 30 seconds, typically. After the spill, the software on the Zedboard iterates through the FMC_IO cards that have been configured to participate in the run, and copies all data corresponding to the spill from the memory of each in turn. The reason this is done is to allow all FMC_IO to acquire data in parallel during the spill, for the fastest possible trigger rate. The data transfer from each FMC_IO to the Zedboard then proceeds one FMC_IO at a time, but between spills, when there is no beam and thus no incoming data.

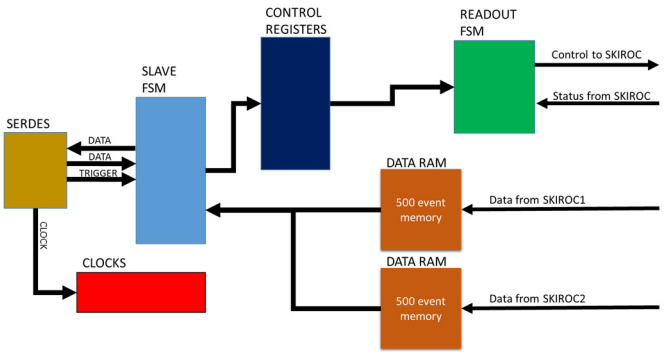


Figure 9. The block diagram of the FMC_IO firmware.

A. *FMC_IO Firmware*

We now discuss the FMC_IO firmware in a little more detail. The HDMI link carries four LVDS pairs for each FMC_IO. Three of the links are broadcast links, directed from the ZedIO to all the FMC_IOs in the system. These are:

A) Trigger
B) Clock
C) Data broadcast from the Zedboard to the FMC_IO

There is one data link from the FMC_IO back to the Zedboard. An important point is that since there is only one HDMI link per DDC, but there are two FMC_IO on each DDC, the HDMI cable carries five signals - the three broadcasts as described above and the two individual return links from each of the FMC_IO cards.

The HDMI data link between the Zedboard and the FMC_IO is Manchester-encoded and nibble oriented. It uses a 2.5V LVDS signaling standard and runs at 320 Mbps. The choice of using Manchester encoding was made to improve the robustness and simplicity of the protocol at the cost of efficiency. Another simplification was the decision to follow a strict Master-Slave model of communications. All communications originate on the Zedboard, and all messages sent require a response from the FMC_IO.

B. *The Zedboard Firmware and Software*

The firmware on the Zedboard interacts with FMC_IO firmware on the one hand and with the software also running on the Zedboard on the other, to operate the DAQ system. The interaction with the software is through three simple memory-mapped interfaces: two dual port RAM (DPRAM) for sending and receiving messages, and a small set of registers to control the sending and receiving of messages. These registers are used for housekeeping functions such as clearing the "send" or "receive" DPRAM blocks, indicating that the software has completed writing the sent message, indicating the status of the data link the arrival of a received message and other similar functions.

The requirement that a single Zedboard be able to communicate with up to 28 FMC_IO is also handled in a very simple way. There is only one transmission channel, routed to all FMC_IO boards via simple buffer-repeaters on the ZedIO board. All messages contain the address of the FMC_IO for which they are intended in the header of the message. The FMC_IO are assigned an address via DIP switches on the DDC. It is up to the operator of the system to make sure that all FMC_IOs have unique addresses. To facilitate this process, the DIP switches on the DDC are accessible on the front panel.

The handling of the reply messages on the Zedboard is also very simple. There is a unique deserializer for each of the 28 links. However, they all route to a single multiplexer, controlled by a register, which routes only one link to the receiver portion of the master communications state machine. In other words, the Zedboard communicates with exactly one FMC_IO at a time, by using an unique address in the header of the outgoing message and by receiving the data from exactly one link. The block diagram for the Zedboard is shown in Figure 10 below.

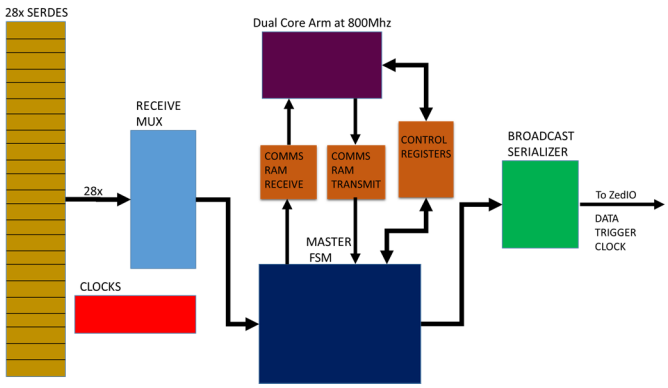


Figure 10. The block diagram of the Zedboard firmware.

OPERATIONAL EXPERIENCE

In the period from March to September of 2016, we operated a number of test beams at both Fermilab and CERN. At Fermilab, we first took beam with a single module in March of 2016, extending the system to four modules in May, and sixteen modules in July. CERN tested a similar system, but with different arrangements of absorbers, and much higher energy range and better purity electron beams in August and September of 2016. A preliminary analysis of the results was presented at the 38th International Conference on High Energy Physics[8] and a more comprehensive analysis is in preparation. From the point of view of the DAQ, the system operated successfully and achieved its goals. A number of features of the system are worth noting. One issue we encountered was the difficulty of reliably connecting the 0.3mm-pitch flex cables given the tight space available for connection and inspection. However, once a reliable connection was established, the system was found to be stable over the several weeks period. Other hardware performed reliably, with an exception of one board where a power supply failed during operation. Other apparent failures were observed, at a very low rate of less than one per week, but none could not be recovered by reprogramming the FPGAs or the SKIROC2 chips. Another observation was the presence of common-mode noise. This was corrected in the analysis of the data, but if it had not been possible to do that, the signal-to-noise would have been degraded by a factor of two and the excellent intrinsic noise performance of the SKIROC2 would have been compromised. The source of the noise was traced to excessive noise on the power supply provided to the SKIROC2. We expect to modify this feature in the next evolution of the system. In Figure 10 and 11, we reproduce some selected highlights of the test beam program. An excellent separation between pedestal and minimum ionizing particles was observed in all channels and all sensors. Figure 10 shows the MIP peak for a particular channel (corresponding to a most-probable-value of around 16 ADC counts above pedestal on a noise (RMS) of 2.3 counts) as well as the mean value for all sixteen layers. Layers 5 and 9 have slightly lower values for the gain due to lower bias (below full depletion) caused by problems not relevant to this paper. Figure 11 is a display of some interesting events from test beams at both Fermilab and CERN.

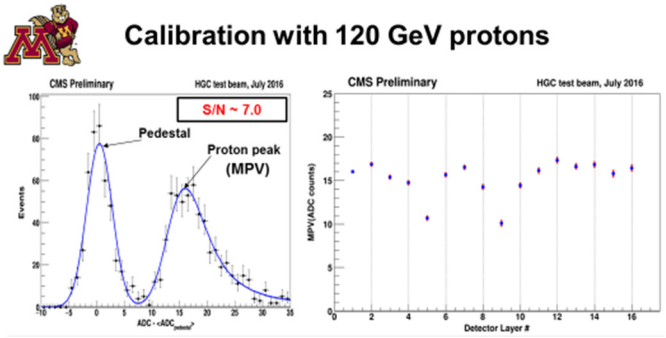


Figure 2. Left: typical channel, showing excellent separation of MIP peak and pedestal. Right: the average position of the MIP peak above pedestal for all layers.

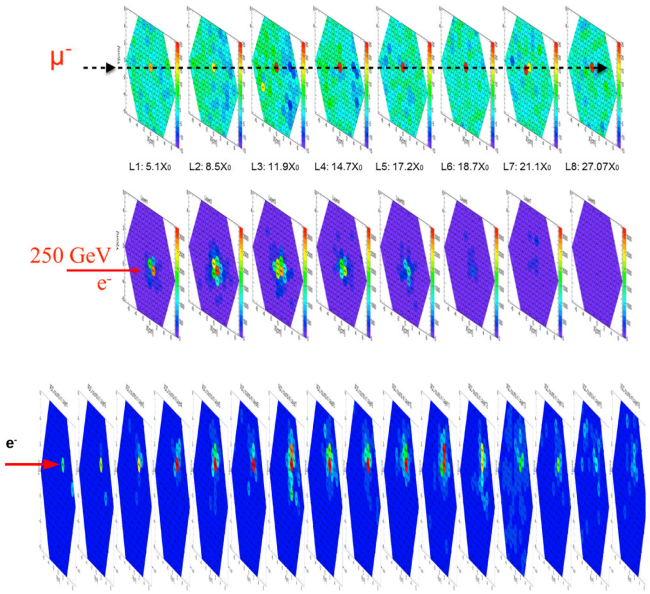


Figure 3. Event displays showing a few different events from the test beam campaigns. Top plot shows a muon track with eight layers, taken at CERN. The middle plot shows the development of a 250 GeV electron shower, also from the CERN test beam, through a total of 27 X_0. The bottom event display shows a 32 GeV electron shower through sixteen layers, all separated by 1 X_0.

IV. SUMMARY

We have developed a flexible, scalable, low cost data acquisition system for use in test beams of the HGCAL detector. The system is flexible because the use of the Zynq chip allows for a mixture of software and firmware, addressing the balance of needs for speed of readout, ease of development and debugging. The system is scalable because the use of FMC standard cards allows them to be mated to either a single commercial FMC carrier, like the Zedboard, or custom FMC carriers like the DDC. In addition, the use of HDMI cables and the architecture of the software and firmware allows the system to grow very easily. The system is low cost because the largest, most complex board (housing memory, FPGA, processor, gigabit Ethernet, etc.) is a commercial board, available at a low cost. Additionally, the use of common standards in every possible case significantly reduces development cost. Example of this are the use of the HDMI cables and the Ethernet readout.

REFERENCES

[1] The CMS Collaboration, "Technical Proposal for the Phase-II Upgrade of the CMS Detector", Technical Report CERN-LHCC-2015-010,LHCC-P-008, CERN, Geneva, June 2015. Available online: cds.cern.ch/record/2020886

[2] R. Poschl, "A large scale prototype for a SiW electromagnetic calorimeter for a future linear collider", March 2012. Available online: arXiv:1203.0249

[3] R. Rusack, "High Granularity Calorimeter for the CMS Endcap at HL-LHC", Strasbourg, November 2016, IEEE NSS/MIC Conference 2016.

[4] S. Callier, F. Dulucq, C. de La Taille, "SKIROC2, front end chip designed for the readout of the Electromagnetic Calorimeter at the ILC", JINST, vol 6, pp. C1204, September 2011.

[5] D. Baker, "Introducing the FPGA Mezzanine Card: Emerging VITA 57 (FMC) standard brings modularity to FPGA designs – VITA Technologies". April, 2008. VITA Technologies.

[6] Chatterjee, R., "First results from a beam test of a high-granularity silicon based calorimeter for CMS at HL-LHC," 2016, presented at the 38th International Conference on High Energy Physics, August 2016, Chicago, USA.