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Evidence of Interface Trap Build-up in Irradiated 14nm Bulk FinFET Technologies

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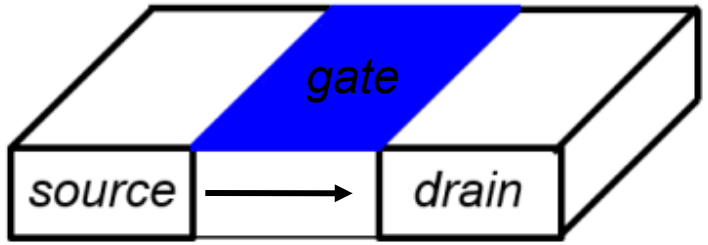
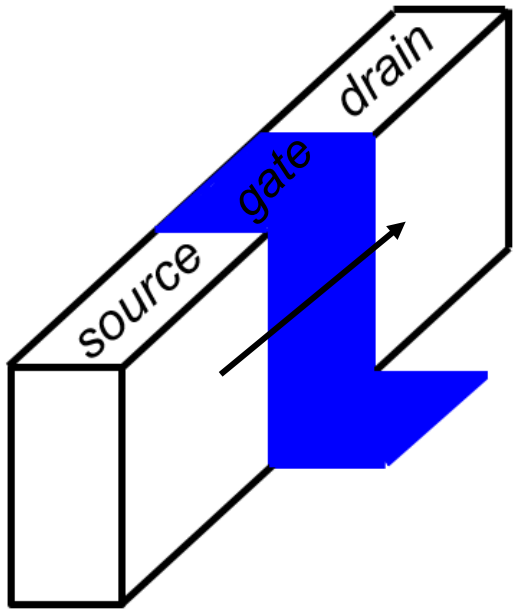
Nuclear & Space Radiation Effects Conference, NSREC, 2020

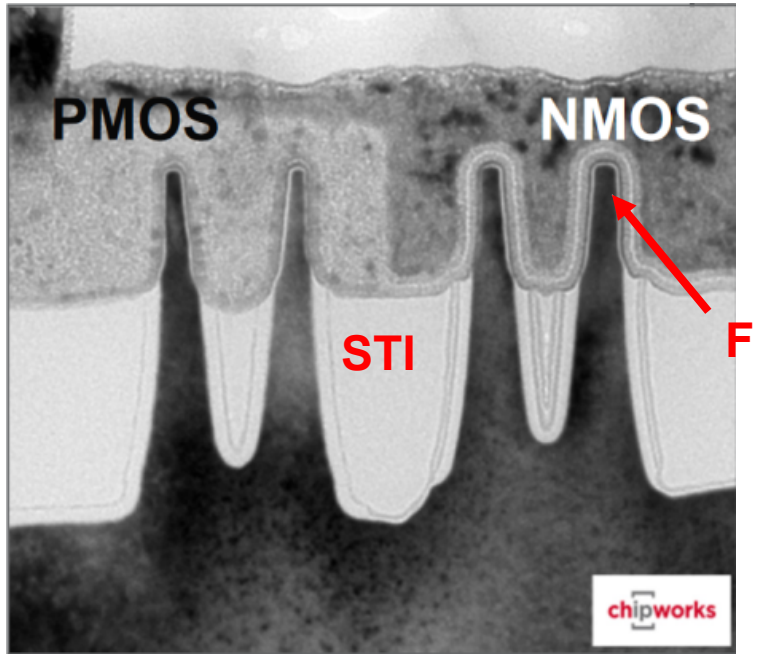
Bulk FinFET structure:
Potential threat with total ionizing dose



Planar structure



FinFET structure



D. James, NCCAVS, 2016

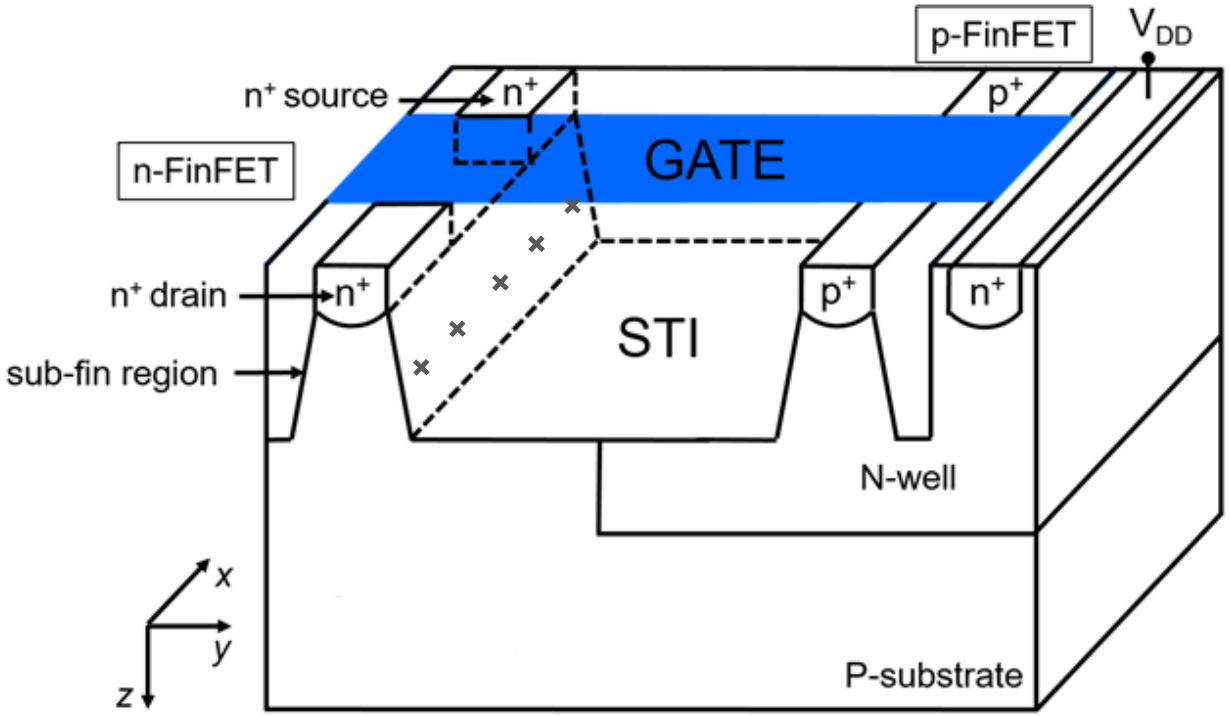
FinFET is the dominant MOSFET structure at or below 14nm node technologies

Defects in Shallow Trench Isolation (STI) might affect the performance and the reliability of scaled bulk FinFETs

Special test structure was designed to characterize TID effects

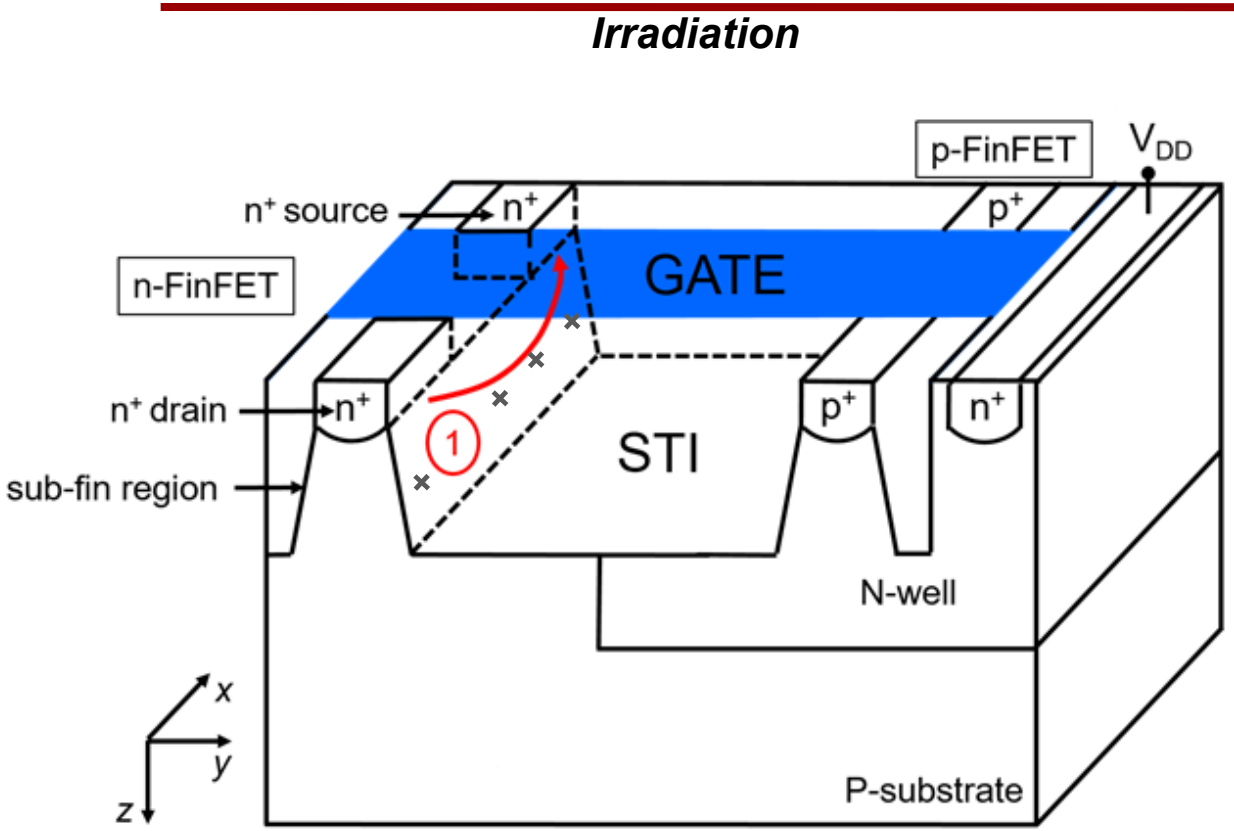
Bulk FinFET structure:
Potential threat with total ionizing dose

Irradiation



3D cross-sectional diagram of the inverter device

Bulk FinFET structure:
Potential threat with total ionizing dose



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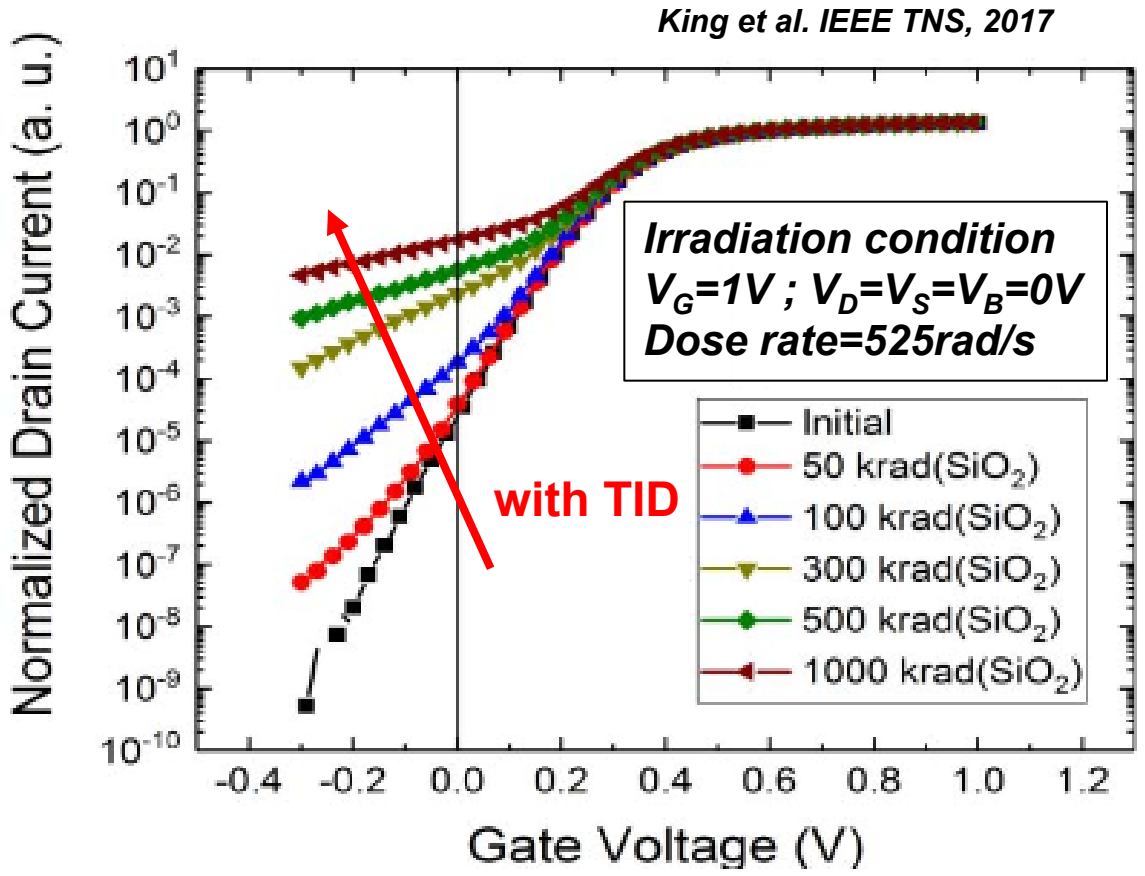
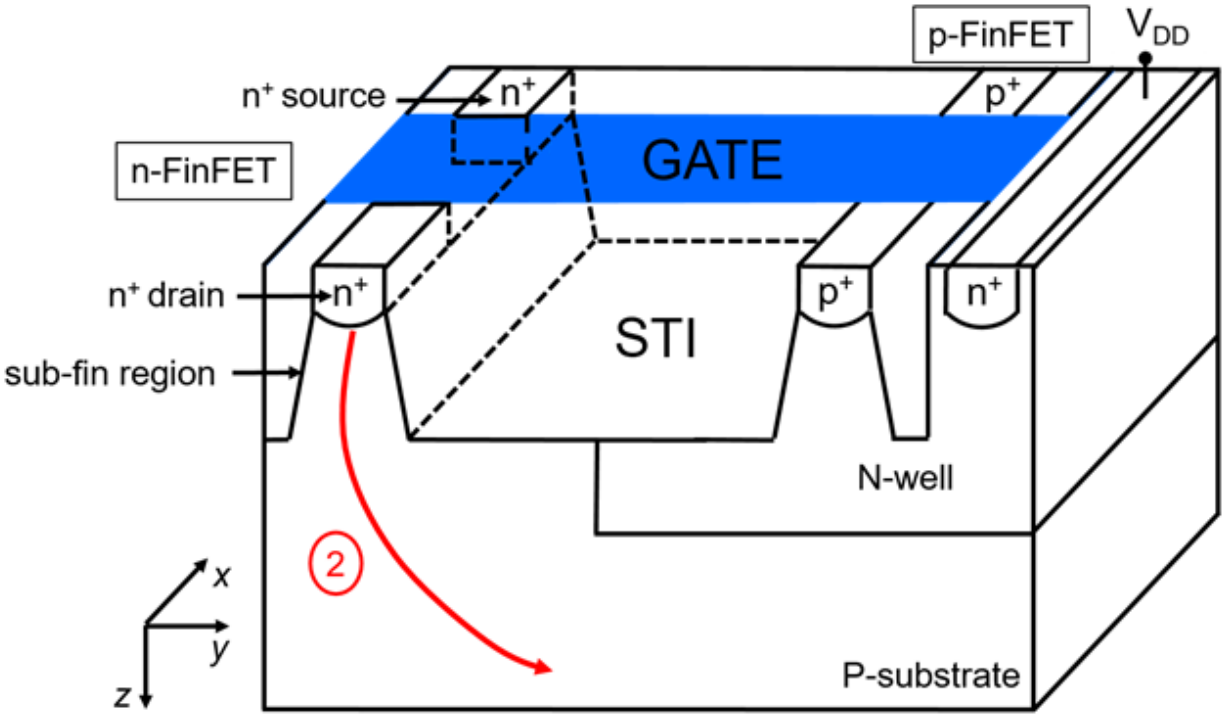


from a commercial 14-nm bulk FinFET process

Charges trapped in STI increase the off-state drain current
The path (1) is considered as the main leakage current

Bulk FinFET structure:
Potential threat with total ionizing dose

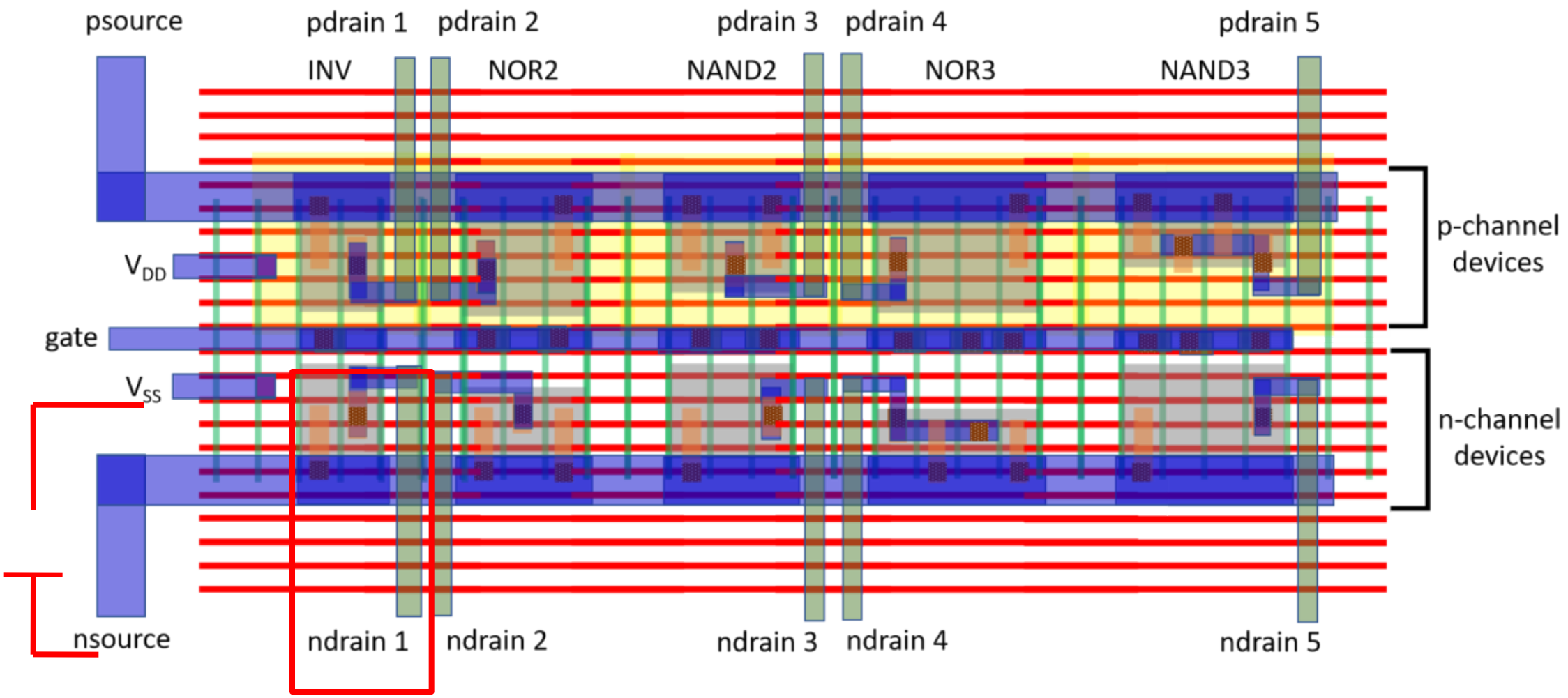
Irradiation



3D cross-sectional diagram of the inverter device

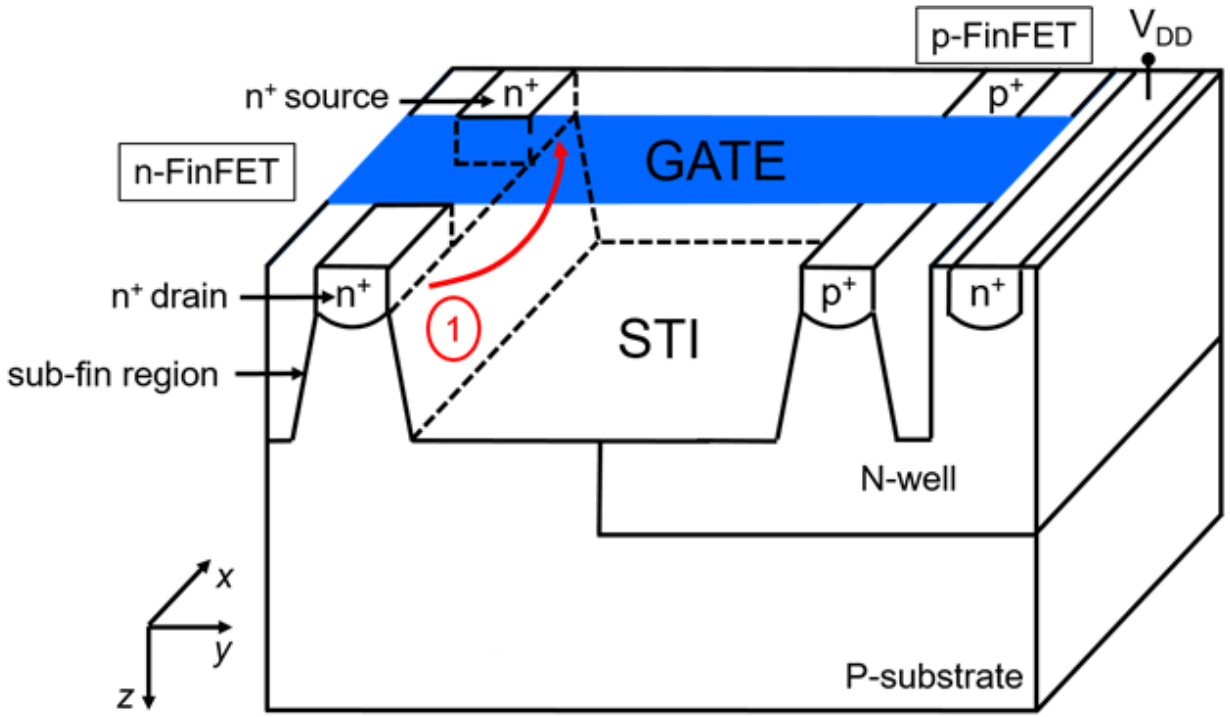
The second radiation-induced leakage path might affect the performance and the reliability of scaled bulk FinFET

Test chip:
Special test structure design



Simplified layout of the elementary structure containing logic gates

Bulk FinFET structure:
Experimental data - ON state



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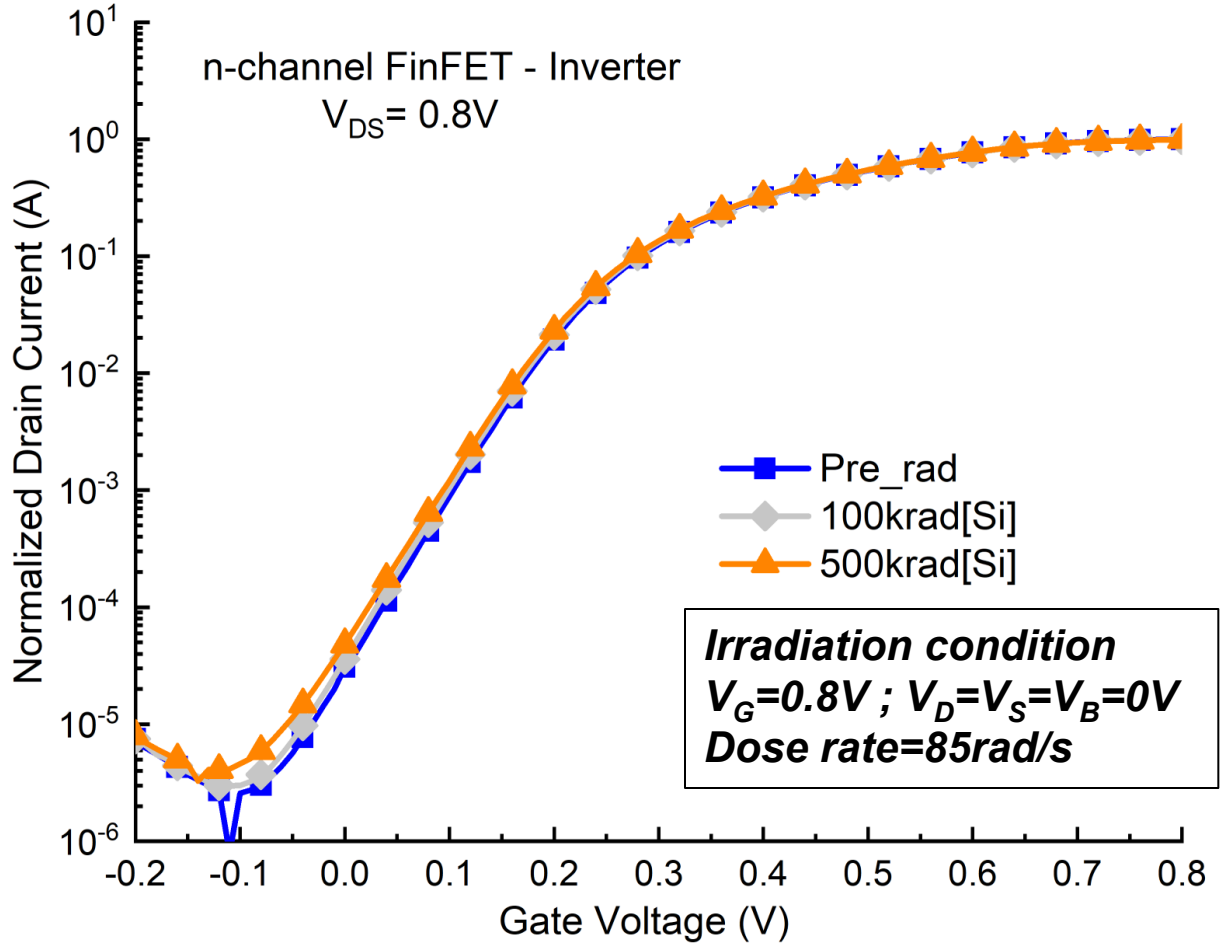
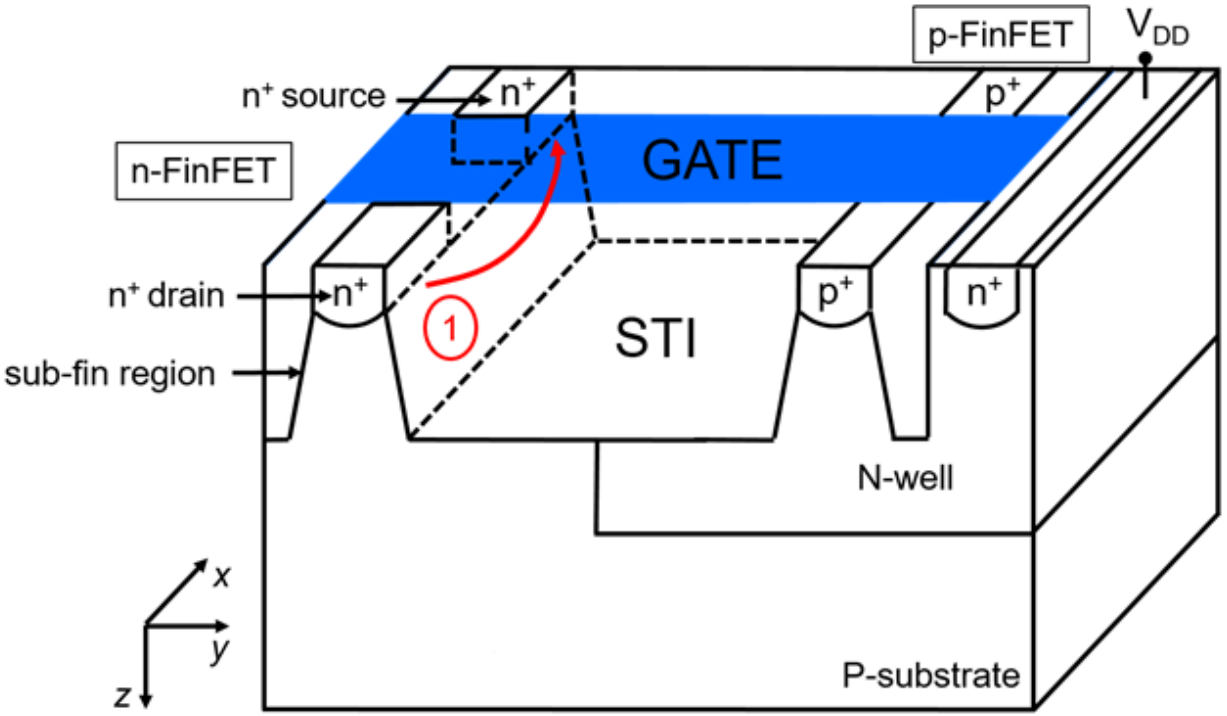


The data show a slight change in the off-state drain current as a function of V_{GS} up to 500krad[Si]

Bulk FinFET structure:
Experimental data - 0V



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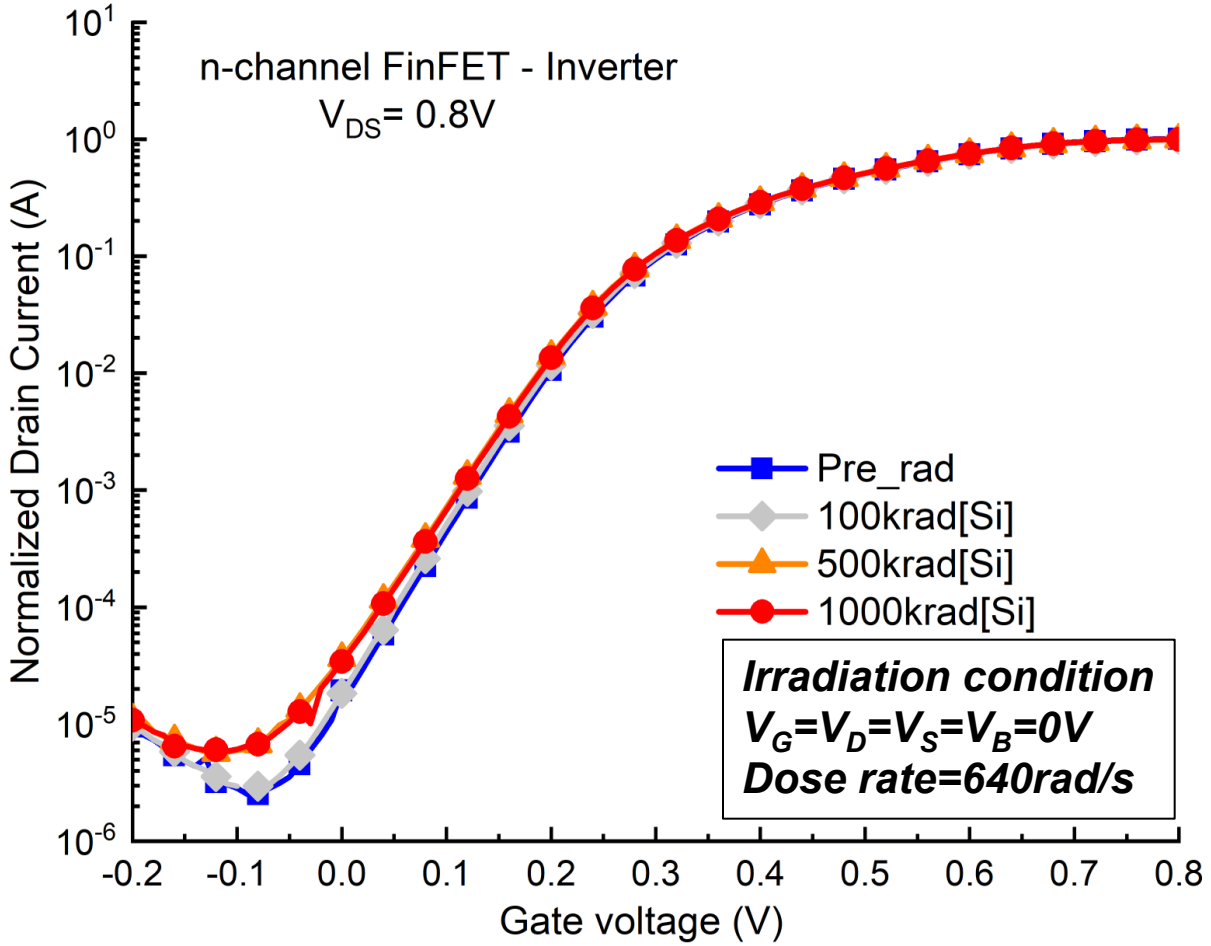

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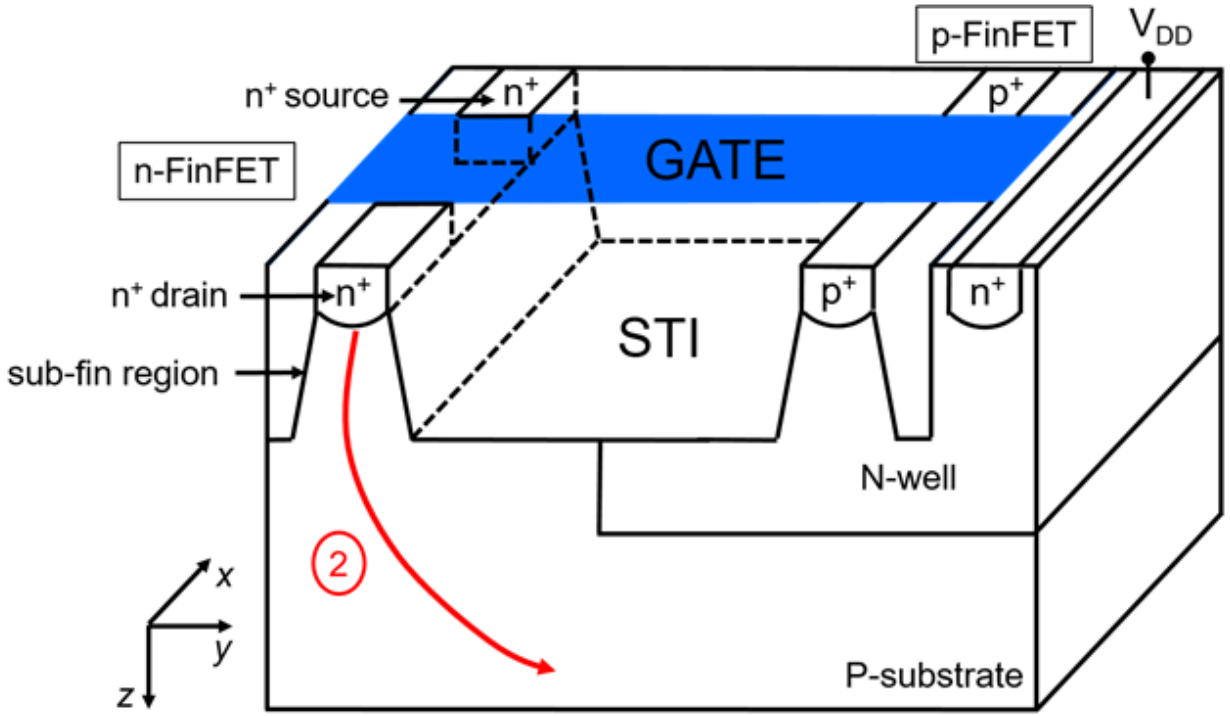
Bulk FinFET structure:
Experimental data - 0V



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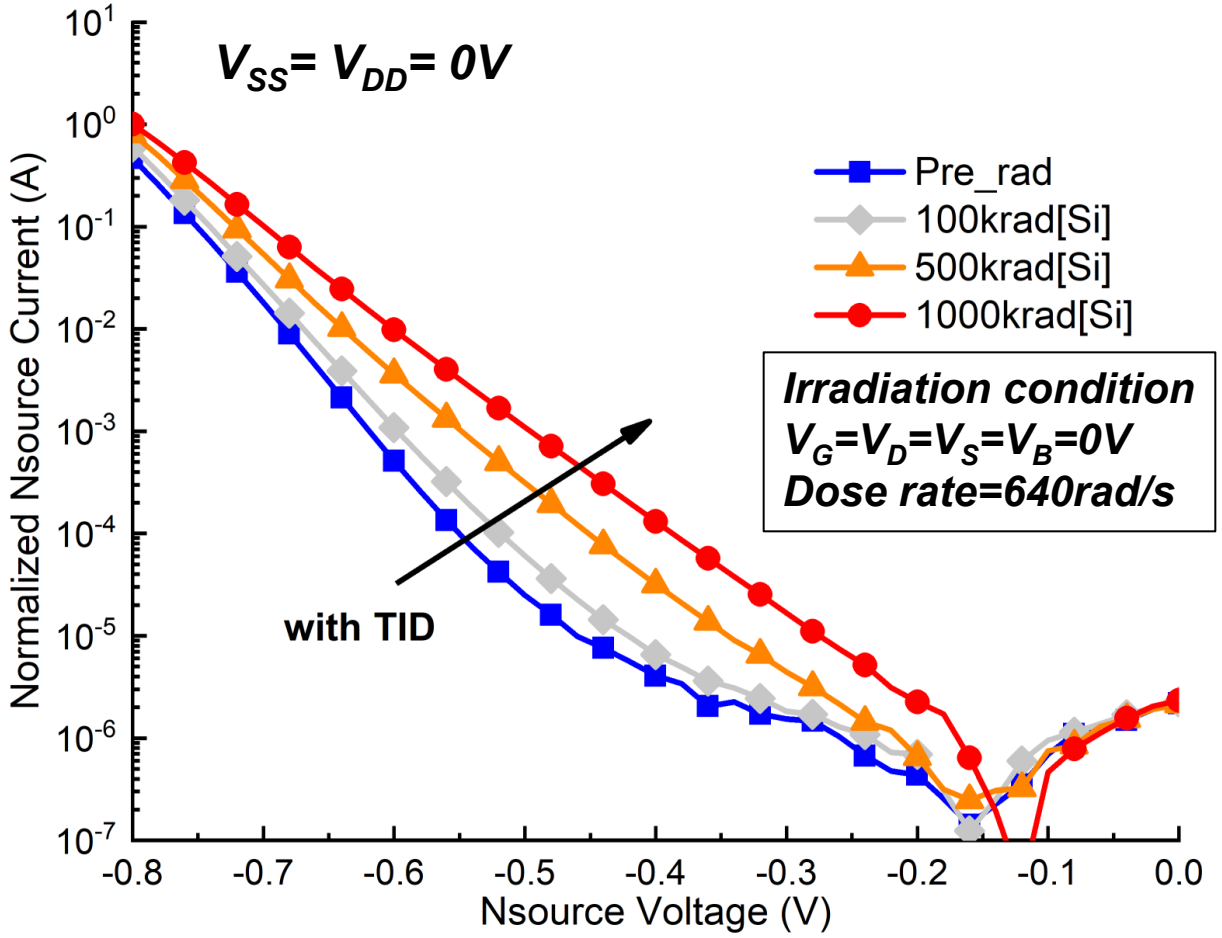
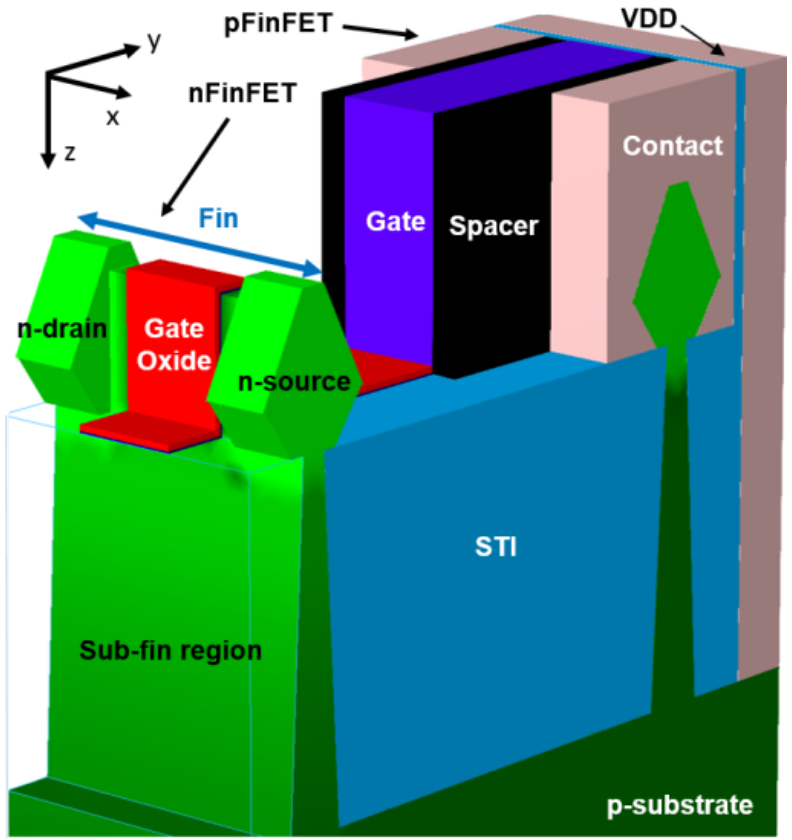


Increase of I_S with TID is characterized by enhanced carrier recombination in the space-charge region of the n+source/p-substrate diode

Bulk FinFET structure:
TCAD simulation



3D TCAD structure of the inverter device

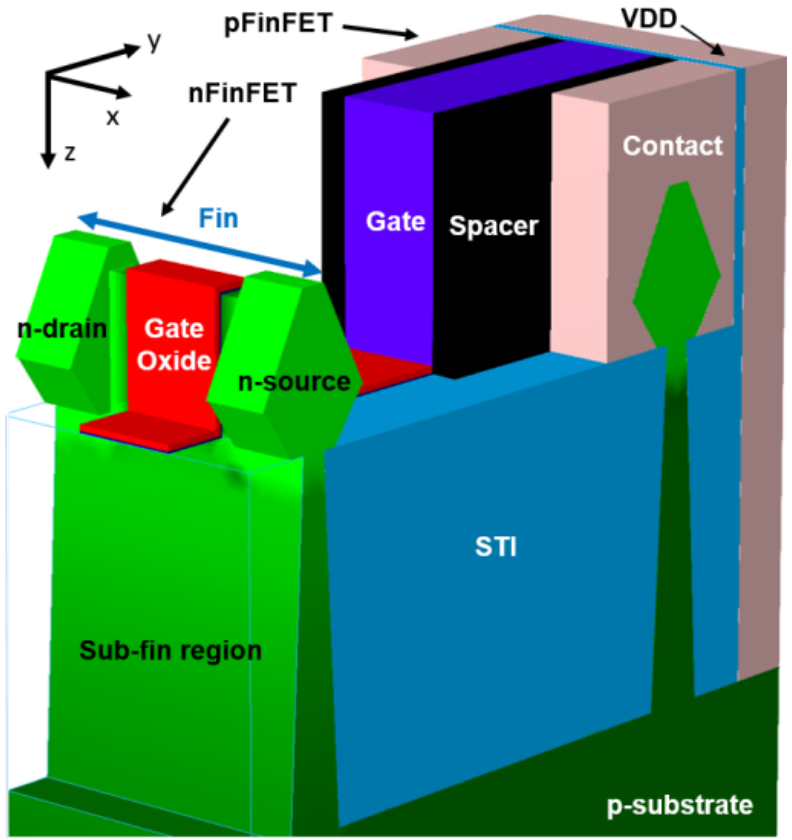
Radiation-induced traps at the Si/SiO_2 interface lead to an increase in surface recombination velocity:

$$\Delta SRV \approx \sigma_S \Delta N_{IT} v_{th}$$

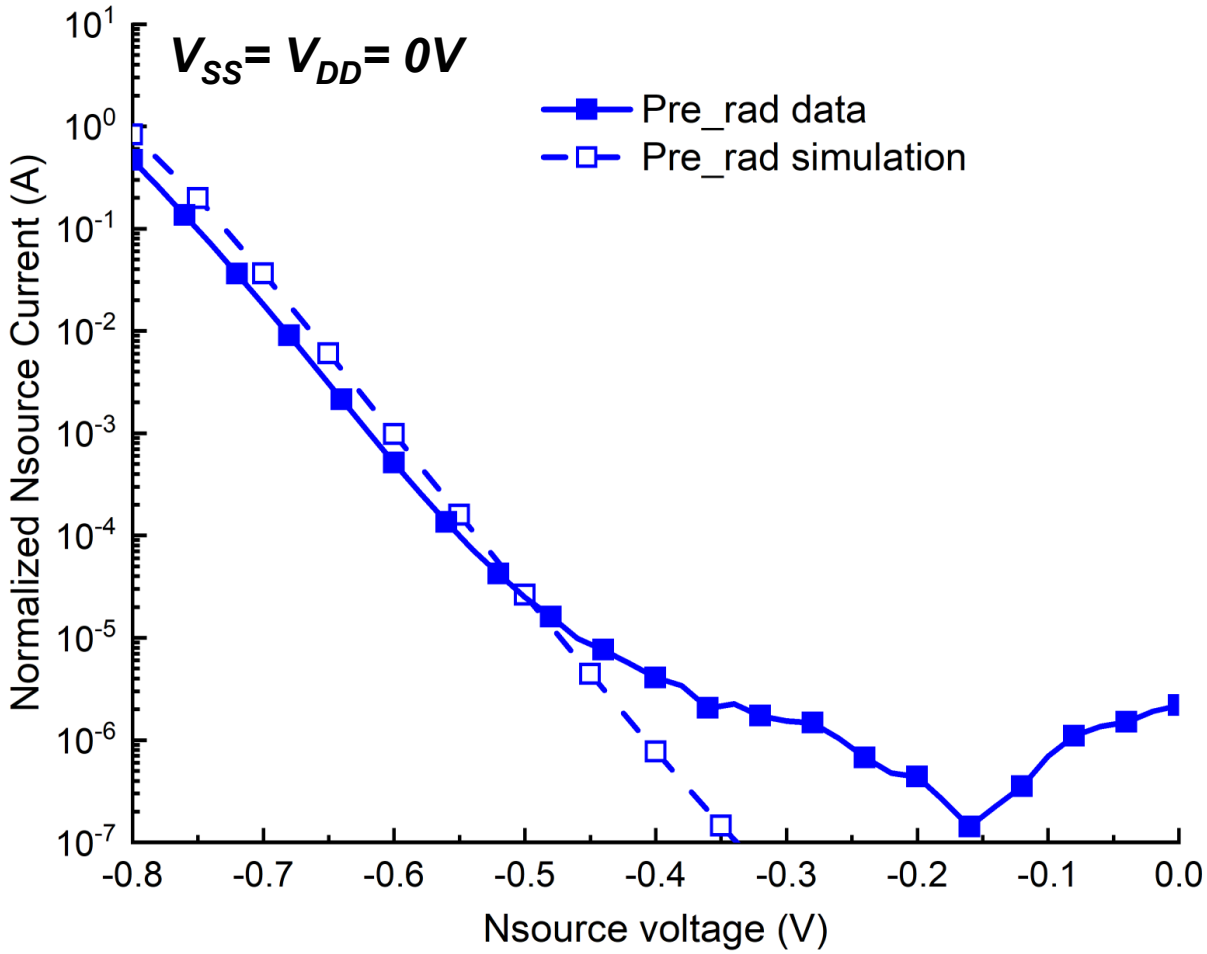
with:
σ_S the carrier capture cross-section
v_{th} the carrier thermal velocity

3D TCAD simulations were performed to support analysis of the identified TID mechanisms and confirm evidence of N_{IT} build-up

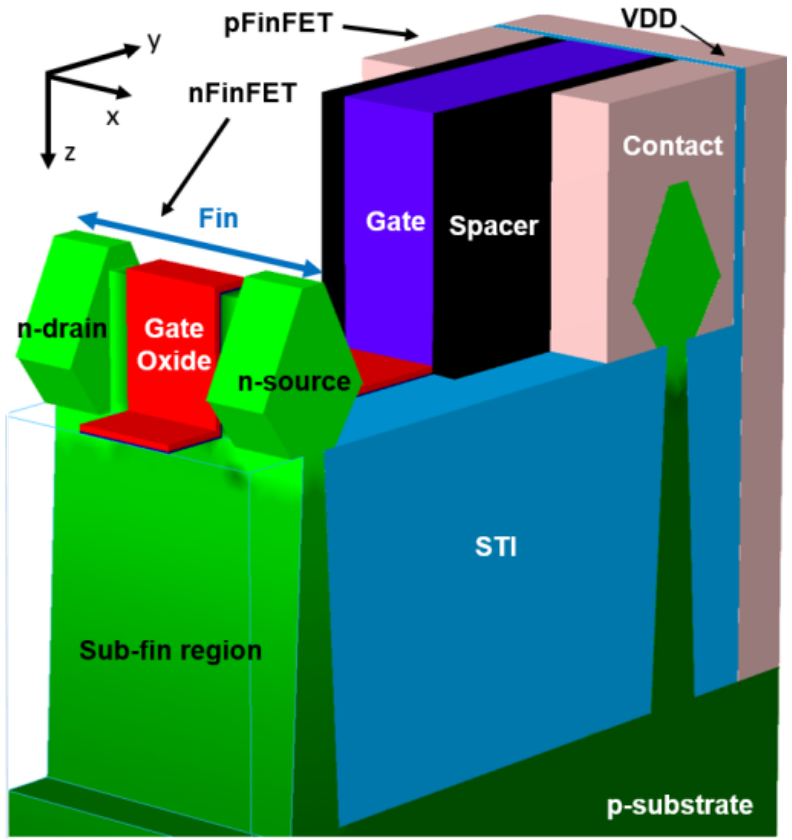
Bulk FinFET structure:
TCAD simulation results



3D TCAD structure diagram of the inverter device



Bulk FinFET structure:
TCAD simulation results



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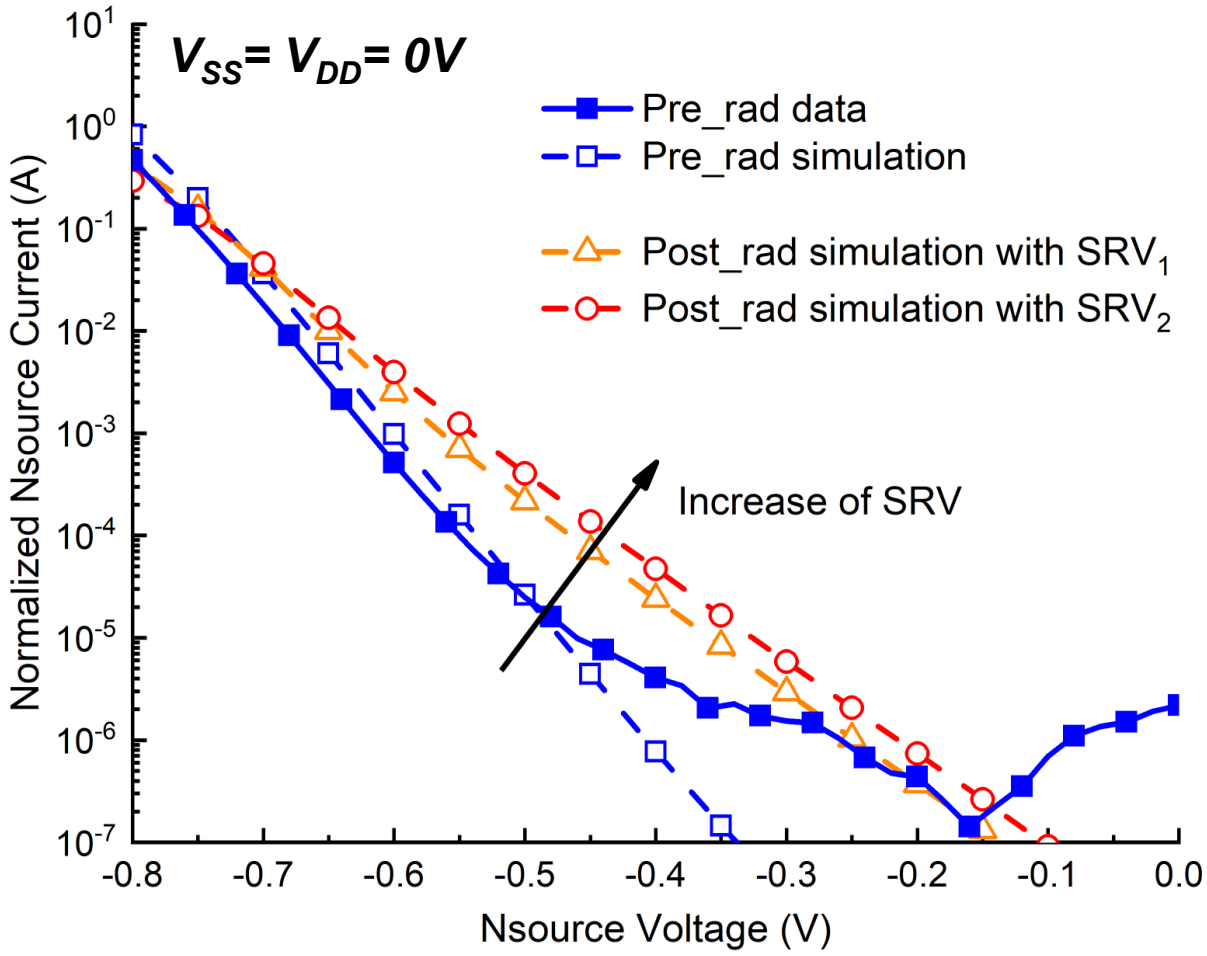
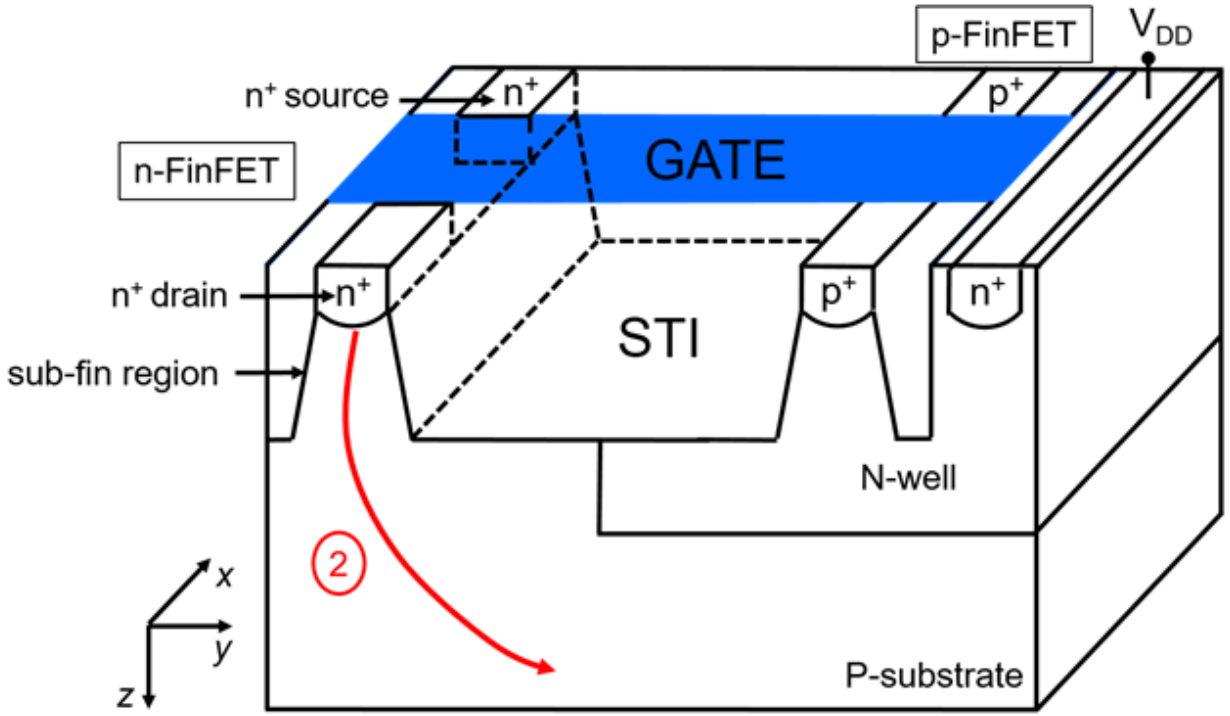


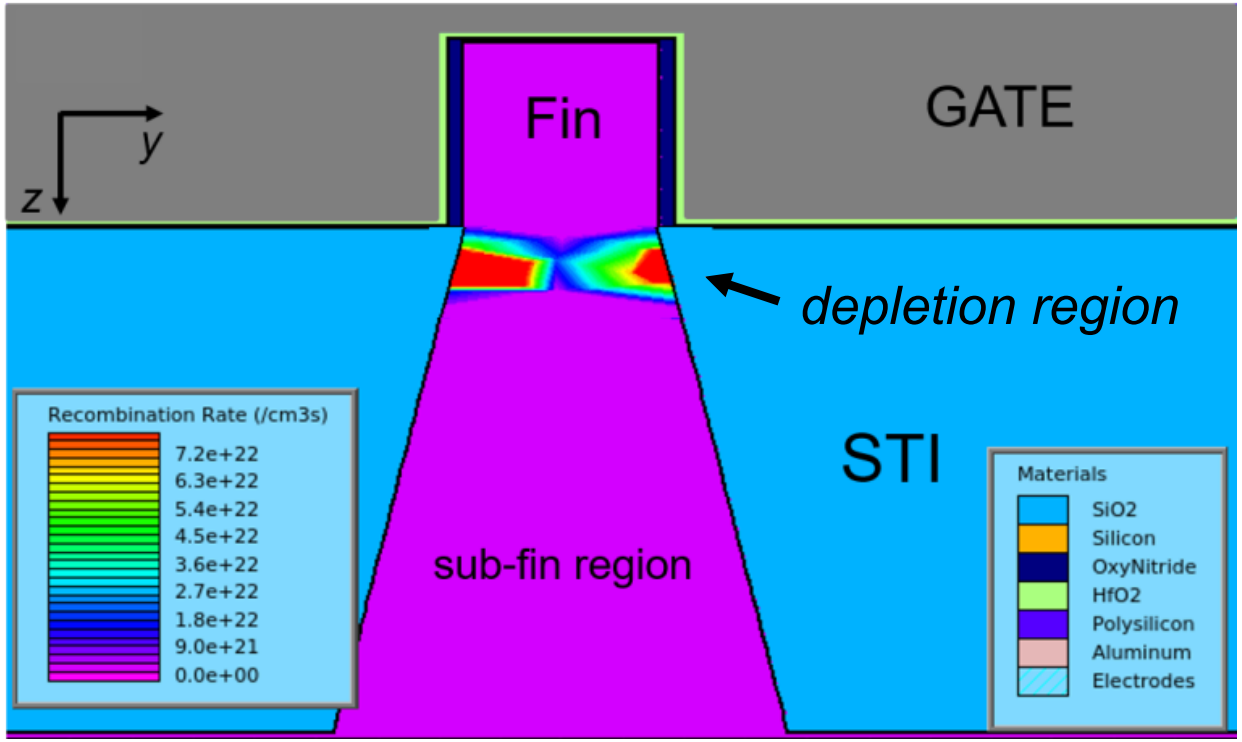
An increase in the source current as a function of the N_{SOURCE} voltage is observed by increasing SRV at the Si/SiO_2 interfaces

Bulk FinFET structure:
TCAD simulation results

Irradiation



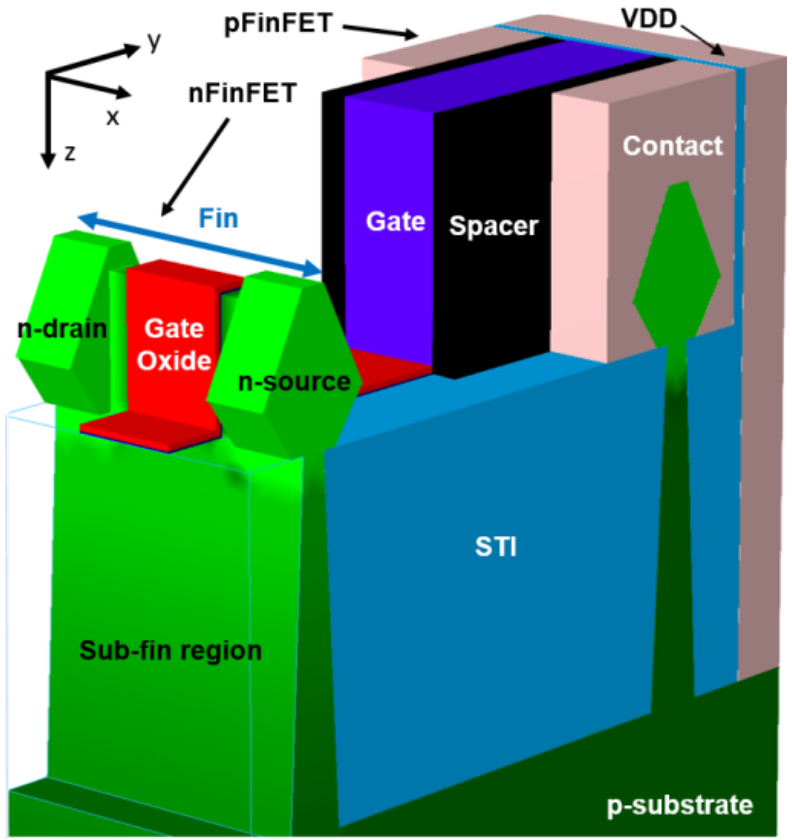
3D cross-sectional diagram of the inverter device



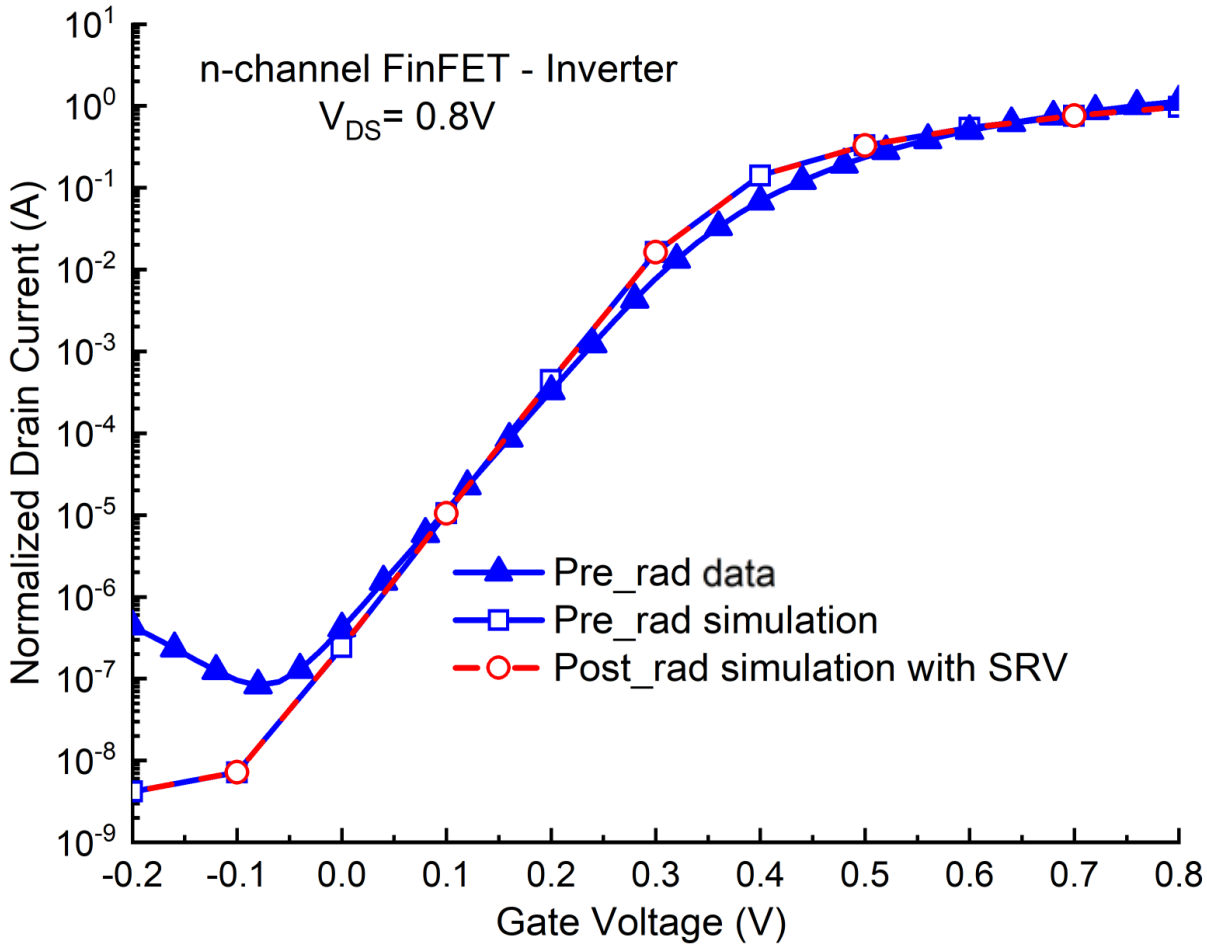
2D cross-sectional of the nFinFET

The origin of the increase of source current is due to carrier recombination at interface traps created in the sub-fin region of the device

Bulk FinFET structure:
TCAD simulation results



3D TCAD structure diagram of the inverter device



Increase in SRV does not impact I_D-V_{GS} characteristic

Conclusion

- Radiation testing and modeling performed on 14nm bulk FinFET
- Results show TID-induced defect build-up in Shallow Trench Insolation continues to be a threat to bulk FinFET technologies

This work reports:

- FinFET leakage current responses differ from previous studies
- Evidence of interface trap buildup in irradiated 14nm bulk FinFET technologies
- These defects found in the STI oxide adjacent to the sub-fin region of the n-channel FinFET could lead to an undesirable increase in current in integrated circuits