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Copper Electrodeposition in High Aspect Ratio Mesoscale TSVs: Scaling from Die Level to Wafer Level Plating

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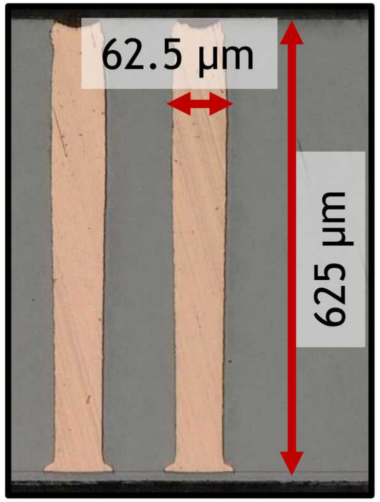
Through-Silicon Vias (TSVs) for MEMS Applications

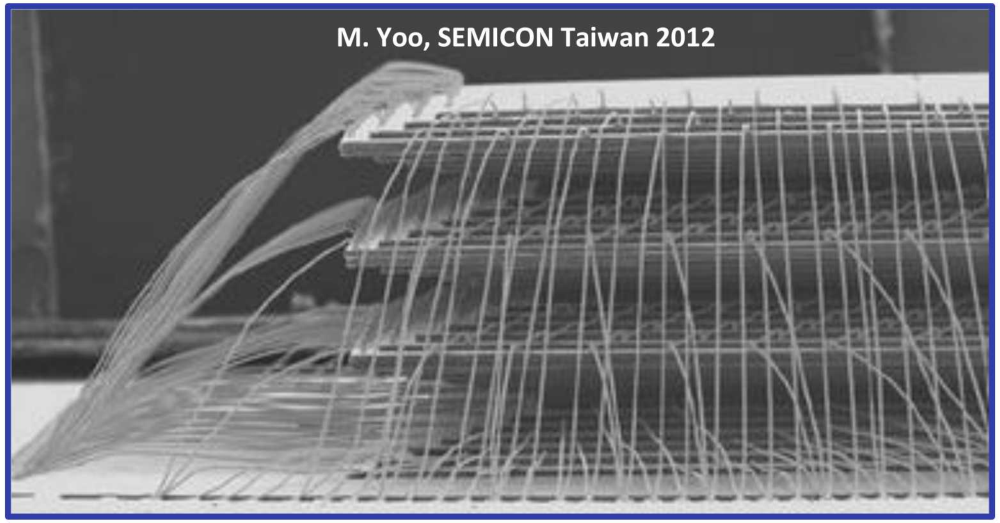
Benefits of mesoscale Cu TSVs

- Increase I/O
- Aid in system miniaturization
- Simplify design and assembly
- Improve thermal management
- Reduce electrical parasitics
- Span full wafer thickness, required for MEMS applications

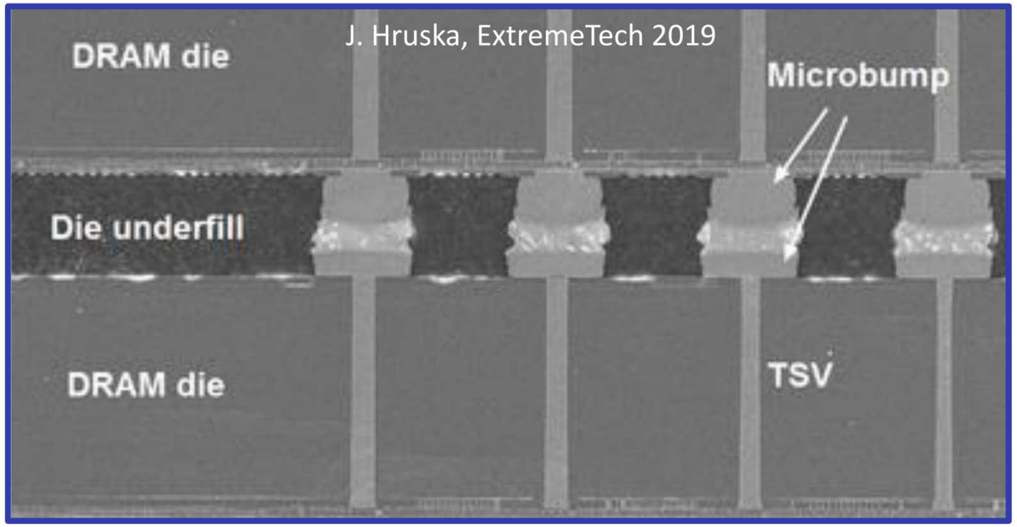
Geometry of our TSVs

- 625 μm in depth
- 62.5 μm in diameter
- 10:1 aspect ratio





Wire bonded 3D Stacked Die

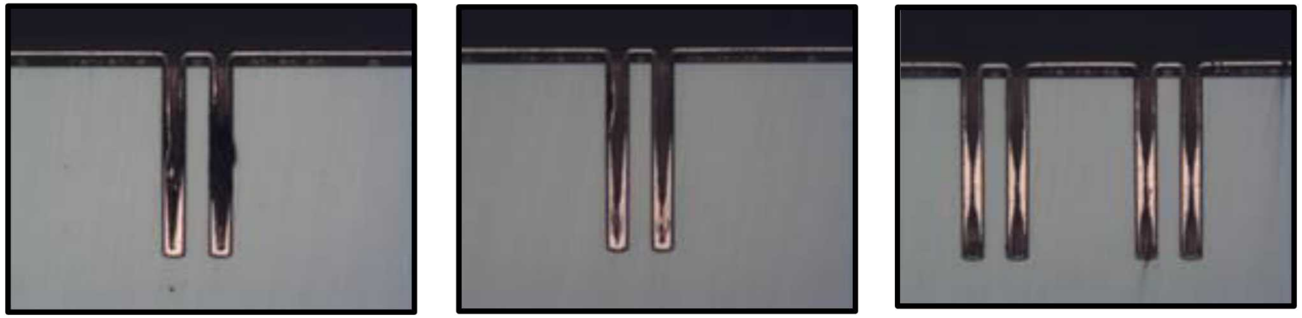


3D Stacked Die with integrated TSVs

Single-additive Electrolyte for Void-free Filling

S-Shaped Negative Differential Resistance (S-NDR) Mechanism, pioneered by Dan Josell and Tom Moffat at NIST[1,2]

- Plating electrolyte containing Cu salt, acid, chloride, and suppressor
- At a given suppressor concentration more negative applied potential pushes deposition higher in the TSV
- Operational window can be roughly determined through cyclic voltammetry

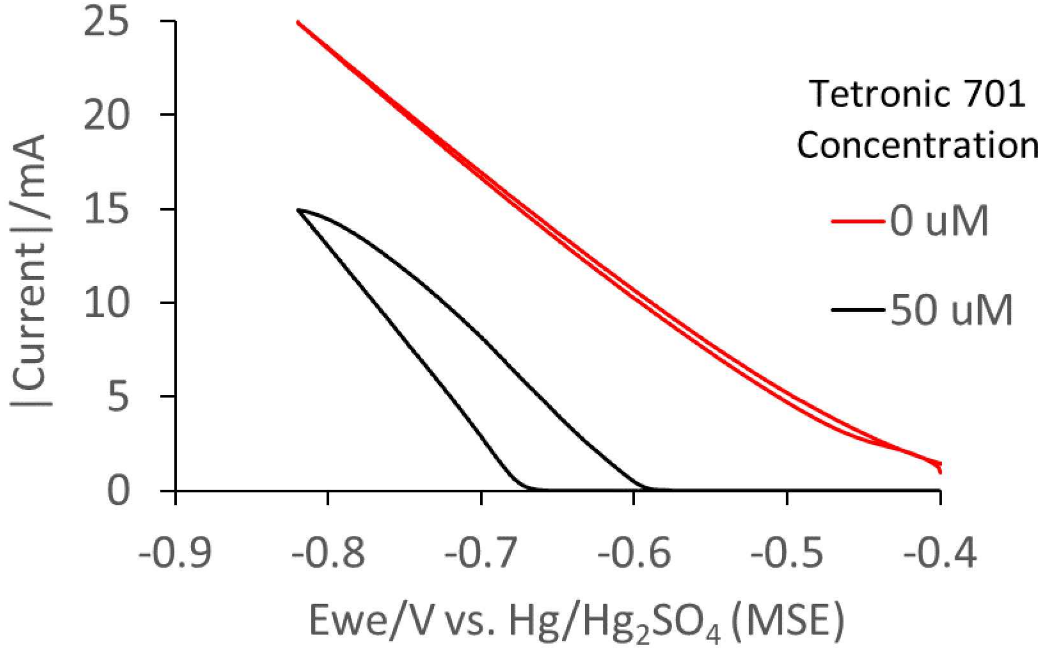


More negative potential →

1. Journal of the Electrochemical Society, 159 (4) D208-D216 (2012)
2. Journal of the Electrochemical Society, 159 (10) D570-D576 (2012)

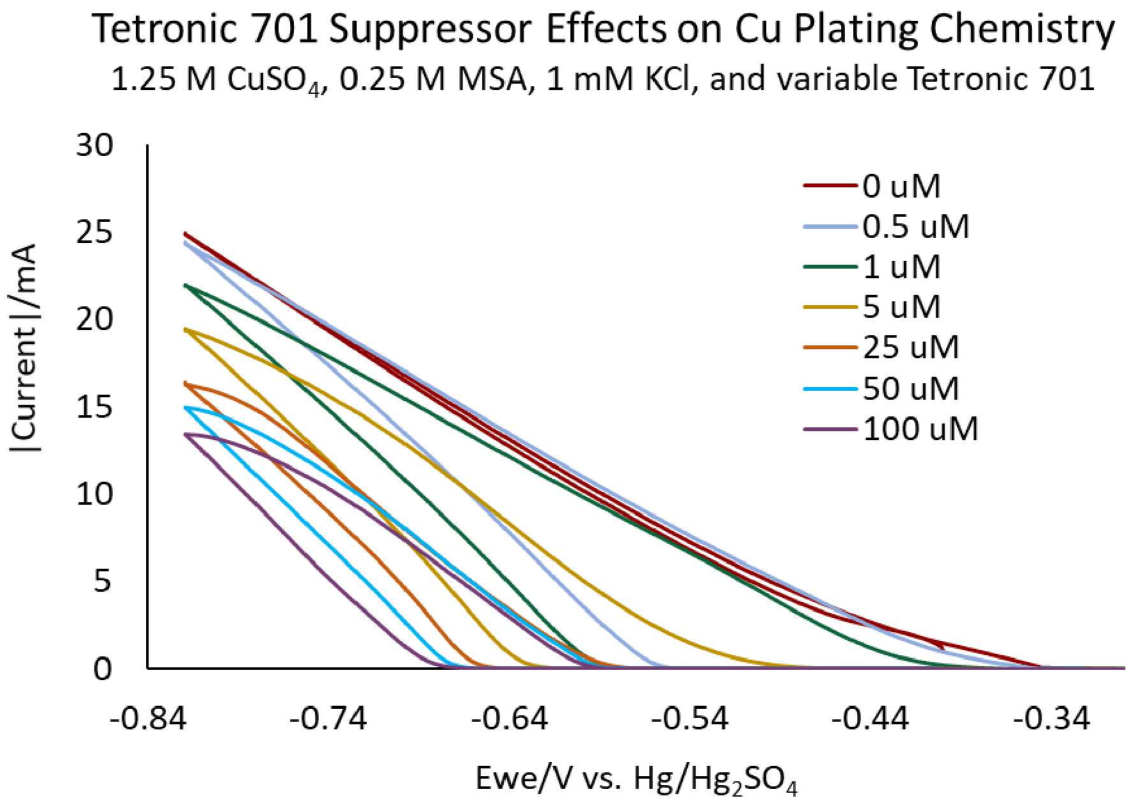
→ Void-free filling can be achieved
→ Delicate balance of applied bias, electrolyte composition, and solution replenishment

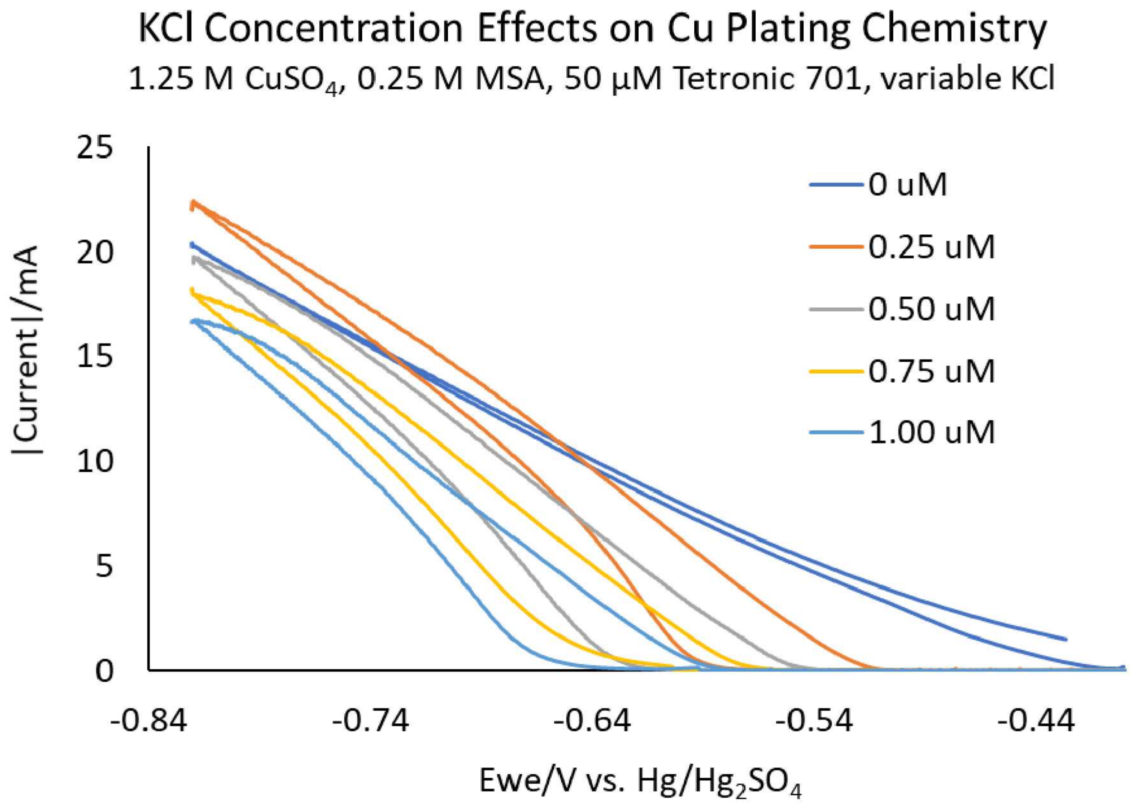
RDE Voltammetry to Analyze Cu Reduction in 1.25 M $CuSO_4$, 0.25 M MSA, 1mM KCl



Controlling Suppressor Behavior

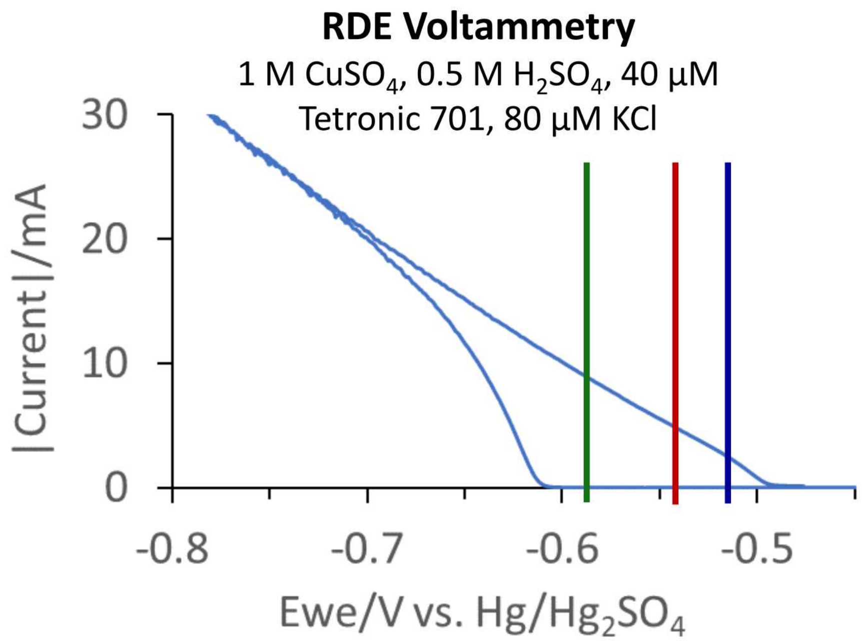
- Suppressor molecules and chloride coadsorb to the metal surface
- Changing the suppressor concentration or the chloride concentration can alter the level of suppression in the system

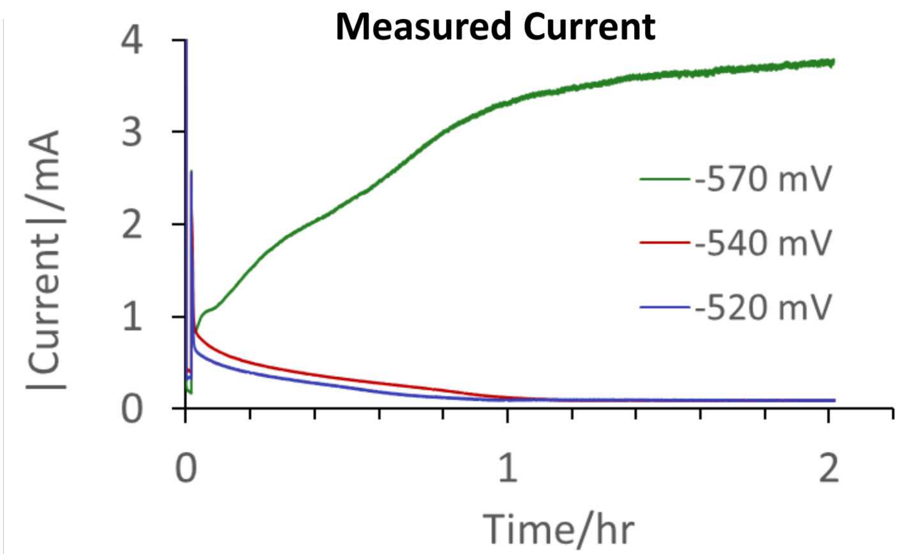


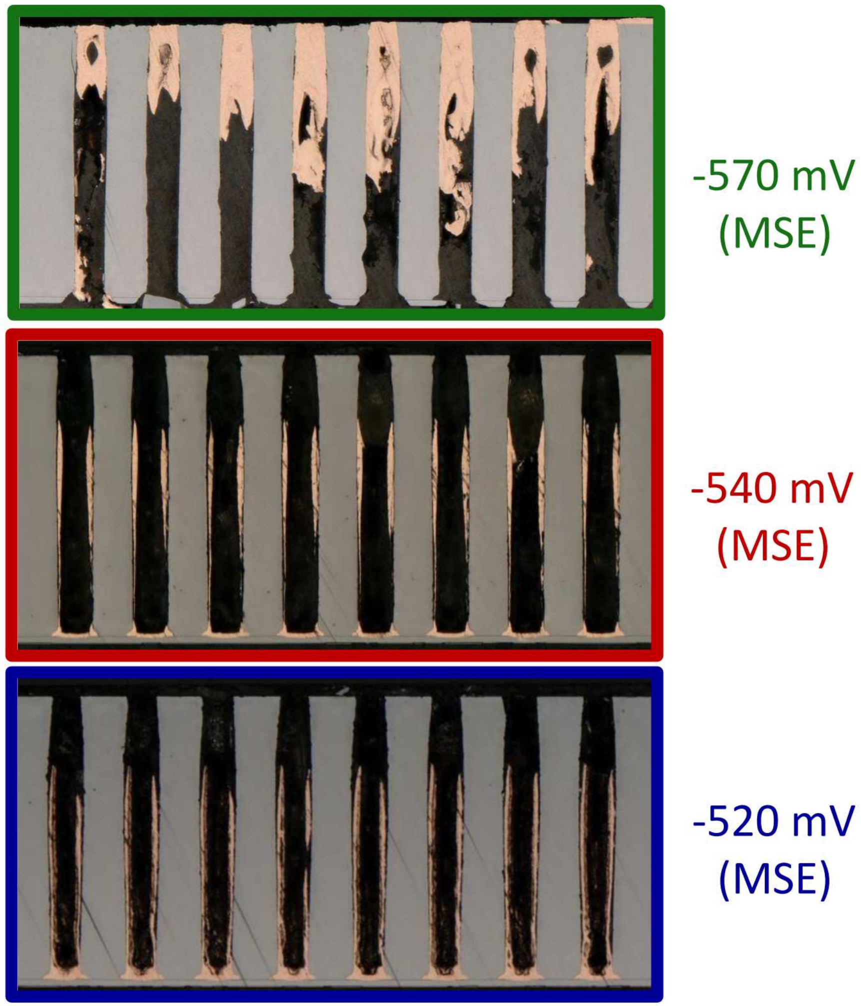


→ Chloride concentration can be used to tune electrolyte system behavior

Establishing an Operational Window







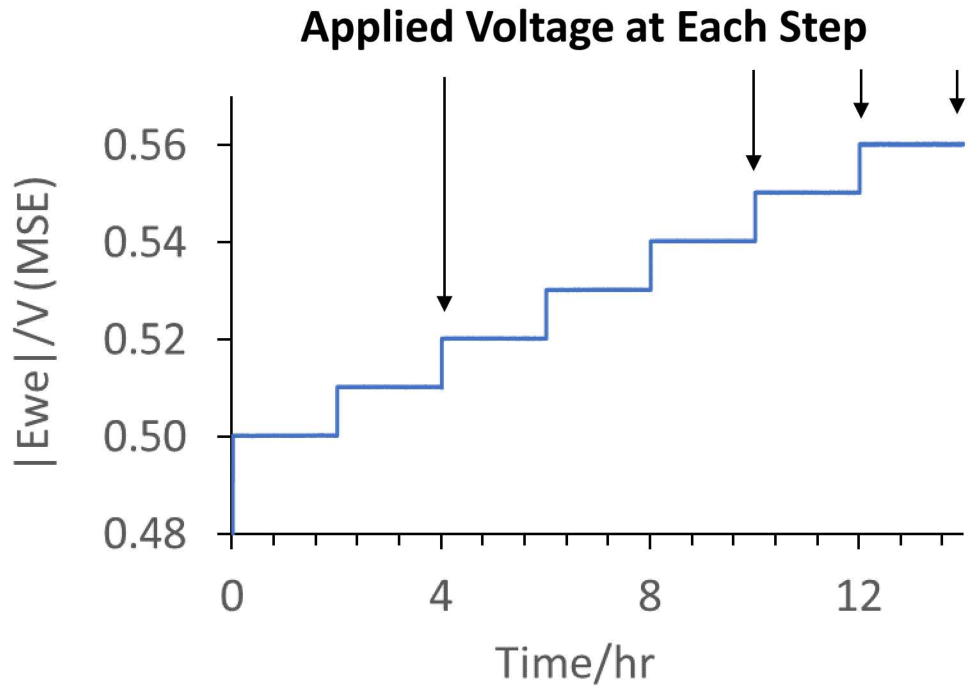
Apply these results to voltage stepping recipe

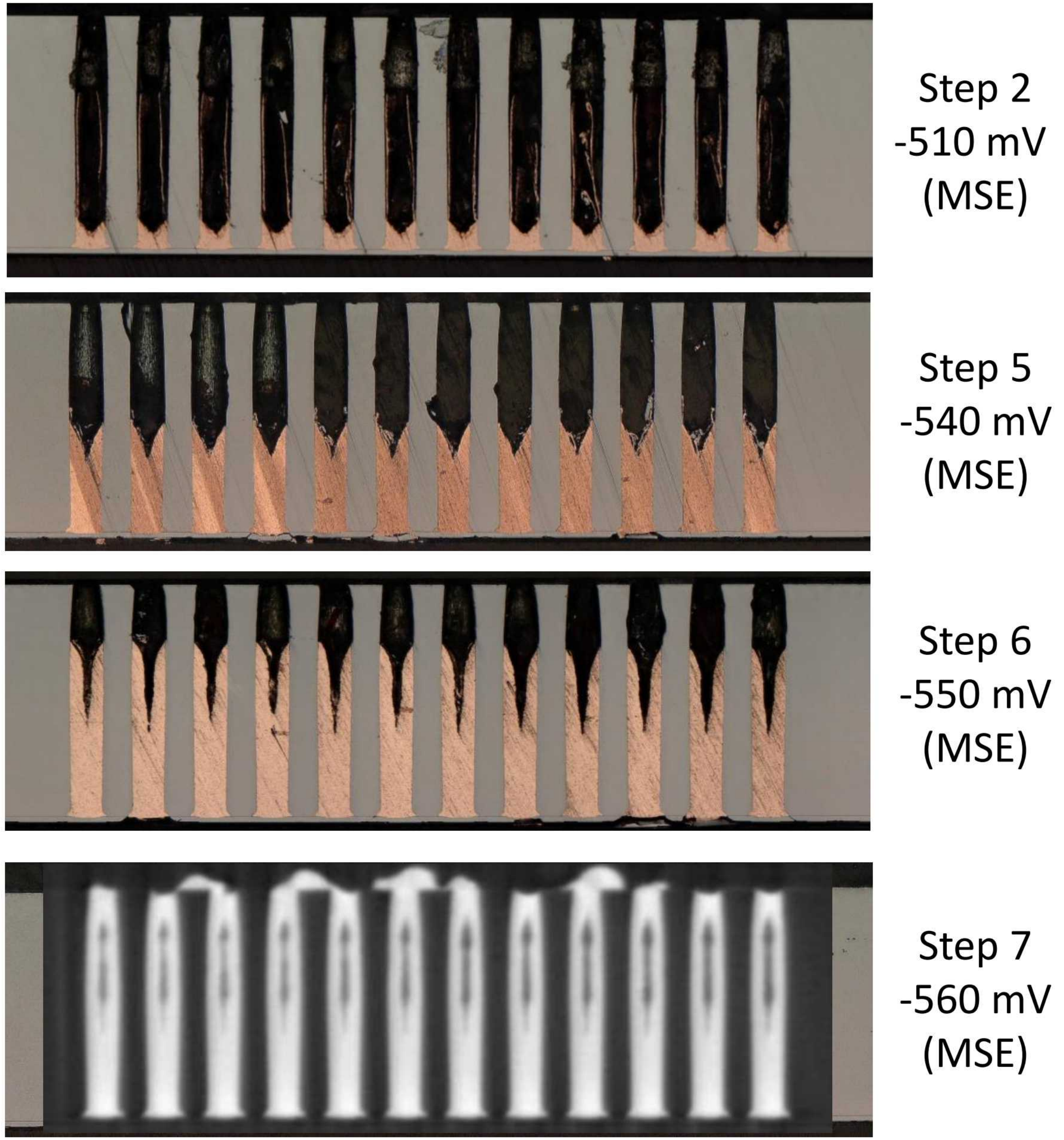
→ Start at a voltage more positive than -520 mV (MSE)

→ Sustain each voltage for ~1-2 hours

Stepping Applied Voltage to Fill the Vias

- Based on the operational window established, create voltage stepping recipe. Step voltage from -500 mV to -560 mV (MSE) in 10 mV increments for 2 hours each



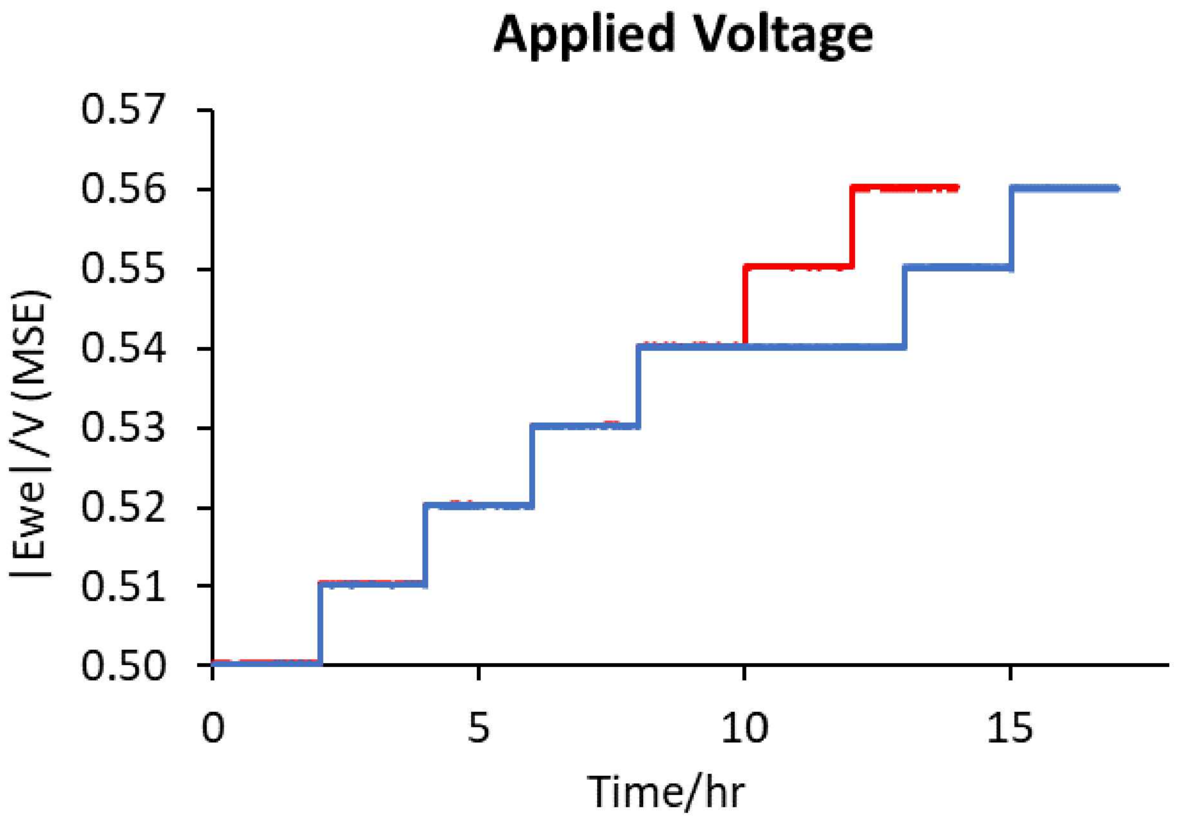


→ CT scan shows minor seam voids

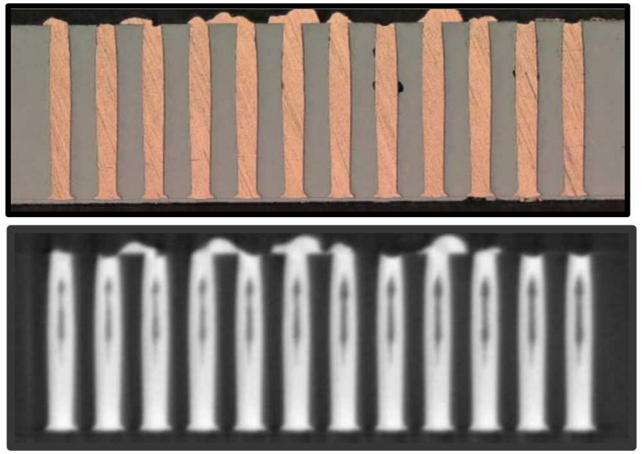
→ Increasing time held at step 5 may eliminate voids

Experimental Changes Leading to Void-free Filling

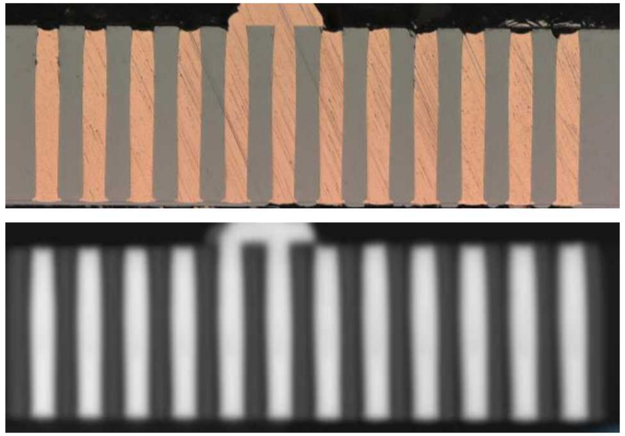
- Increase length of step number 5 (-540 mV) to mitigate void formation



Short Step #5 (2 hrs)



Long Step #5 (5 hrs)

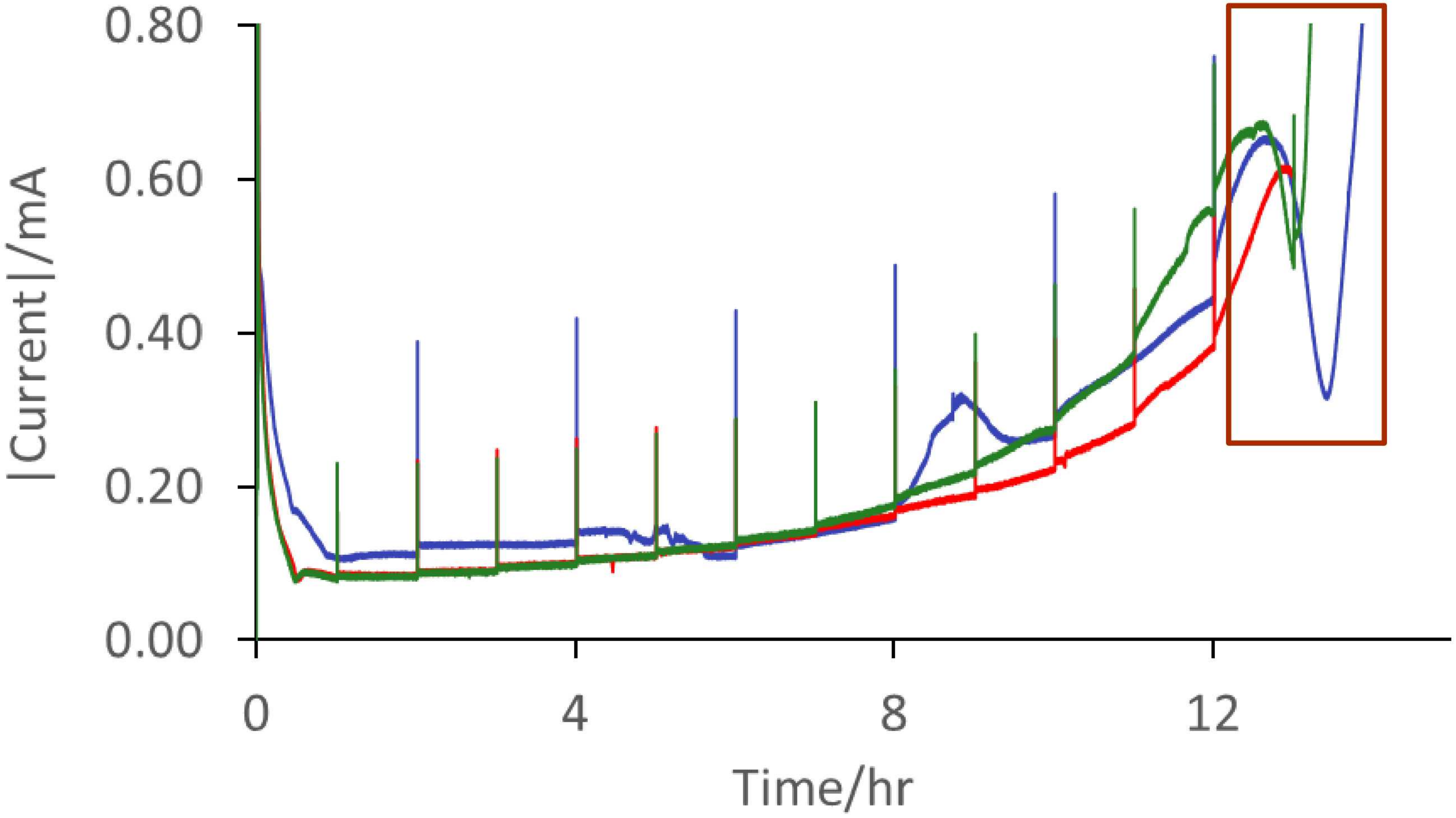


CT scan results confirm void-free, bottom-up filling!

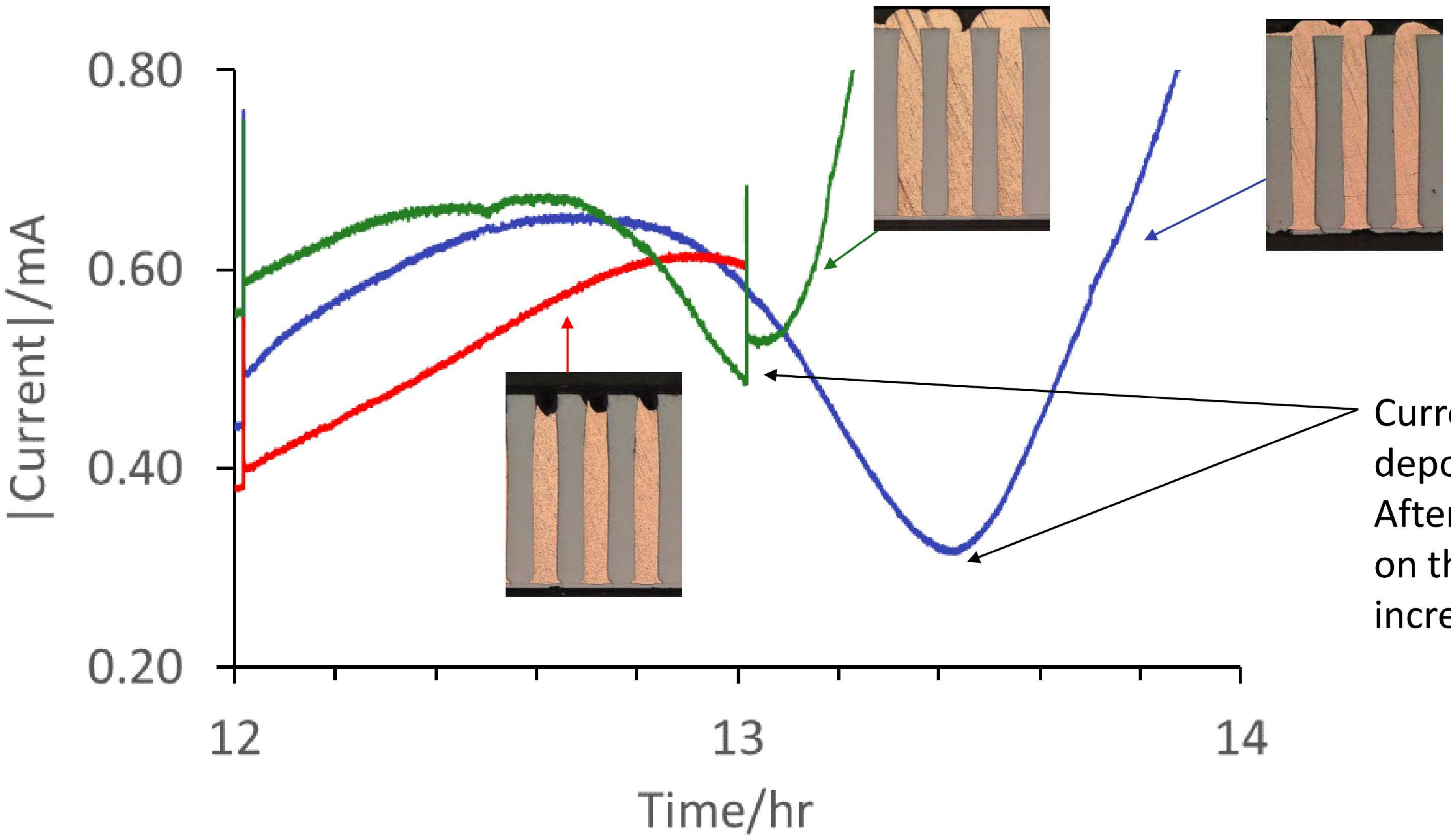
Endpoint Detection Method to Determine Fill Completion

Why is there a characteristic dip in current the end of the deposition?

Measured Current for Voltage-controlled Experiments

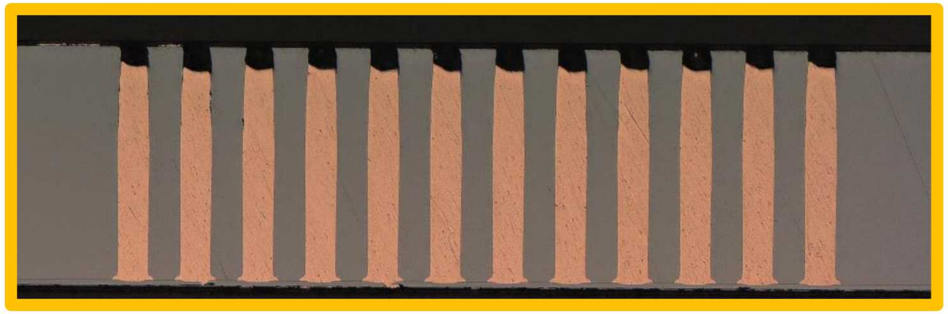


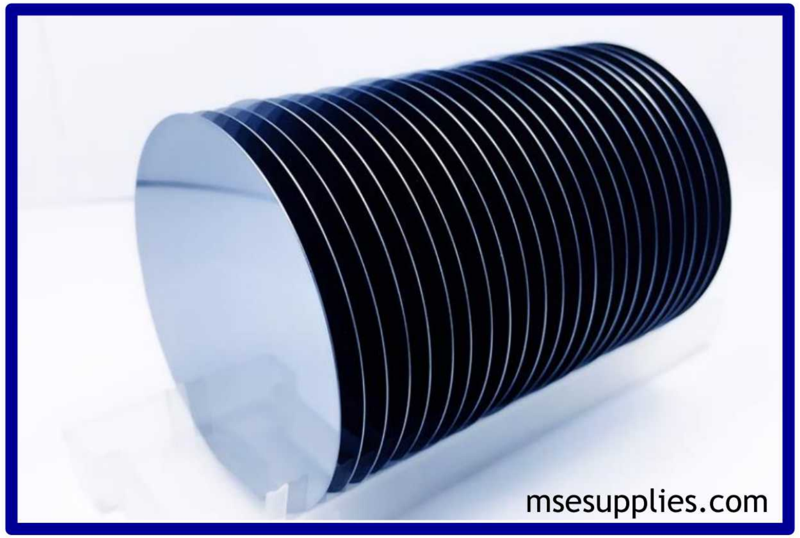
Endpoint Detection Method to Determine Fill Completion



Current minima indicating deposition reached top of via. After suppression breakdown on the field surface, current increases rapidly.

Moving from Die Level to Wafer Plating (WLP)





Potential issues when moving to WLP

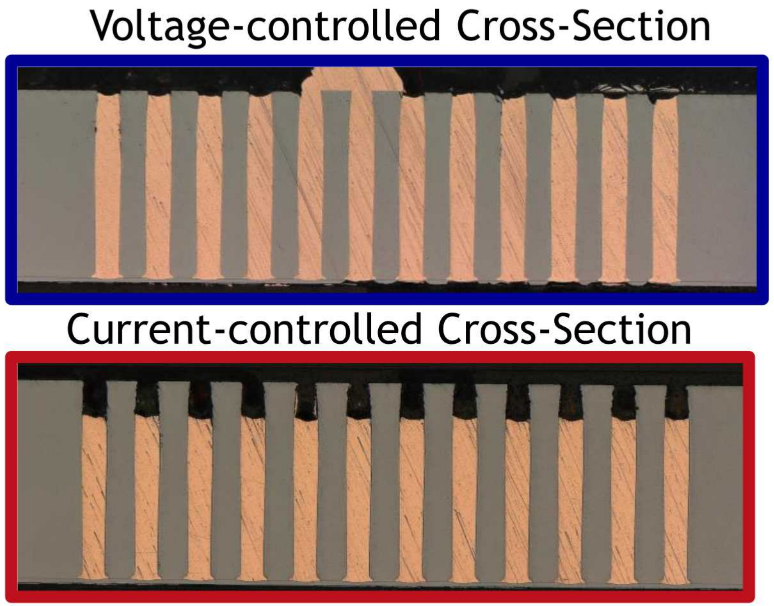
1. Voltage-controlled filling is not compatible with production scale plating tools
2. Sample surface area will increase from small 1 cm^2 die to full wafer size
3. Vias at different points along wafer radius move at different linear velocities

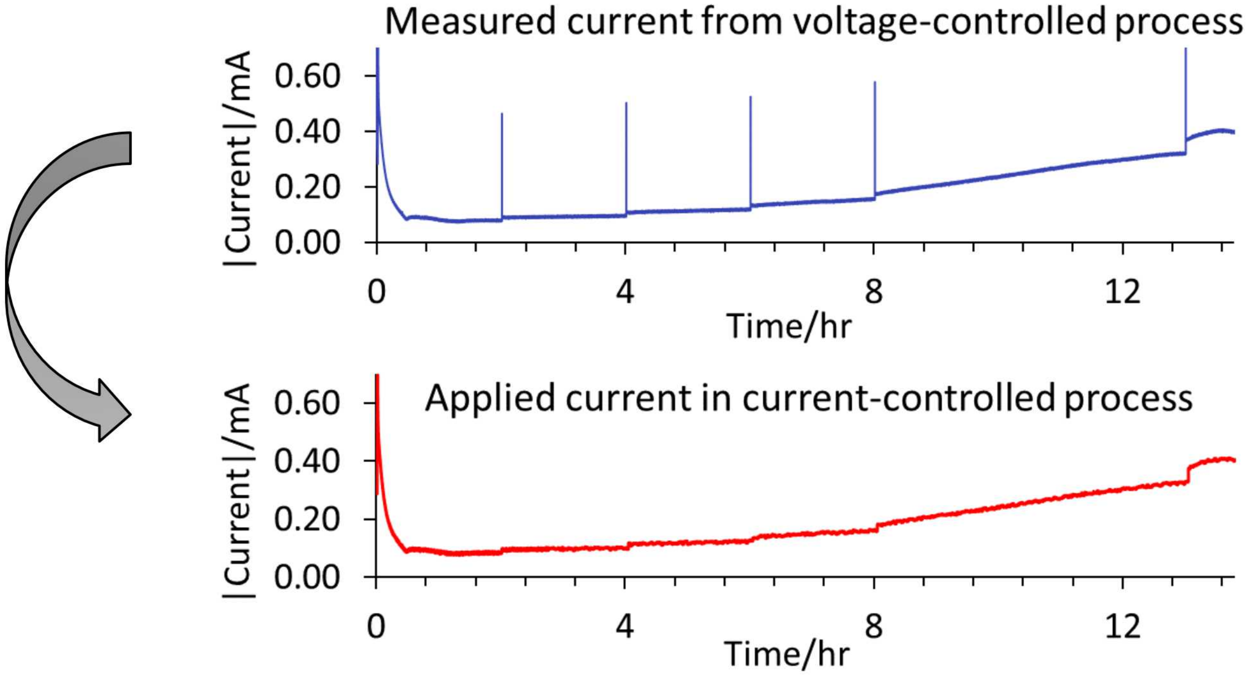
How can these issues be solved?

1. Can we derive current-controlled plating processes from our voltage-controlled deposition recipe?
2. How does current scale with increasing die size? Does current scale with total conductive surface area or via cross-sectional area?
3. What is the impact of rotation rate on Cu fill profile?

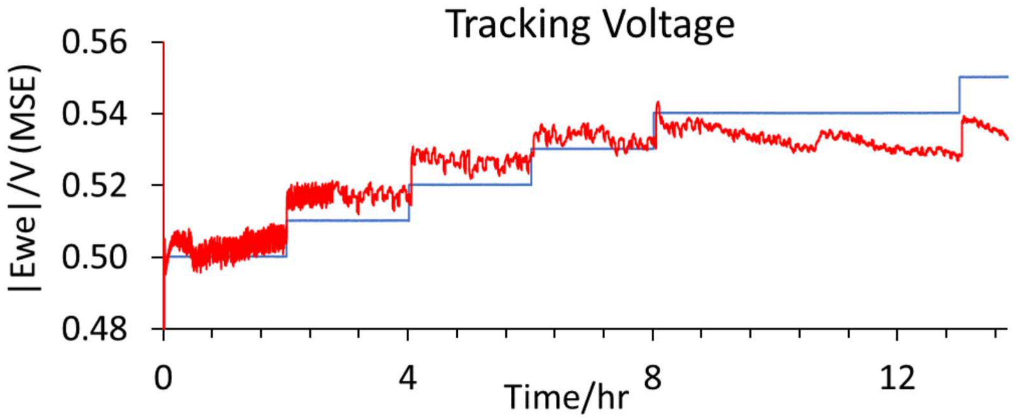
Developing a Current-controlled Filling Solution

→ Take voltage-controlled method and measure current. Use measured current to develop a current- controlled process.



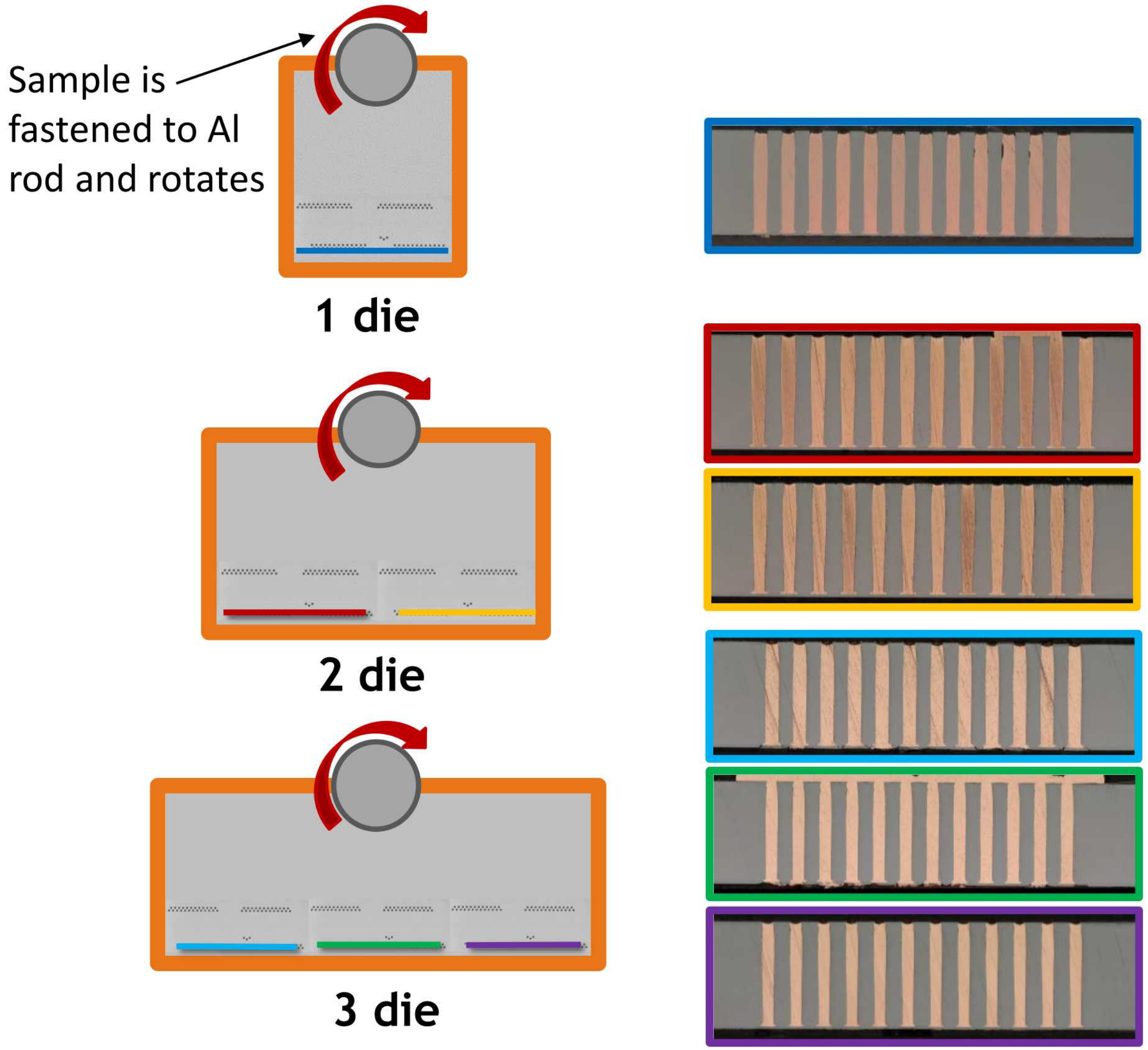


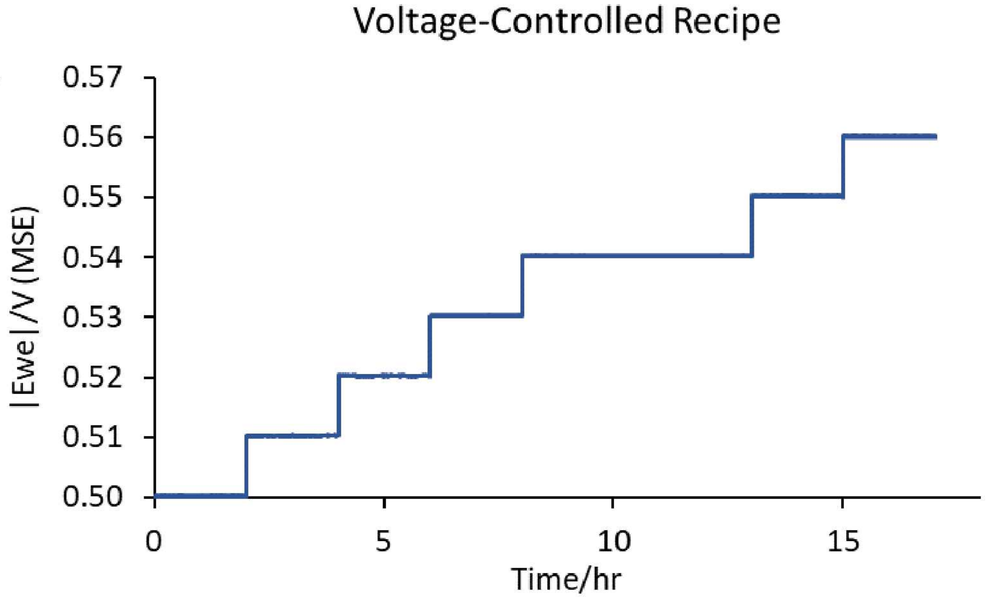
- Current-controlled sample appears to be void-free
- Deposition slower than for voltage-controlled
- For current-controlled deposition, voltage tracks well with the applied voltage recipe

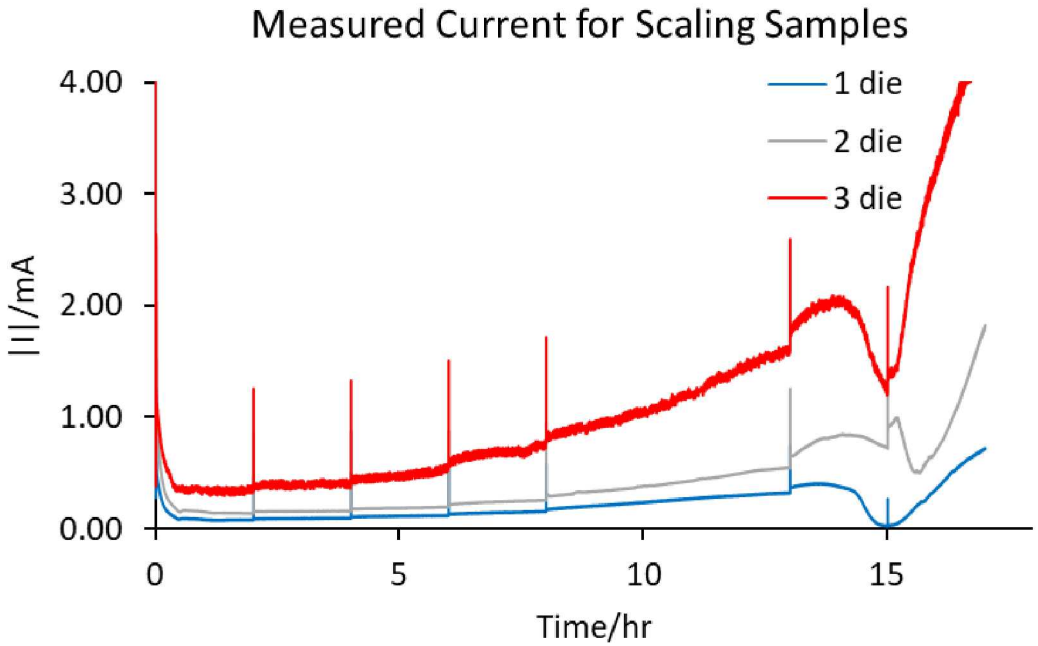


Scaling Die Size for WLP Development

- → Determine required current density profile for plating a full wafer
- → Does current scale with number of vias or conducting surface?

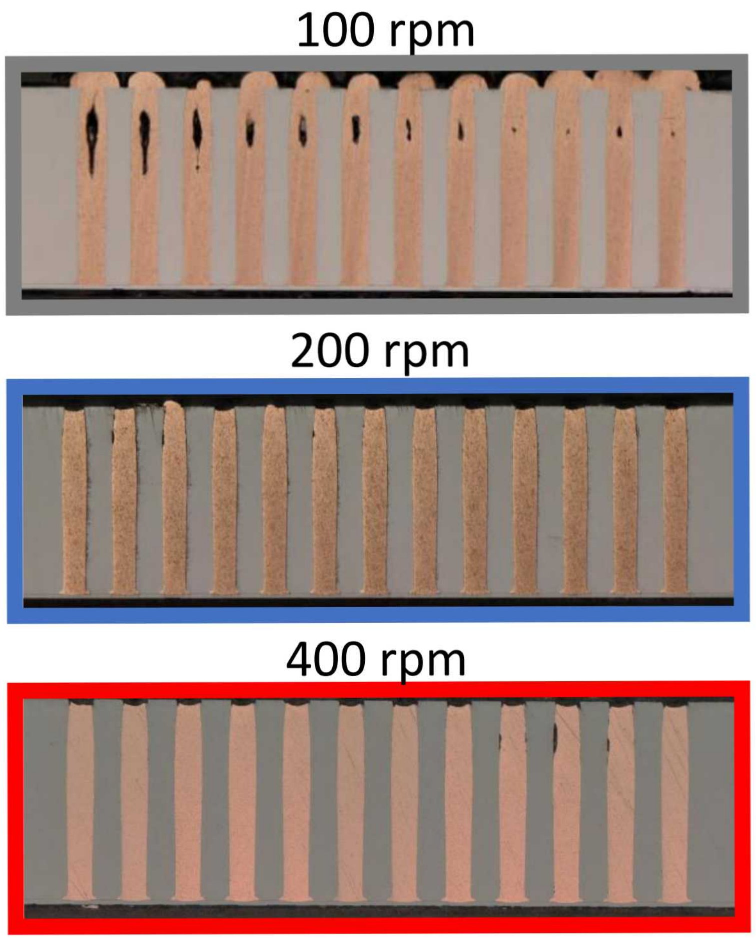


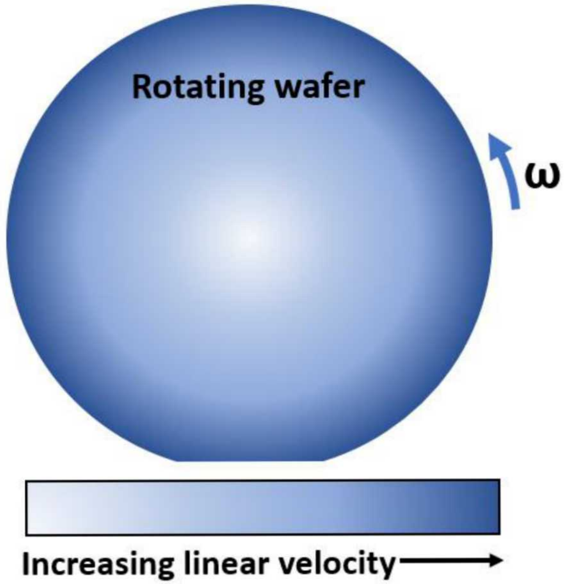


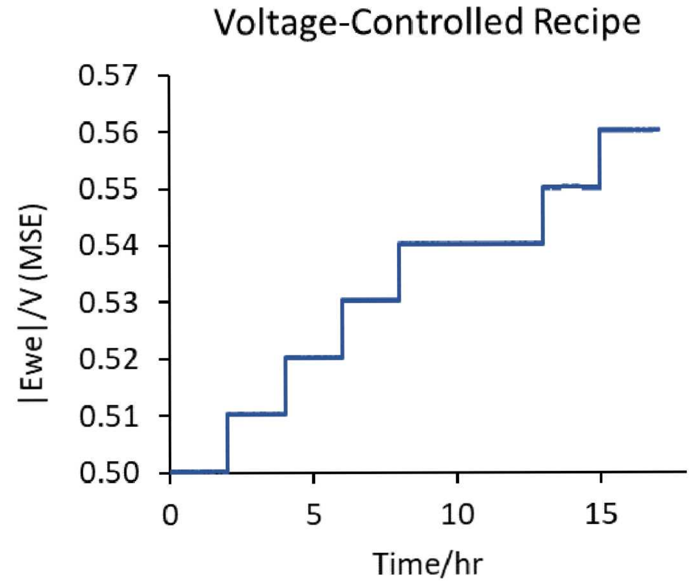


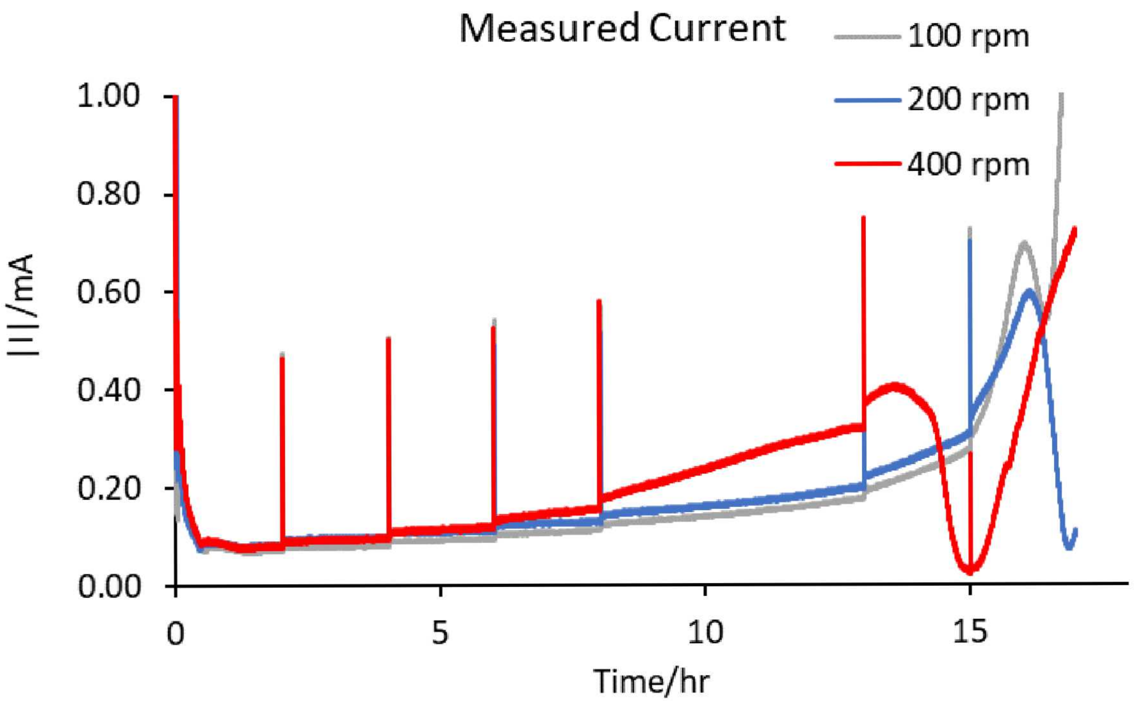
Rotation Rate Experiments

- → Rotate die level samples at different rotation rates to obtain information about fluid velocity relative to TSVs and corresponding TSV fill profiles
- → Mimic these conditions for wafer level plating









Future Work

- → Process tuning and development will continue as we scale the single die, voltage-controlled recipe, performed in a 200 mL plating bath, to a current-controlled, full wafer level process in a 10 L tool.
- → Perform more targeted studies to evaluate if current scales with number of vias or the sample’s total conducting surface.
- → Produce a wafer level plating process for full wafer thickness TSVs for MEMS applications and other microelectronics applications.

Acknowledgements

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Thank you – Questions?

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