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2021 Annual Progress Report

Vehicle Technologies Office

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I Electric Drive Technologies

I.1 Electric Drive Technologies Research

I.1.1 Power Electronics: Vertical GaN Device Development (Sandia National Laboratories)

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Project Introduction

This project is part of a multi-lab consortium that leverages U.S. research expertise and facilities at national labs and universities to significantly advance electric drive power density and reliability, while simultaneously reducing cost. The final objective of the consortium is to develop a 100 kW traction drive system that achieves 33 kW/L, has an operational life of 300,000 miles, and a cost of less than $6/kW. One element of the system is a 100 kW inverter with a power density of 100 kW/L and a cost of $2.7/kW. New materials such as wide-bandgap semiconductors, soft magnetic materials, and ceramic dielectrics, integrated using multi-objective co-optimization design techniques, will be utilized to achieve these program goals. This project focuses on a subset of the power electronics work within the consortium, specifically the design, fabrication, and evaluation of vertical GaN power devices suitable for automotive applications.

Objectives

Gallium Nitride (GaN) is a promising wide-bandgap (WBG) semiconductor material that could enable higher-performance power electronic devices than traditional Silicon (Si) or even its WBG counterpart, Silicon Carbide (SiC). This is based on the increased critical electric field of GaN, which would enable lower-resistance devices with the same hold-off voltage as devices fabricated from the other materials. This is a key performance metric for power devices. Laterally-oriented, High Electron Mobility Transistors (HEMTs) based on AlGaN and GaN materials are common in high-frequency applications and are being established in lower-voltage power switching applications (approximately 600 V and below). However, with the emerging commercial maturation of GaN substrates, traditional vertically-oriented device structures (such as are common in Si and SiC) can now be realized in GaN, with several promising demonstrations of high-voltage pn diodes and vertical transistors appearing in the literature [1], [2], [3]. While GaN pn diodes may be of interest, the ~3 V turn-on voltage, determined mainly by the bandgap of the material, discourages their use in some power-switching circuits due to the loss of power conversion efficiency resulting from this high turn-on voltage. Instead, more promising candidates for these power conversion systems, including automotive inverters, are GaN Schottky barrier diodes (SBDs) and Junction Barrier Schottky (JBS) diodes, shown in Figure I.1.1.1 (a), which have turn on voltages of ~1 V as determined by the Schottky barrier height of the metal to the semiconductor material, rather than the semiconductor bandgap.

Similarly, vertically-oriented GaN transistors promise high-performance as power electronic devices if several key growth and fabrication challenges are overcome for the GaN material system. Interestingly, several different types of vertical GaN transistors have been demonstrated including Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) in the trench configuration (T-MOSFET, shown in Figure I.1.1.1 b), the double-well

(D-MOSFET) configuration (shown in Figure I.1.1.1 c), and the Current Aperture Vertical Electron Transistor (CAVET) configuration [4], [5], [6]. Each of these device topologies has benefits and challenges associated with fabrication and performance, but the MOSFET designs show the most promise for power switching applications and are being investigated during this effort. With the MOSFET device designs, challenges exist in making the semiconductor/insulator (or oxide) interface due to the lack of a good native oxide for GaN (Si and SiC both have native oxides). In addition, selective-area doping control, which is needed to form lateral pn junctions, cannot be easily achieved in GaN. Current state-of-the-art GaN devices use techniques such as ion implantation with special anneal processes (high-pressure and high-temperature) [7] or epitaxial regrowth [8] to realize selective-area doping control. Both techniques are relatively immature in GaN, and their behavior needs to be studied and techniques need to be developed to control these processes for eventual use in power systems for electric vehicles.

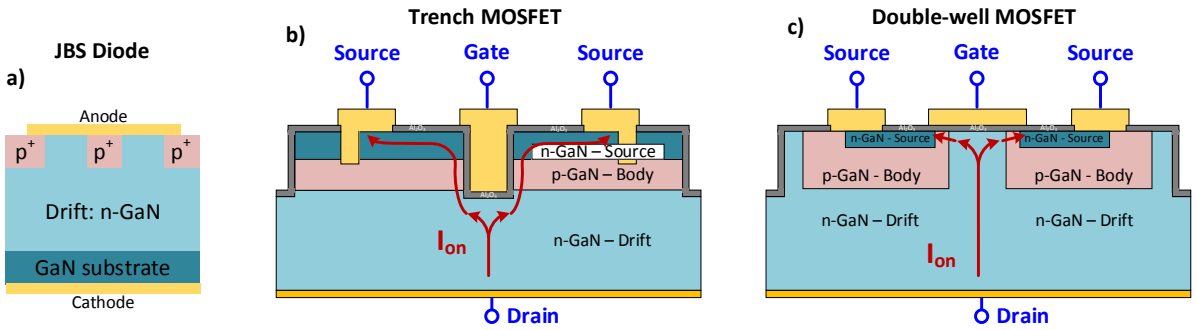

Figure I.1.1.1. (a) Schematic drawing of JBS diode, (b) schematic drawing of Trench MOSFET, and (c) schematic drawing of a Double-well MOSFET.

The first year of this effort focused on the development of simulation and modeling capabilities to help drive the designs of future GaN diodes and transistors. In parallel, epitaxial growth and fabrication processes were initiated toward realizing and demonstrating these devices. The second year of this effort has focused on fabrication and a first-generation demonstration of these devices. With demonstrators for both the JBS and trench MOSFET complete, the third year of the program (this year) focused on improving the baseline performance. This year's focus included iterating to improve passivation quality, tackling challenges related to etch-and-regrowth, and improving off-state characteristics for both the JBS and MOSFET devices. In the future, once devices of sufficient performance are achieved these will be further characterized in a performance and reliability test-bed (created under a different project within the consortium) to evaluate their suitability for electric drive applications, especially regarding their ability to meet the DOE consortium targets. Also, with increasing maturity, the devices can be shared with the consortium partners, who will evaluate them in electric drive systems and provide feedback to us for further improvement in their performance for power electronics.

Approach

The focus of this past year has been on improving baseline performance for both the JBS and MOSFET device. In many cases, challenges faced by both devices can more easily be addressed through cycles of learning on a simpler device. For instance, the pn diode platform can be used to benchmark passivation quality and to evaluate edge termination effectiveness, a simple Schottky Barrier diode can be used to understand the influence of etch damage and etch-damage recovery procedures on n-type GaN, and the MOSCAP can be used to evaluate gate dielectric performance on m-plane GaN. Experiments on these three devices were heavily leveraged in the past year to improve device performance for the JBS and MOSFET platforms. Examples of the three devices are shown in Figure I.1.1.2.

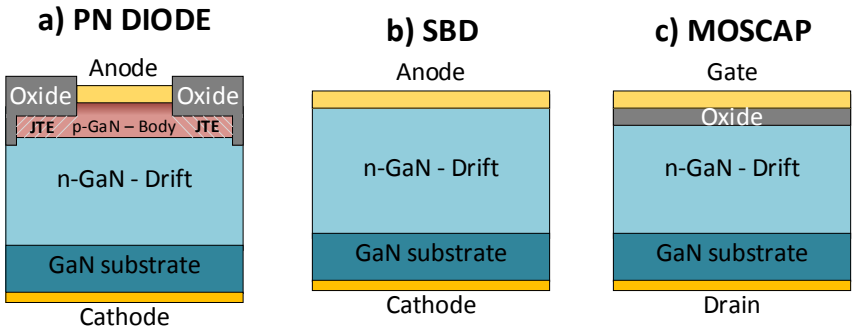

Figure I.1.1.2. Studies on these three devices, the pn diode, the Schottky Barrier diode, and the MOSCAP lends insight into improving performance for the JBS and MOSFET devices.

Results

Vertical GaN PN Diodes

Previous results from the JBS demonstrator indicated that issues with the etch-and-regrowth process and issues with the passivation process contributed substantially to the leakage current in reverse bias. To address the issues related to the passivation we conducted a set of passivation experiments on the pn diode platform. Although the passivation serves many roles when examining device reliability, our initial metric is to create a passivation that does not contribute a substantial leakage current to the device. In order to assess the quality of the passivation, and the impact to reverse leakage current, it is necessary first to establish a known-good pn diode process. To do this we took the JBS process and eliminated the steps related to etch-and-regrowth which then yields a pn diode rather than a JBS diode. This baseline pn diode structure is depicted in Figure I.1.1.3a and is comprised of a single-zone step etched JTE and a 1-2kV drift epi design. From this simplified process we have been able to consistently demonstrate noise-floor level reverse leakage characteristics for unpassivated pn diodes across multiple device lots (see the black curves in Figure I.1.1.3 b & c). This demonstrates the effectiveness of our edge termination scheme, and our ability to make quality high-voltage, low reverse-leakage pn diodes.

Using this platform, various passivation films have been evaluated in regard to the impact on reverse IV performance. Our early experiments with an electron-beam deposited SiO_2 film (500 nm thick) showed a

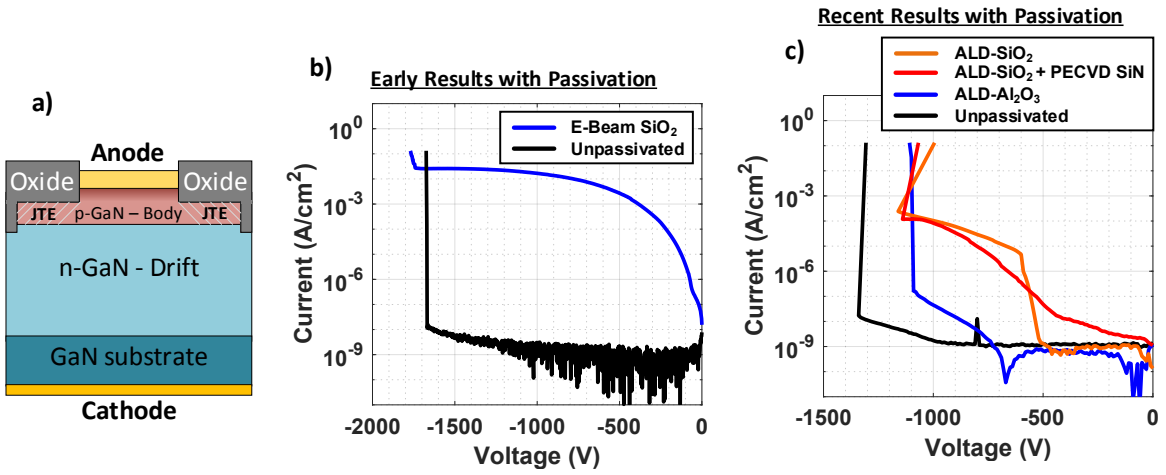

Figure I.1.1.3. Sandia's recent progress for GaN passivations. Using a pn diode (a) to test passivated and unpassivated devices (b) showing how poor passivation can result in substantial leakage currents. Recent passivation results for atomic layer deposited films (c) look promising for realizing low leakage pn diodes. Note, all devices are tested under flourinert during high voltage testing.

substantial increase in reverse-leakage current compared to our baseline unpassivated devices on a sister-wafer (Figure I.1.1.3b). This serves as an example of how a poor passivation process can have a dramatic impact on diode performance. Our recent work with thermal atomic layer deposited films (Figure I.1.1.3c) shows that the ALD-Al_2O_3 film (100 nm thick) has noise-floor level leakage current in reverse out to a few hundred volts before breakdown. The results presented in Figure I.1.1.3c are each from separate quarter-wafer pieces from the same wafer. Some doping variations are expected across the wafer, so absolute breakdown results are also expected to shift from one quarter to another.

We are working to establish a bi-layer passivation process to create a substantially thick passivation film. Our prime candidate at this time is a bi-layer ALD-Al_2O_3 (100 nm) + PECVD-SiN (thickness TBD) film. Previous experience at Sandia with PECVD films on GaN demonstrated considerably high leakage currents under high reverse bias which may be the result of unwanted plasma damage to the surface from the PECVD process. This drives the desire to have an intermediate dielectric layer between the GaN surface and the substantially thick PECVD film. Once a baseline passivation process can be established (one that does not add significantly to reverse leakage), more work should be undertaken regarding long term reliability of these films, especially related to stress from high humidity and high temperature.

Passivation induced leakage current was a major contributor to the leakage current seen in the JBS devices [9] and the ability to make quality passivated pn diodes is a step in the right direction towards making low leakage JBS devices.

Vertical GaN Schottky Barrier Diodes

The impact of etch-induced-damage on the n-type Schottky contact can be more easily quantified by evaluating a Schottky Barrier diode (SBD) rather than experimenting directly on the JBS diode. The etch-and-regrowth process and subsequent etch-back steps are critical pieces in the JBS process flow and solving the challenges involved in these processes is the most difficult piece of making a GaN JBS diode. We have made great progress in this past year towards developing an etch-damage-recovery process for improving the performance of Schottky contacts on etched n-type GaN. The baseline structure for evaluating the impact of etch-damage and recovery techniques is a simple SBD structure as represented in Figure I.1.1.5a. With this structure we can demonstrate a baseline undamaged SBD with near noise floor level reverse leakage current out to -100 V bias. In contrast, the etch damaged device shows a large initial leakage current near the zero-bias point, and a larger leakage slope leading to an increase in leakage current of five orders of magnitude by the -100 V bias point. This is a great example of just how much etch-damage can influence the diode characteristics. To remedy this problem, we are evaluating several etch-damage-recovery techniques that show promise for recovering the noise floor out to -20 or -40 V bias, and can reduce the leakage at -100 V by two orders of magnitude compared to the untreated (etch-damaged) sample. These results are presented in Figure I.1.1.5b.

The ability to recover an etch-damaged surface is a major step towards making low leakage etched-and-regrown JBS devices. In this next year we plan to study the impact of our recovery techniques on etched-and-regrown pn diodes, and we also will be testing these techniques on the full JBS device. Further information on the state of the JBS progress can be found in Ref. [9].

Vertical GaN MOSCAPs

In the past year we have demonstrated a 1st generation process for vertical GaN trench MOSFETs, and our goal is to improve on that baseline by reducing the off-state leakage current and increasing the blocking voltage limit. The three major aspects we are concerned with are improving the passivation quality to reduce passivation related leakage current, improving the gate trench etch and etch-damage removal processes, and improving the quality of the gate dielectric and the dielectric/semiconductor interface. The first two items we have already discussed (improving passivation and improving etch-damage-removal processes), the last item we will address here.

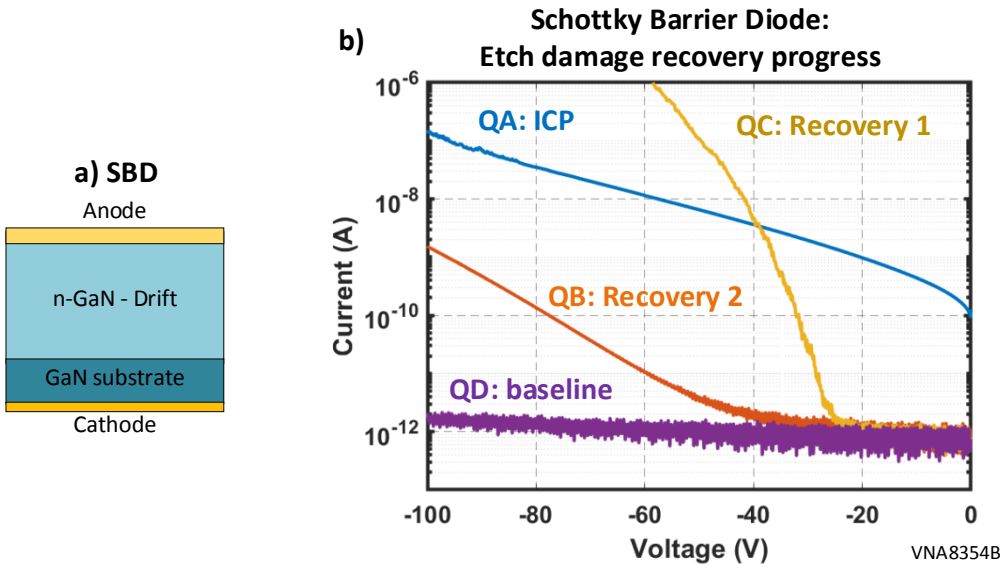

Figure I.1.1.5. Sandia's progress towards developing an etch-damage-recovery process for treating ICP-etch-damaged n-type GaN. The SBD baseline structure (a) consists of a shadow-mask evaporated Pd/Au Schottky contact on n-type GaN. The baseline device (QD) has no etch damage, the other three samples are etch-damaged with QB and QC having different etch-damage-recovery processes prior to metallization. Results of the experiment (b) show good progress towards developing an etch-damage-recovery process that can recover the noise floor and reduce leakage current at higher voltages.

Improving the gate dielectric is a complex process with a lot of knobs to turn. Our most promising gate dielectrics have been atomic layer deposited (ALD) films. Films deposited by ALD are generally very high quality making this a favorable method for depositing non-native oxides. In this past year we have focused primarily on developing ALD-SiO_2 and ALD-Al_2O_3 films for use as the MOSFET gate dielectric. These films have also shown good success in operating as the first layer in a bi-layer passivation used on pn diodes as we discussed

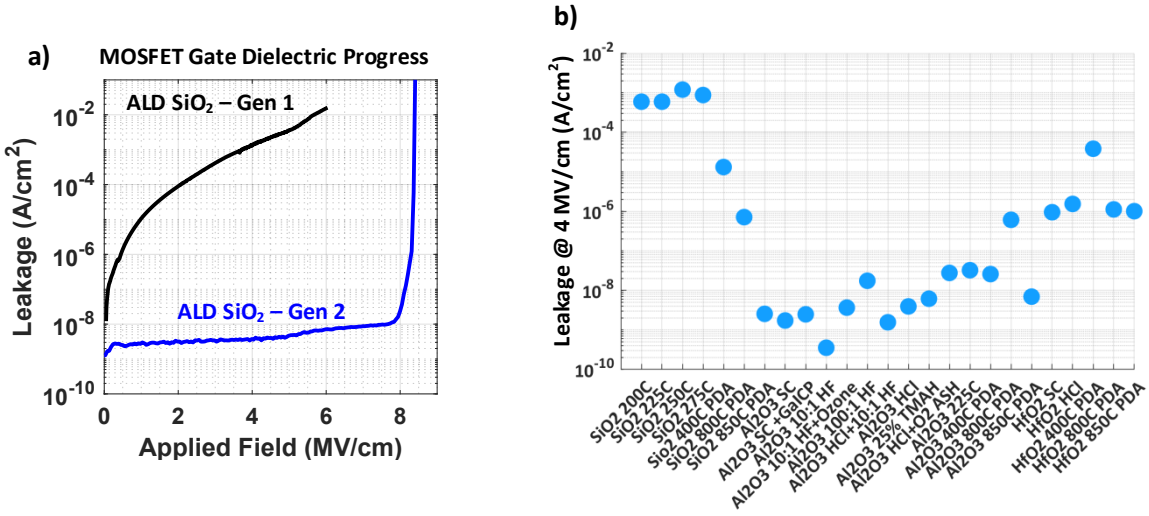

Figure I.1.1.4. Examples of our recent progress on GaN dielectrics showing (a) the improvement made from our first-generation SiO_2 process to the second-generation film, and (b) the static leakage performance of a large variety of different thin-film processes and surface treatment techniques for establishing a successful gate dielectric process on GaN.

earlier in this report (see Figure I.1.1.3). Substantial progress has been made especially for improving the leakage characteristics and dielectric strength of our ALD-SiO_2 film by adding a high temperature post deposition anneal. Leakage performance comparing the first-generation film to the second-generation film with a post deposition anneal are shown in Figure I.1.1.4a.

The relationship between the dielectric and semiconductor interface plays a critical role in the dynamic behavior of a MOS device, and therefore the conditioning of the interface prior to depositing the dielectric needs special care. We have conducted a large survey of surface treatment options and performed experiments to assess the impact of surface treatments on both static and dynamic performance of MOSCAPs. A summary of some of the static characteristics can be found briefly in Figure I.1.1.4b. More details on our GaN dielectric study can be found in Ref. [10].

Conclusions

GaN offers the promise of power electronic devices with performance that exceeds conventional Si and even SiC-based devices. This is due to its advantageous material properties, chiefly its higher breakdown electric field. Due to the increased maturity of GaN substrates, vertical GaN devices showing promising performance are being demonstrated and are being considered for insertion into power conversion applications. This project has focused on the design, simulation, and fabrication processes needed to build vertical GaN diodes and transistors for use in electric drive traction systems. Following the successful demonstration of a JBS device and a trench MOSFET in the past year, this year's work has focused on improving the baseline performance of these devices. Substantial progress has been made developing an improved passivation process, developing etch-damage-removal processes, and improving our gate dielectric process. The improved passivation process as well as the new etch-damage-removal techniques look promising for reducing the leakage current on the JBS device. In the next year we plan to continue to improve our baseline performance and we are pushing closer towards test-bed evaluation of some of our devices. The progress on passivation in this past year should enable us to start packaging devices in the near future for better collaboration with the circuits and systems team.

Key Publications

1. A. T. Binder *et al*., "Etched and Regrown Vertical GaN Junction Barrier Schottky Diodes," in *The 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2021),* 2021.
2. C. E. Glaser, A. T. Binder, L. Yates, A. A. Allerman, D. F. Feezell, and R. J. Kaplar, "Analysis of ALD Dielectric Leakage in Bulk GaN MOS Devices," in *The 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2021),* 2021.
3. L. Yates, A. Binder, J. Dickerson, G. Pickrell, and R. Kaplar, "Electro-thermal Simulation and Performance Comparison of 1.2 kV, 10 A Vertical GaN MOSFETs," Rio Grande Symposium on Advanced Materials, Albuquerque, NM (September 2019).

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[9] A. T. Binder *et al*., "Etched and Regrown Vertical GaN Junction Barrier Schottky Diodes," in *The 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2021)*, 2021.
[10] C. E. Glaser, A. T. Binder, L. Yates, A. A. Allerman, D. F. Feezell, and R. J. Kaplar, "Analysis of ALD Dielectric Leakage in Bulk GaN MOS Devices," in *The 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2021)*, 2021.

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