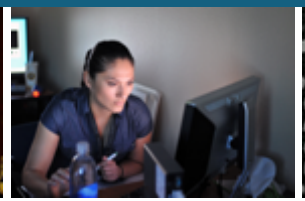
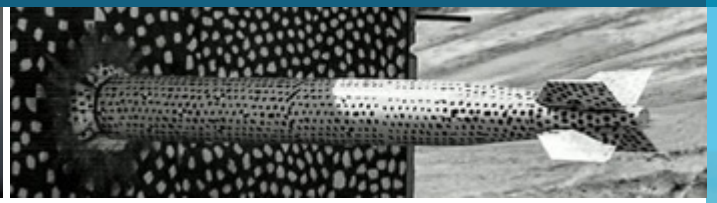
SAND2020-12548C

Sandia National Laboratories

Low-Temperature Processing for Atomically Precise Dopant Incorporation with CMOS Integration





Presented by:

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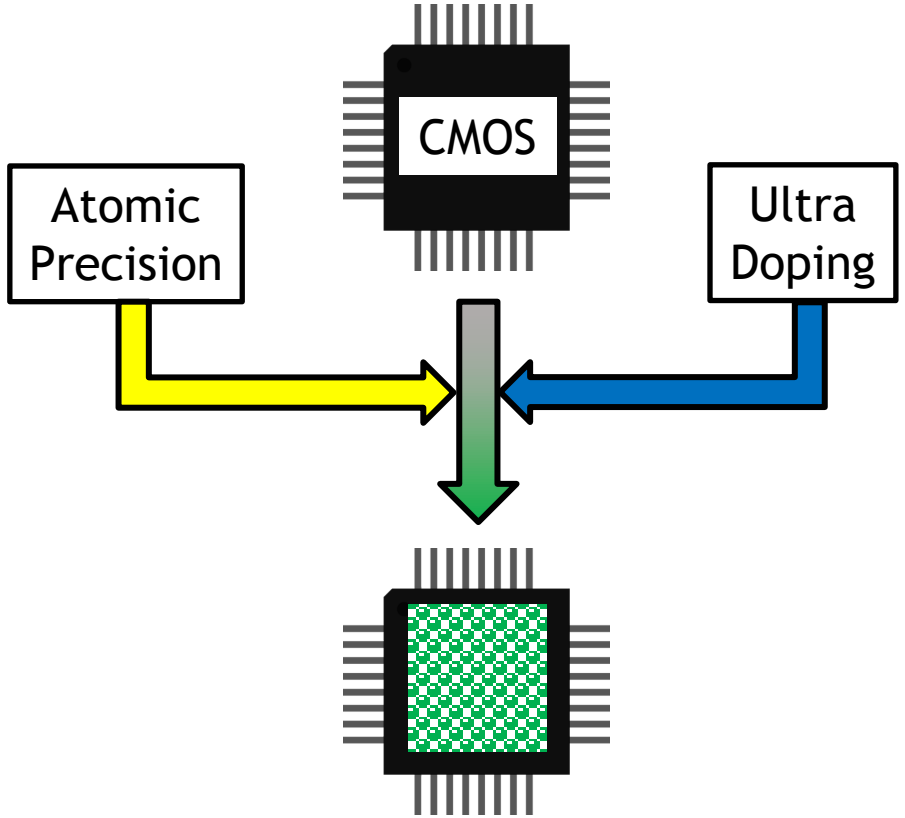
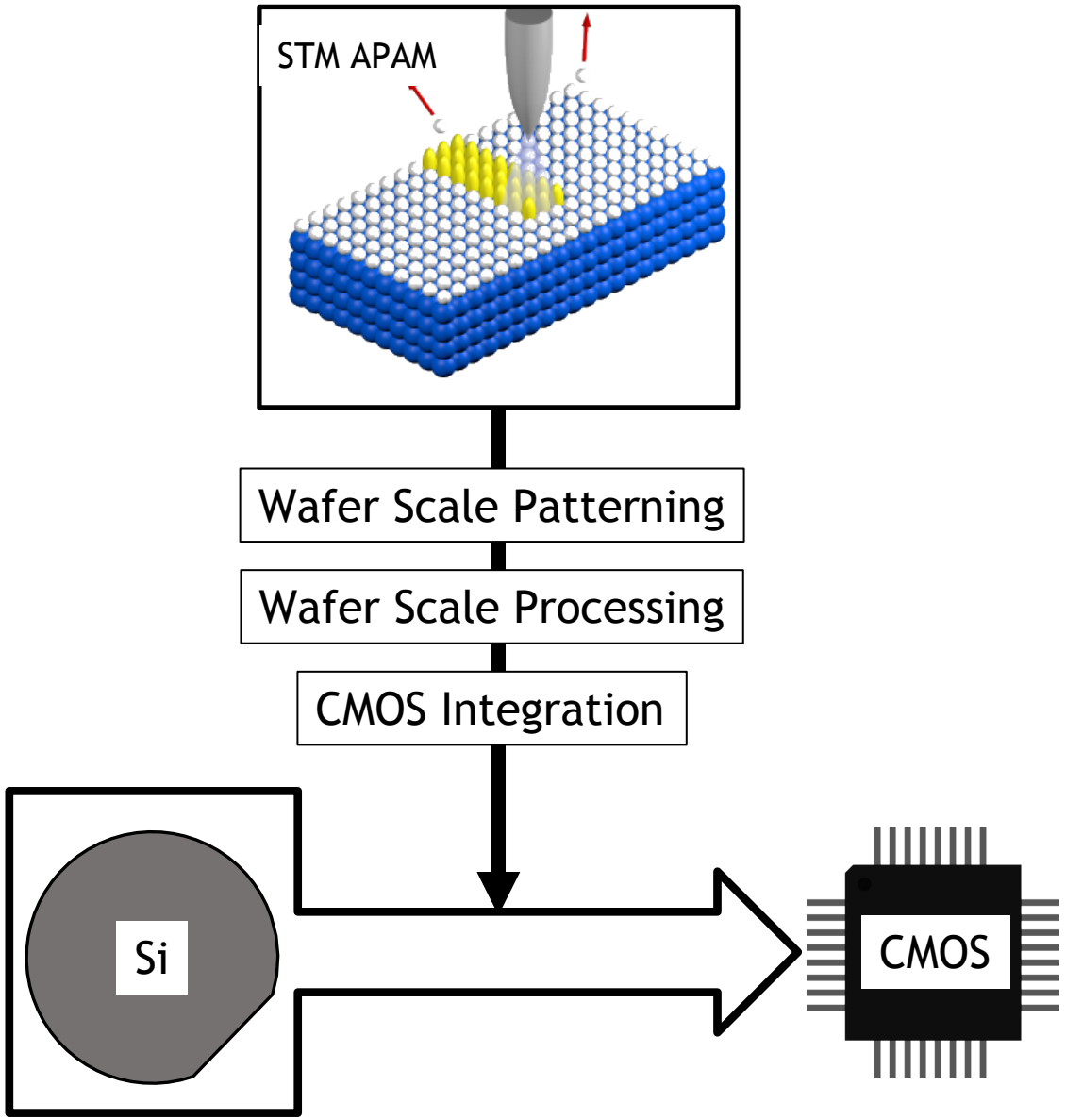
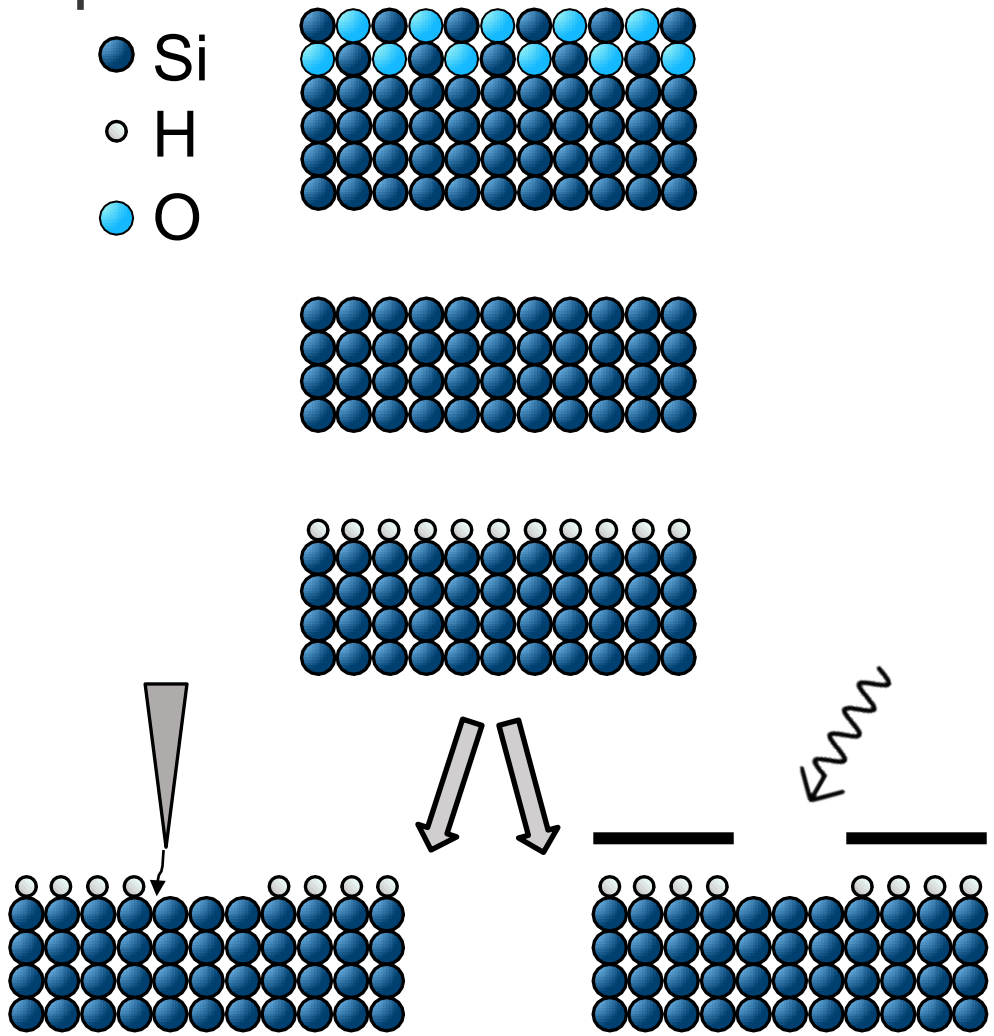
Motivation

CMOS + Atomic Precision + Ultra-Doping
→ New Capabilities

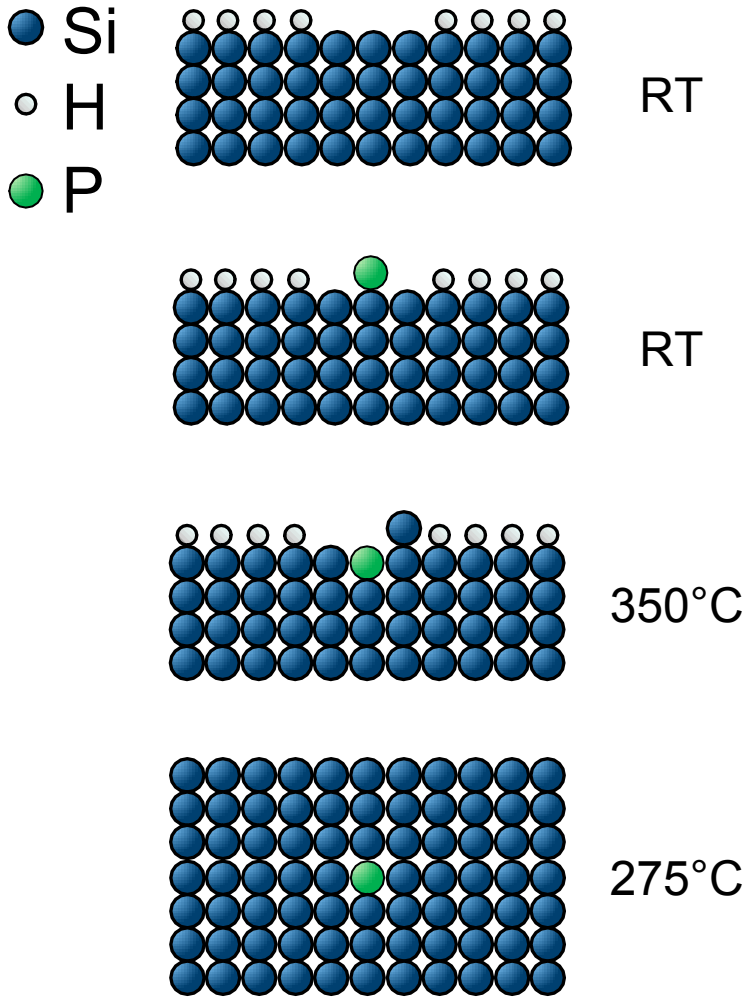




Atomic Precision Advanced Manufacturing → Novel Capabilities



Patterned Dopant Chemisorption and Incorporation

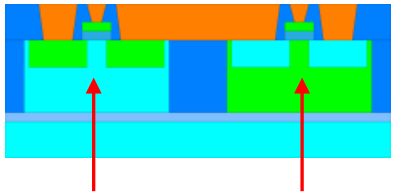


J.W. Lyding et al. Appl. Phys. Lett. 64, 2010 (1994)
D.R. Ward et al. EDFA Magazine, 22 1:4-10 (2020)
A.M. Katzenmeyer et al. Proc. SPIE Adv. Litho. (2020)

FEOL/BEOL Integration – Where can we insert APAM?

CMOS

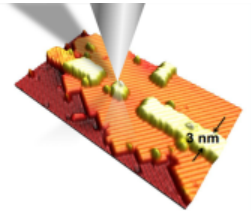
Front end of line (FEOL)



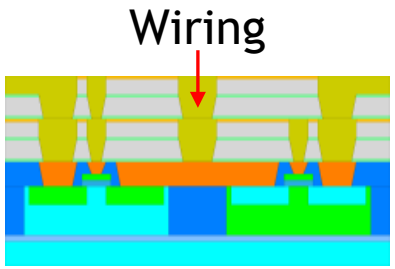
Transistors

- Implants/activation
- Temps >850°C

APAM Direct Integration

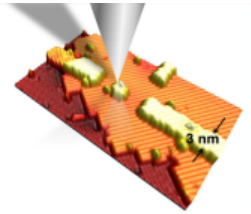


Back end of line (BEOL)



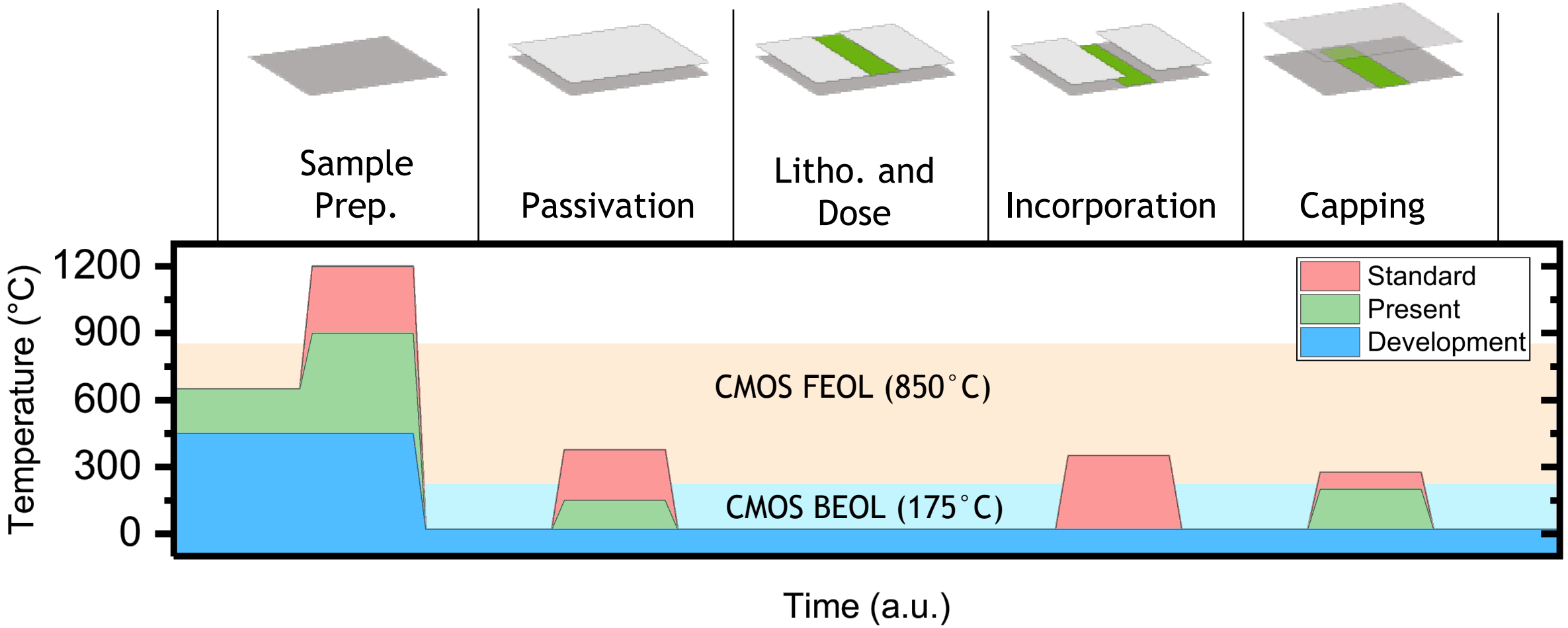
- Metal lines
- Max temp: 450°C
- Ideal: <175°C

APAM Post-CMOS Integration

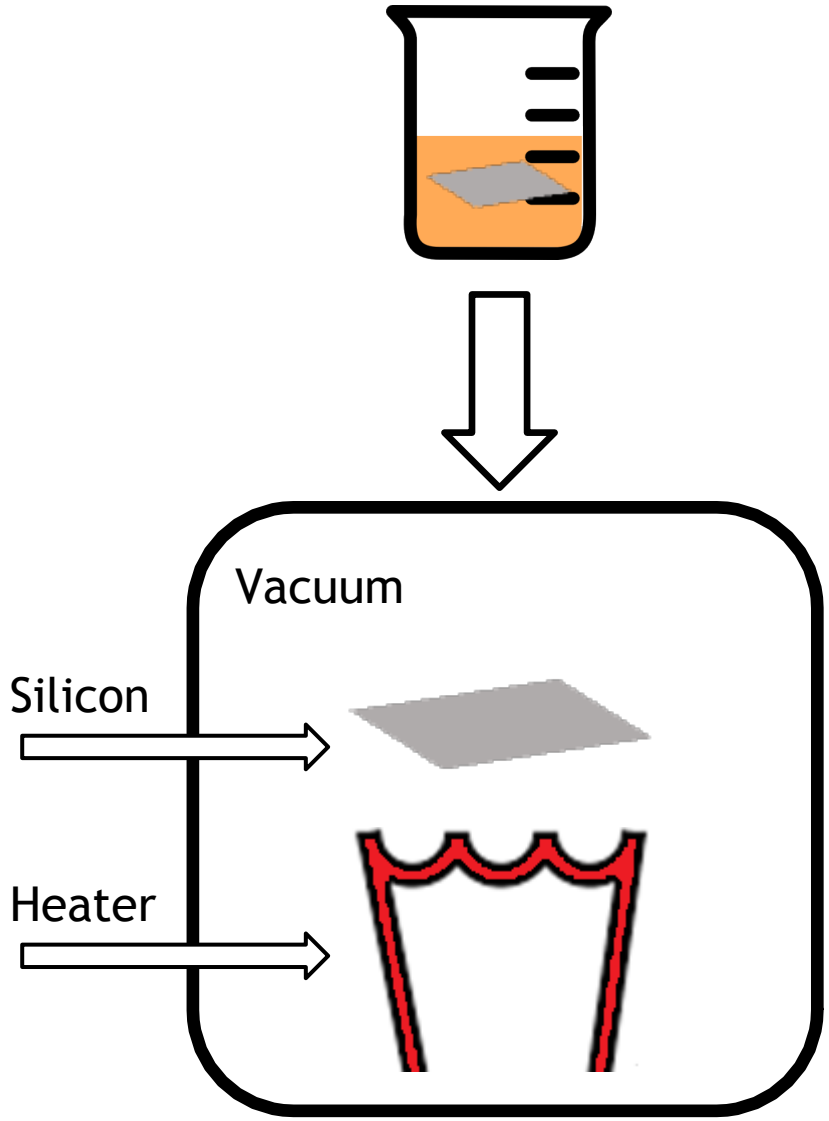


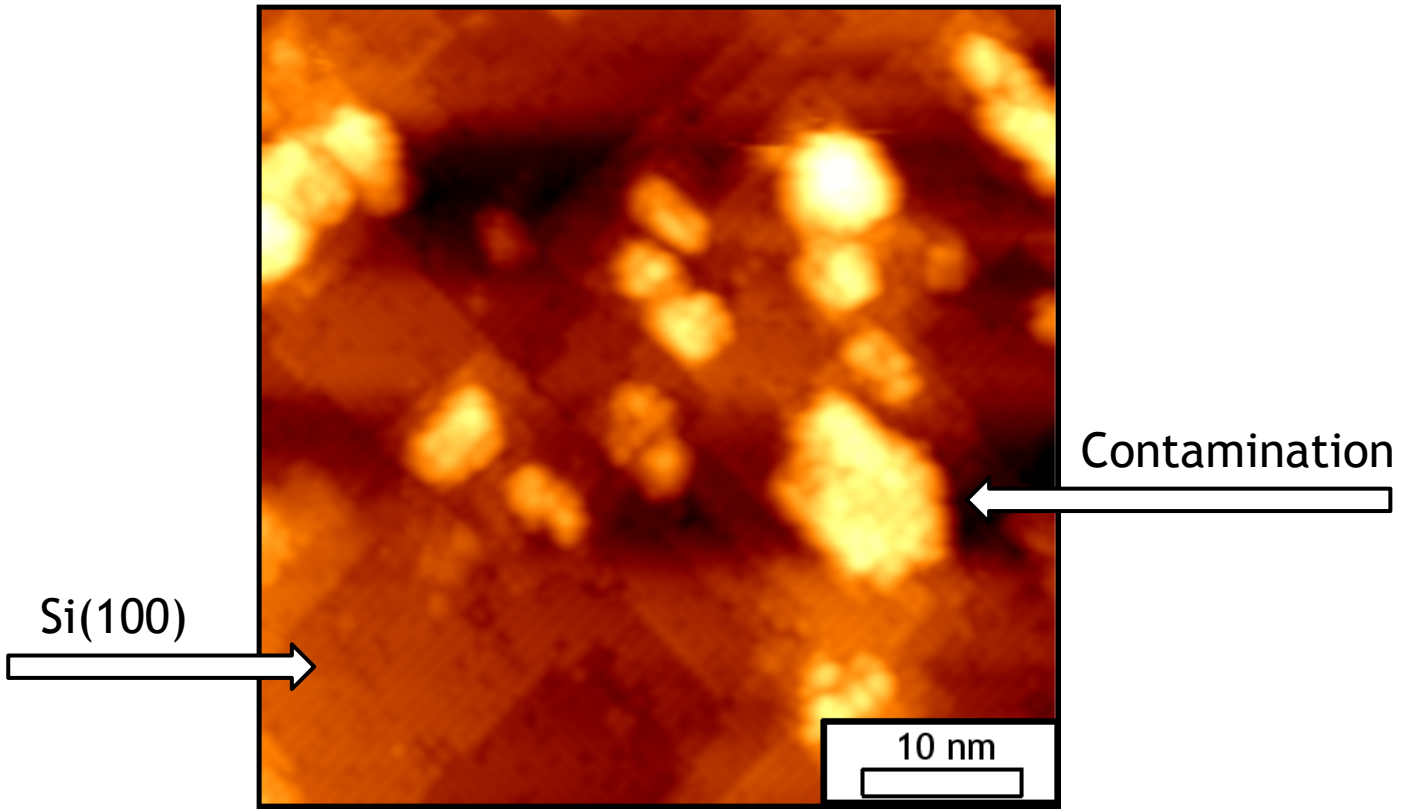
FEOL = high temperature steps, BEOL = low temperature steps

Thermal Budget and APAM Processing



Low-Temperature Sample Preparation – Wet Chemistry

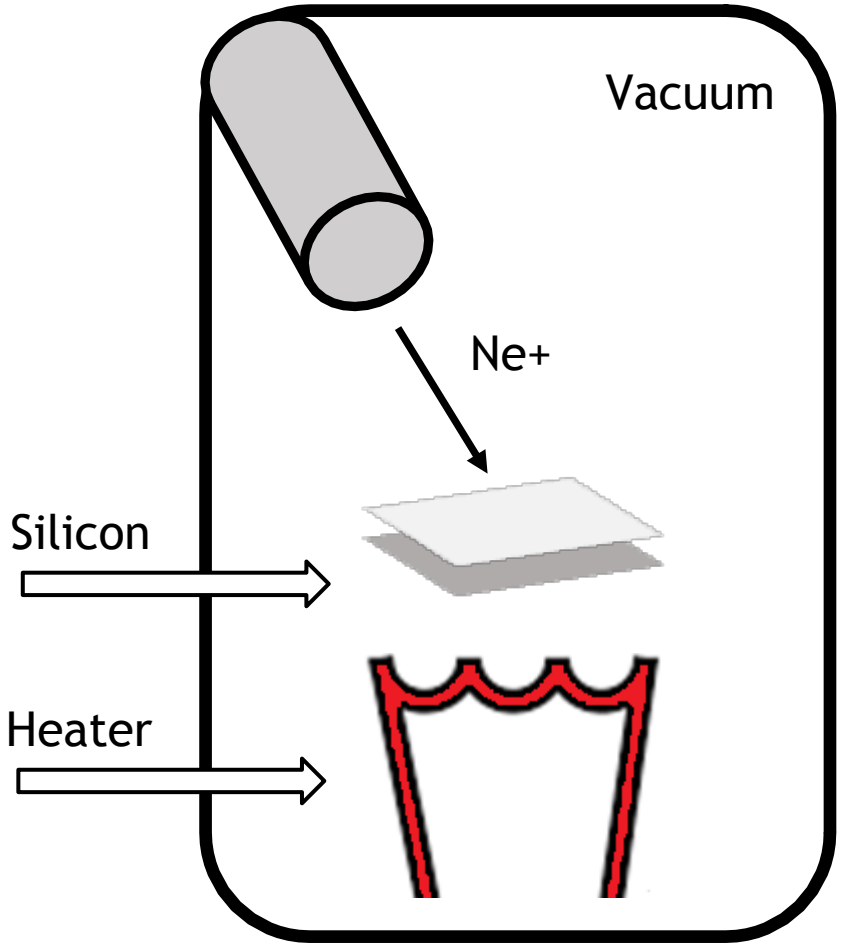


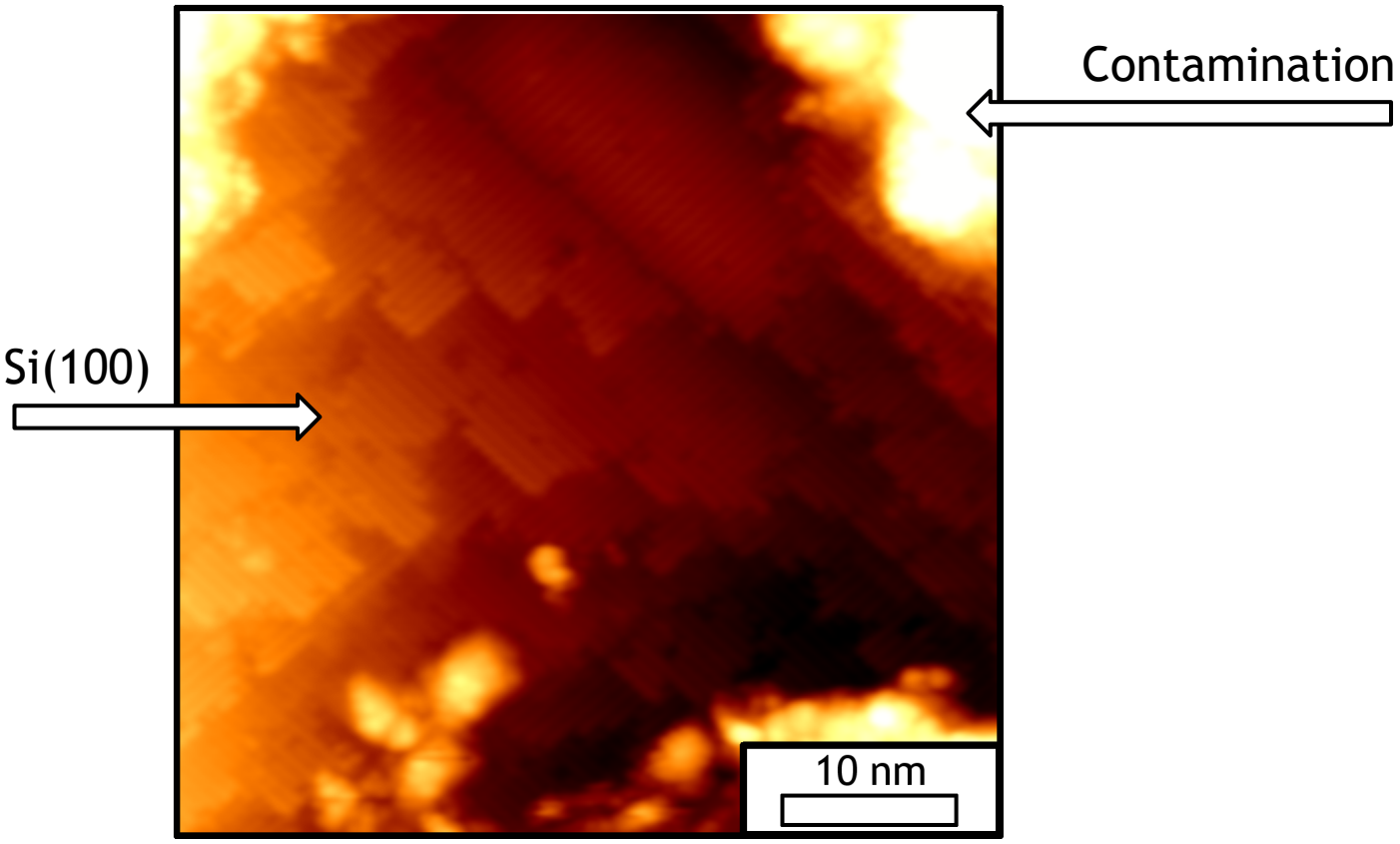


NH_4F-etch, 700°C *in situ* anneal

Hines Etch: I.T. Clark et al., J. Phys. Chem. C 114, 423(2010)

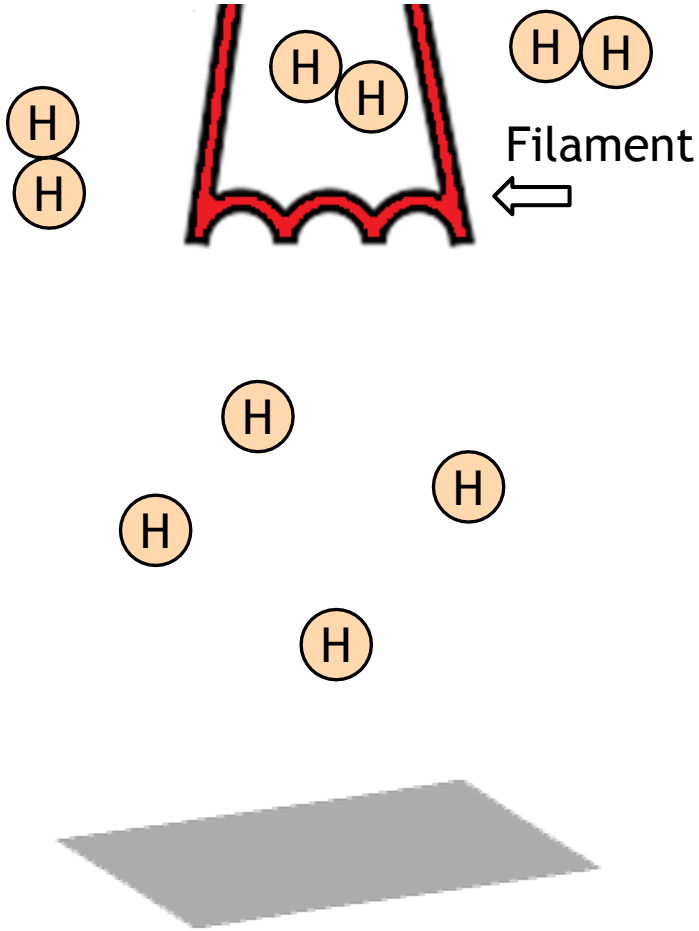
Low-Temperature Sample Preparation – Sputter Cleaning



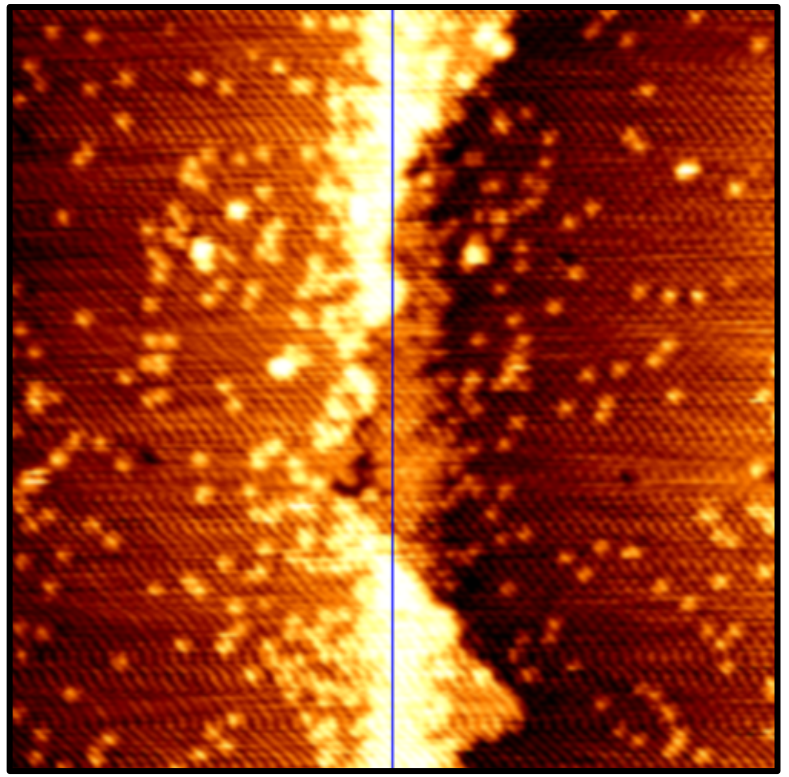


200 eV Ne ion milling ~ 700°C

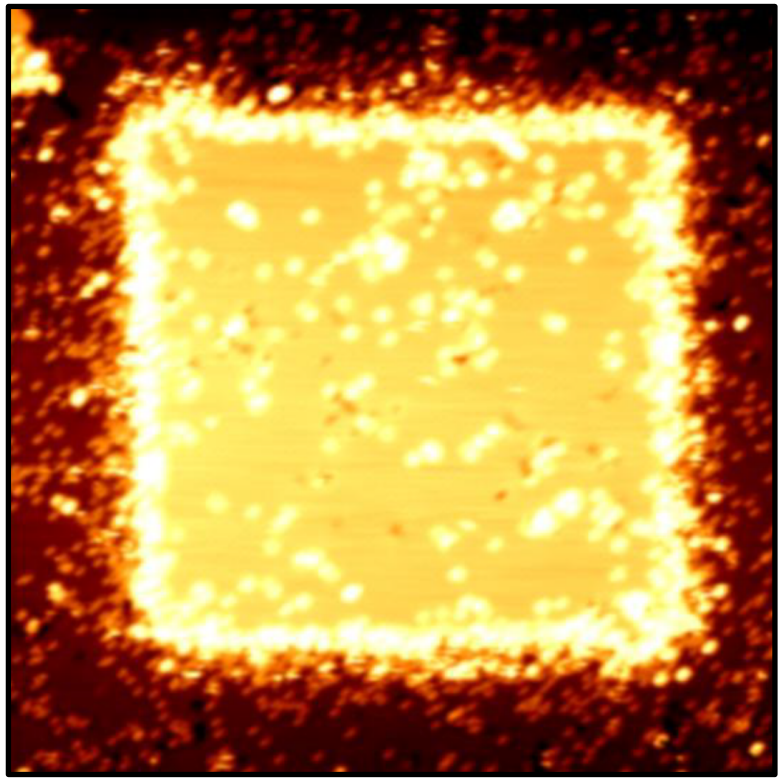
Low-Temperature Hydrogen Passivation



Sample unheated, beyond radiative filament heat. Est. T >125°C



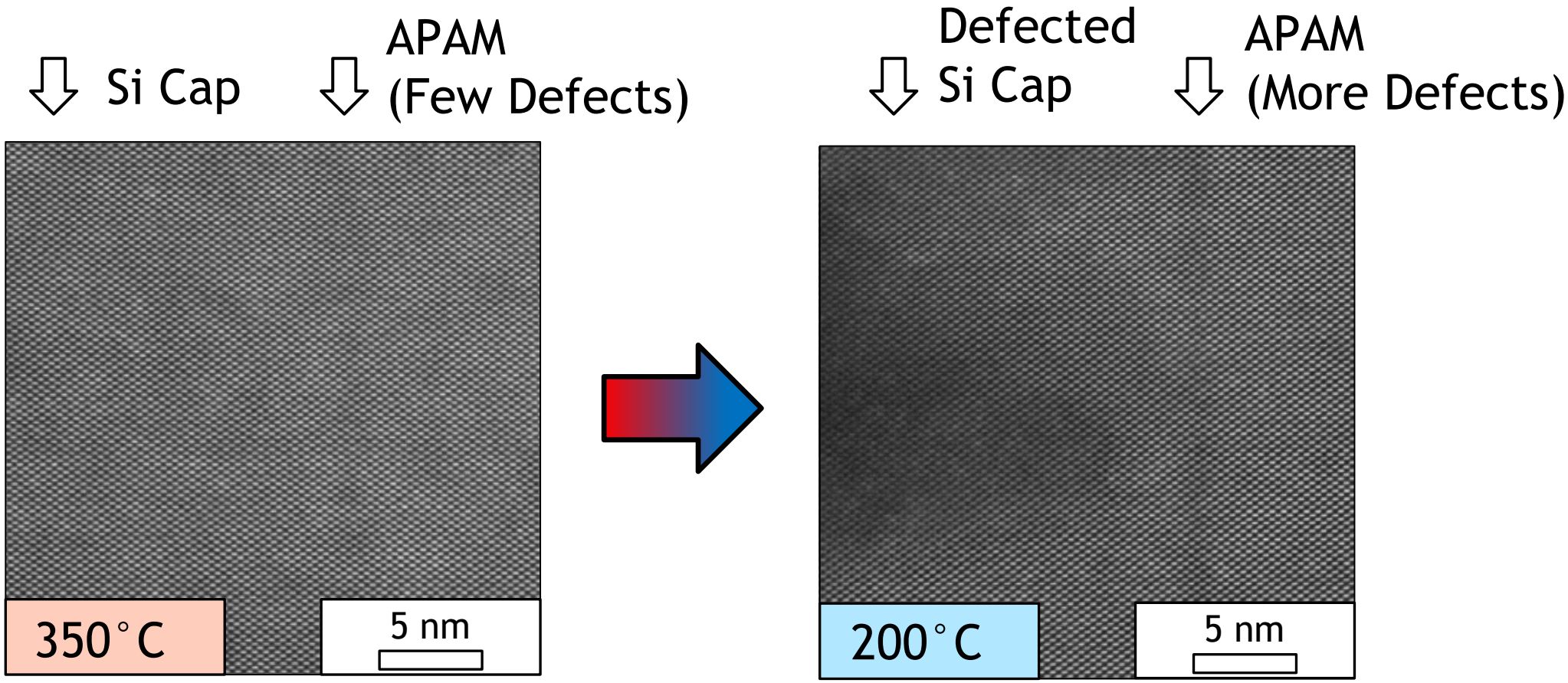
Si(100) 2×1:H, Litho



Si(100) 2×1 after multiple lithographic passes

Cheng et al., PRB (1991) → Lower T = Si(100) 3×1 surface
O'Brien et al., Proc. SPIE 4590 (2001) → APAM process compatibility with Si(100) 3×1

Low-Temperature Limited-Thickness Silicon Epitaxy



$n \sim 1.7 \times 10^{14}$ cm^{-2}
$\mu \sim 50$ cm^2/V-s
$\sigma \sim 2$ mS/sq.

Electrical transport at 4K not significantly impacted

$n \sim 1.4 \times 10^{14}$ cm^{-2}
$\mu \sim 20$ cm^2/V-s
$\sigma \sim 0.6$ mS/sq.

Limited Thickness Epitaxy: D.J. Eaglesham et al., J. Cryst. Growth 111, 833 (1991)

What are the next steps?

Sample Prep. | Passivation | Litho. and Dose | Incorporation | Capping

- **So far: explore each step in isolation. Next: merge these steps together into a full low-temperature process flow**
- **So far: standard silicon blanks. Next: processing on actual CMOS parts.**
- **Ongoing Development: Ion milling at lower energies and temperatures**
- **Future Development: Looking for help with wafer scale chemistry**