Monolithic Integration of Lateral HV Power MOSFET with LV CMOS for SiC Power IC Technology

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***Abstract*—This paper reports the design and process flow for monolithic integration of lateral high voltage (HV) power MOSFET with low voltage (LV) CMOS circuits for SiC Power IC technology. The reported devices and circuits are fabricated on a N-/N+ 4H-SiC substrate at 150mm, production grade-Analog Devices Inc. (ADI) Hillview fabrication facility located in San Jose. The static performance characteristics of HV NMOS and LV CMOS are reported. For future high temperature applications, the static performances are fully characterized and are reported up to 200ºC. Finally, to validate the fabricated CMOS, a 5-stage ring oscillator is also demonstrated.**

Keywords— 4H-SiC, lateral MOSFET, RESURF, CMOS, IC

I. Introduction

Silicon has been the go-to material for the power electronic and power system applications. However, limited by its inherent material properties, silicon-based devices have not been able to meet the growing requirements for high voltage and high temperature in today's world. Silicon carbide (SiC) has been regarded as a promising material for the next generation electronic applications. Recent advancements in device processing and designs have enabled commercial production of SiC power MOSFETs, JFETs and BJTs showing improved device performances.

Apart from the usual applications of SiC HV discrete power devices, SiC offers tremendous potential for power integrated circuits to operate at elevated temperatures and power ratings with lower losses when compared to its Si counterparts. SiC power ICs have potential applications in HV power management ICs, DC-DC converters for distributed power resource systems, on-board charging for electric vehicles (EV's), power supplies for high performance servers and battery management ICs. In today's world, the discrete SiC power devices are driven by Si ICs. To completely exploit the attributes of the 4H-SiC, there is a need for a fully integrated SiC based power electronic systems with the power switch to reduce the losses, size, and cost.

Unlike the popular vertical architecture, SiC power IC technology demands lateral architecture for the HV power switch. Multiple groups including our group have demonstrated lateral HV power MOSFETs. Our previously demonstrated lateral HV MOSFET outperformed all the previously reported HV MOSFETs [1]. The ultimate goal of this work funded by ARPA-E is to demonstrate a fully integrated HV SiC Power MOSFET ICs [2]. As our initial milestone in reaching that landmark, we report the monolithic integration of HV NMOSFET with LV CMOS circuits in this paper using a single process flow.

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II. Fabrication Process

Fig. 1 shows the cross-section of the fabricated HV NMOS, LV NMOS and LV PMOS structures on a 6-inch N^-/N^+ substrate. The devices are fabricated at the ADI Hillview fabrication facility. A 6 µm thick, 2.5 × 10^{16} cm^{-3} doped N^- drift layer on N^+ substrate was used as the starting material.

Ion-Implantation

Aluminum ion implants were used to form P Well, P^+ source/drain and P top. A 2.5 µm deep P Drift was formed by channeling implantation of Aluminum. Nitrogen ion implants were used to form N Well and N^+ source/drain. Subsequent to ion implantation process, the wafers were annealed at 1650ºC for 10min with carbon cap to activate the implanted aluminum and nitrogen ions.

Gate Oxide and Gate Poly Formation

The gate oxide recipe was optimized to simultaneously achieve maximum electron and hole channel mobilities and superior dielectric quality. A 50 nm thick gate oxide was formed with high temperature CVD oxide. Post Oxidation annealing (POA) was performed for 180 min in N_2O and N_2 atmospheres. Once gate oxide was formed, 0.5 µm gate poly silicon was deposited, doped with phoshphorous and patterned.

Ohmic and Metal layers

Followed by the gate formation, a first interlayer dielectric (ILD-1) of thickness 1µm was deposited and etched for Contact to form ohmic contacts. A single metal (Nickel) was used to simultaneously form the n-type and p-type ohmic contacts. 1000 Å Nickel was deposited on the front side, followed by annealing at 750ºC for 2 min to form Nickel silicide and further annealing at 965ºC for 2 min. Ohmic contact was also formed on the back side of the wafer as well. A 0.5 µm thick Aluminum metal (metal 1) was deposited, patterned, and etched. A second layer of 1.5 µm ILD-2 was deposited followed by planarization using CMP. The ILD-2 was etched for Via and filled with W-based metal. Topside metal of 4.5 µm thick Aluminum (metal 2) was deposited, patterned, and etched. Finally, the surface was passivated by silicon nitride and polyimide.

III. Electrical Charateristics of Devices and Circuits

The design and electrical performance of the fabricated devices and circuits are discussed in this section. Section-A discusses the design and electrical performances of the HV NMOS followed by LV NMOS and PMOS in section-B. The electron and hole channel mobilities are discussed in the section-C. And finally, the performance of the ring oscillator and interlayer dielectric breakdown are discussed in sections-D and E, respectively.

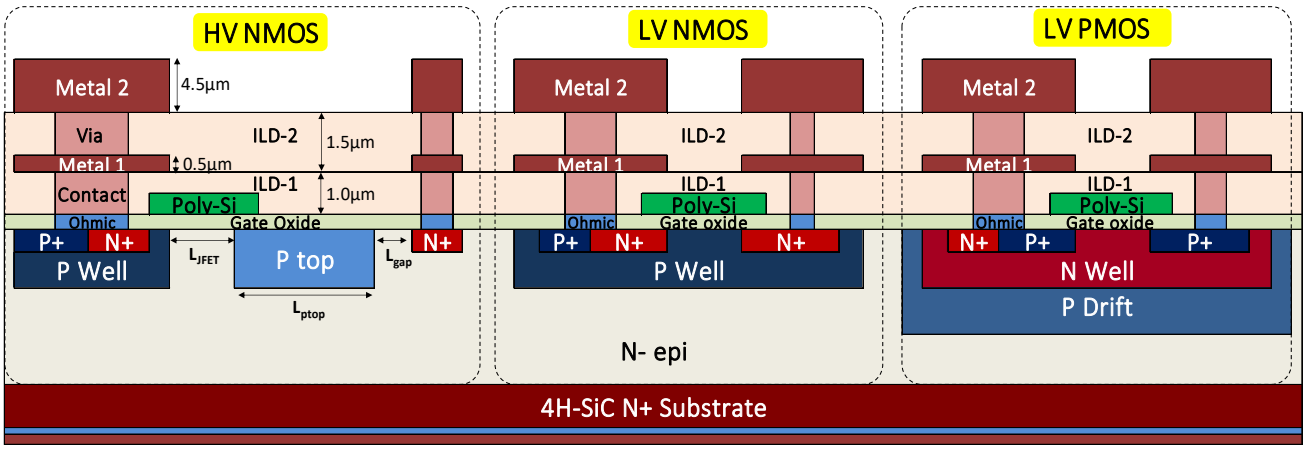

Figure 1: Cross-section of the fabricated HV NMOS, LV NMOS and LV PMOS on an N-epi grown on N+ substrate.

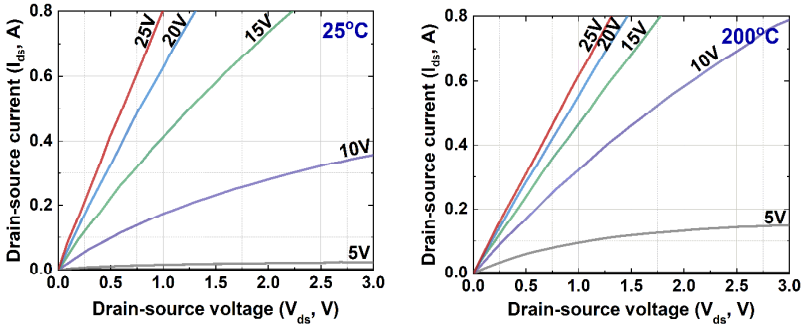

Figure 2: Output characteristics of HV NMOS at 25°C and 200°C

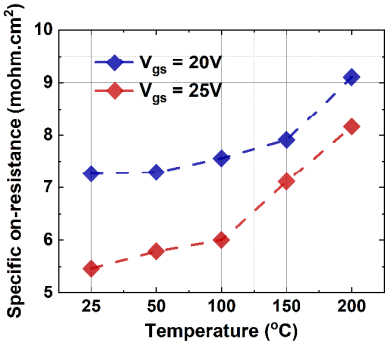

Figure 3: Ron,sp variation of HV NMOS over 25°C to 200°C

A. *HV NMOS design*

The design of HV NMOS incorporates REduced SURface Field (RESURF) technique. Al implanted P top is used as the RESURF to reduce the surface electric field and enhance the breakdown voltage. The design and critical parameters of HV NMOS in this work is similar to our previously reported design fabricated at X-Fab [1]. However, the HV NMOS disclosed in this work has shown better trade-off between breakdown voltage and specific on-resistance (BV-$R_{on,sp}$), and therefore an improved device FOM ($BV^2/R_{on,sp}$; 370 MW/cm^2) when compared to our previous work (262 MW/cm^2). Moreover, this work implements an backend process that supports a > 400V voltage differential across interlayer dielectric (ILD) exhibiting a breakdown field of 4 MV/cm between metal layers, which is extremely important for the integration of HV Power ICs.

Figs. 2 and 3 show the typical on-wafer output characteristics and the extracted $R_{on,sp}$ of the HV NMOS over 25°C to 200°C. The $R_{on,sp}$ of HV NMOS at 25°C with gate-source voltage (V_{gs}) of 20 V and 25 V is 7.30 mΩ·cm^2 and 5.82 mΩ·cm^2, respectively. The $R_{on,sp}$ increases with the rise in temperature due to the increase in the resistances of drift layer, JFET region and the interconnect metal layer. Fig. 4 shows the transfer characteristics of the HV NMOS and the extracted threshold voltage (V_{th}) at a drain-source current (I_{ds}) of 100 µA is about 2.4 V at 25°C, adequate for power electronic applications. Fig. 5 shows the blocking characteristics of the HV NMOS demonstrating a BV of 520 V at I_{ds} of 100 µA and V_{gs} of 0 V validating a voltage supporting capability of 104 V/µm in the lateral direction.

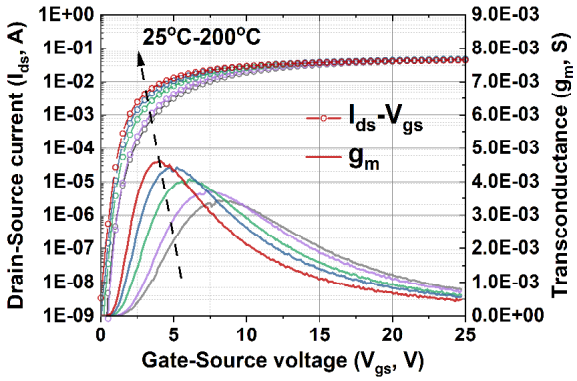

Figure 4: Transfer characteristics of HV NMOS at 25°C to 200°C

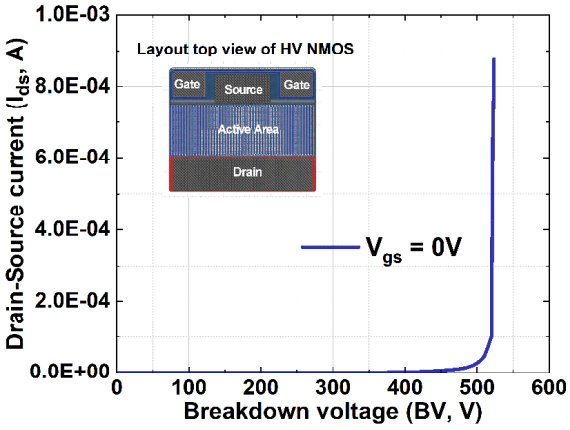

Figure 5: Blocking characteristics of HV NMOS measured at 25°C

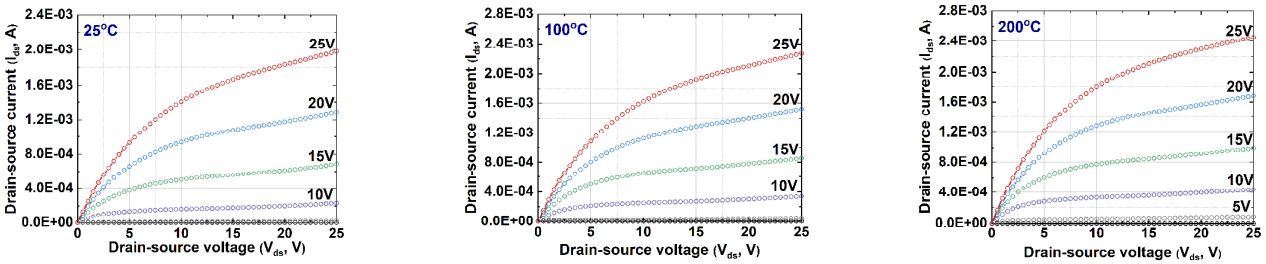

Figure 6: Output characteristics of 10 µm wide, 1 µm long LV NMOS at 25°C, 100°C and 200°C

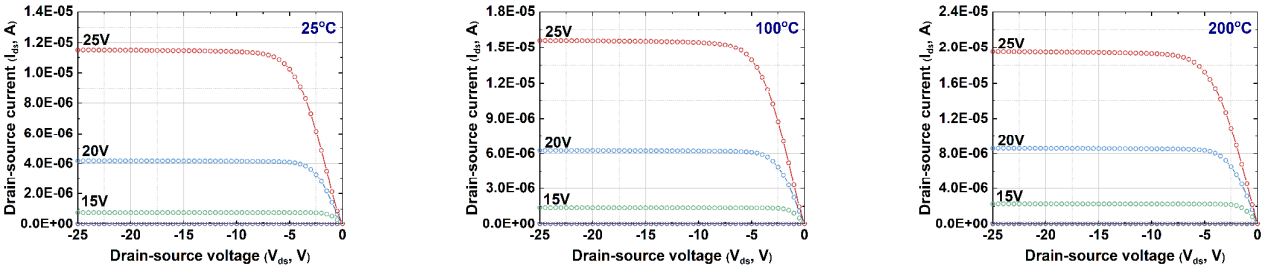

Figure 7: Output characteristics of 10 µm wide, 10 µm long LV PMOS at 25°C, 100°C and 200°C

B. LV NMOS and LV PMOS

The LV NMOS is formed by P Well and N^+ implants. The P Well used for the LV NMOS is same as the P Well optimized for HV NMOS. The LV PMOS is formed by the N Well and P^+ implants. The channeling P Drift implant is used to form the accumulation channel for LV PMOS. The I-V characteristics at 25°C, 100°C and 200°C of the 10 µm wide and 1 µm long LV NMOS and 10 µm wide and 10 µm long LV PMOS are shown in Figs. 6 and 7, respectively. The transfer characteristics of the LV NMOS and LV PMOS are shown in Figs. 8 and 9. The threshold voltages are extracted using linear extrapolation method at maximum transconductance. Fig. 10 shows the extracted threshold voltages of LV NMOS and LV PMOS from 25°C to 200°C. The threshold voltages have a negative temperature coefficient due to the decrease in the electrons trapped in the interface states as the temperature increases [3]. The dielectric qualities of LV NMOS and PMOS are analyzed by gate-source breakdown as shown in Fig. 11. The gate-source showed very low leakage current demonstrating a high breakdown field of about 10 MV/cm.

C. Electron and Hole Mobilities

The field effect mobilities of electrons and holes are extracted from 200 µm x 200 µm and 20 µm x 20 µm test structures (FATFETs). The NMOS FATFETs in this work have accumulation channel while PMOS FATFETs have inversion channel. Figs. 12 and 13 shows the field effect accumulation channel mobilities of electron and inversion channel mobilities of holes. The summary of the peak mobilities of electrons and holes is shown in Fig. 14.

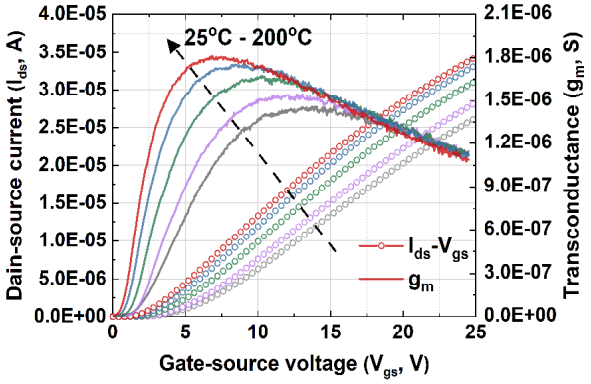

Figure 8: Transfer characteristics (at Vd=0.1 V) of LV NMOS

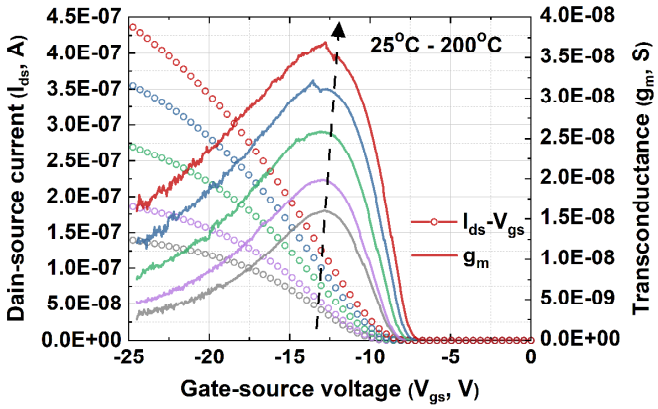

Figure 9:Transfer characteristics (at V_d=0.1 V) of LV PMOS

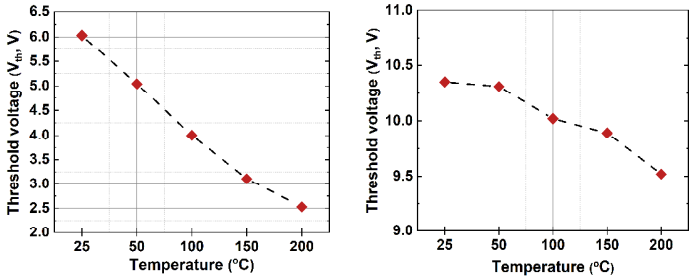

Figure 10: Vth variation of LV NMOS (left) PMOS (right) across 25°C to 200°C

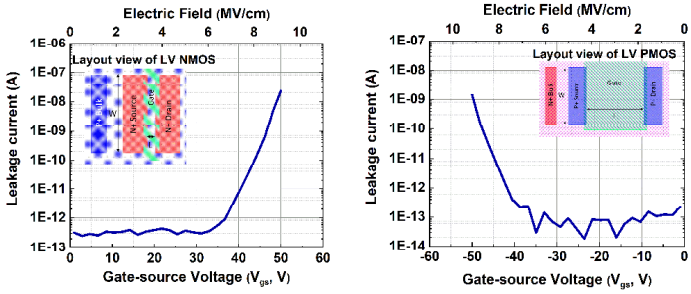

Figure 11: Gate-source dielectric breakdown of LV NMOS (left) and PMOS (right) at 25°C

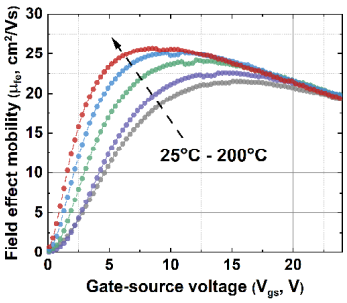

Figure 12: Field effect mobility of electrons over 25°C to 200°C

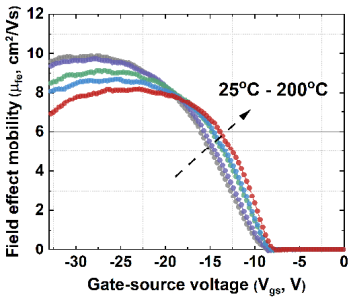

Figure 13: Field effect mobility of holes over 25°C to 200°C

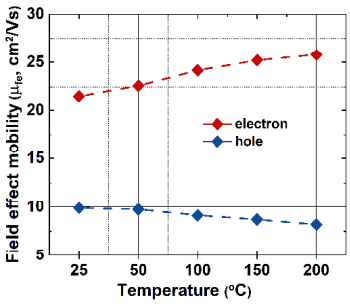

Figure 14; Peak mobility variation of electrons and holes over 25°C to 200°C

D. Ring Oscillator

To validate the fabricated CMOS, a 5-stage ring oscillator was designed. Fig. 15 shows the output waveform of the ring oscillator operating at supply voltage of 25 V at 25°C. The operating frequency has been increased from 0.69 MHz at 25°C to 1.38 MHz at 200°C. Fig. 16 shows the increase in operating frequency with increase in supply voltage and temperature. The operating frequency increases to 1.94 MHz at 200°C with a supply voltage of 30 V.

E. Interlayer dielectric breakdown

In SiC power ICs, it is important that the dielectric between the metal layers can withstand high voltage due to the complex metal crossovers. This current work implements dual metal layers with a 1.0µm dielectric material between them as shown in Fig. 1. Fig. 17 shows the dielectric breakdown measured from a MIM capacitor. The insulator demonstrates a voltage capability of 400V with 1nA leakage and a breakdown field of 4MV/cm between metal layers.

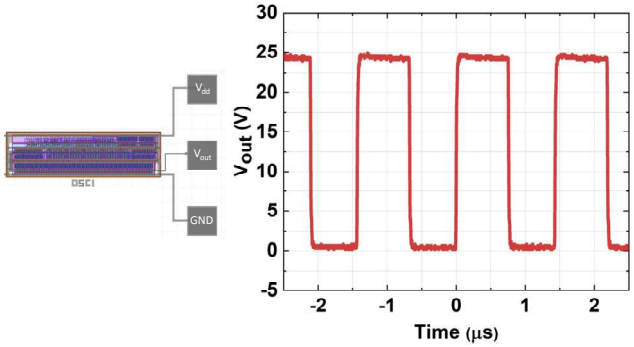

Figure 15: Layout view of CMOS ring oscillator and its operation for V_{dd} of 25 V at 25°C

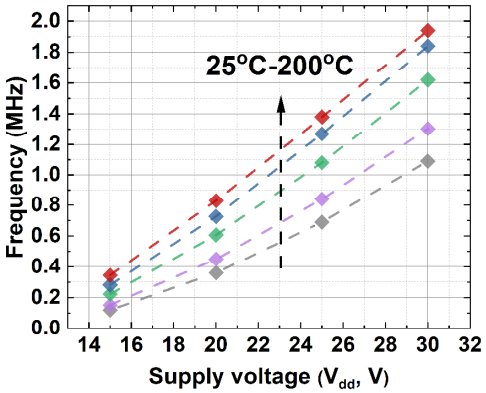

Figure 16: Ring oscillator frequency as a function of V_{dd} over 25°C to 200°C

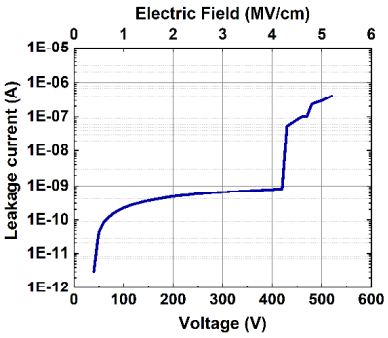

Figure 17: ILD breakdown across metal 1 and metal 2

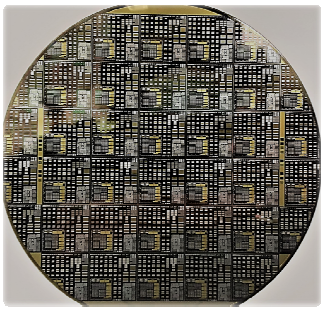

Figure 18: Successfully fabricated 150mm SiC wafer integrating HV, LV MOSFETs & IC blocks

IV. Conclusions

Monolithic integration of HV power lateral MOSFET and LV CMOS have been successfully demonstrated on a 6-inch 4H-SiC substrate as displayed in Fig. 18. The significant electrical characteristics of the devices and circuits have been reported up to 200°C. A single gate oxide and ohmic recipe was developed to simultaneously target optimum channel mobilities and contact resistances. Based on the demonstrated technology a fully integrated and isolated 4H-SiC power IC will be developed in future.

Acknowledgment

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References

[1] N. Yun, J. Lynch, and W. Sung, "Demonstration and analysis of a 600 V, 10 A, 4H-SiC lateral single RESURF MOSFET for power ICs applications," *Appl. Phys. Lett.*, vol. 114, no. 19, p. 192104, May 2019, doi: 10.1063/1.5094407

[2] "Arpa-E,Open2018" [Online]. Available: https://arpae.energy.gov/sites/default/files/documents/files/OPEN_2018_Project_Descriptions_FINAL%20VERSION.pdf

[3] N. S. Saks, S. S. Mani, and A. K. Agarwal, "Interface trap profile near the band edges at the 4H-SiC/SiO2 interface," *Appl. Phys. Lett.*, vol. 76, no. 16, pp. 2250–2252, Apr. 2000, doi: 10.1063/1.126311.