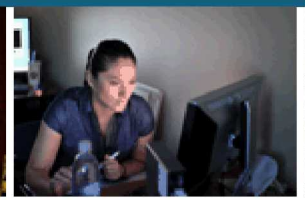
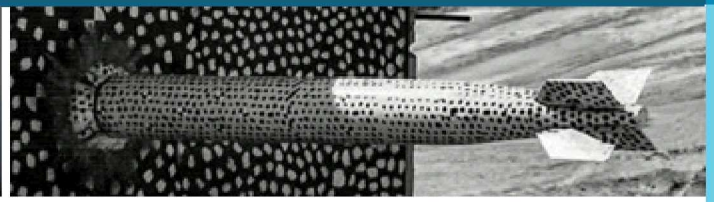
SAND2020-10654C

SCHOOL OF ENGINEERING

DFF Architecture Impact on SEU Response in Different Semiconductor Technologies





PRESENTED BY

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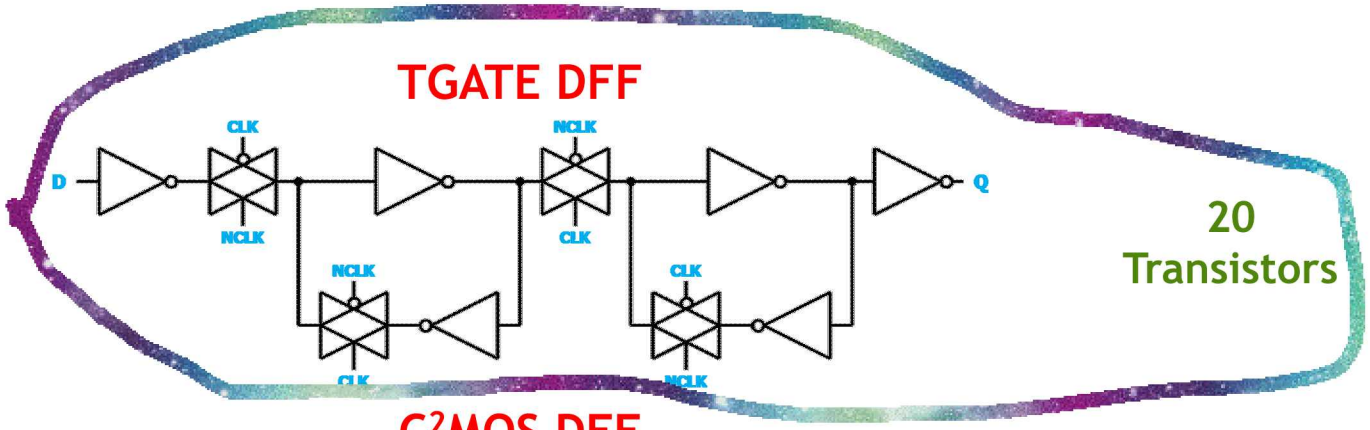
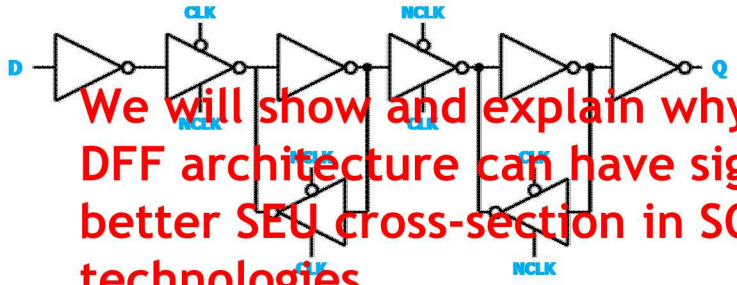
Which DFF Architecture is Best for SEU Response?

TGATE DFF



20 Transistors

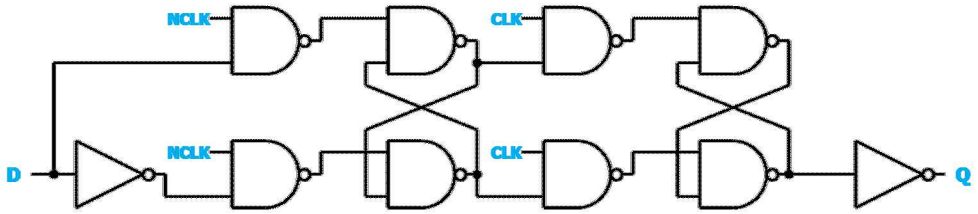
C²MOS DFF



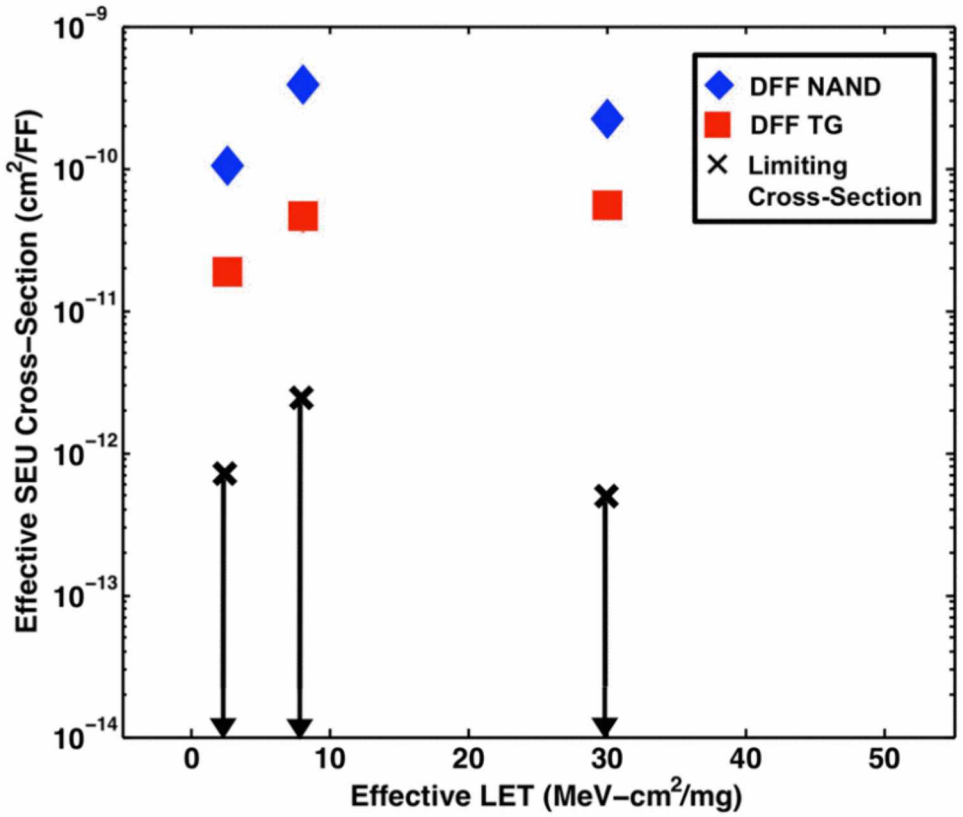
24 Transistors

We will show and explain why the TGATE DFF architecture can have significantly better SEU cross-section in SOI technologies

NAND2 DFF



28 Transistors



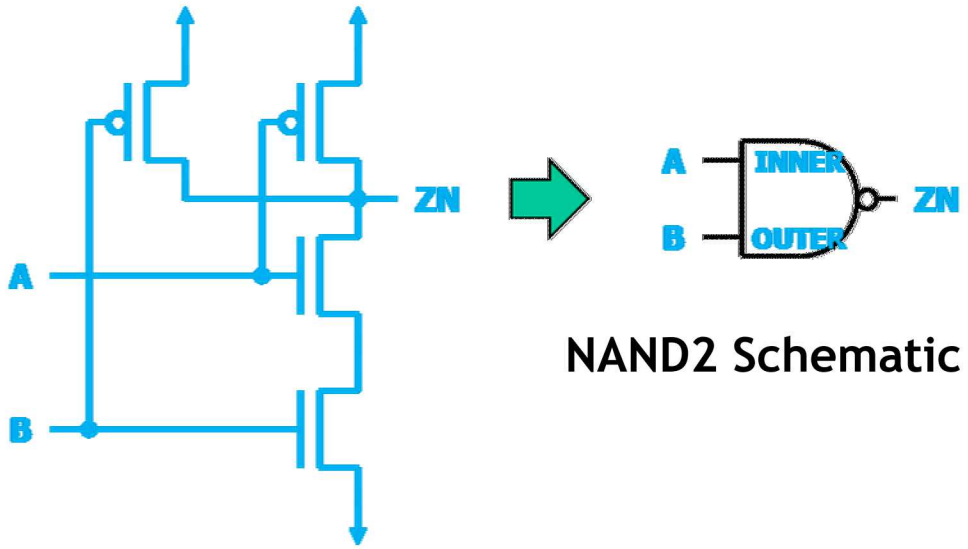
½ load on clock distribution

May be more efficient in IC

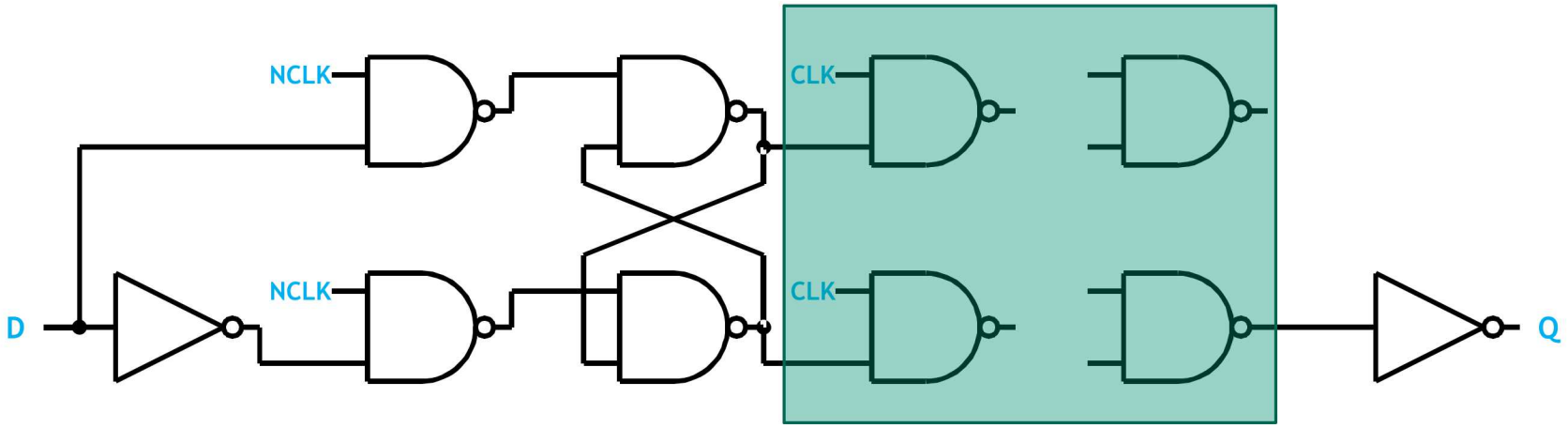
R. C. Quinn et al., "Heavy-Ion SEU Test Data for 32nm SOI Flip-Flops," 2015 *IEEE Radiation Effects Data Workshop (REDW)*, Boston, MA, 2015, pp. 1-5

Can Input Choice Affect SEU Response?

For example, is there a best way to connect each left NAND2 to its respective right NAND2 and cross-coupling the right NAND2 outputs to the other input?



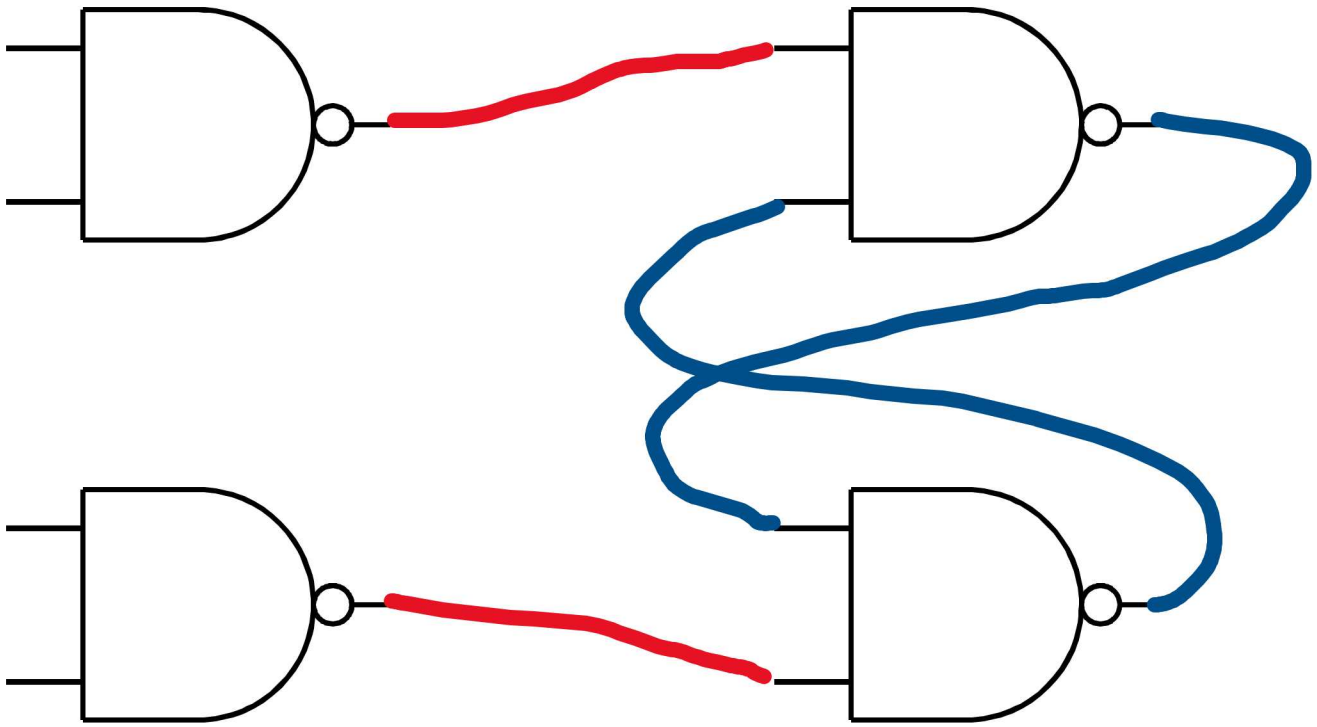
NAND2 Schematic



NAND2 DFF Schematic

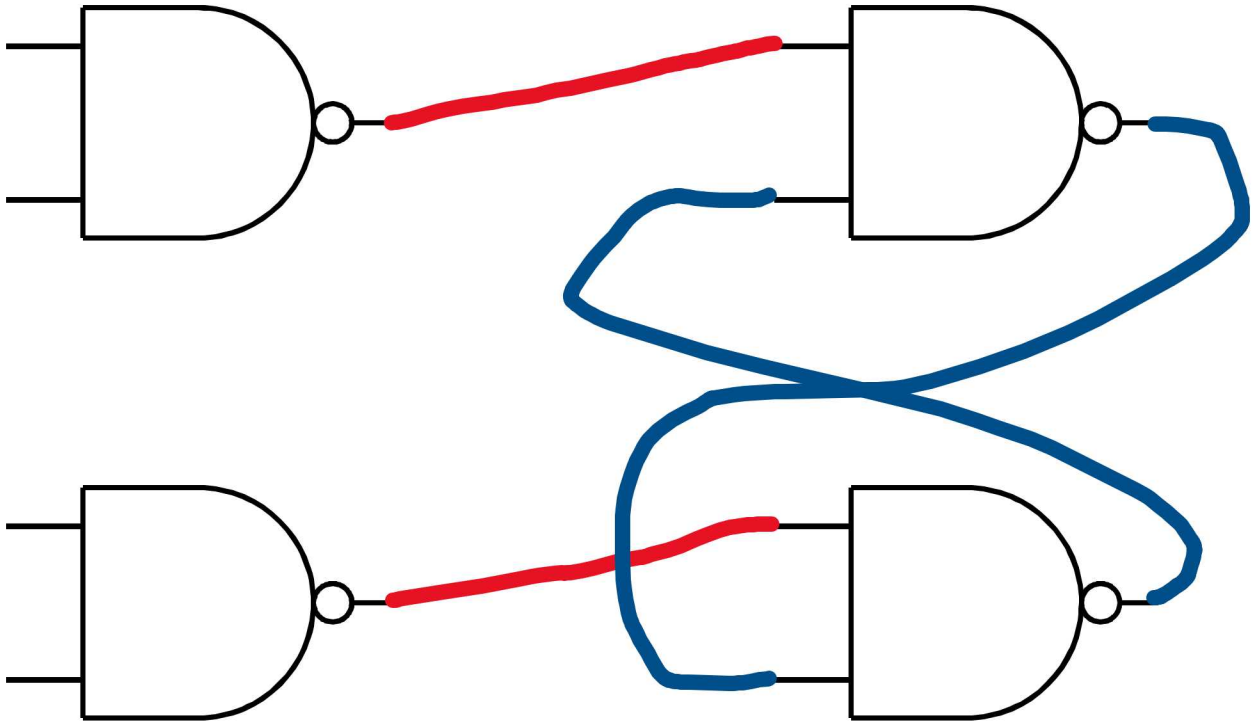
Can Input Choice Affect SEU Response?

My aesthetic method for schematic drawing, minimally overlapping signals – not best choice, but not worst either in SOI technologies



Can Input Choice Affect SEU Response?

Best choice in SOI technologies, we will show you why



Outline

Background: 350-nm PD Body Contacted SOI

TCAD Simulation Results

- SOI Scaling: 32-nm PD Floating Body SOI
- Floating Body vs. Body Contacted SOI
- Bulk Si vs. SOI: 14-nm Bulk FinFET

Single Event Mechanism

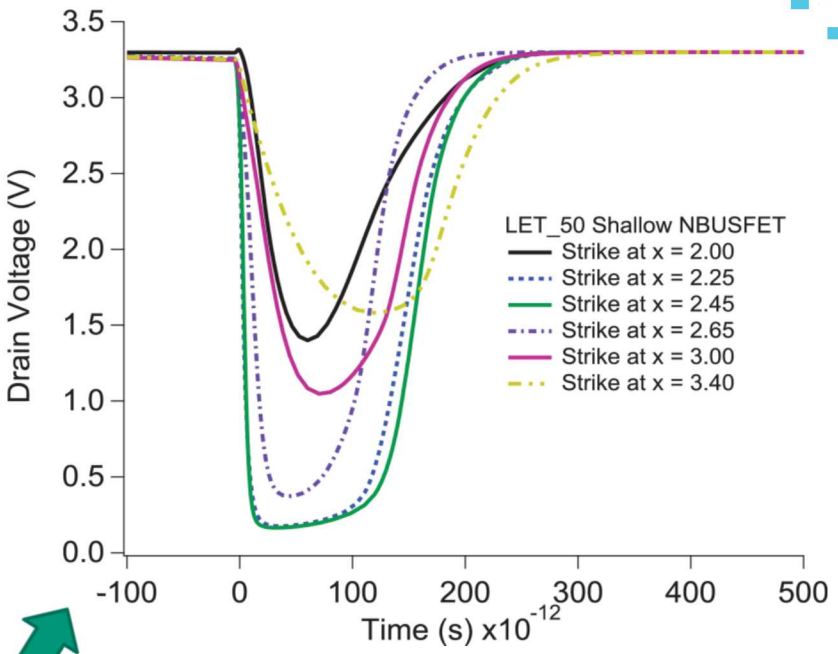
Best Design Choices

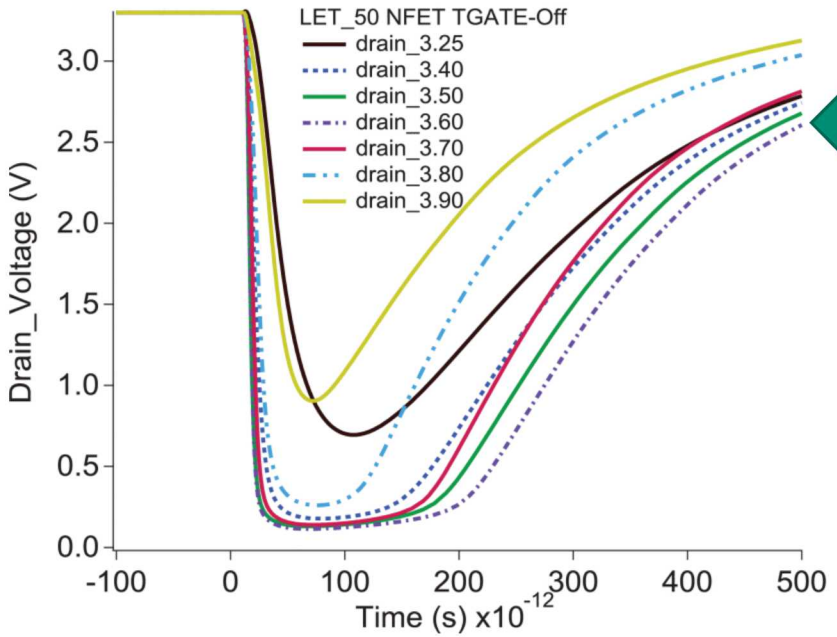
Background: 350-nm Partially Depleted Body Contacted SOI

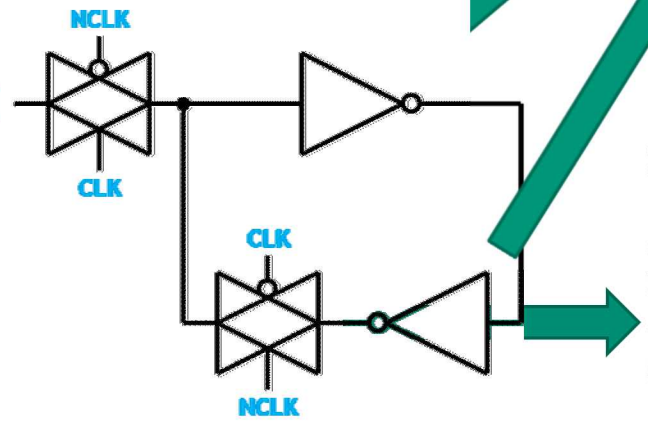
Static SEU simulation with clock low and alternating data input

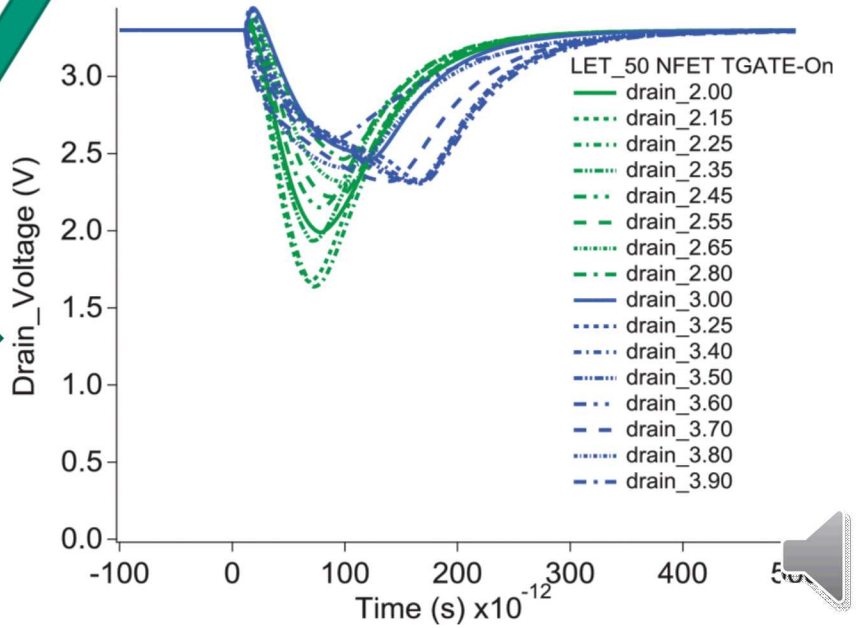
- INVs – Propagates SET
- TGATE ON – Only propagates SET in a few locations closest to the body tie (green vs. blue in lower right figure)
- TGATE OFF – Propagates SET like INV, but longer pulses

Saw a large difference between INV and TGATE SEU response and wondered if it applied to other technology









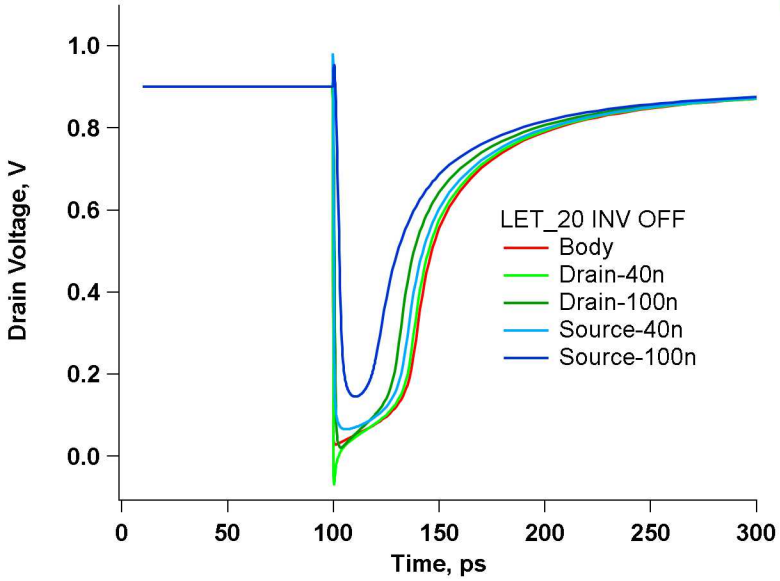
J. D. Black et al., "DFF Layout Variations in CMOS SOI—Analysis of Hardening by Design Options," *IEEE TNS*, vol. 67, no. 6, pp. 1125-1132

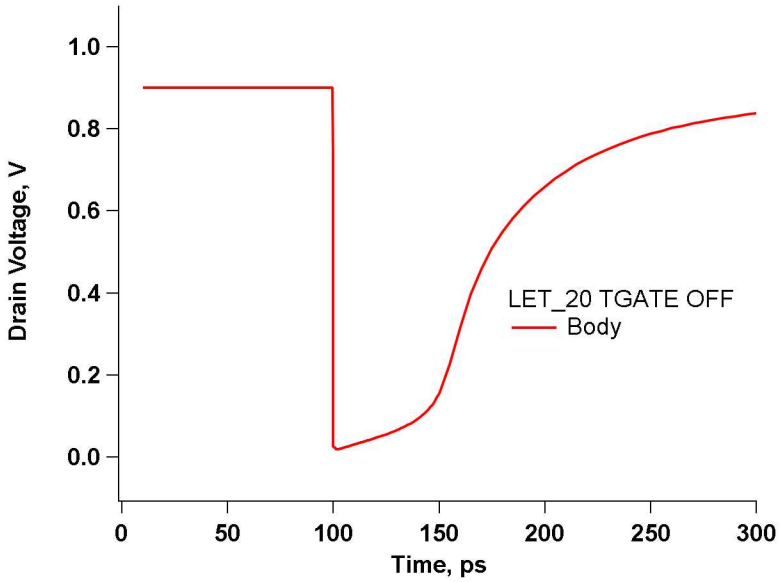
TCAD Simulation Results – SOI Scaling 32-nm Partially Depleted Floating Body

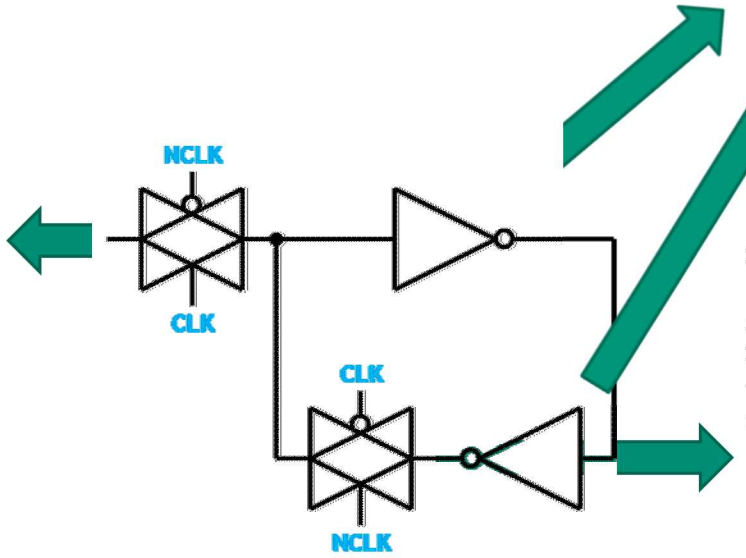
32-nm simulations generally agree with 350-nm simulations

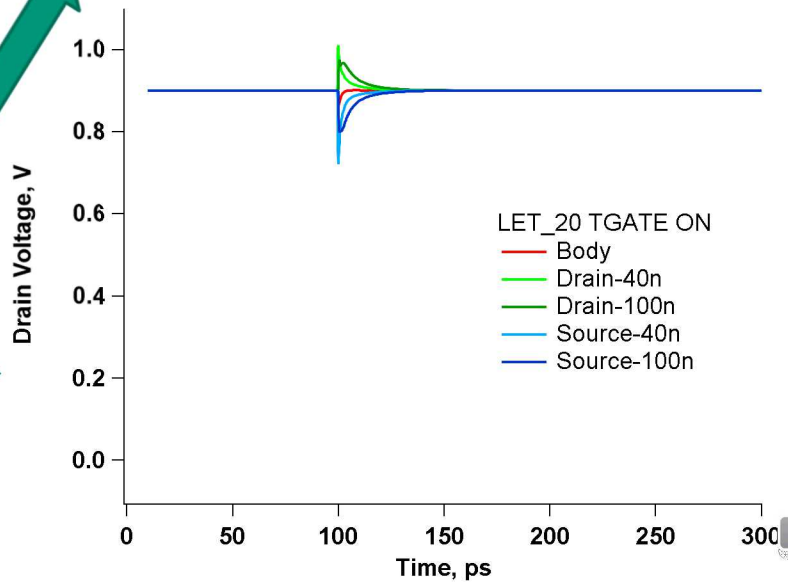
Disagreement in the TGATE ON simulations where no SETs propagate in 32-nm

Difference between INV and TGATE SEU response scales in SOI technology, is the change in the TGATE ON SEU response due to scaling or floating body vs. body contacted





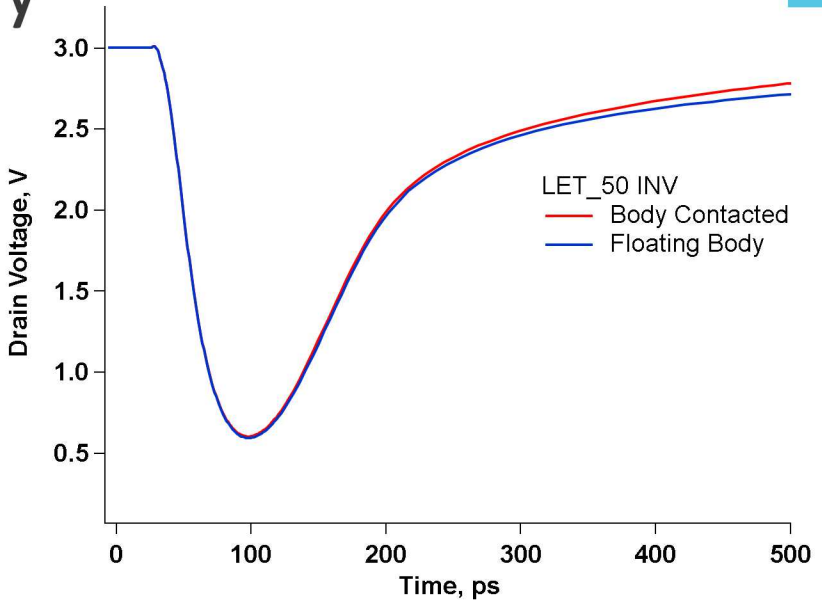


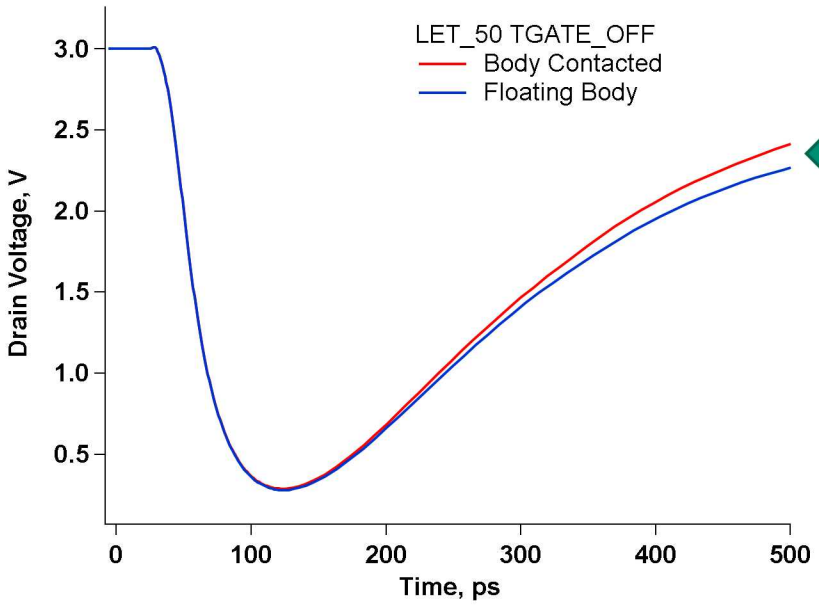


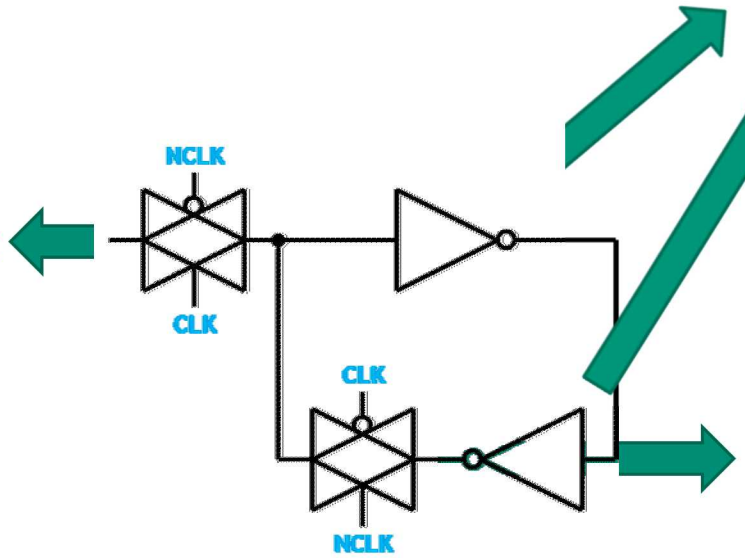
TCAD Simulation Results – Floating Body vs. Body Contacted SOI

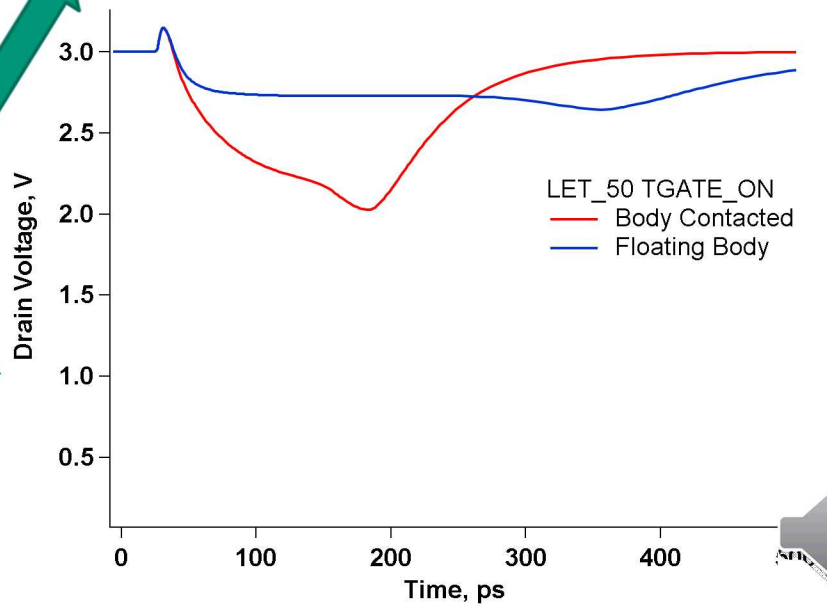
350-nm Body Contacted SOI vs “Floating Body” SOI

- Floating Body created by adding 10 kΩ resistor from body contact to ground, BUSFET in INV also swapped to isolation FET which was used in TGATE simulations
- INV and TGATE OFF – SETs are slightly longer in floating body devices
- TGATE ON – SETs disappear for floating body devices









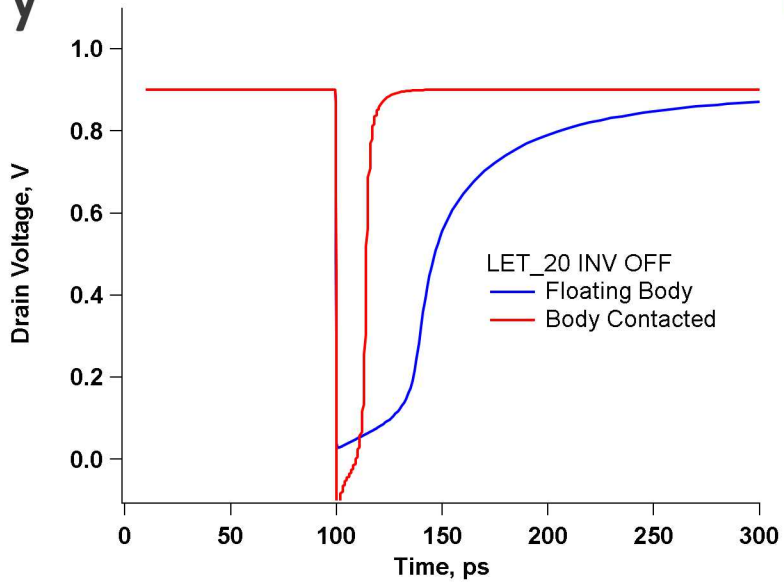
TCAD Simulation Results – Floating Body vs. Body Contacted SOI

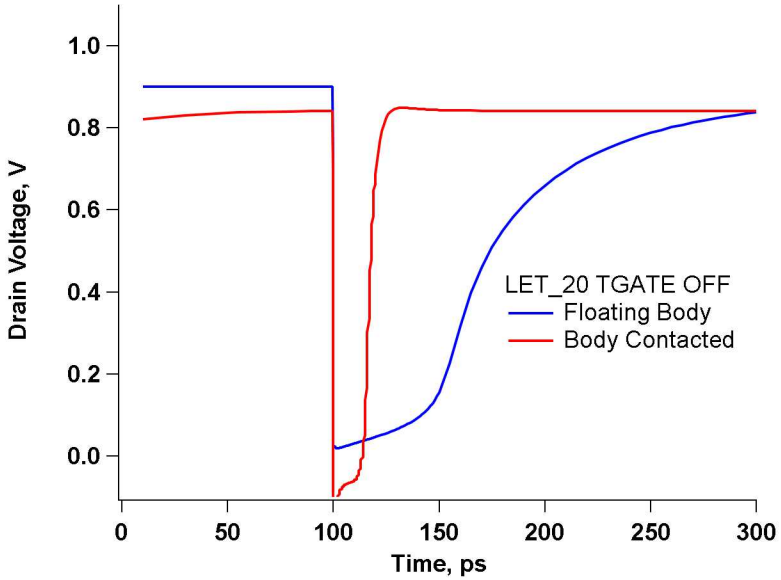
32-nm “Body Contacted” SOI vs Floating Body SOI

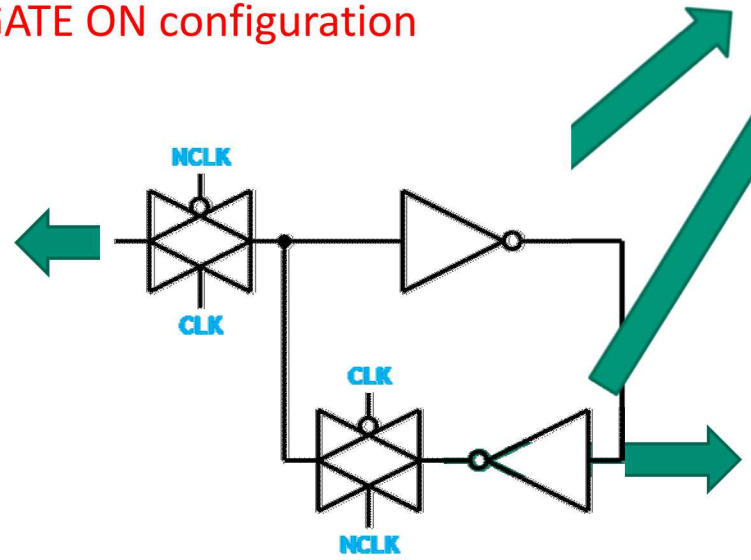
- Body contact created by placing non-physical interface on bottom of Si island, otherwise 3D structure is exactly the same
- Results consistent with 350-nm SOI

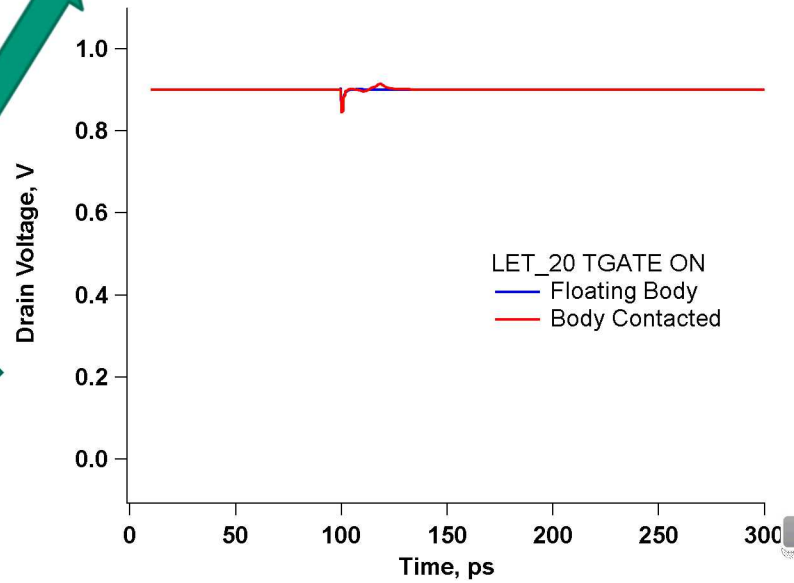
SOI body contact plays a role in SET propagation

- Shortens SETs in INV and TGATE OFF configurations
- Increases transient voltage in TGATE ON configuration









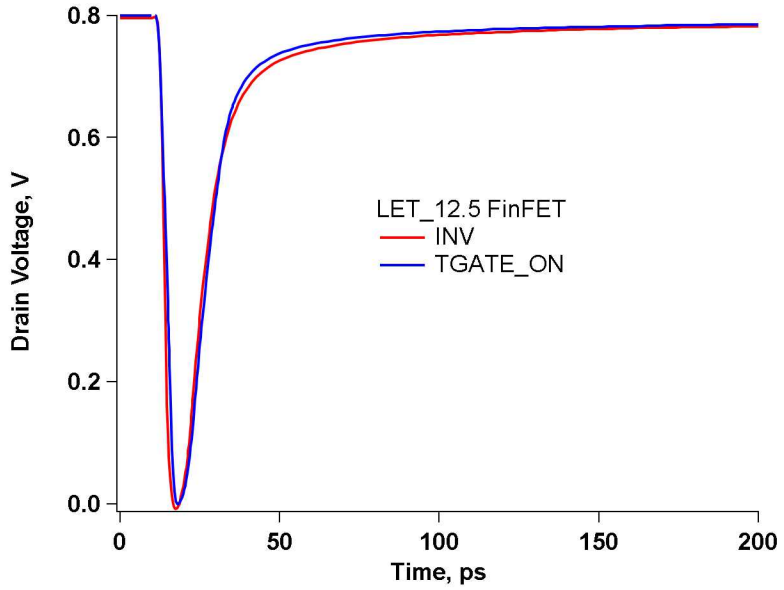
TCAD Simulation Results – Bulk Si vs. SOI 14-nm FinFET

INV – SETs propagate

TGATE ON – SETs propagate like INVs

Well/Substrate (body) contacts implemented with long path to devices, ~2-4 μm, maximum SEU well current is 100s of ps after the SEU

Results are inconsistent any SOI simulation



Single Event Mechanism

Transistor body potential

- Body contact sets this, but also limits departure through body resistance
- Drain/body or source/body junctions can forward bias and limit body potential departures near the transistor

Single event response at reverse biased drain/body junction

- Drain potential displaces towards body potential, body potential displaces towards drain potential
- Body potential displacement controlled by source/body junction and drain potential (once they collapse together) and/or body contact
- Drain potential displacement controlled by body potential (once they collapse together) and restored through other transistor drive

Rail-to-rail single event transient on transistor drain

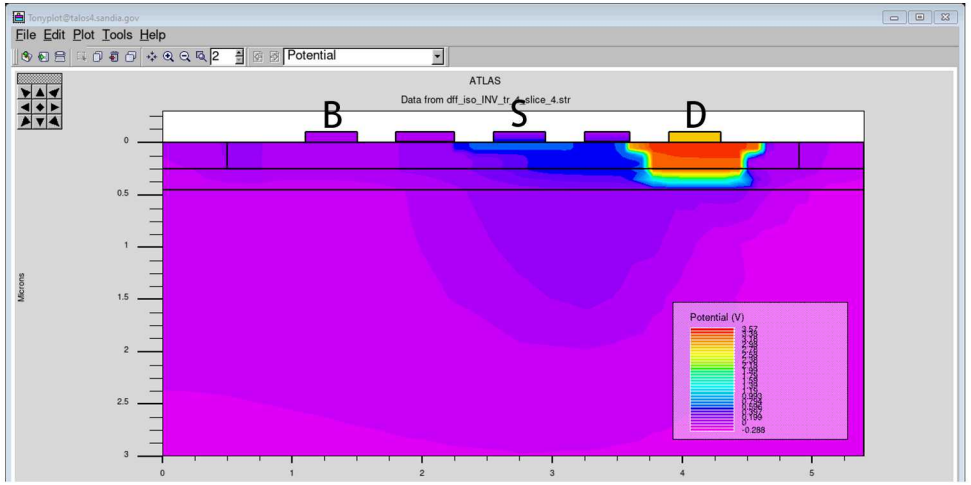
- Floating body SOI – Only in transistors with source biased same as body
- Body contacted SOI – In transistors with source biased same as body and possibly in transistors nearer to body contact
- Bulk – In 14-nm bulk Si, any reverse bias junction can generate SET

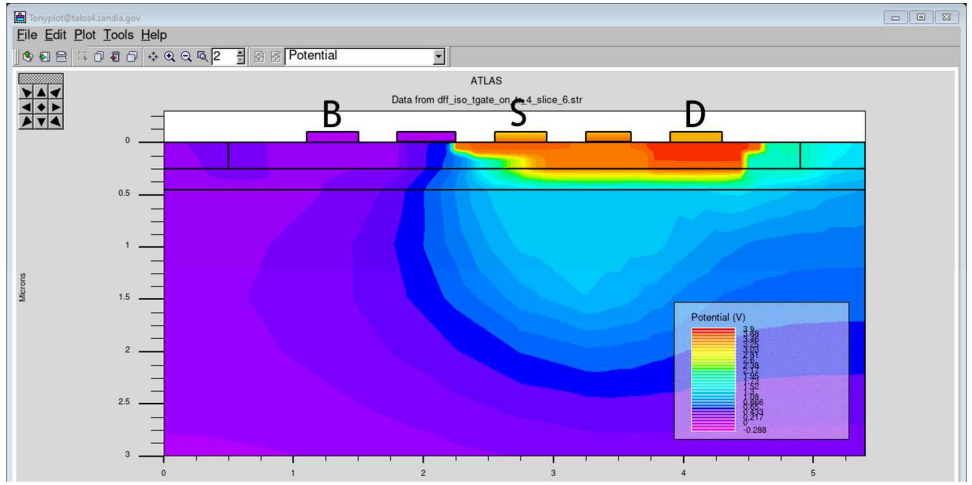
TCAD Potential Plots – 350-nm SOI During Single Event

INV

TGATE ON

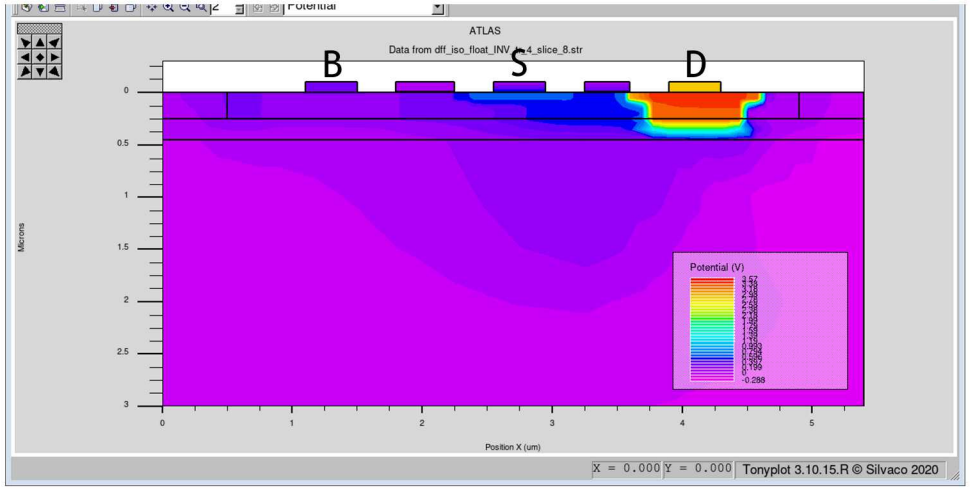
Body Contacted

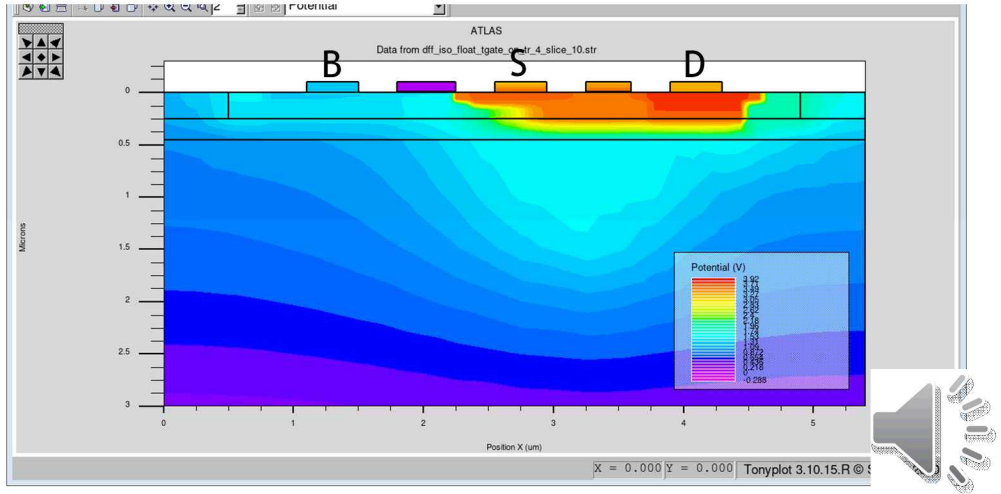




INV source controls body potential strongest. Body contact controls body potential with resistive path from its contact

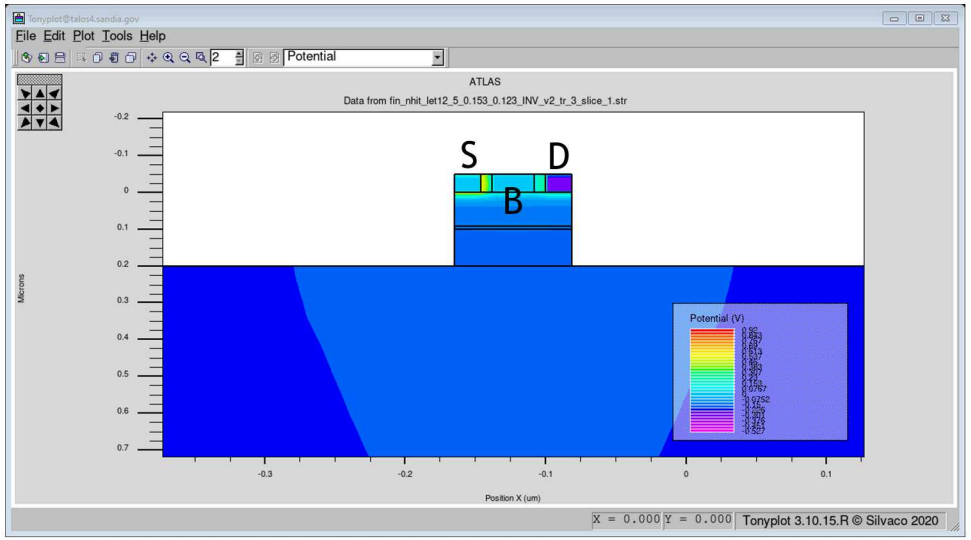
“Floating Body”



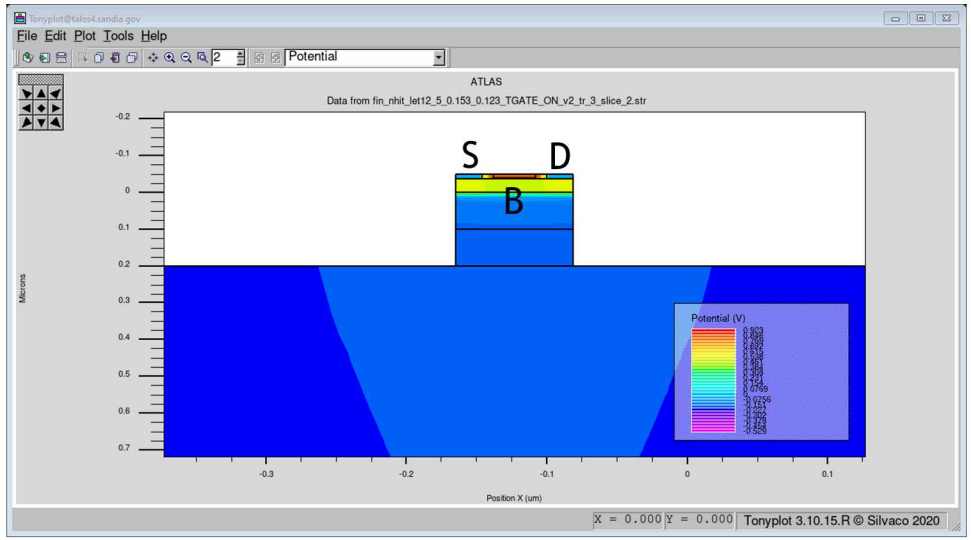


TCAD Potential Plots – 14-nm bulk FinFET Max Drain Current

INV



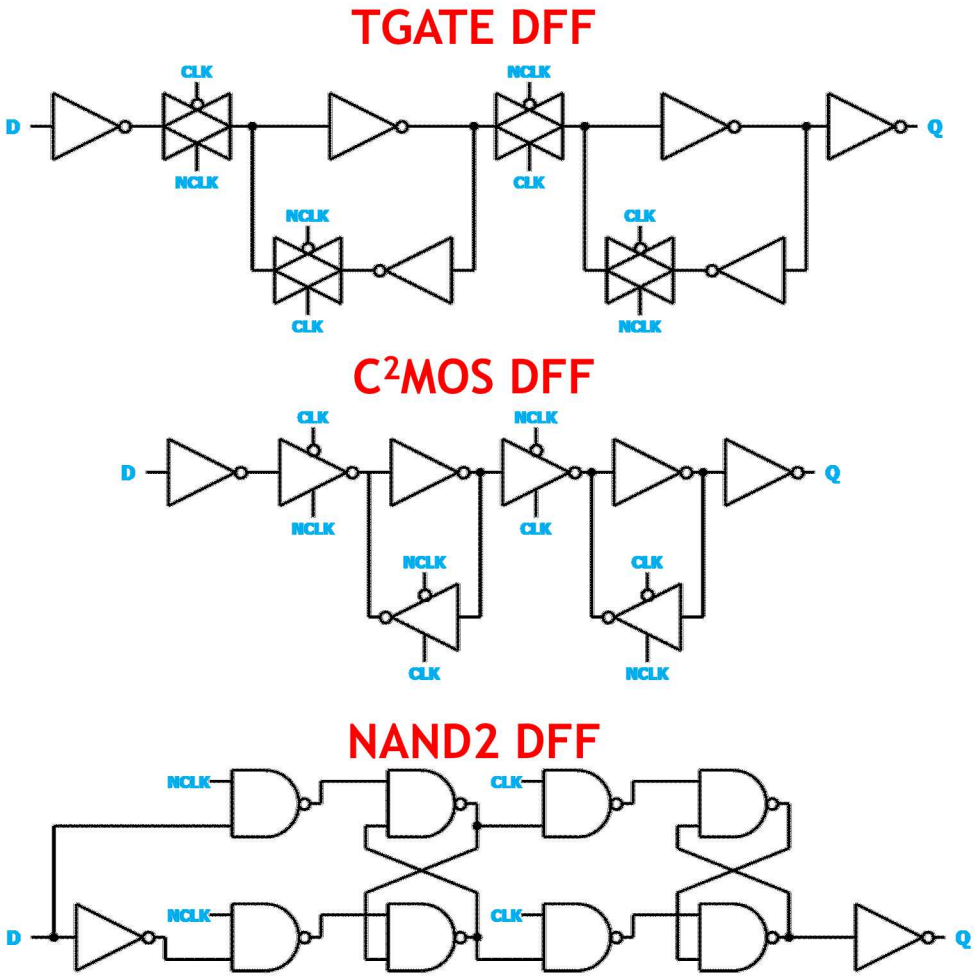
TGATE ON



Well (body) has displaced, but not near the transistor in both cases

Drain in INV and source/drain in TGATE ON have fully displaced

Best Design Choices – 14-nm Bulk FinFET



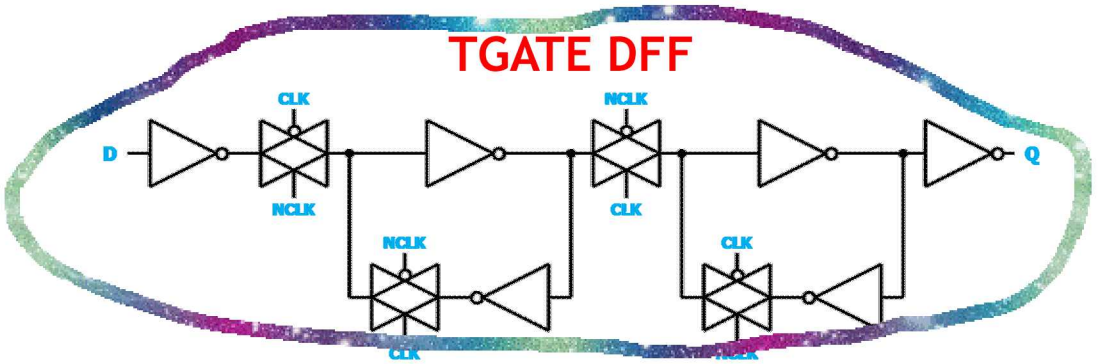
14-nm bulk FinFET

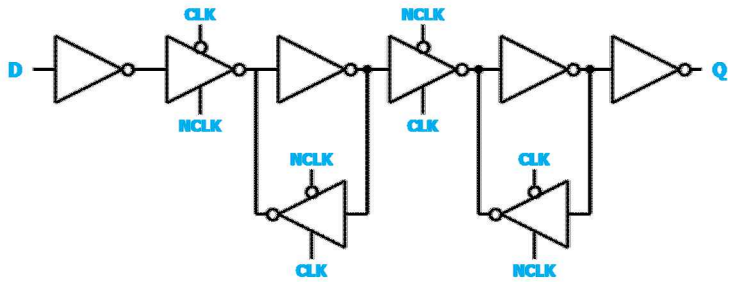
For design hardening, traditional rules apply

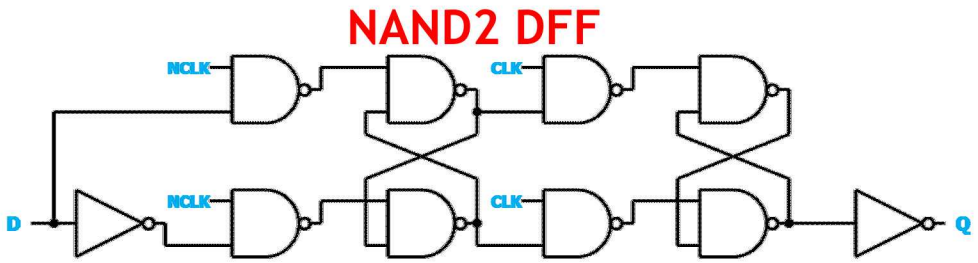
- Minimize number of sensitive circuit nodes
- Maximize nodal capacitance
- Maximize restoring currents

Architecture choice may have some impact on hardening, but other performance metrics may dictate selection

Best Design Choices – SOI, DFF Architecture

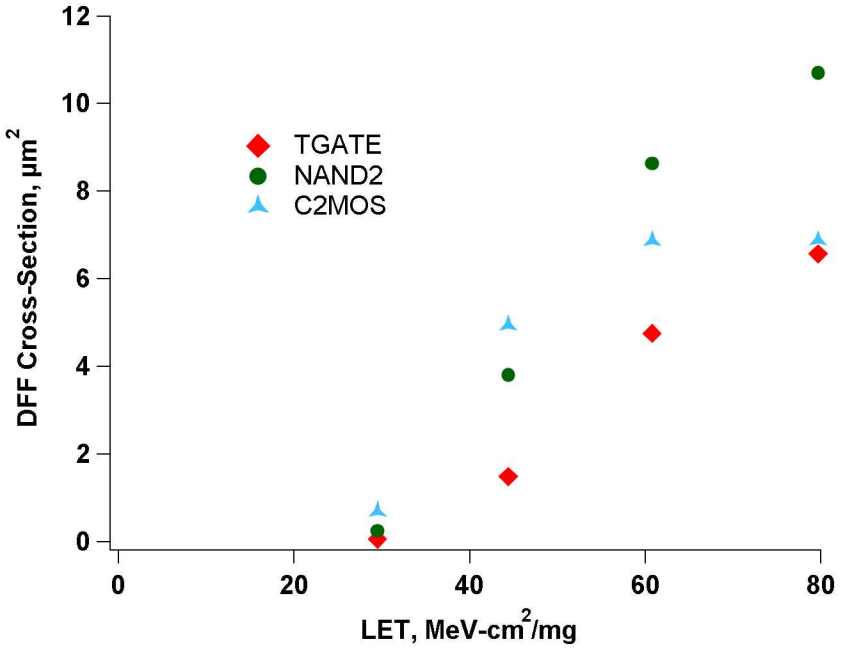






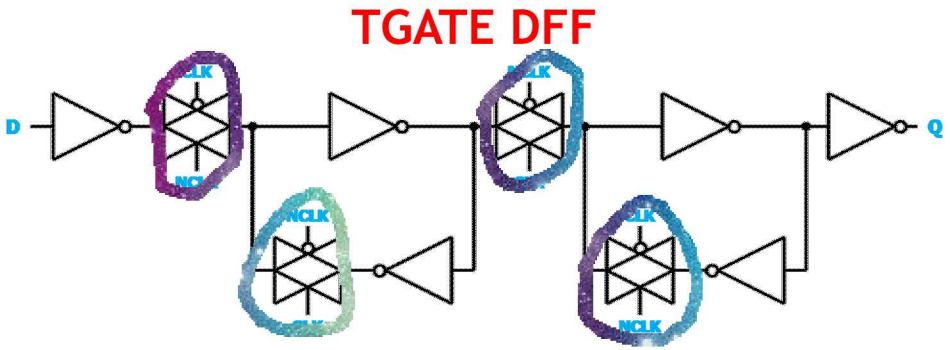
SOI

TGATE DFF is clearly best choice for single event effect mitigation



350-nm SOI predictions based on MRED modeling approach from previous research

Best Design Choices – SOI, TGATE Logic Cells



SOI

TGATE DFF is clearly best choice for single event effect mitigation

TGATE Logic Cells

- Floating body transistors preferred
- If combined with other logic cell in same Si island -> place furthest away from source
- If body contacted technology -> place furthest away from body contact or make body contact weaker

INV, NAND Logic Cells

- Body contacted devices provide shortest SETs, but only a small difference to floating body devices

Best Design Choices – SOI, Multiple Input Logic Cell

NAND2 with one input quasi-static H

- Adding an asynchronous reset to the DFF
- DFF is clocked infrequently, C^2MOS or NAND2 DFF

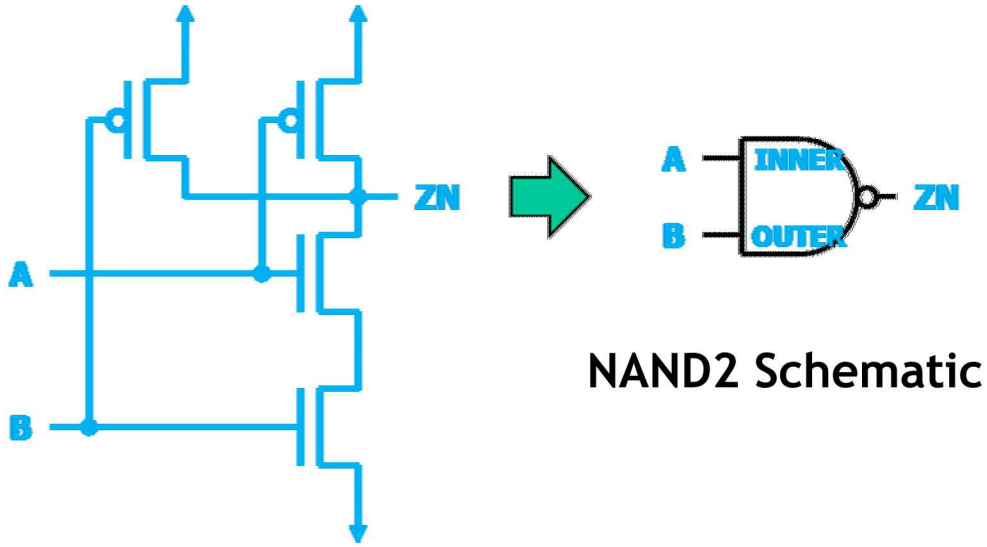
From a simple logic perspective, the NAND2 gate becomes an INV

If A is quasi-static H

- Inner NMOSFET becomes a TGATE ON
- Outer NMOSFET is only one to have a source to control the body
- Single event behavior resembles TGATE ON

If B is quasi-static H

- Outer NMOSFET becomes a TGATE ON
- Shared source/drain becomes another source to control the body
- Single event behavior resembles INV



NAND2 Schematic