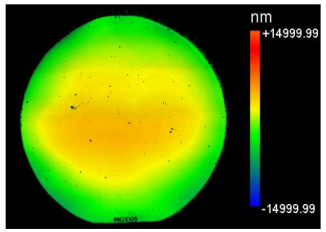

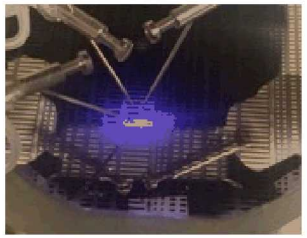
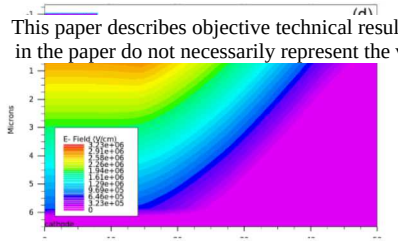
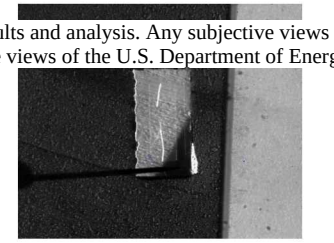

SAND2020-10242C

U.S. NAVAL RESEARCH LABORATORY

Development of High-Voltage Vertical GaN PN Diodes

arpa·e
CHANGING WHAT'S POSSIBLE
OPEN

R. Kaplar[1], A. Allerman[1], M. Crawford[1], B. Gunning[1], J. Flicker[1], A. Armstrong[1], L. Yates[1], A. Binder[1], J. Dickerson[1], G. Pickrell[1], T. Anderson[2], J. Gallagher[2], A. Jacobs[2], A. Koehler[2], M. Tadjer[2], K. Hobart[2], M. Ebrish[3], M. Porter[4], R. Martinez[5], K. Zeng[5], D. Ji[6], S. Chowdhury[5], O. Aktas[7], and J. Cooper[8]

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[3]National Research Council, Washington, DC, USA, residing at NRL
[4]Naval Postgraduate School, Monterey, CA, USA, residing at NRL
[5]Stanford University, Stanford, CA, USA
[6]Formerly at Stanford, now at Intel Corp., Santa Clara, CA, USA
[7]EDYNX Inc., Livermore, CA, USA
[8]Sonrisa Research Inc., Santa Fe, NM, USA

The authors gratefully acknowledge the support of the ARPA-E OPEN+ Kilovolt Devices Cohort managed by Dr. Isik Kizilyalli

Outline

- Introduction
- High-Voltage GaN Diodes for EMP Protection
  - Growth
  - Processing
  - Testing
- GaN Diode Foundry Process
  - Growth and Wafer Metrology
  - Processing and Edge Termination
  - Electrical Results and Yield
  - Reliability and FA

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- **Introduction**
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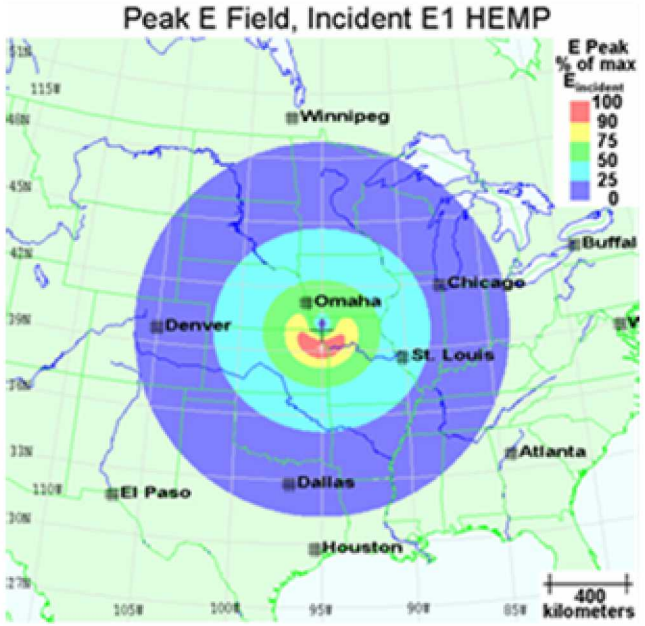
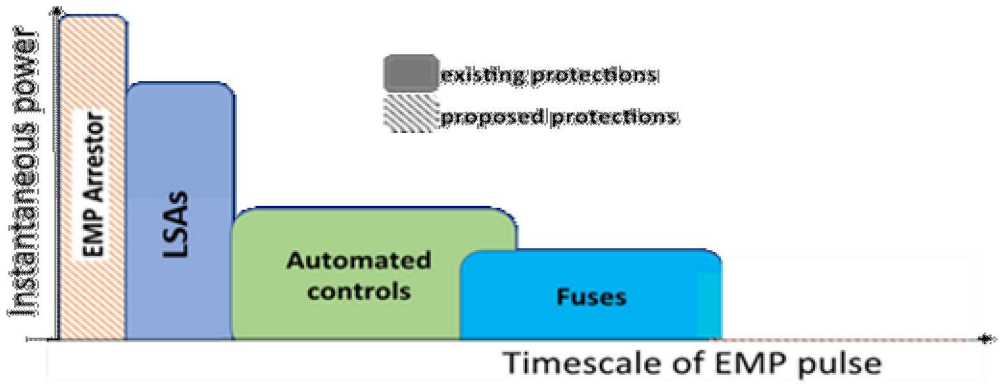
Protection for the Electric Grid



- Transient protection is needed for MV grid-connected systems

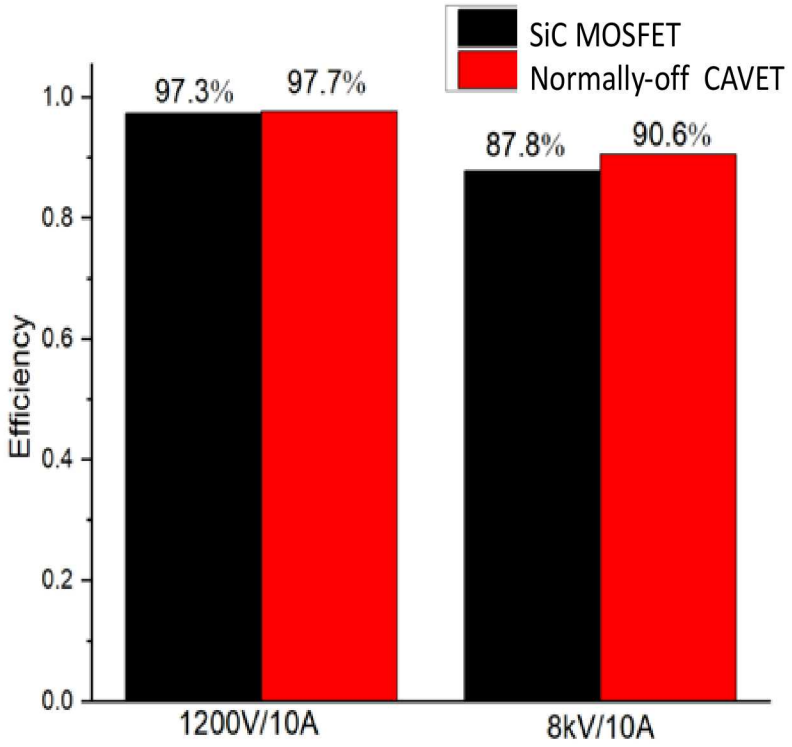
- Electromagnetic pulses are a threat to the grid
  - Very fast E1 component (< 1 ms)
  - Unaddressed by current SOA technology (LSAs)



J. S. Foster Jr. et al., "Report of the Commission to Assess the Threat to the United States from Electromagnetic Pulse (EMP) Attack: Critical National Infrastructures," *Defense Technical Information Center* (2008).

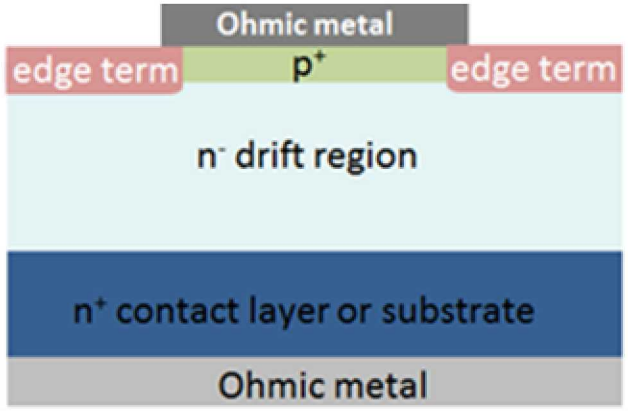
Vertical GaN Advantages for Power Electronics

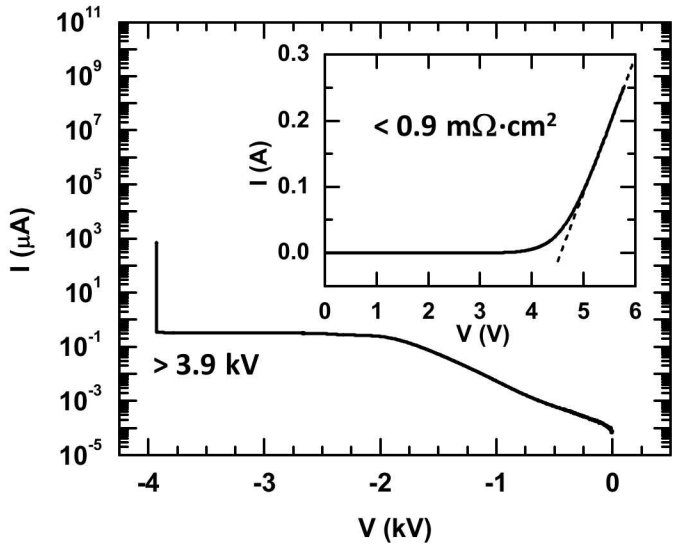
- Critical field of GaN ~2.8 MV/cm at $N_D = 1\times10^{16}$ cm^{-3} and room temperature based on most recent impaction ionization measurements [1]
- Slightly higher than E_C of SiC at the same temperature and doping [2]
- But higher mobility of GaN ~1200 cm^2/Vs [3] compared to ~950 cm^2/Vs for SiC [2] at the same doping and temperature lead to improvements in power converter efficiency [4]
- But devices are not widely available – a vertical GaN foundry is needed that monitors yield, reliability, etc.



[1] D. Ji, B. Ercan, and S. Chowdhury, "Experimental Determination of Impact Ionization Coefficients of Electrons and Holes in Gallium Nitride Using Homojunction Structures," *Appl. Phys. Lett.* **115**, 073503 (2019).
[2] J. A. Cooper and D. Morisette, "Performance Limits of Vertical Unipolar Power Devices in GaN and 4H-SiC," *Elec. Dev. Lett.* **41**, 892 (2020).
[3] I. C. Kizilyalli, A. P. Edwards, O. Aktas, T. Prunty, and D. Bour, "Vertical Power PN Diodes Based on Bulk GaN," IEEE Trans. Elec. Dev. 62(2), 414 (2015).
[4] D. Ji and S. Chowdhury, "On the Progress Made in GaN Vertical Device Technology – Special Issue on Wide Band Gap Semiconductor Electronics and Devices," *Int. J. High-Speed Elec. Sys.* **28(01n02)**, 1940010 (2019).

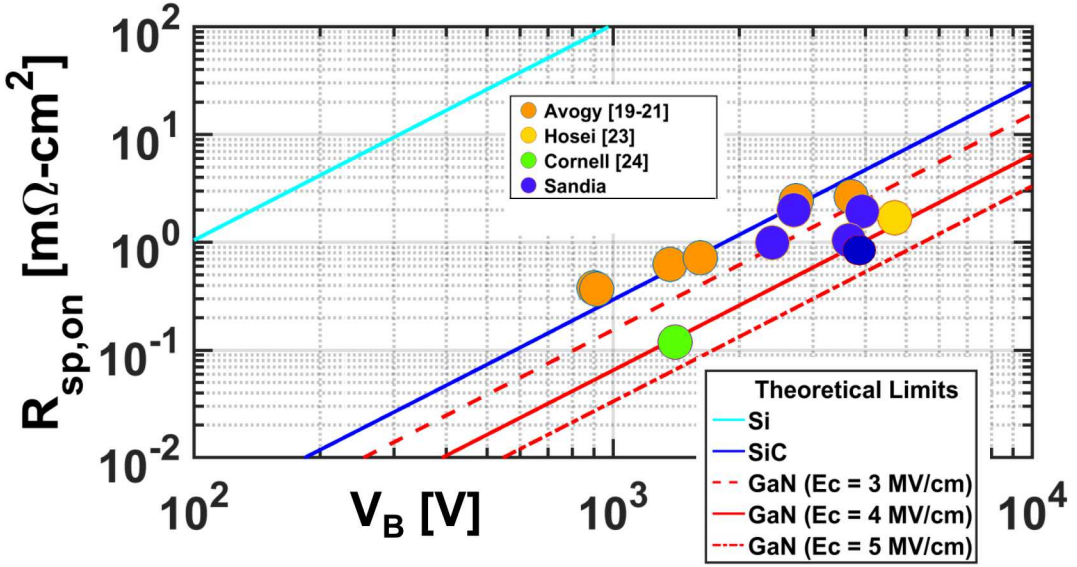
Program Goals for Vertical GaN Technology





A. Armstrong et al., Elec. Lett. 52(13), 1170 (2016)

- **Extend the limits of vertical GaN power device technology**
  - **Increase V_B by 4x from today's SOA**
  - **Challenges: Thick drift region, low net doping, edge termination**
- **Establish a domestic foundry process for vertical GaN power devices**



Team Structure

Sandia National Laboratories

Sandia
- Epitaxial growth
- Device design, processing, and test
- MV grid applications

EDYNX
- Reliability and failure analysis

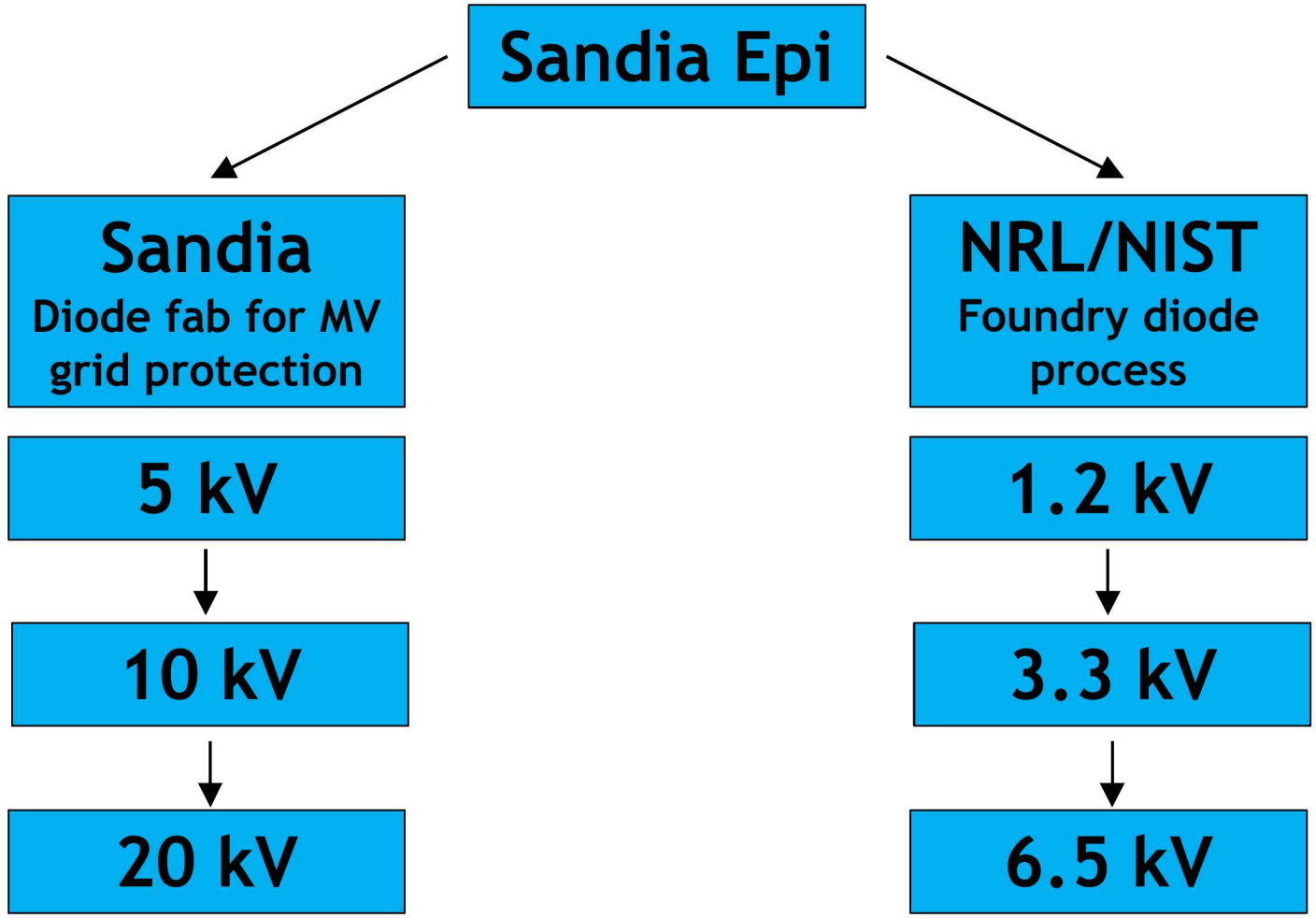
Sonrisa
- Device design

U.S. NAVAL RESEARCH LABORATORY

NRL/NIST
- Foundry process
- Failure analysis

Stanford
- Device design
- Back-side processing
- Breakdown analysis

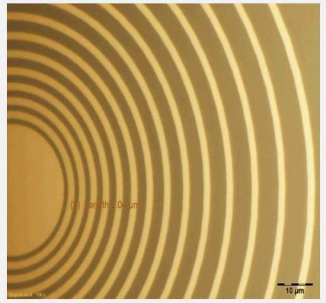
Vertical GaN PN Diode Progression

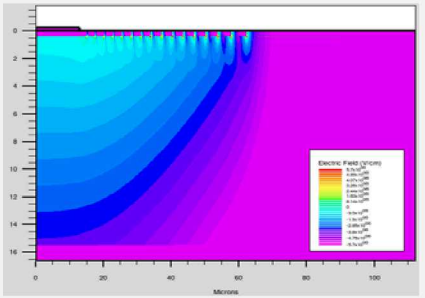


Edge Termination Strategy

1. Foundry: Implanted Guard Rings + JTEs

- Modeling and fabrication: NRL/NIST
- Legacy process with N^+ implant
- Add field plate for possible 3.3 kV diode

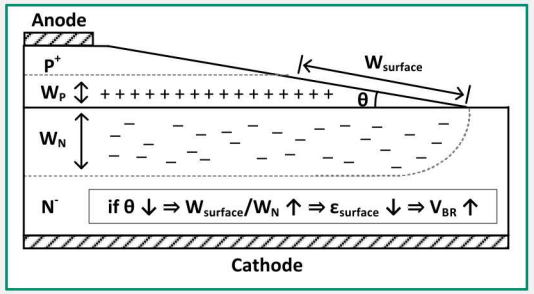




J. Dickerson et al., EMC (2016)

2. Foundry: Bevel (possibly for higher voltage diodes)

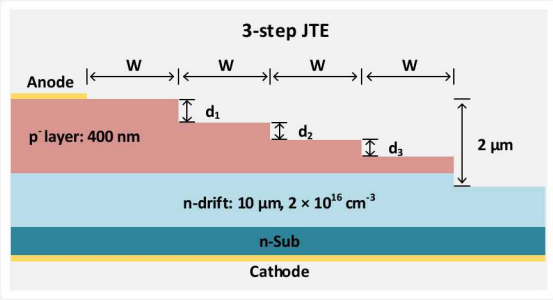
- Modeling and design: Stanford, Sonrisa
- Fabrication via grayscale lithography: Stanford, NRL
- Etched and implanted approaches

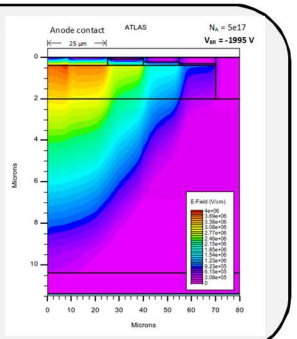


A. Binder et al., submitted to WiPDA (2019)

3. EMP Diodes: Multi-Zone JTEs

- Modeling and Design: Sandia, Sonrisa
- Fabrication: Sandia
- Etched and implanted approaches





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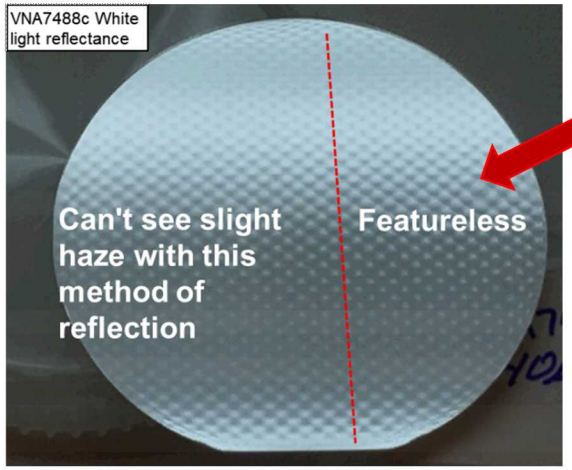
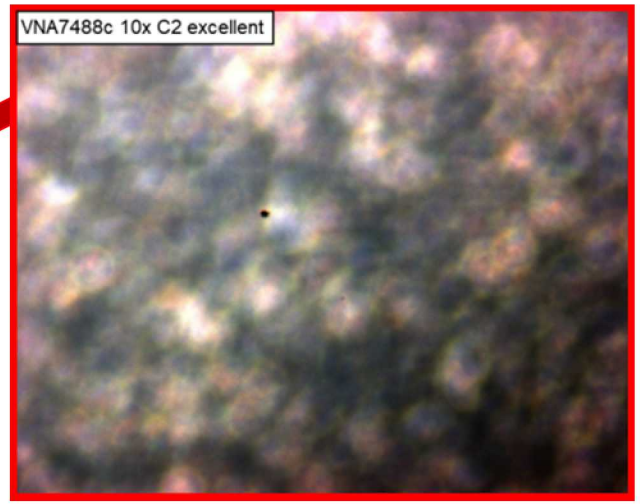
Growth of 5 kV Class Drift Layer

- Investigate influence of substrate
- Target 40 μm of epi growth

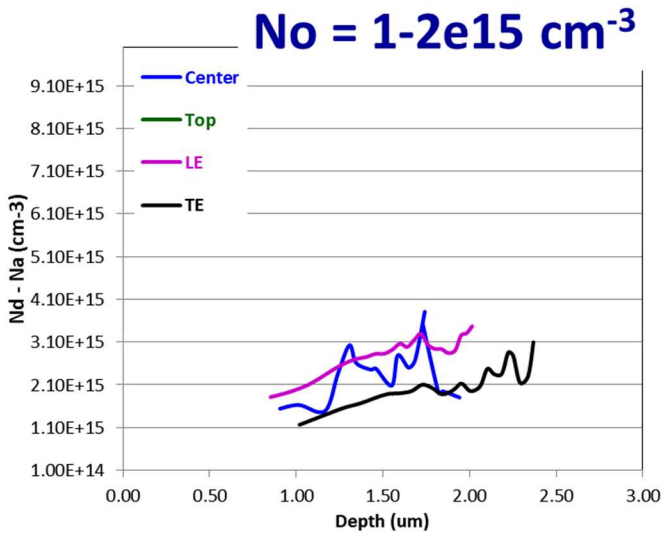
White-light reflectance image



Nomarski image (microscope)



Hg probe CV



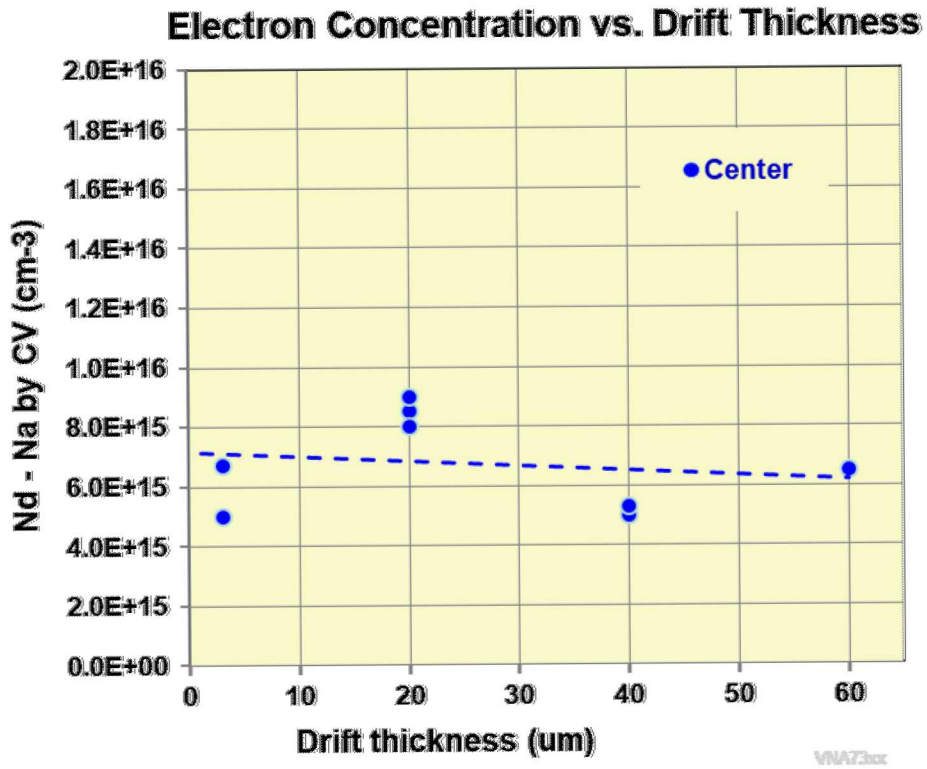
40 μm drift layer

- About half of wafer is featureless

➡ Growth surface of GaN is stable for 45 um thick layer

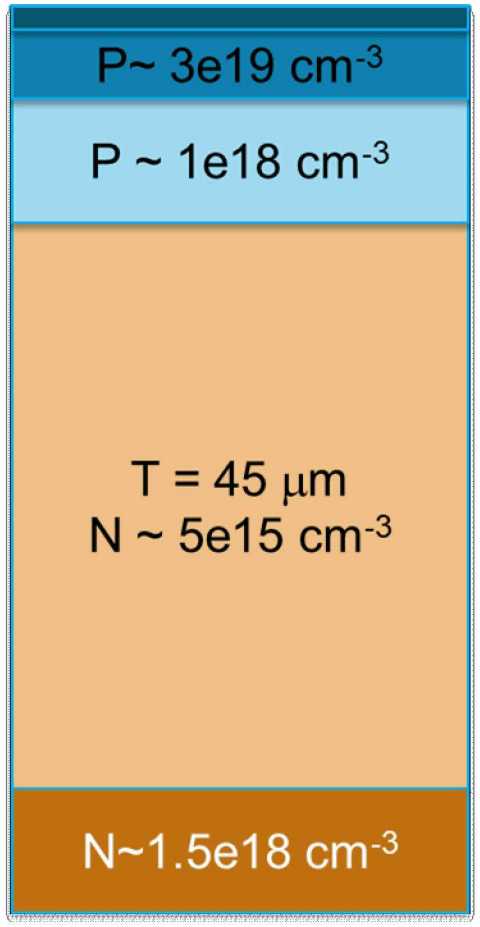
➡ Can get very smooth epi surface (45 μm) with proper substrate and N_o @ 1-2e15 cm^{-3}

Controlled Doping in Epilayers up to 60 μm Thick



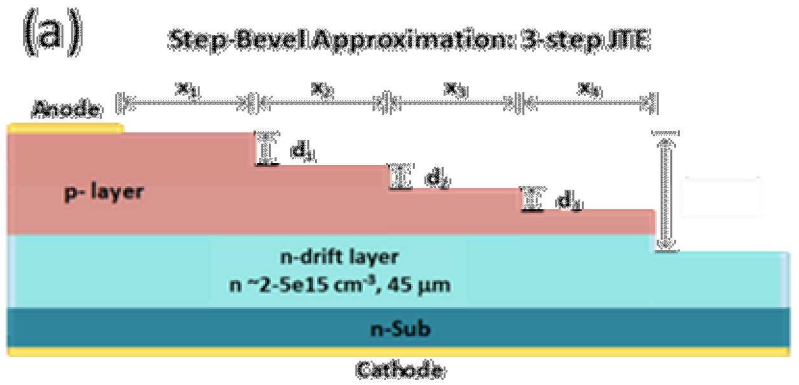
➡ *Carrier concentration of drift layer is stable to at least 60 μm*

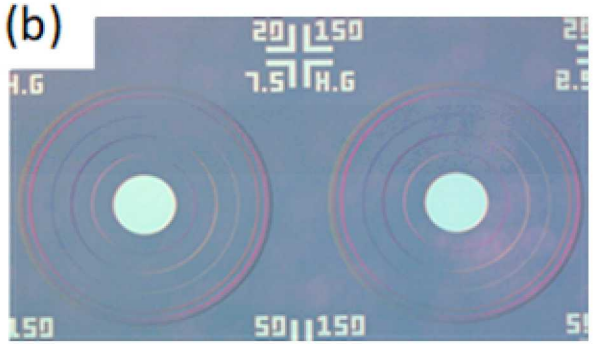
Fabrication of Devices with Thick Drift Regions



CV mapping confirmed highest reverse voltage devices from regions of wafer with drift region carrier density ~2.2-3.0E15 cm^{-3}

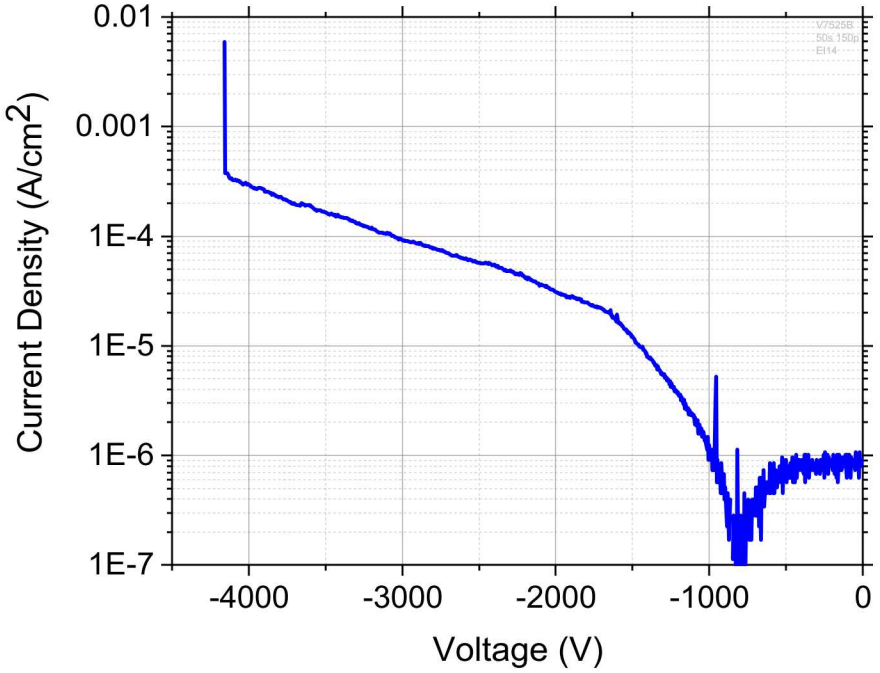
Multi-step ICP-etched JTE



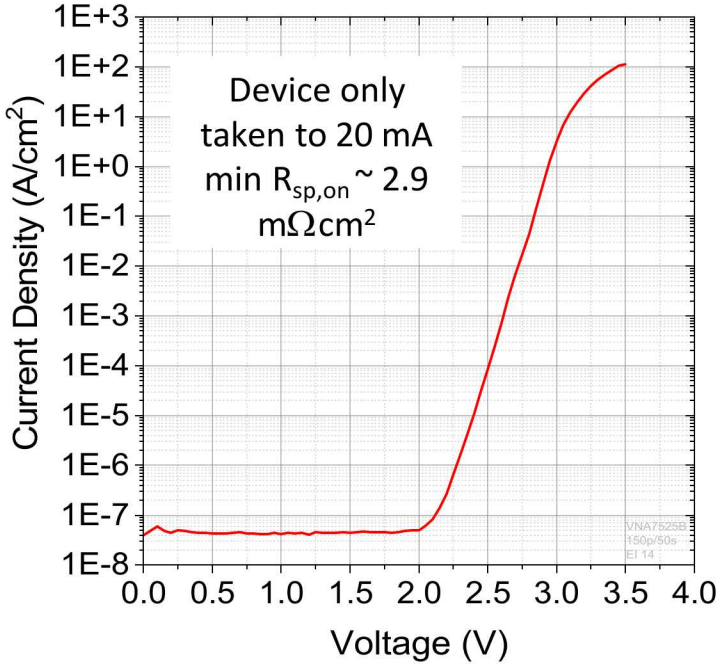


Vertical GaN Technology

REVERSE IV



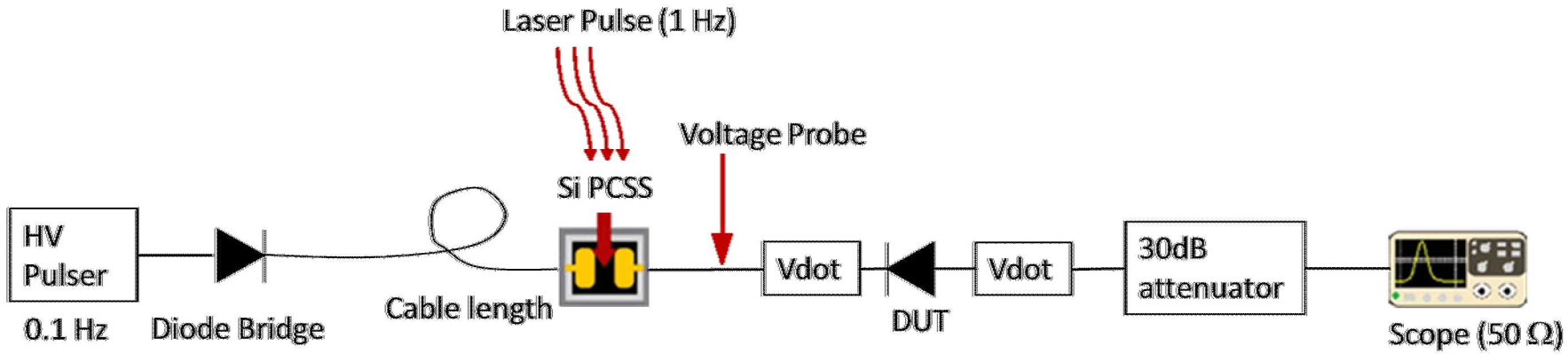
FORWARD IV



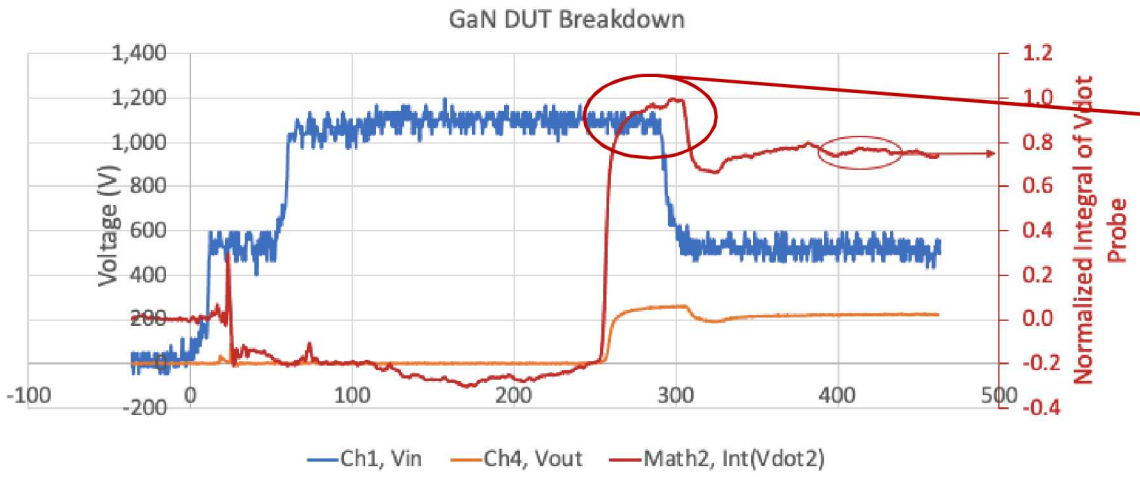
- **Best devices up to -4.6 kV; estimate ~70% V_B of ideal planar diode**
- **Less than 1 mA/cm² leakage @ 80% V_B target**

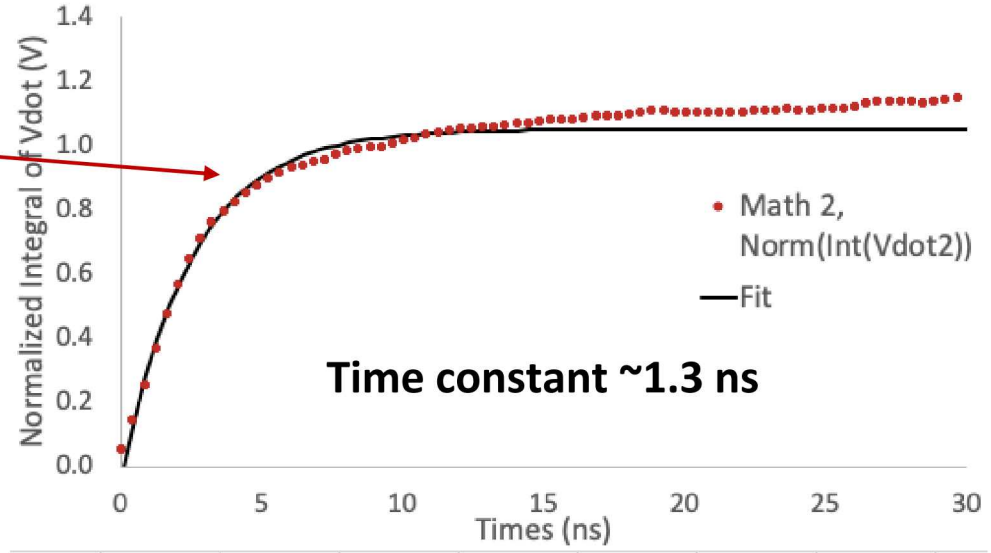
  (Note: Data taken with 10 kV SMU, data below ~1 kV is not very accurate)

Time Response of Breakdown



Tested 1.2 kV vertical GaN diode





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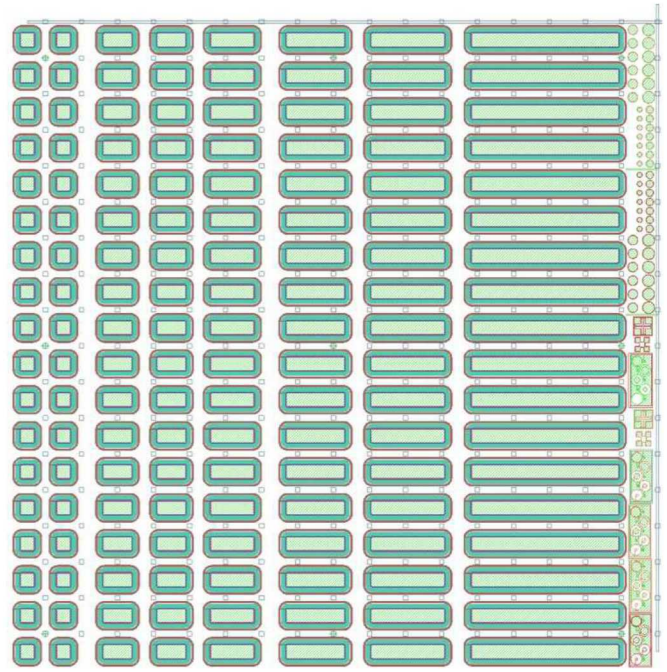
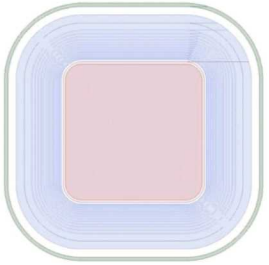
  - **Reliability and FA**

Foundry Mask Layout



Base cell:
0.35 x 0.35 mm² anode

Larger devices scaled only in x-direction to avoid crossing dot-core (for now)



Geometry	Area (mm²)	Devices (per 2" wafer)
A	0.105	280
B	0.215	280
C	0.325	150
D	0.430	150
E	0.535	150
F	1.05	140
Total		1150

Features:

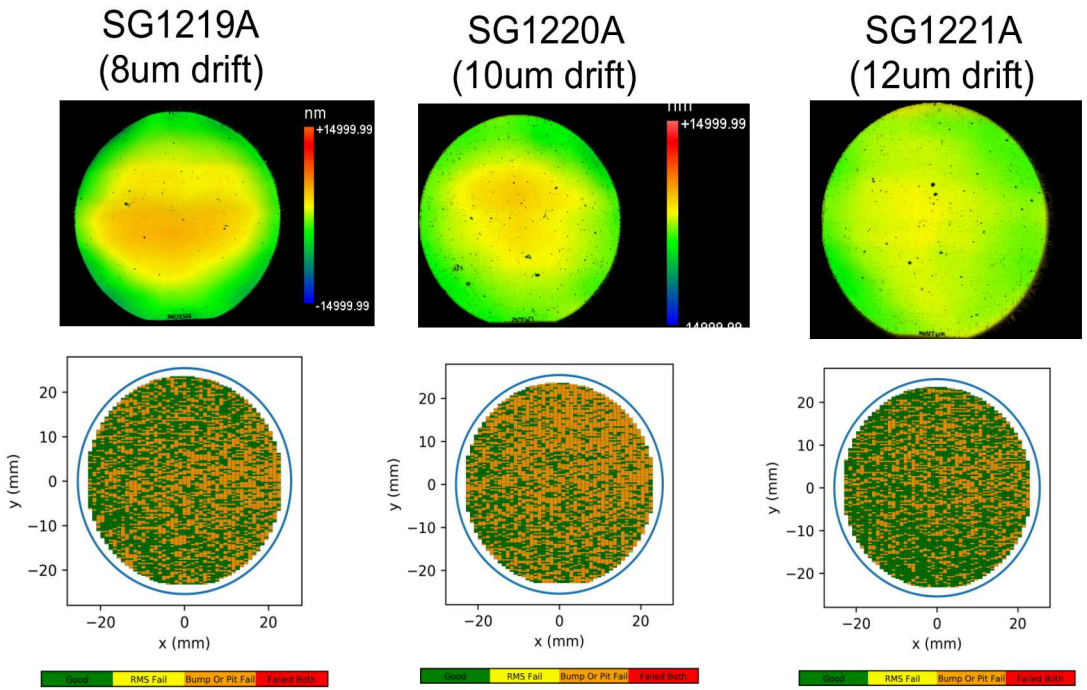
- Global alignment (Type IIa wafers)
- P-GaN ohmic CTLM
- P-GaN Hall
- Isolation test
- Termination test
- Small diameter circular diodes
- JTE and GR termination designs
- Passivation / Overlay for packaging

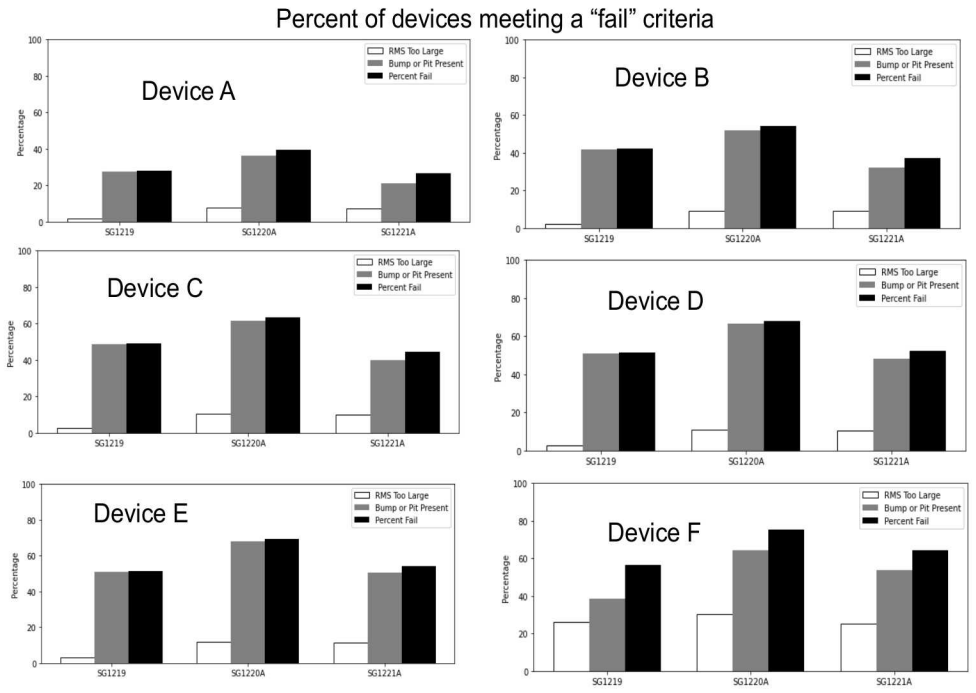
GaN Epi Deliveries for Foundry Process

To date, Sandia has delivered 26 GaN wafers to NRL and 6 to Stanford from the Nippon Sanso reactor for the pilot foundry effort. These are targeted for ~1500 V breakdown for a 1200 V rated device.

	Lot 0 9/24/19	Lot 1 11/27/19	Lot 2 12/20/19	Lot 3 3/2/2020	Lot 4 5/1/2020	Lot 5 7/24/2020
# Wafers	4	4	4	4	7	12
Substrate(s)	(4) Mitsu-LED	(4) Mitsu-LED	(4) Mitsu-LED	(2) Mitsu-LED (1) Mitsu-LD (1) SCIOCS	(7) Mitsu-LED	(12) Mitsu-LED
Drift	8 µm @ 1.3e16	8 µm @ 1.3e16	8 µm @ 1.3e16	8 µm @ 1.3e16	8 µm @ 1.3e16 10 µm @ 1.3e16 12 µm @ 1.3e16	8 um @1.3e16
Purpose/Goal	Varied p+ contact layer for activation and ohmic contact testing	Specifically chosen substrate serial numbers to evaluate wafer-to-wafer and batch-to-batch substrate variability	Varied p-GaN anode thickness to evaluate control of implant process at various target depths	Evaluate different substrate types and vendors with same epi structures	Evaluate dependence of breakdown voltage on drift region thickness	5 wafers to NRL and 5 to Stanford for evaluation of bevel termination; 2 wafers to Stanford for back-side work

Typical Incoming Wafer Metrology



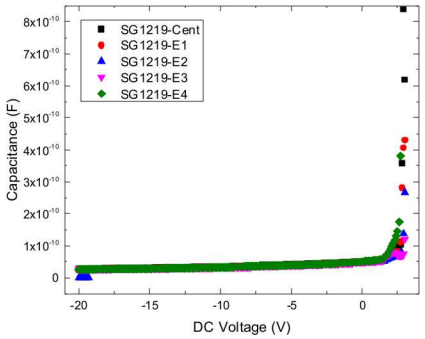


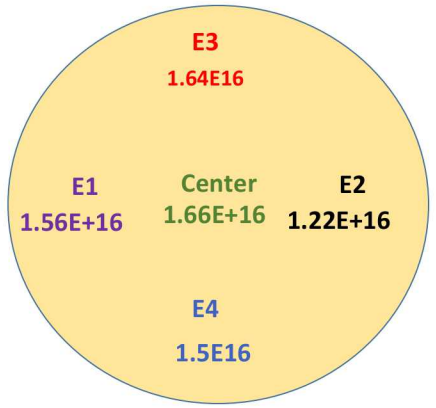
- **Evaluate yield based on particles/pits and RMS roughness**
- **No clear trend in RMS roughness with particle thickness**
- **Evaluate yield for device geometries A-F**

Geometry	Area (mm^2)	Devices (per 2" wafer)
A	0.105	280
B	0.215	280
C	0.325	150
D	0.430	150
E	0.535	150
F	1.05	140
Total		1150

Incoming Wafer C-V Analysis

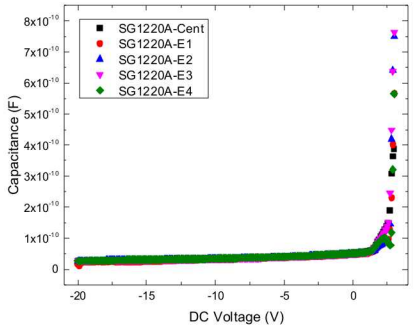
SG1219

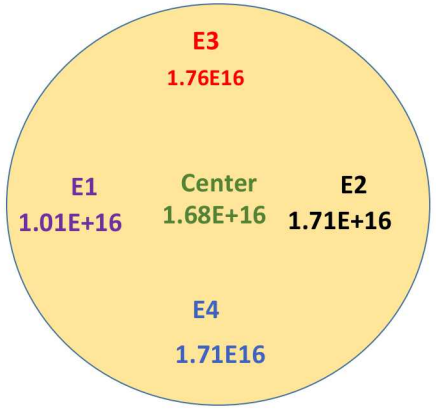




Spec (Sandia) = 1.6E16

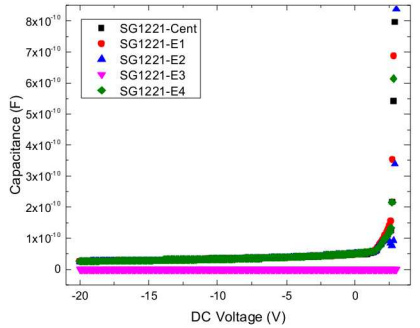
SG1220

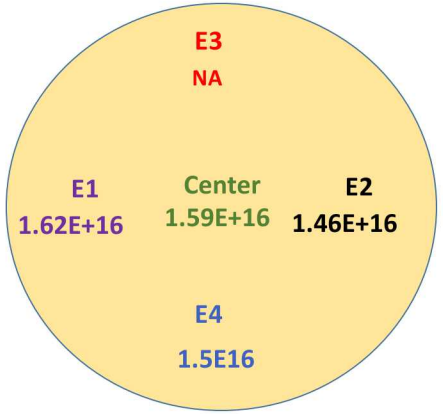




Spec (Sandia) = 1.5E16

SG1221





Spec (Sandia) = 1.7E16

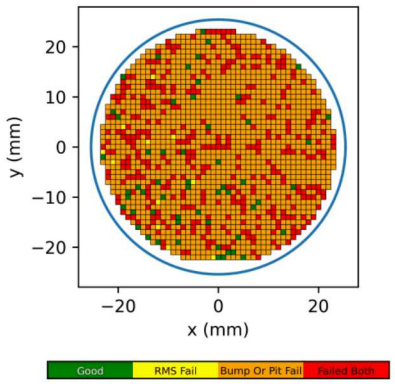
Hg probe C-V is uniform and consistent with design spec and Sandia measurements

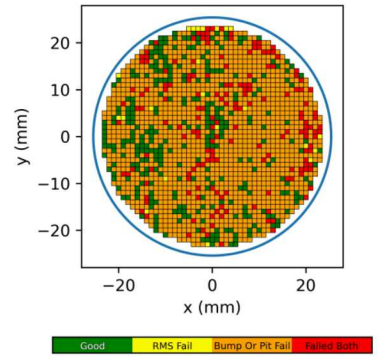
Large-Area Device Analysis

SG1170B (LED-grade)

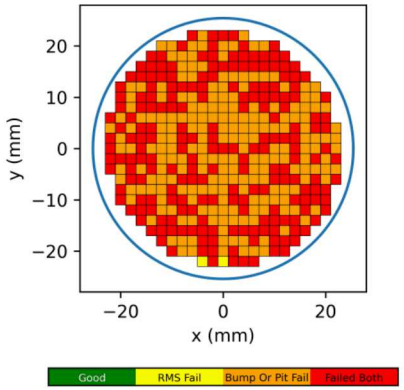
SG1171A (LD-grade)

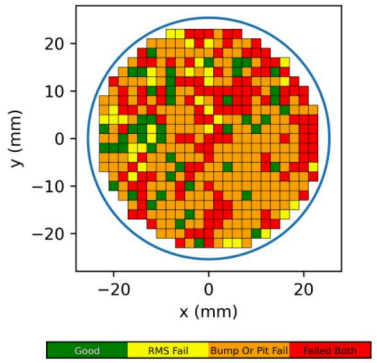
1x1mm device



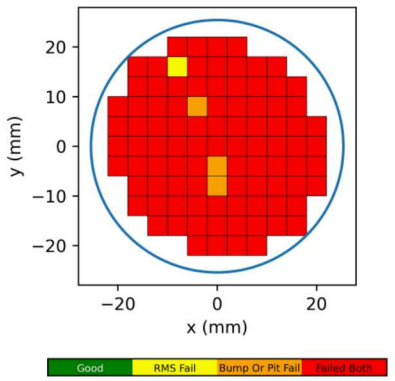


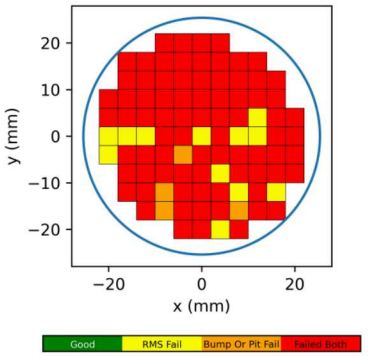
2x2mm device





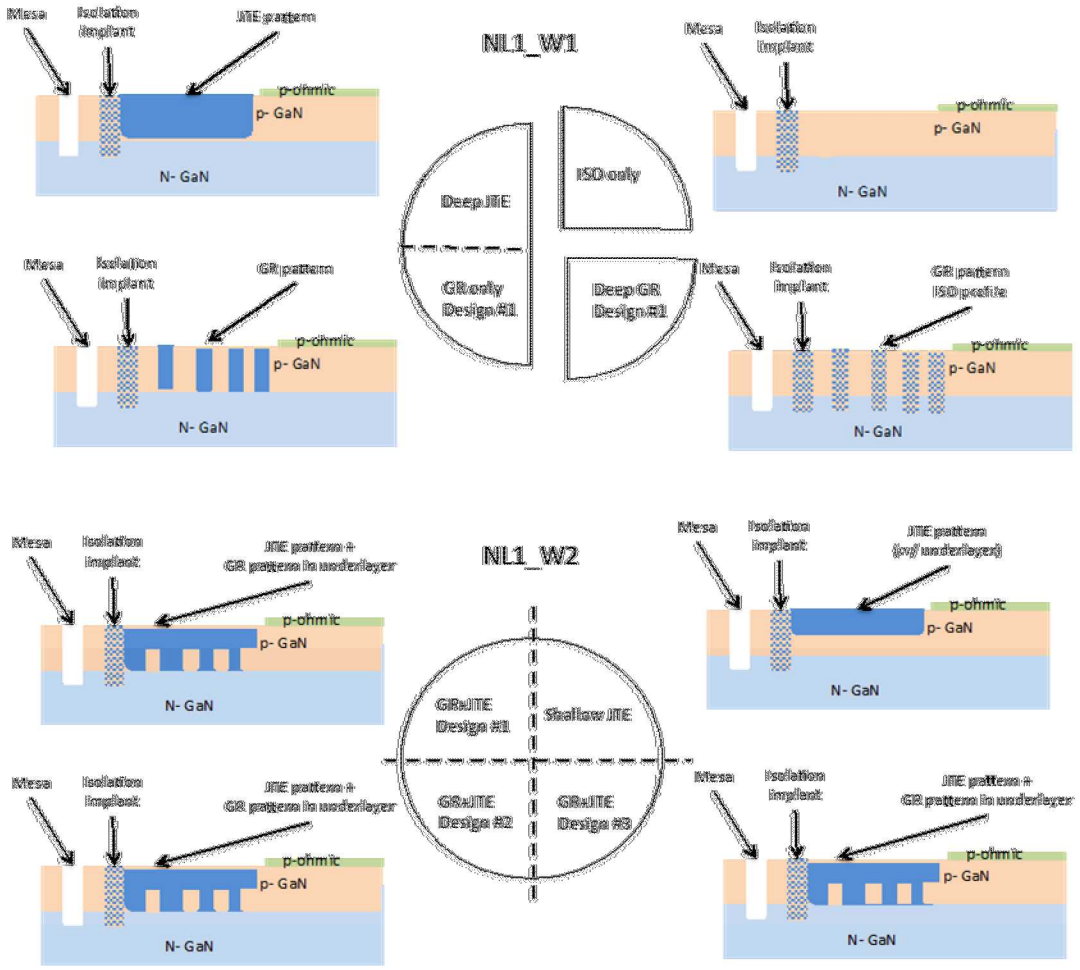
4x4mm device





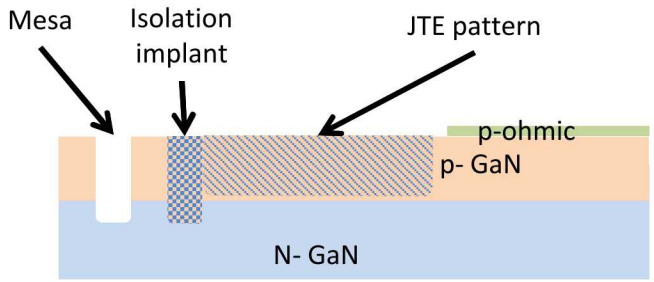
- Extended Zygo analysis to large device dimensions up to 4x4 mm^2 to evaluate scaling effects
- Conclusion: Yield losses are dominated by particles at small device size (red), but 2x2 and 4x4 mm^2 devices also exhibit unreasonably high roughness – median RMS > 40 nm
- Yield is essentially 0% at 4x4 mm^2 device size

Edge Termination DOE

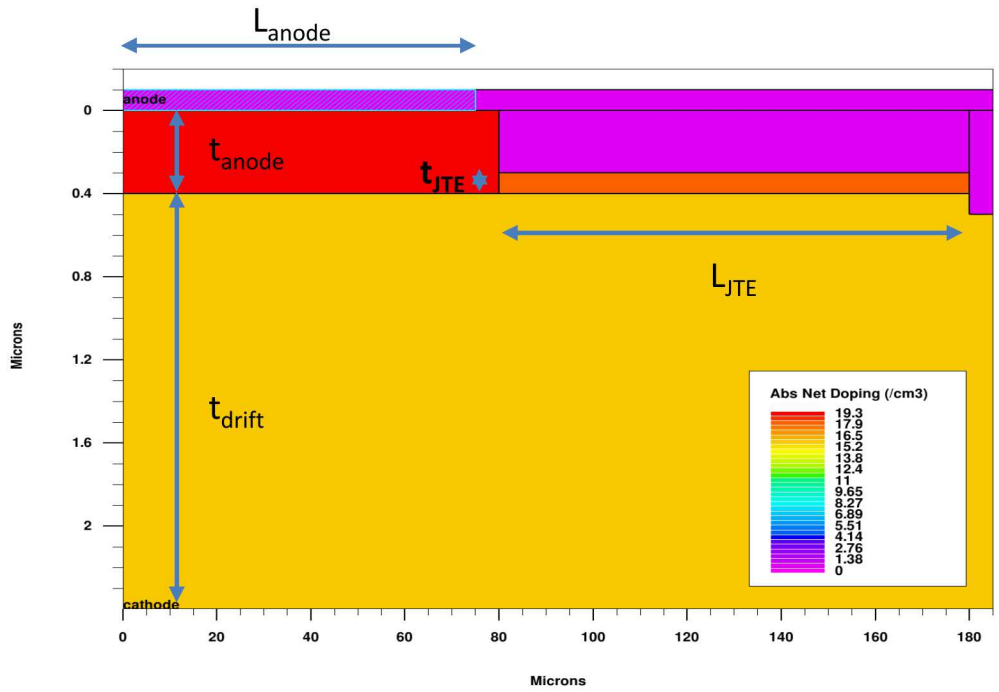


- Edge termination approach based on N implant
- Shallower profile to compensate only part of the anode layer
- Additional control over total depth/dose achieved by utilizing spacer layers and superimposing multiple structures
- 7 designs studied in Lot 1

NRL JTE Optimization via TCAD

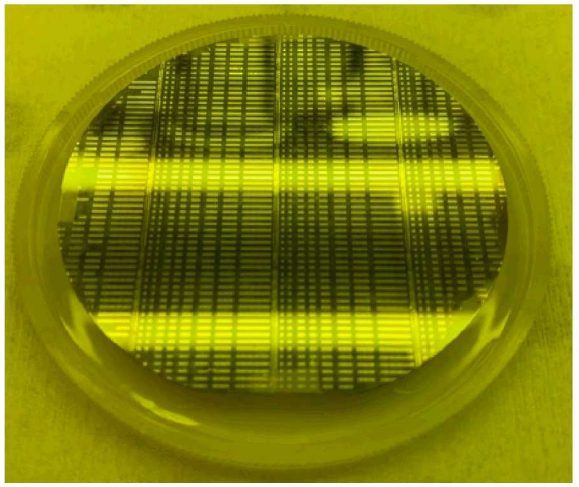


- **Initial edge termination modeling and optimization carried out for uniform implant JTE design**
- **Assumed avalanche coefficients based upon Stanford measurements**
- **Implant distribution modeled as uniform doping profiles**
- **Optimization variable: JTE thickness, secondary variable: JTE layer doping**

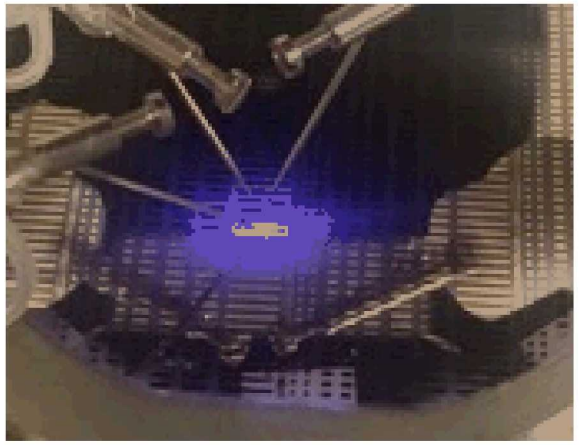


Electrical Testing and Results

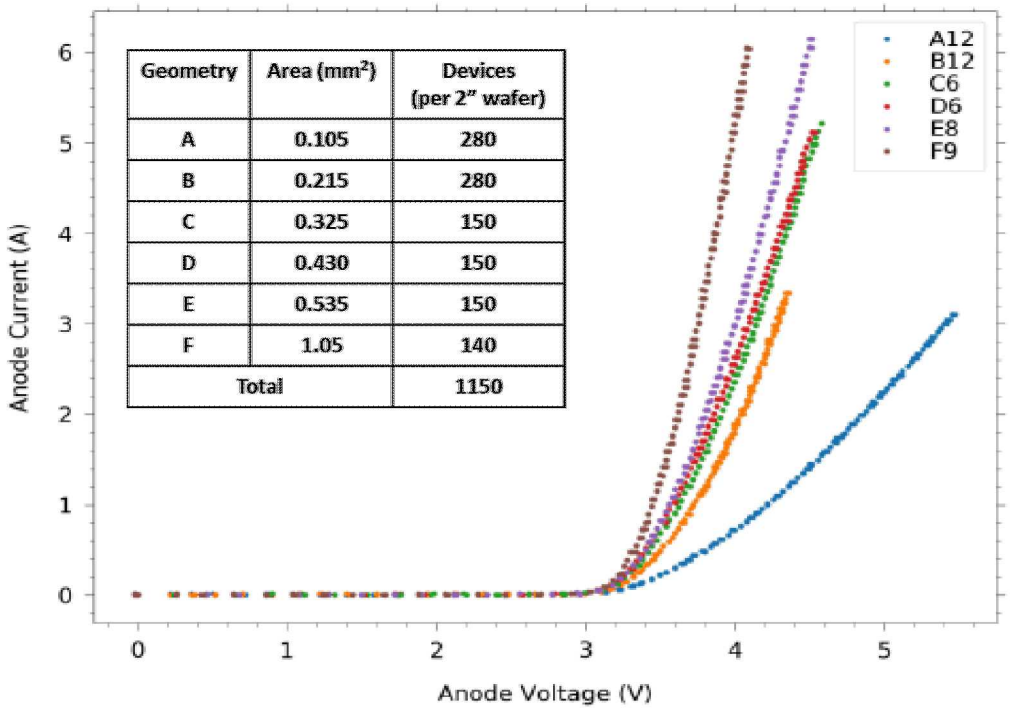
Typical foundry wafer



Wafer under test



Geometry	Area (mm^2)	Devices (per 2" wafer)
A	0.105	280
B	0.215	280
C	0.325	150
D	0.430	150
E	0.535	150
F	1.05	140
Total		1150

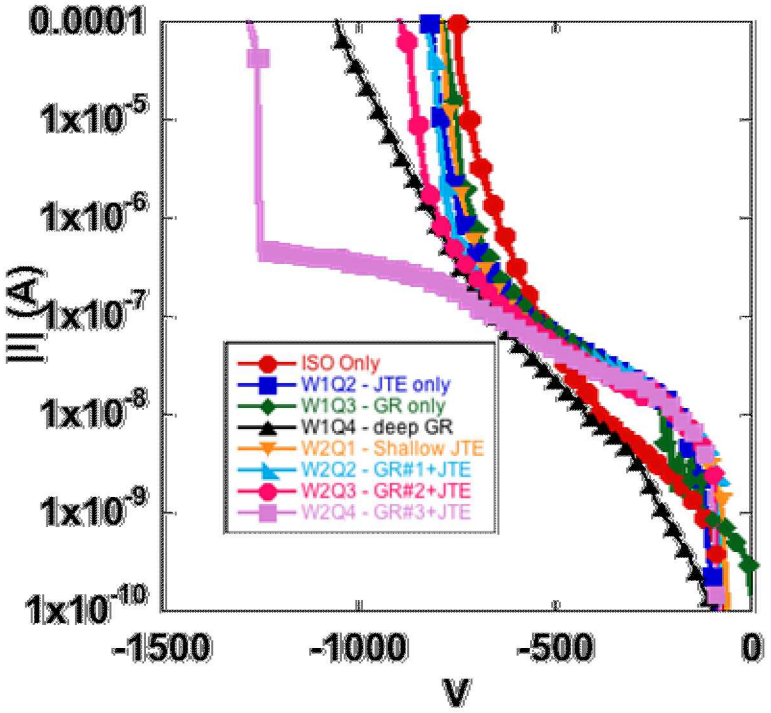


Representative forward I-V curves for devices A-F

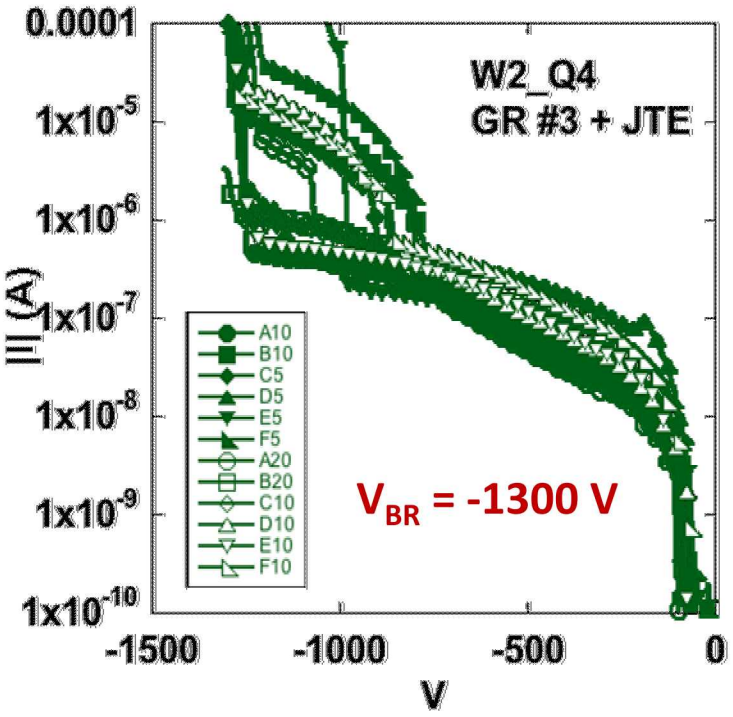
- **Largest devices achieve ~ 6A forward current**

Breakdown Results

All ET designs



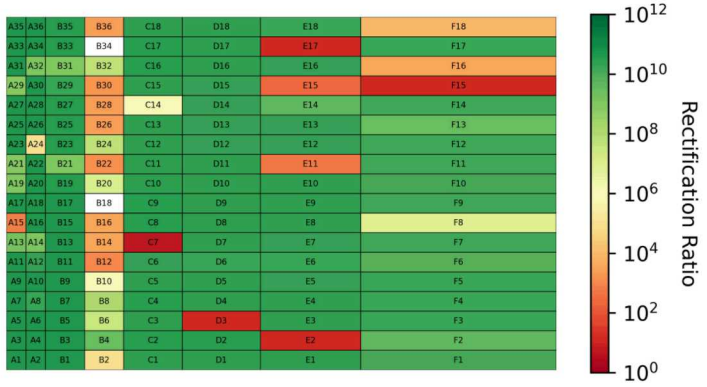
Best ET design



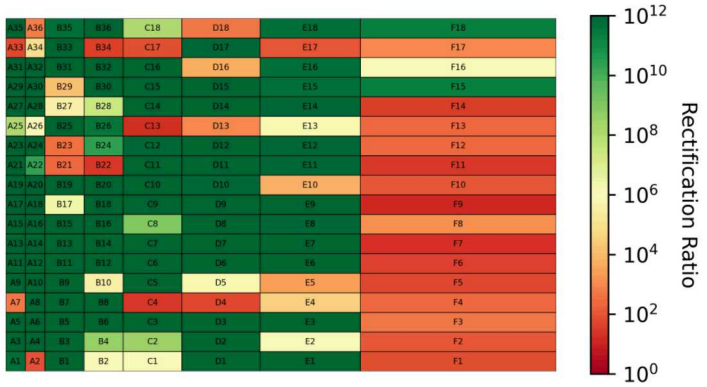
- Isolation profiles alone resulted in high leakage and soft breakdown
- Additional shallow N profiles produced some termination
- Guard ring + JTE design #3 is superior for this anode design (Similar to GR Design #1, which had low photo yield)
- Multiple devices achieve breakdown > 1.3 kV, which is 90% of theoretical parallel-plane value

Device Yield Analysis

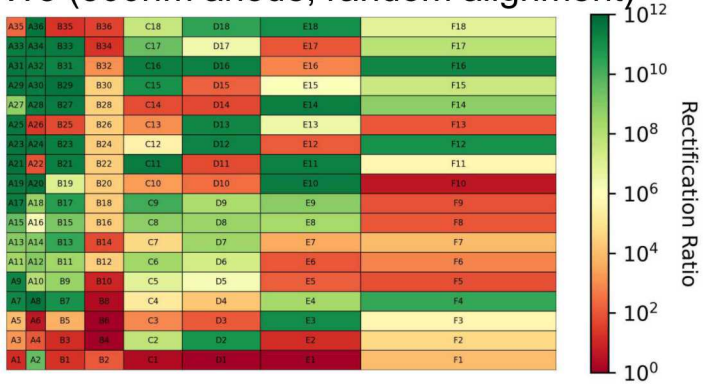
NL2-W1 (base structure, aligned to dot-core)



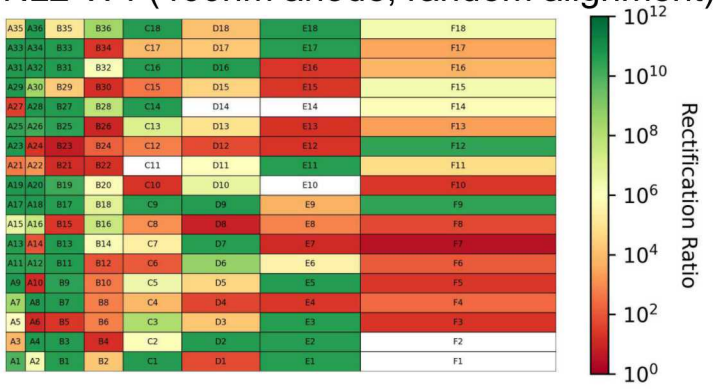
NL2-W2 (base structure, random alignment)



NL2-W3 (300nm anode, random alignment)

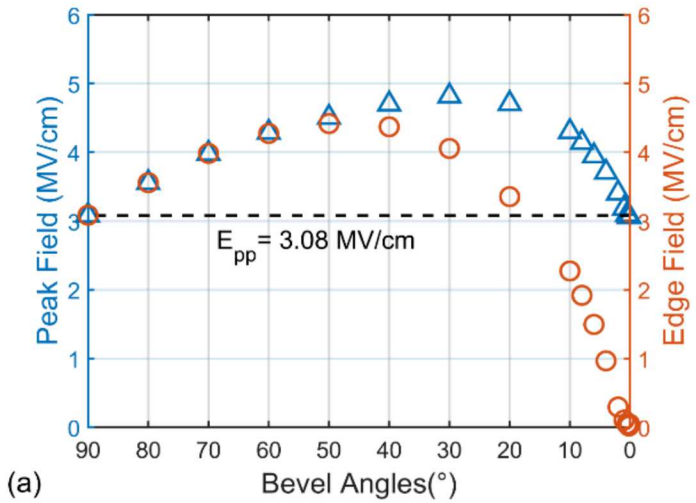


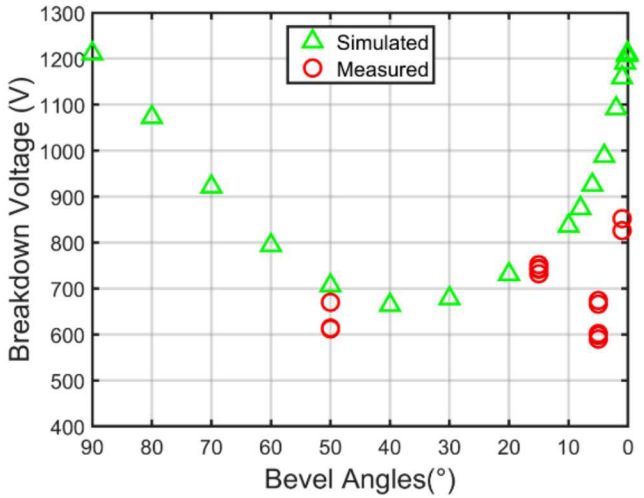
NL2-W4 (400nm anode, random alignment)



- **ON/OFF ratio used for preliminary yield analysis – captures both devices that don't turn on OR don't turn off**
- **Excellent yield on 2 wafers, not as good on later wafers**
- **Related to particles or alignment to dot-cores?**

Alternate Foundry Edge Termination: Bevel





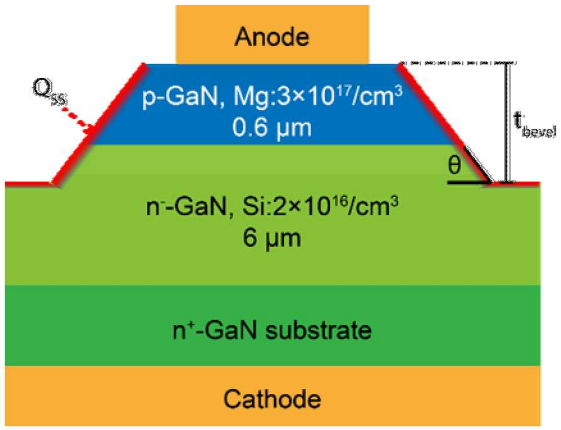
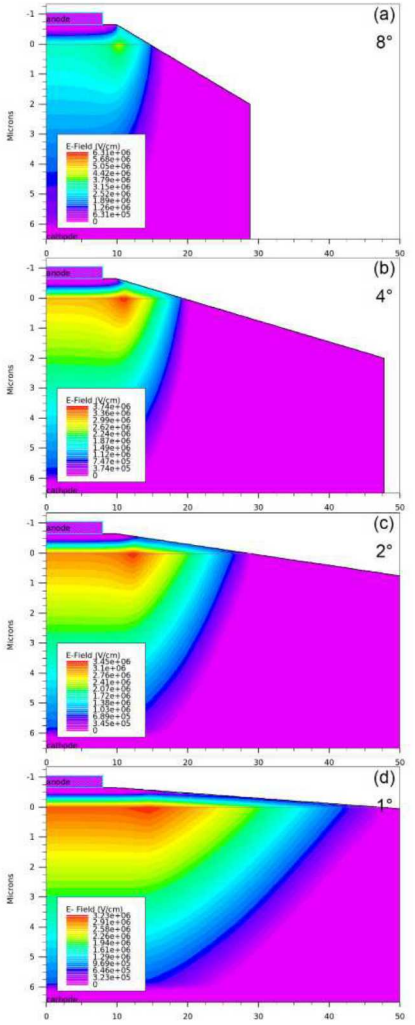


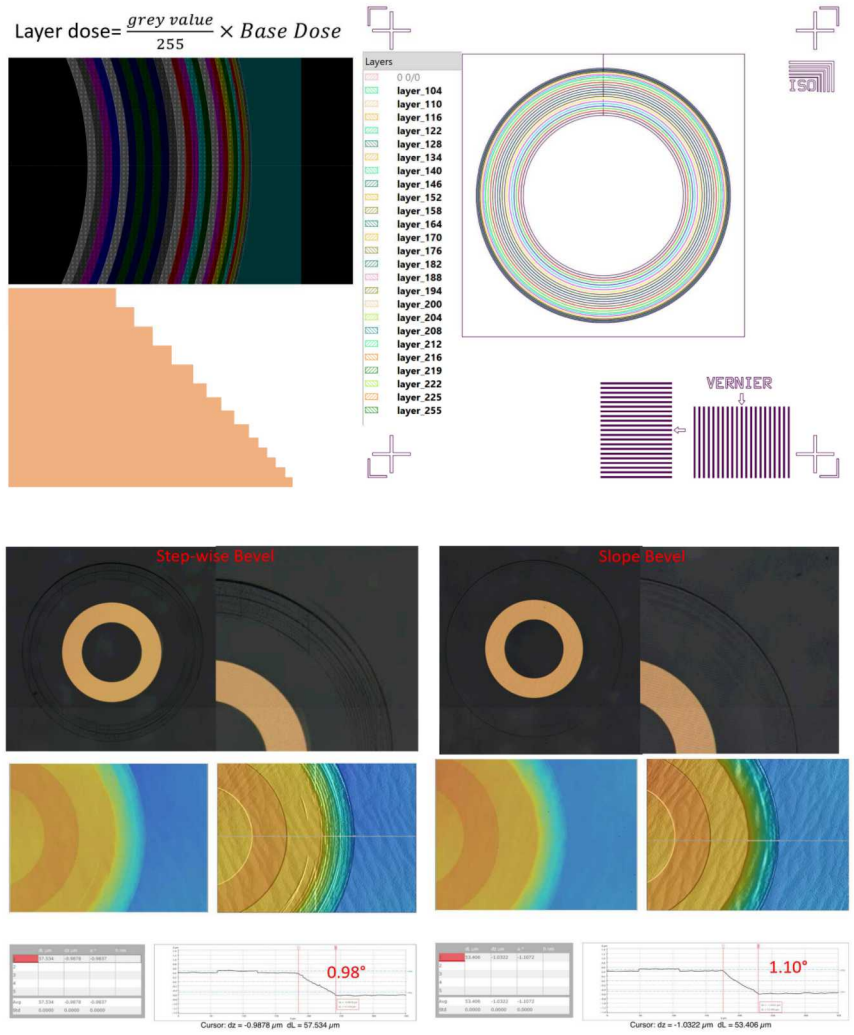
TABLE I
V_{BR} AND E_{PP} FOR VARIOUS DOPING CONFIGURATIONS

Doping Configuration	Avalanche Voltage V_{BR}	Parallel Plane Peak Field E_{PP}	Transition Angle θ_t
p-3E17 /n-2E16 (Baseline doping)	1212.5 V	3.08 MV/cm	10°
p-3E16 /n-2E15 (Doping /10)	1624.9 V	2.6 MV/cm	20°
p-6E17 /n-4E16 (Doping ×2)	724.5 V	3.26 MV/cm	10°
p-1E17 /n-2E16 (N_a /3)	1254.4 V	3.06 MV/cm	20°
p-9E17 /n-2E16 (N_a ×3)	1170.0 V	3.03 MV/cm	4°
p-3E17 /n-6E15 (N_d /3)	1522.3 V	2.77 MV/cm	10°
p-3E17 /n-6E16 (N_d ×3)	570.1 V	3.38 MV/cm	30°

[a]The thickness of p and n-type region are kept constant as 0.6 µm and 6 µm respectively.



Bevel Edge Termination Fabrication

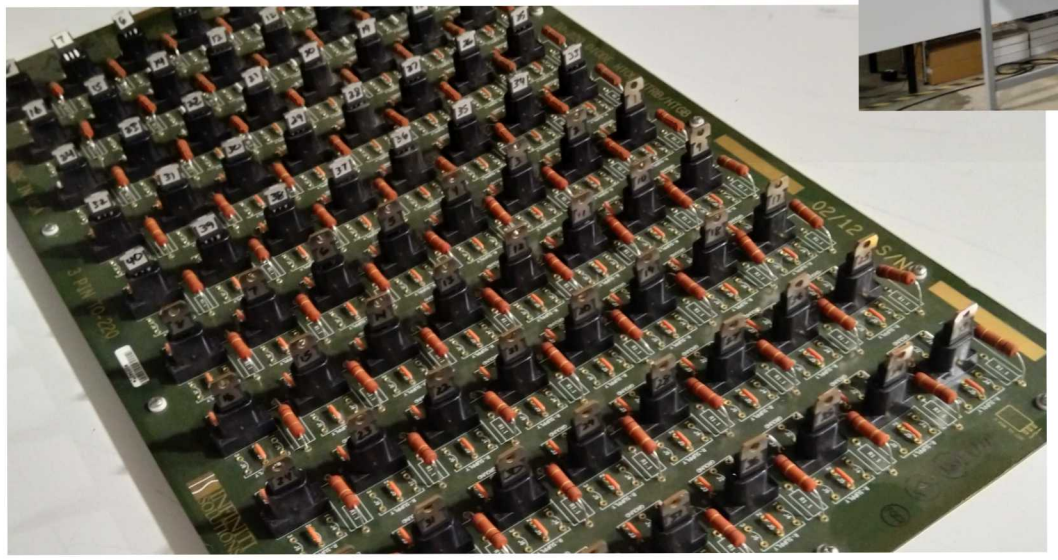


- Fabricated diodes with 1°, 5°, 15°, and 50° bevel terminations
- Used available epi with 6 μm thick drift region and 2E16 cm^{-3} doping
- Higher bevel angles use hard-baked photoresist to achieve angle; 1° bevel uses grayscale lithography

Reliability and Failure Analysis

- Extensive reliability and FA effort ongoing
- Starting with pre-existing diodes, transitioning to foundry diodes

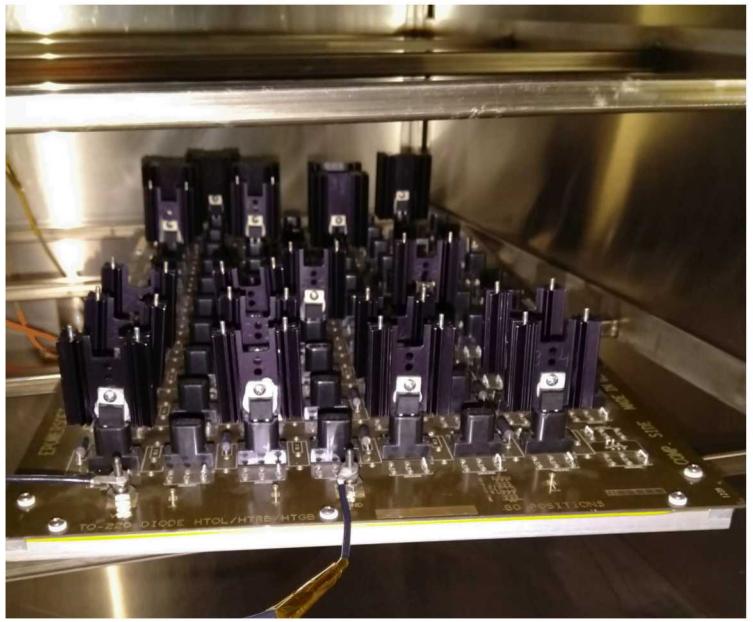
Reliability test ovens and power supplies



Test board

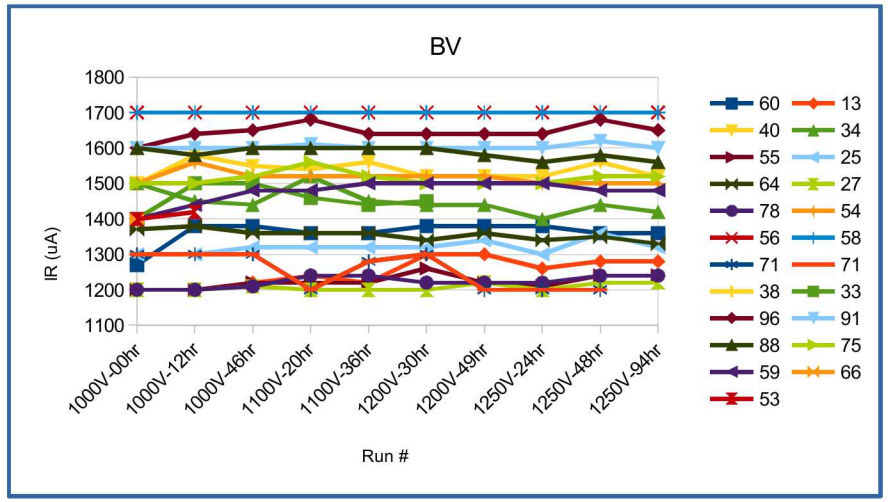
HTRB Reliability Testing

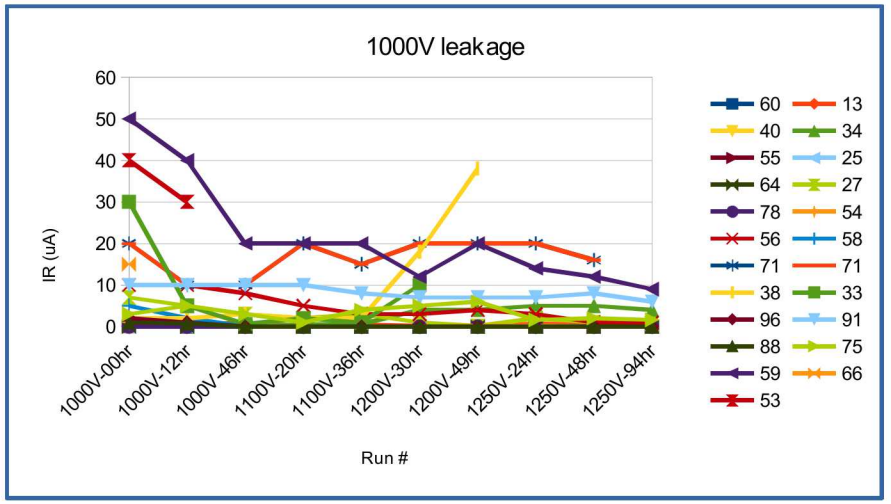
- Observe temperature stability
- Observe initial test group at ~48 hours HTRB and increase stress
  - Used 1000, 1100, 1200, and 1250 V stress points
- 2 devices failed at 1000 V
- 2 devices failed at 1200 V
- 2 devices failed at 1250 V
- 1 device sent to FA based on increased current
- 1 device sent to FA to identify leakage mechanism
- Reads made at room temperature using curve-tracer



Ozgur what was temperature for this test?

Representative HTRB Test Results

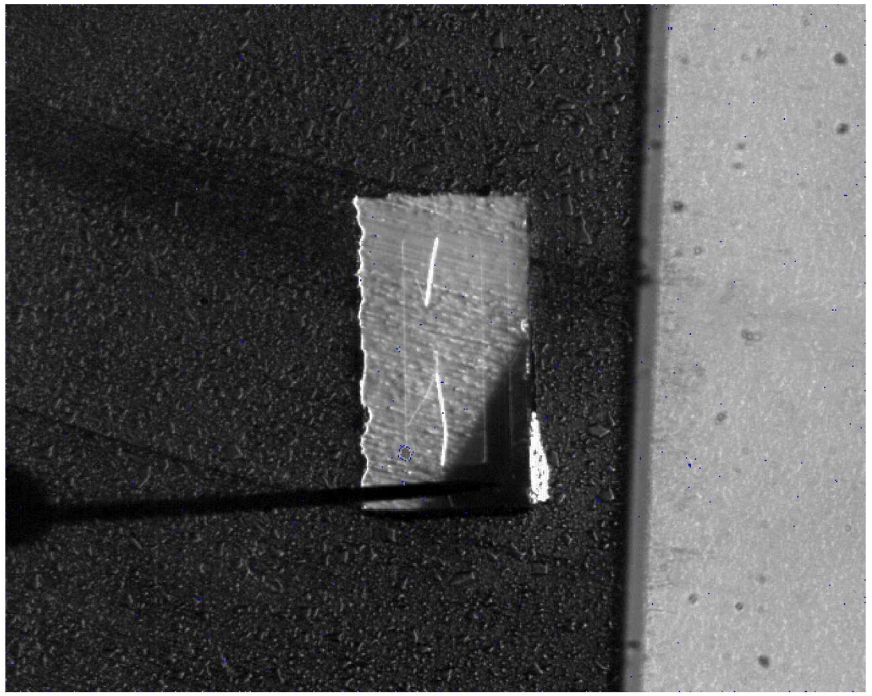




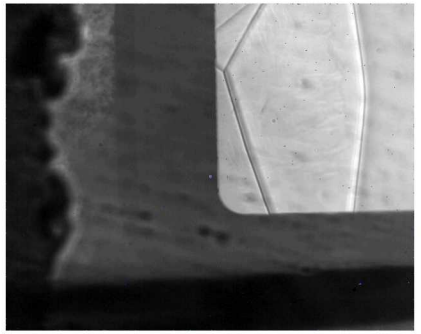
- **BV values stay approximately stable**
- **1000 V leakage shows 3 types of devices:**
  - **Stable I_R (1st leakage mechanism)**
  - **Increasing I_R (2nd leakage mechanism)**
  - **Decreasing I_R (3rd leakage mechanism)**

Failure Analysis of HTRB-Failed Device

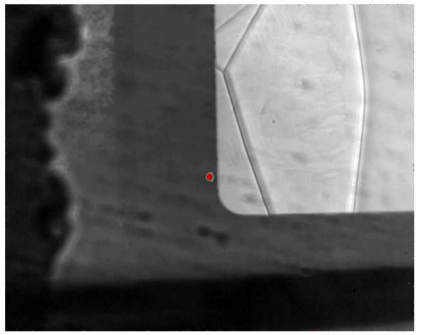
Emission Microscopy (EMMI) results



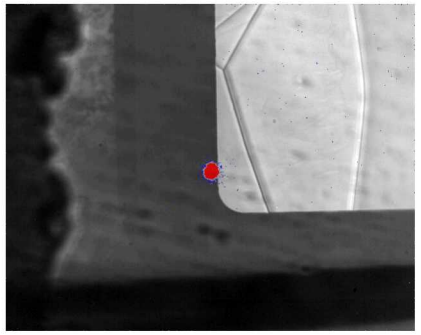
1 kV, 0.5 uA @ 2.5X



800 V @ 20X



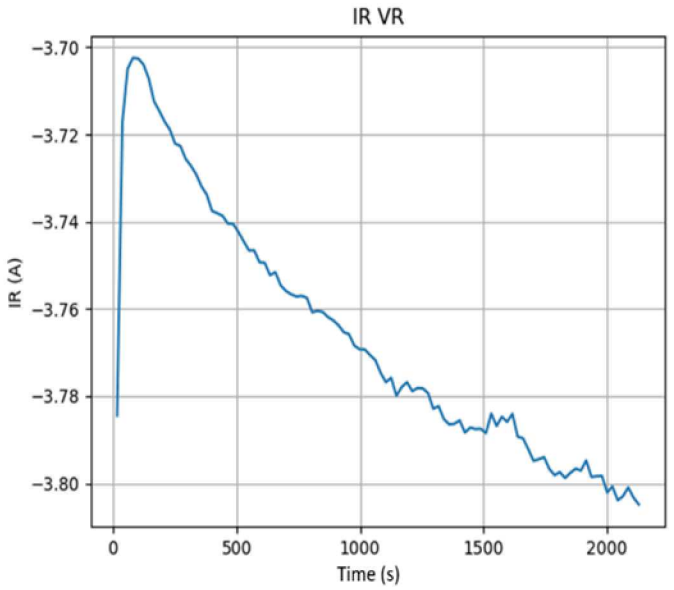
900 V @ 20X



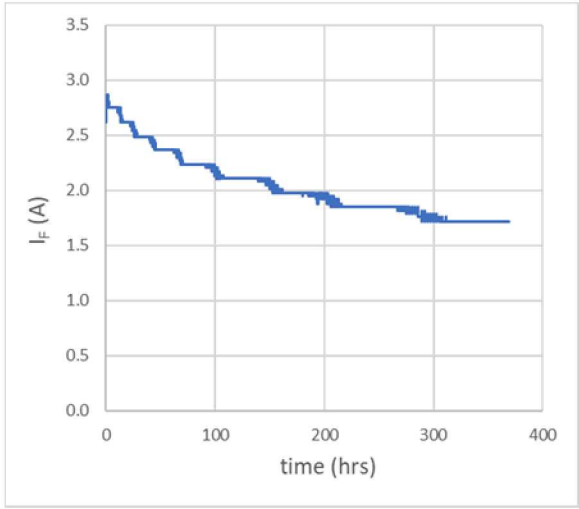
1000 V @ 20X

Individual HTRB and HTOL Testing

- **Individual testing of devices avoids problems with parallel testing**
  - **For example, high-impedance load in parallel HTRB**
- **Individual power supplies connected directly to DUTs**
  - **IR up to 20 mA (i-HTRB), IF up to 60 A (i-HTOL)**



HTRB I_R vs. time characteristic at 150˚C and 1410 V



HTOL I_F vs. time characteristic at X˚C and X V

Ozgur can you please fill in temperature and voltage

Summary

- Introduction
- High-Voltage GaN Diodes for EMP Protection
  - Growth
  - Processing
  - Testing
- GaN Diode Foundry Process
  - Growth and Wafer Metrology
  - Processing and Edge Termination
  - Electrical Results and Yield
  - Reliability and FA

Questions?
Bob Kaplar: rjkapla@sandia.gov

arpa·e CHANGING WHAT'S POSSIBLE

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