SAND2020-10192C

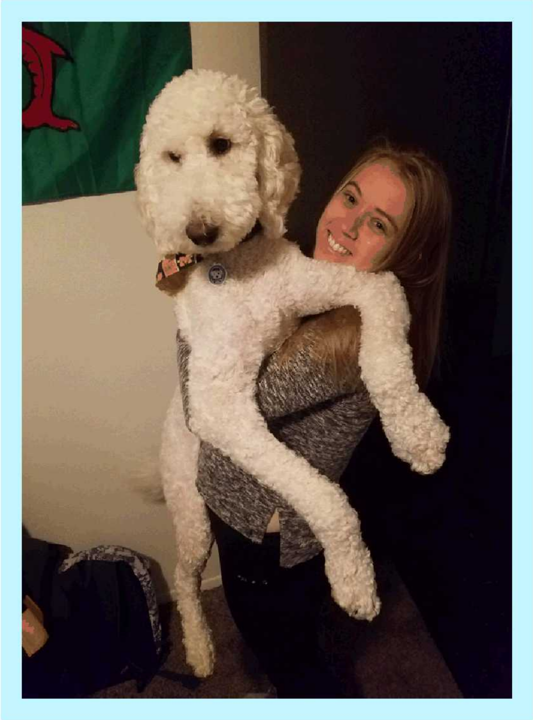
Heterogenous Integration Interconnects

Summer Presentation 2020
Kimberly Beers
Mentor/Manager – Drew Hollowell/Andre Claudet
Org. 5232
kbeers@sandia.gov
kimbeers@umich.edu; kimberlyebeers@ufl.edu

Introduction: About Me

SNL Graduate R&D Intern

- **2019**, Onsite 858EL, Micro-Fab, and Packaging Lab
- **2020**, 100% Virtual Intern



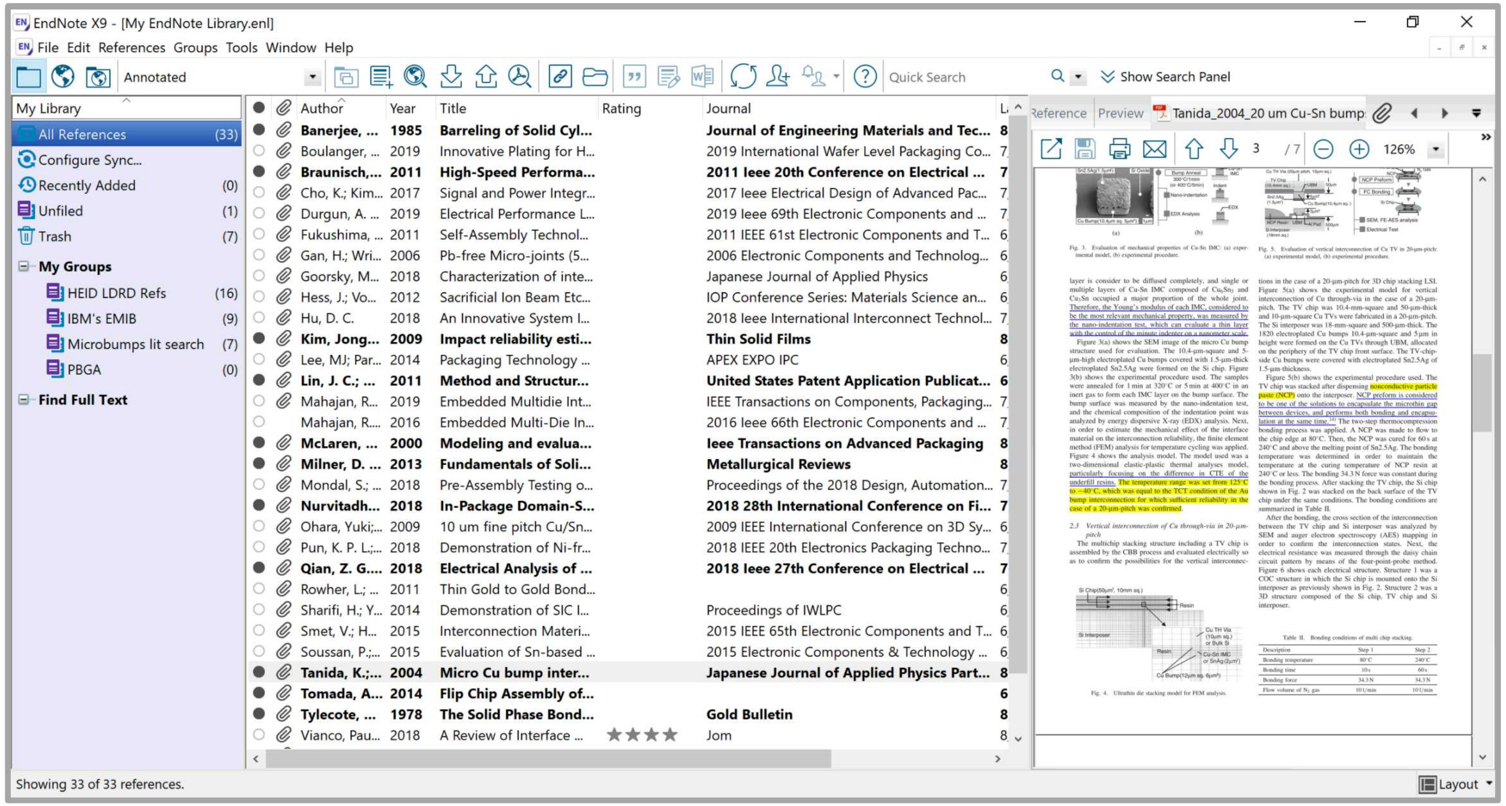
- B.S. in Materials Science and Engineering – University of Florida, 2018
- M.S. in Materials Science and Engineering – University of Florida, 2020

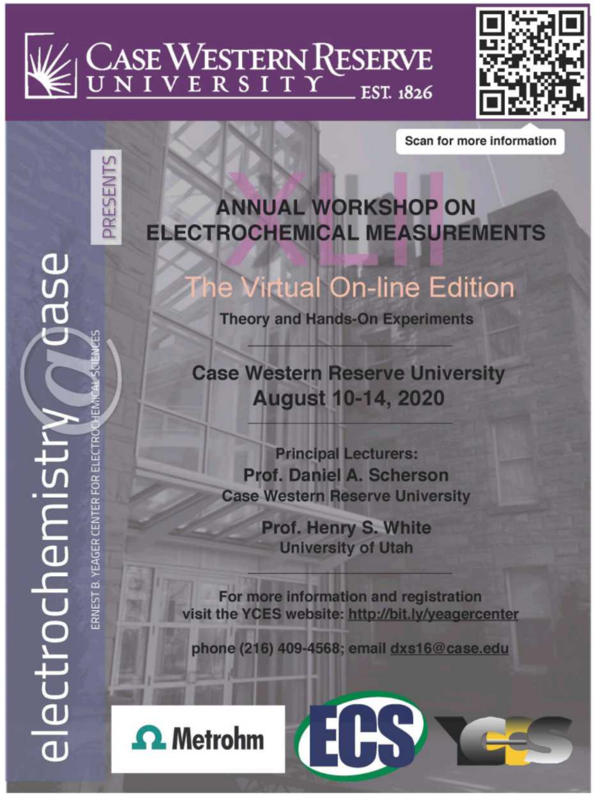
- Ph.D. in Electrical Engineering – University of Michigan, Beginning this Fall 2020
  - Microsystems and MEMS – Thermoelectric Generation for MEMS Devices

Tools & Training

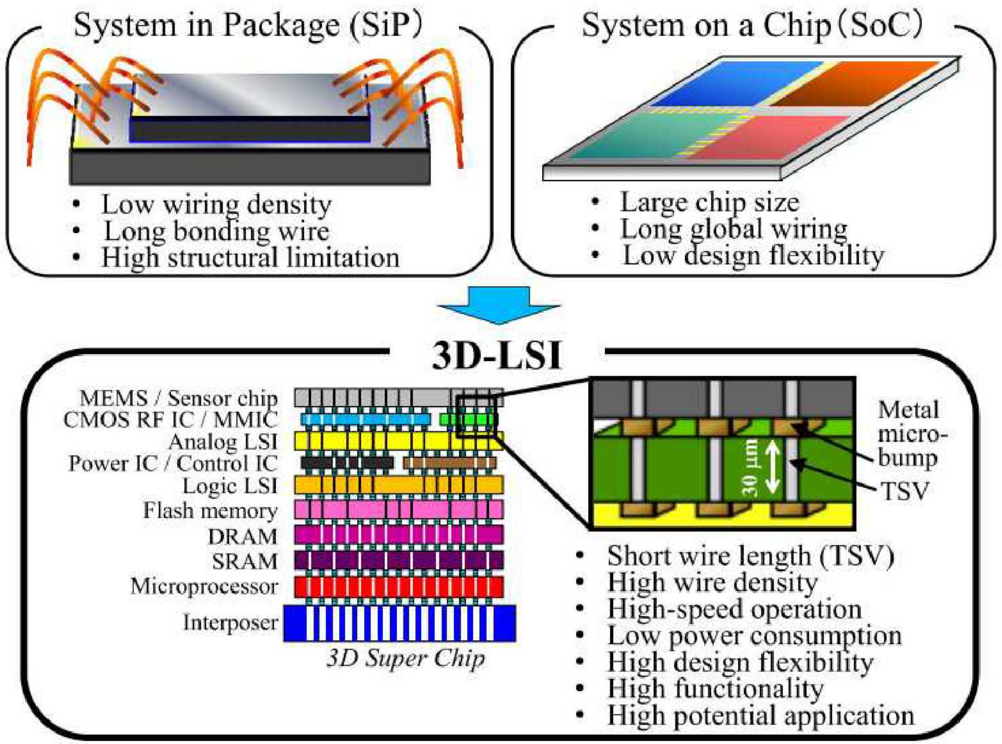
- EndNote
- Sandia Technical Library
- JMP

- Corporate Mandated Trainings
- Virtual Case Western Electrochemistry Workshop





Motivation for Heterogeneous Integration



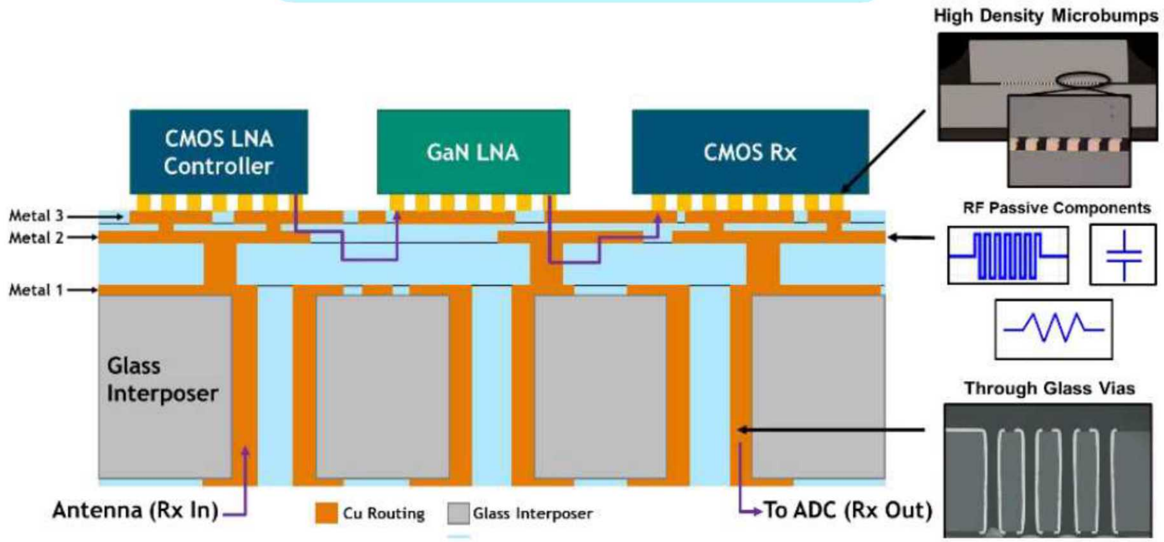
Fukushima, T., et al. (2011)

- High speed
- Low power
- Reduced chip size
- High throughput

Background information on LDRDs

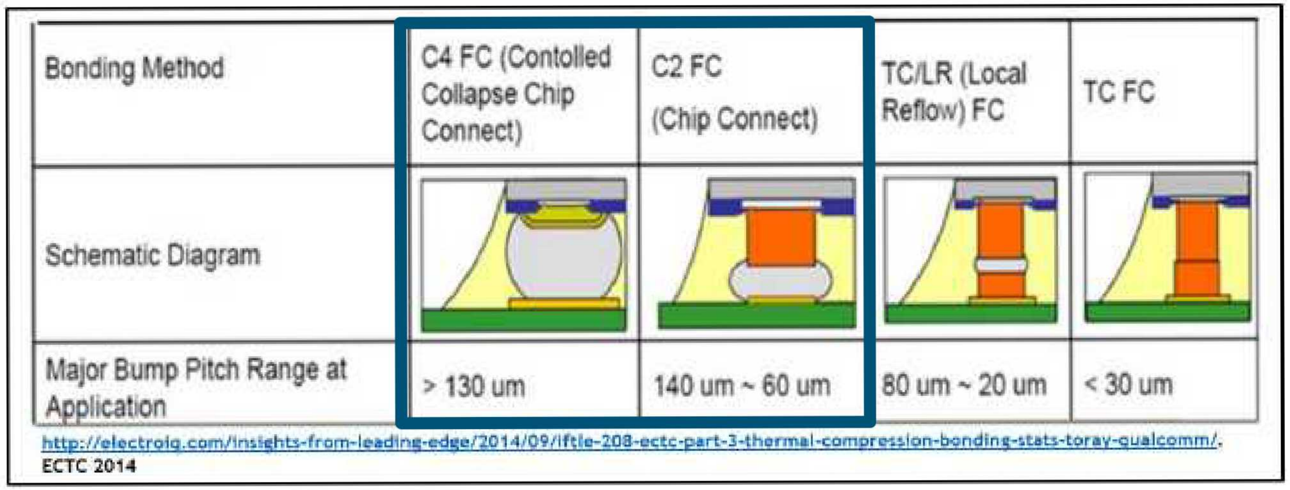
- Heterogenous Ecosystem Interconnect Design (HEID)
- Heterogeneous Integration for Parasitic Loss Reduction in RF Microsystems (HIPR-RF)

Both LDRDs accepted for funding!!



C4 Flip Chip Development (Last Summer's Work)

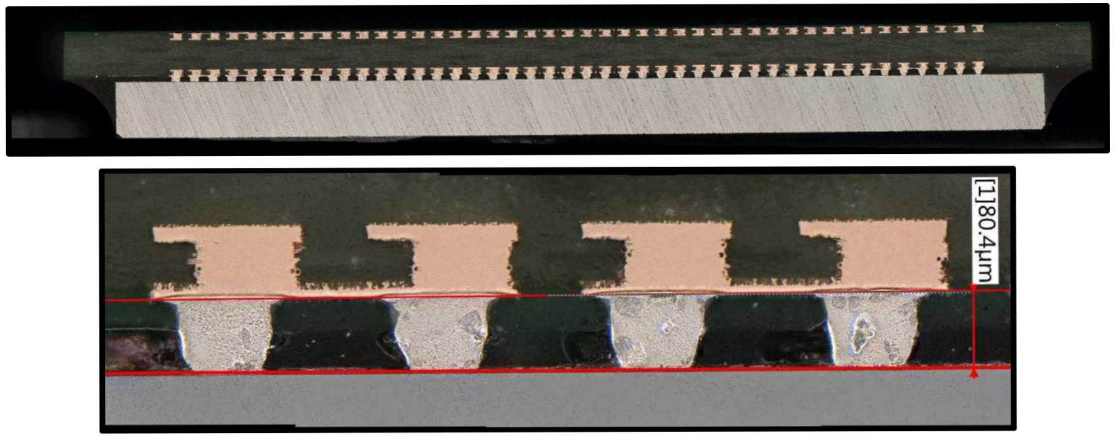
Controlled Collapse Chip Connection (C4) is used to connect chips by means of solder bumps partially crushed between two chip surfaces



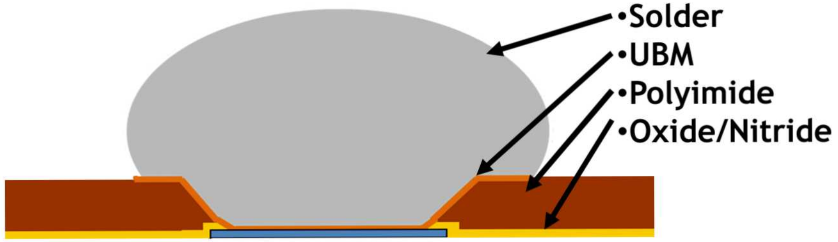
Bonding Method	C4 FC (Contolled Collapse Chip Connect)	C2 FC (Chip Connect)	TC/LR (Local Reflow) FC	TC FC
Schematic Diagram				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um

http://electroiq.com/insights-from-leading-edge/2014/09/iftle-208-ectc-part-3-thermal-compression-bonding-stats-toray-qualcomm/, ECTC 2014

Initial C4-like flip chip bonding results

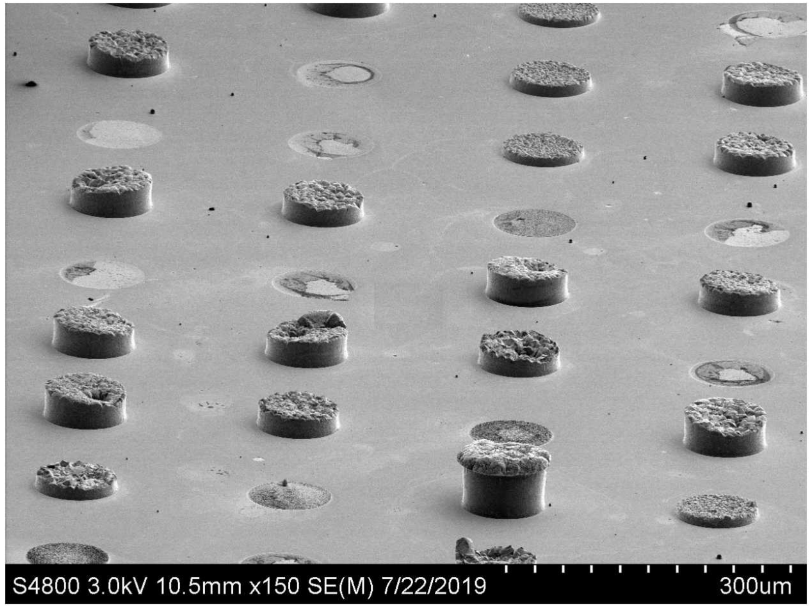


Standard solder bump integration

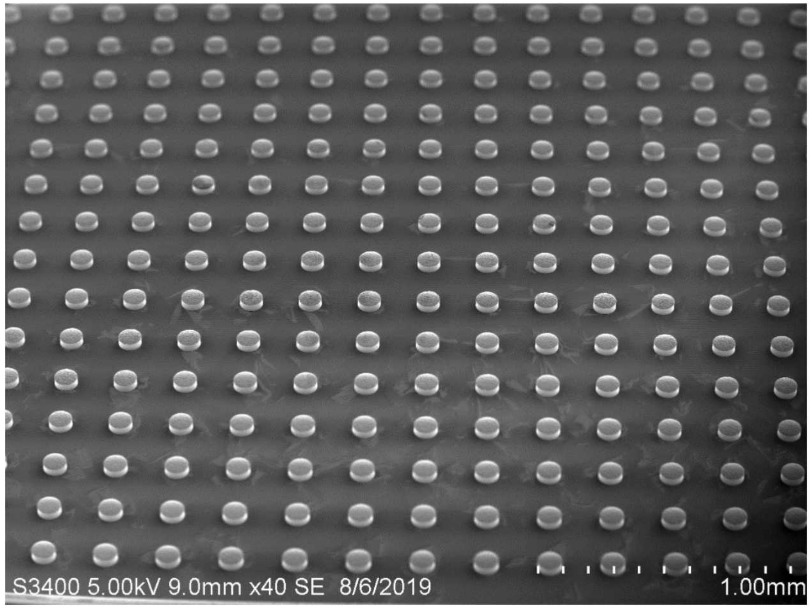


SnAg Plating Development

Before:



After:



Experimental Variables

- Electrical Contact
  - Alligator clamp
  - Duck bill clamp with Cu foil
  - Pogo pin
- Controlling Plating Area
  - Tape
  - XP2000
- Current Density
  - 200mA/cm^2
  - 100mA/cm^2
  - 80mA/cm^2
  - 60mA/cm^2
  - 30mA/cm^2

  (100–60mA/cm^2: TDS recommended range)
- Height of Bumps
  - 10µm
  - 45µm
- Cu Seed Metal Etchants
  - 1:1 acetic acid and 30% H_2O_2
  - 30% NH_4OH + sodium chlorite

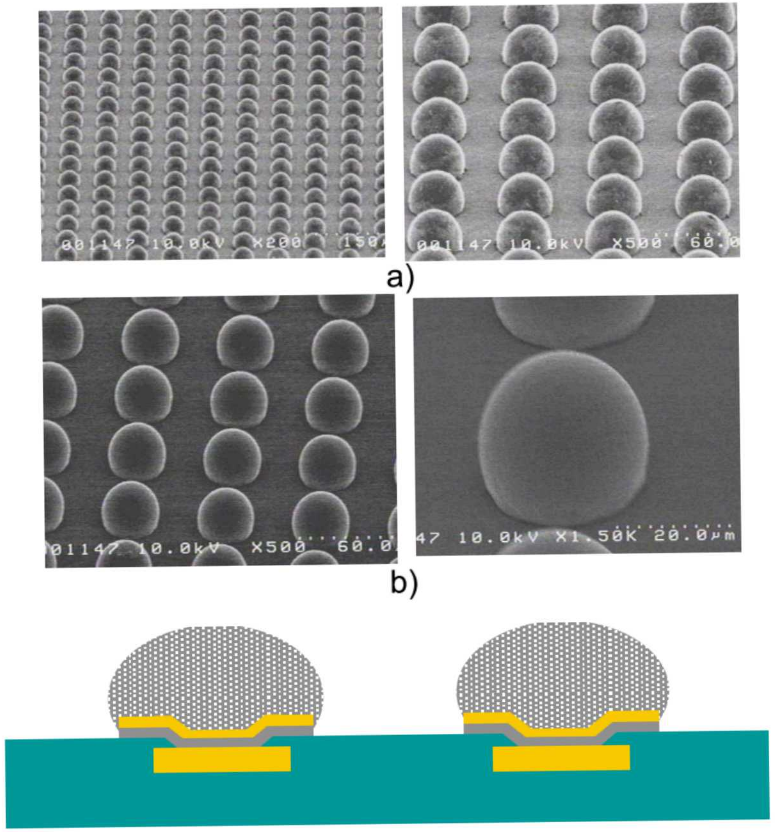
51x51 array/die

- 90µm bump diameter
- 50µm PR height
- 40µm bump height

Directed Study: High Density Interconnects

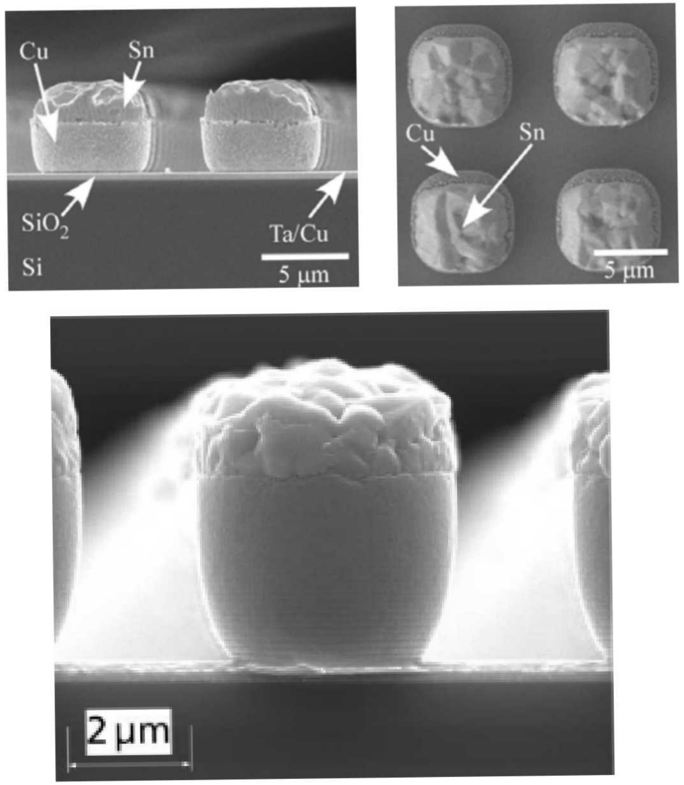
- Ultra-fine to fine pitch ranging from 5-100 μm

C4 solder microbumping



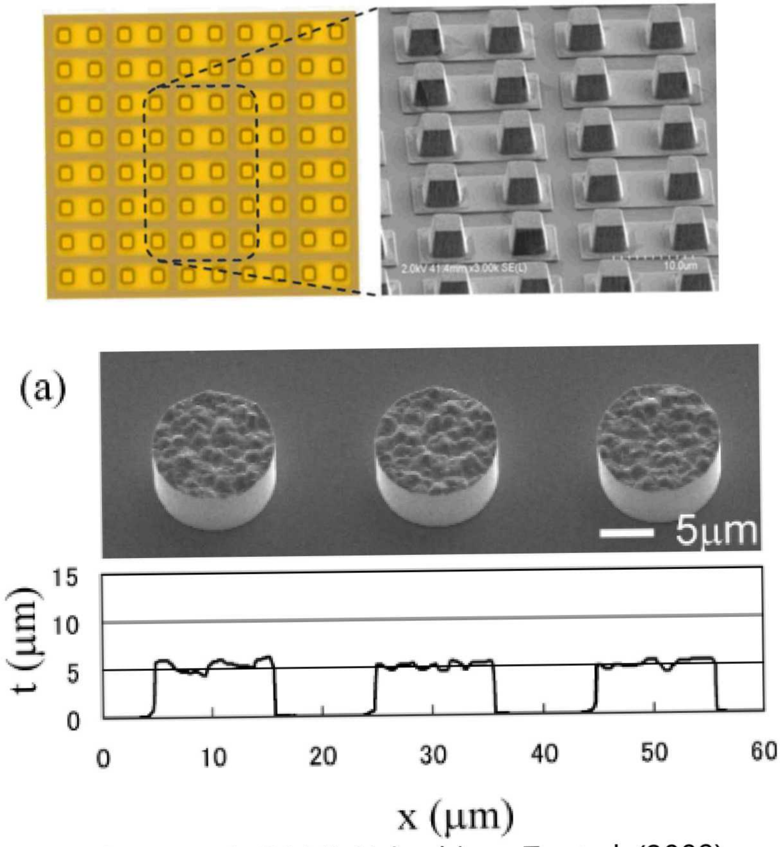
Gan, H., et al. (2006)

Cu pillars



Ohara, Y., et al. (2009), Hess, J. and H. Vogt (2012)

Au microbumps



Sharifi, H., et al. (2014), Yokoshima, T., et al. (2009)

Common Intermetallic Contact Materials and Interfaces

- Microbumps: Cu, Au, In
- Solders: SnPb, CuSn, SnAg
- Under Bump Metallization (UBM): Electroless-Ni, Electroless-Pd, Immersion-Au (ENEPIG), Electroless-Ni, Immersion-Au (ENIG)

SnPb:
- Good control of height uniformity

CuSn:
- Favorable intermetallic adhesion
- Pb-free
- Low resistance

Gan, H., et al. (2006)

SnAg:
- Pb-free
- Low melting temperature (~221^{0}C) *relative to other Pb-free alloys

Cu:
- Low CTE
- Low resistance
- High mechanical strength
- Good control of bond line thickness

Soussan, P., et al. (2015)

Au:
- Low resistance
- No native oxide
- High ductility

Pun, K. P. L., et al. (2018).

In:
- Good electrical and thermal conductivity
- Low melting temperature (~156^{0}C)
- High ductility

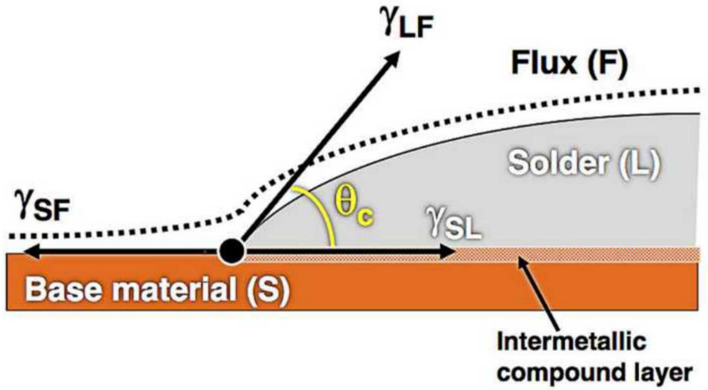
Fukushima, T., et al. (2011)

Intermetallic Compounds (IMC) Formed Between Metals

Vianco, P. T. (2018). "A Review of Interface Microstructures in Electronic Packaging Applications: Soldering Technology." JOM 71(1): 158-177.

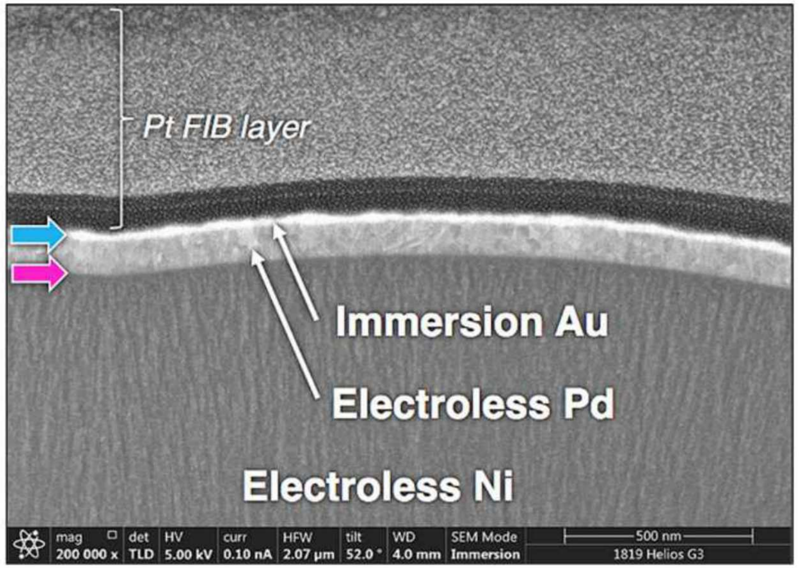
Soldering Technology and Interfaces

- Wetting and spreading are improved when the flux minimizes the value of interfacial tension between liquid solder and flux
- Solid-state diffusion controls the development of IMC layers and long-term reliability of the solder interconnect
- Purity of base material can have a significant effect on the tendency of void to form at the IMC/base material interface



Coatings and Finishes

1. Physical Vapor Deposition (PVD)
2. Plating Processes
    1. Electro- (galvanic) plating
    2. Electroless (autocatalytic) plating
    3. Conversion ("immersion") plating
3. Thick Film Layers



Vianco, P. T. (2018)

ENIG and ENEPIG Bonding to Gold Bumps

Benefits of Gold and ENEPIG

Gold:

- Low electrical resistance
- No native oxide
- Biocompatible
- Can be used in harsh environments
- Low temperature

ENIG/ENEPIG:

- Low cost
- Mask-less process
- Compatibility with wide range of interconnects

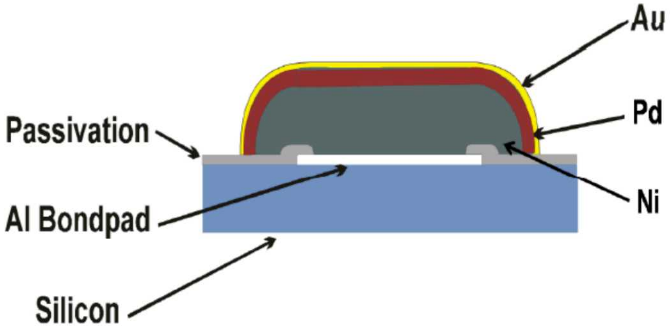
Applications

Advanced circuits and systems applications

- Wafer scale integration and low pitch-dimension package scaling

Bonding of devices with higher interconnect densities and pitch

- Direct interconnects using ENIG/ENEPIG bump metallization



Rowher, L. and D. Chu (2011)

(a) (b) (c)

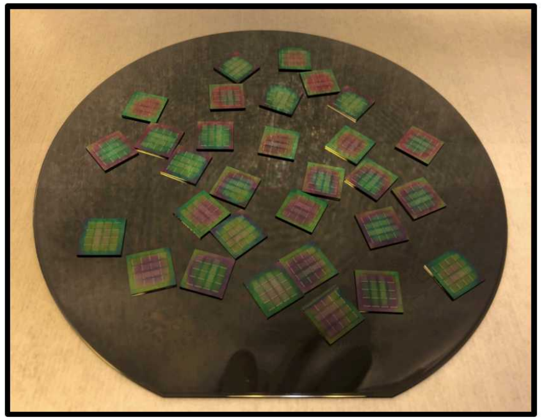
Figure 10. Plating on 9/9 μm line/space region of the COF with (a) Electrolytic Ni/Au, (b) ENEPIG, and (c) IGEPIG

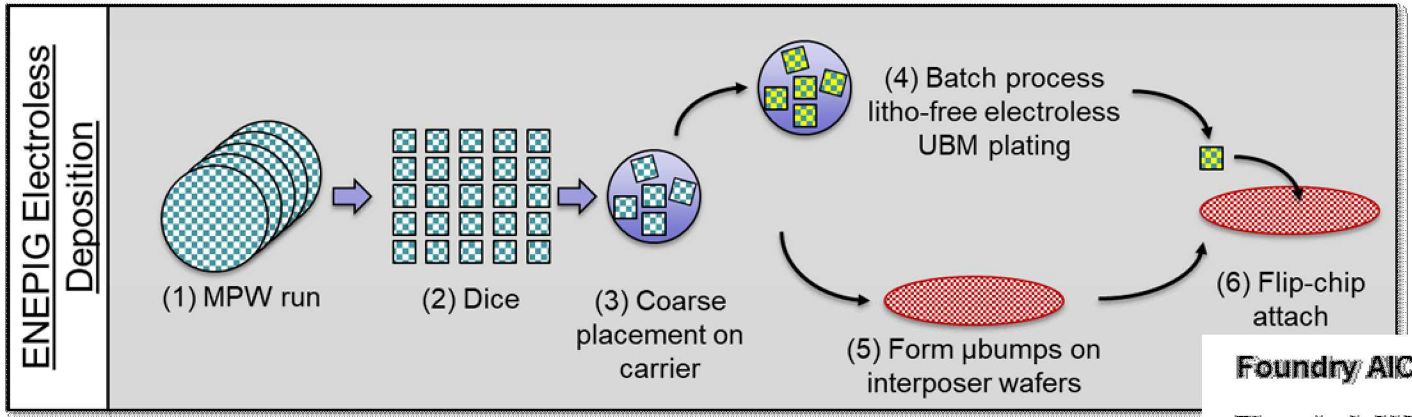
Pun, K. P. L., et al. (2018).

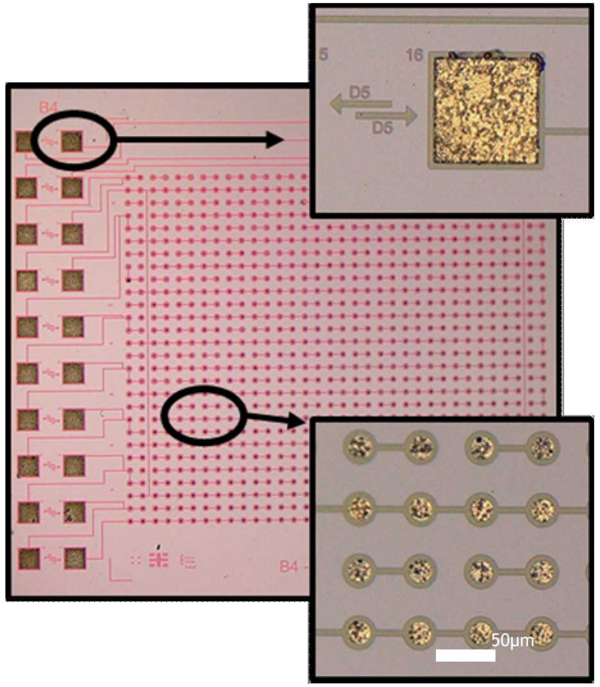
Surface roughness/finish plating characterizations is important to the bonding mechanism of the TC bonding process

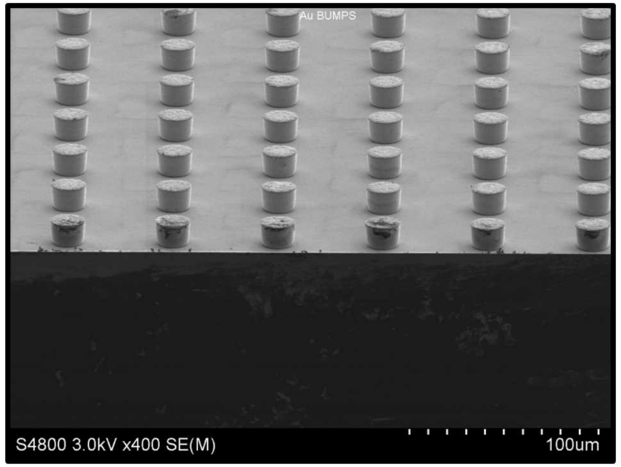
Our Process

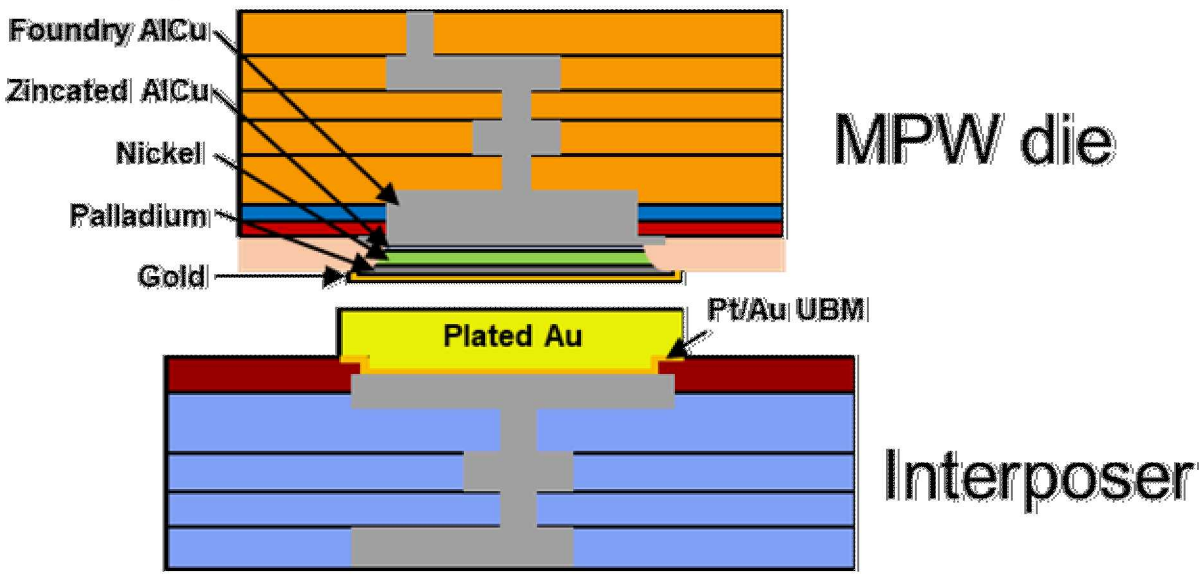
Au to ENEPIG bonding





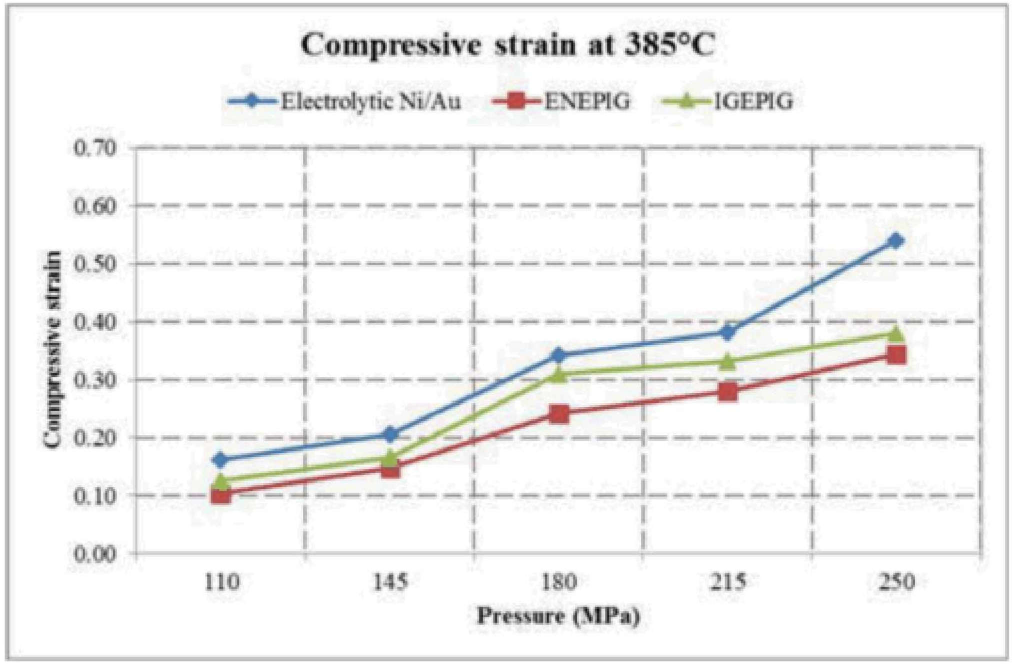






Bonding Parameters

- Bump height
- Bump diameter
- Joint material
- Bond pad material
- Bond pad thickness
- Bonding temperature
- Bonding force
- Bonding time
- Joint surface cleanliness



- Over-deformation results in excessive stress
- As bonding pressures increase, more deformation occurs
- Bond deformations occur at increasing temperatures
- Experiments at SNL to determine best bonding conditions

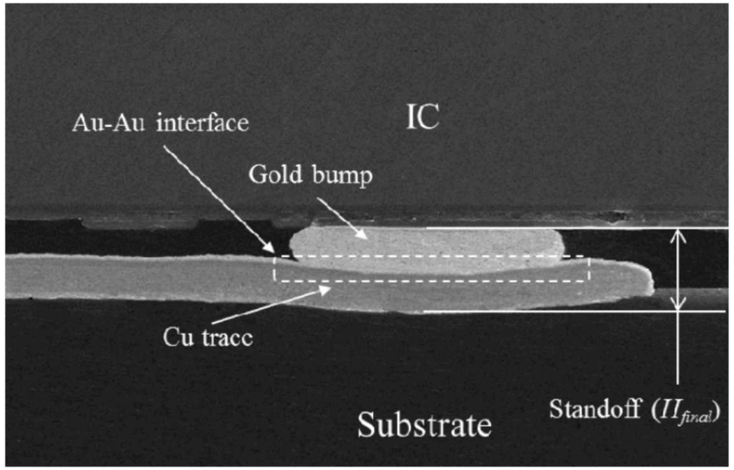


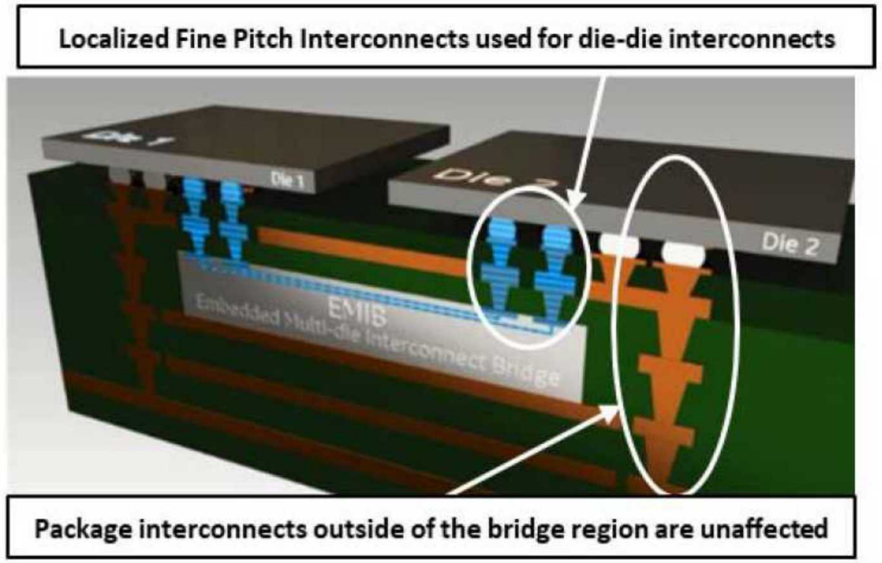
Figure 16. Schematic of the bond deformation

Pun, K. P. L., et al. (2018).

State of the Art – Current Emerging Technologies

Embedded Multi-die Interconnect Bridge (EMIB)

- Advantages:
  - Acts as a localized, ultra-high density wire connection between two die assembled on a substrate
  - Uses very small Si bridge die embedded as part of the substrate fabrication process (removes need for extra TSVs)
  - No Si interposer, die are fabricated right on the package
  - Connects multiple heterogeneous die to a single package
  - Different bump layouts enabled in a single package design
- Disadvantages:
  - EMIB process increases substrate manufacturing complexity
  - Must accommodate a greater CTE mismatch between die and package



Mahajan, R., et al. (2019)

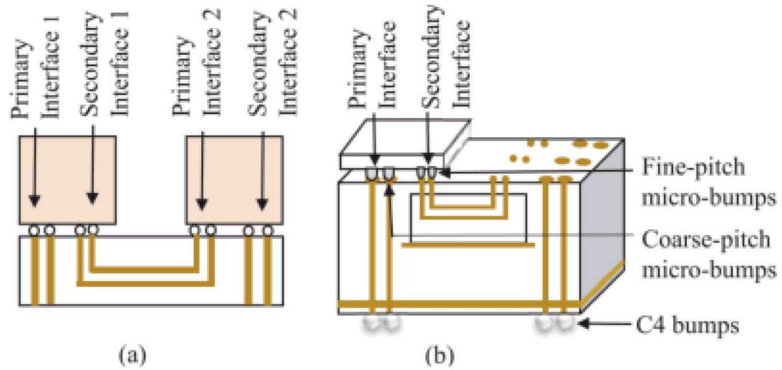
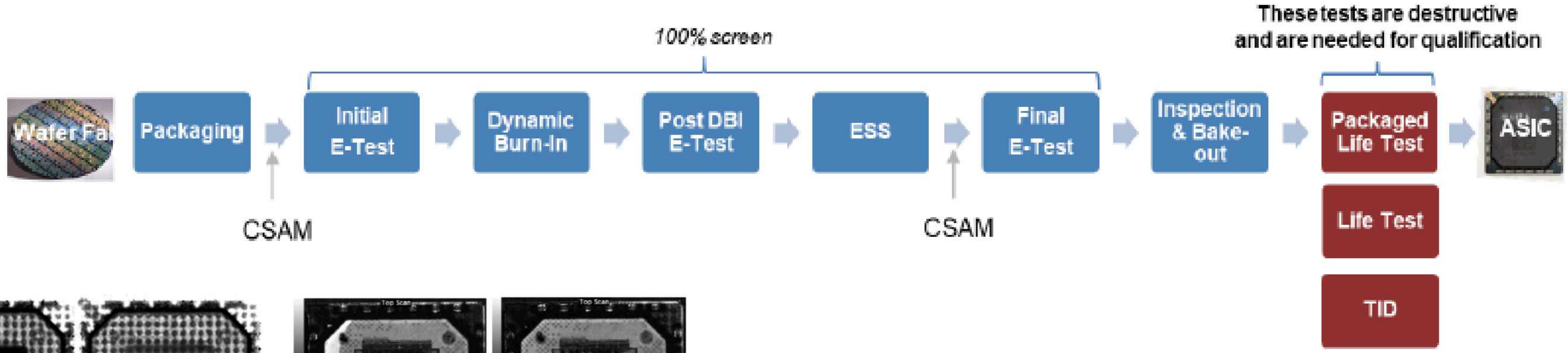
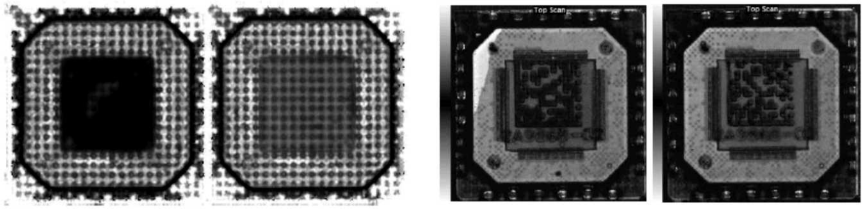


Fig. 1: P1838-compliant test interfaces for: (a) Interposer-based IC; (b) EMIB die.

Mondal, S. and K. Chakrabarty (2018)

Moisture Uptake in Plastic Ball-Grid Array ASICs

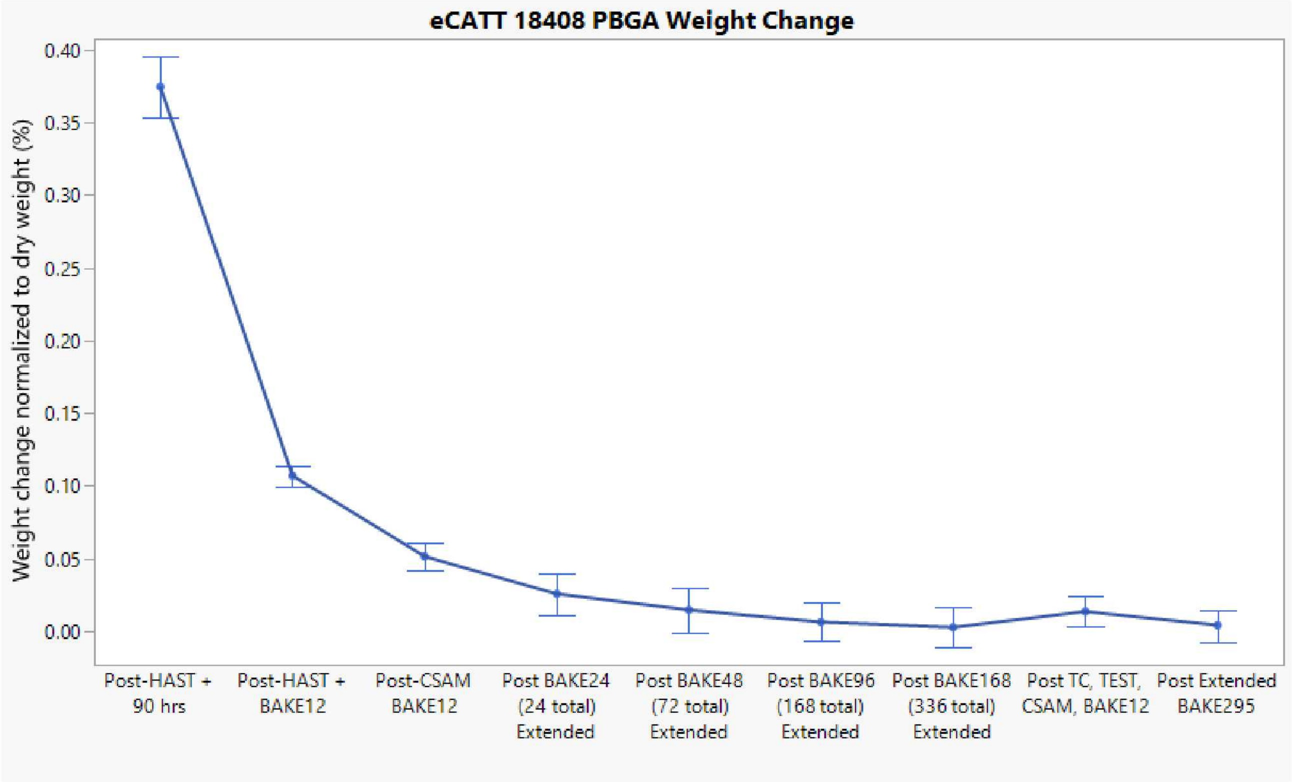




Die Detachment vs. Good, Through-Scan Mold Delamination vs. Good, Top Scan

Figure 8.2.2 CSAM Images of Die Detachment and Mold Delamination

- A substantial amount of moisture weight gain was detected after Highly Accelerated Stress Testing (HAST) conditioning
- Extended bake out was suggested to remove additional moisture from HAST
- Extended bake out post-HAST greatly reduces moisture weight in packages



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Questions?