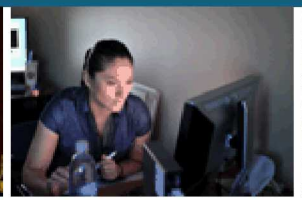
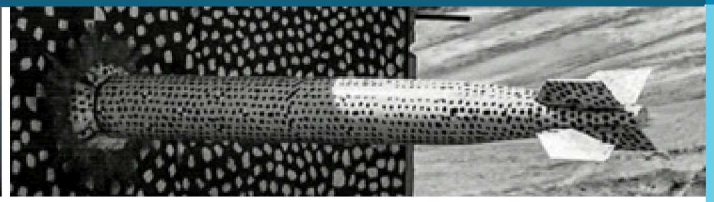
SAND2020-8495C

New Generation Multijunction Thermal Converters at Sandia National Laboratories





CPEM 2020

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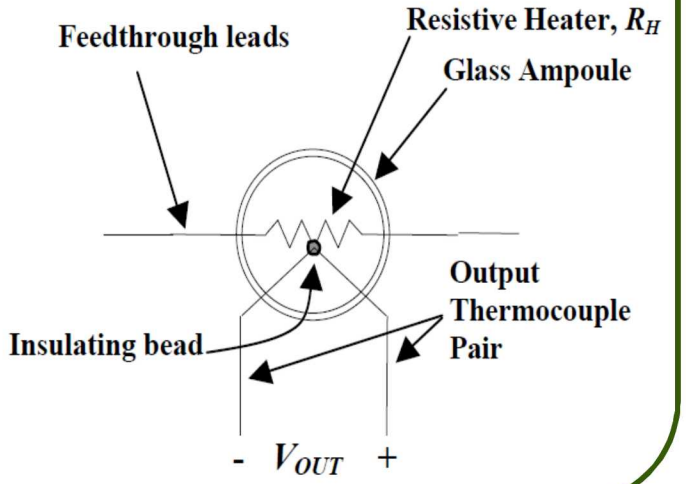
Outline

- Brief overview of thermal converters and multijunction thermal converters (MJTC)
- Motivation for high resistivity substrates
- Sandia National Laboratories (SNL) fabrication process and results of MJTC devices
  - Initial results using legacy process
  - ac-dc difference results and dc results on normal silicon substrate
  - ac-dc results for high resistivity silicon substrates
- Future work
  - COMSOL modeling efforts

Single-Junction Thermal Converters

Single Junction Thermal Converter



- ✓ **Simple design**
- ✓ **Conventional AC transfer standard since 1950's**
- ✗ **Extremely fragile**
- ✗ No overvolt protection
- ✗ **Low output (mV)**

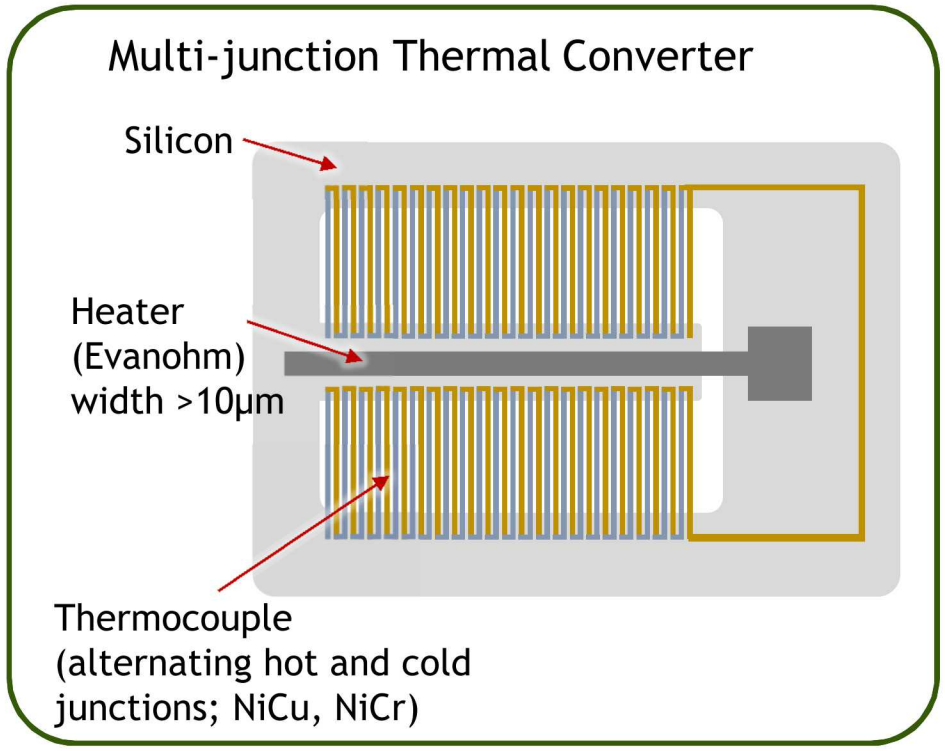
Transfer Standard for AC-Voltage and AC-Current

- AC and DC voltage or current through wire
- Wire heats up, thermocouple detects temperature change → DC voltage out

$$\delta = \left. \frac{V_{ac} - V_{dc}}{V_{dc}} \right|_{E_{dc}=E_{ac}}$$

δ = ac-dc difference
V_{ac}, V_{dc} = Input ac and dc voltage
E_{ac}, E_{dc} = Output ac and dc emf

Multi-Junction Thermal Converters



- Designed late 1990's, early 2000's
  - PTB, NIST and Sandia (Tom Wunsch PhD Thesis, UNM, 2001)
- Concept similar to single junction thermal converter
- Many thermocouples to increase output voltage and sensitivity

$$\delta_t = \frac{(E_{as} - E_{ds})}{n_s E_s} - \frac{(E_{at} - E_{dt})}{n_t E_t} + \delta_s$$

✓ **Increase output voltage**

✓ **Low uncertainty (~1-2 ppm, depending on range)**

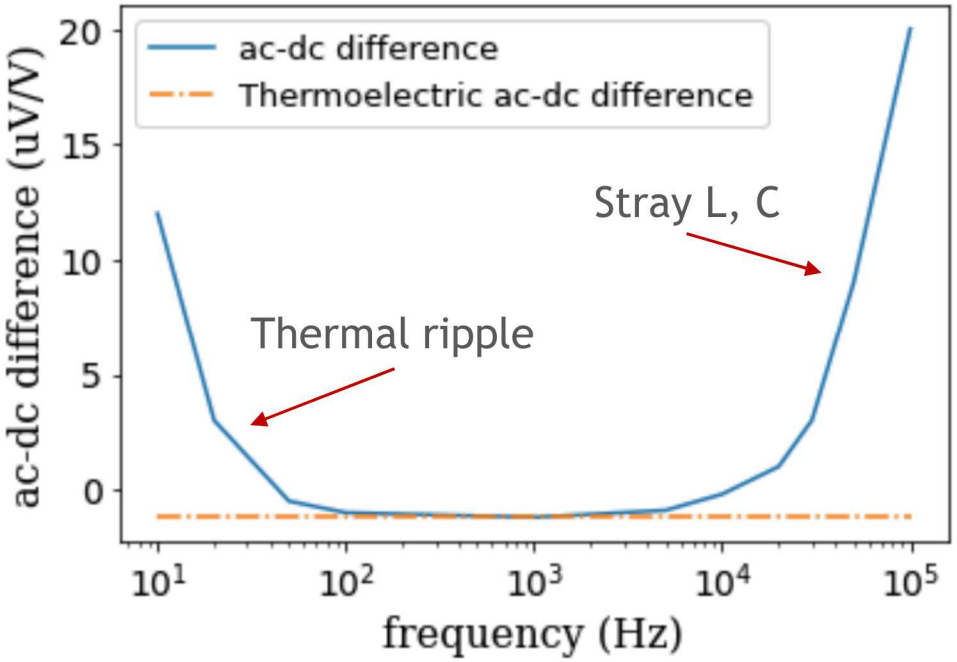
✗ **High uncertainties at low voltages and high/low frequencies**

✗ **No overvolt protection**

✗ **High resistance of thermocouple output**

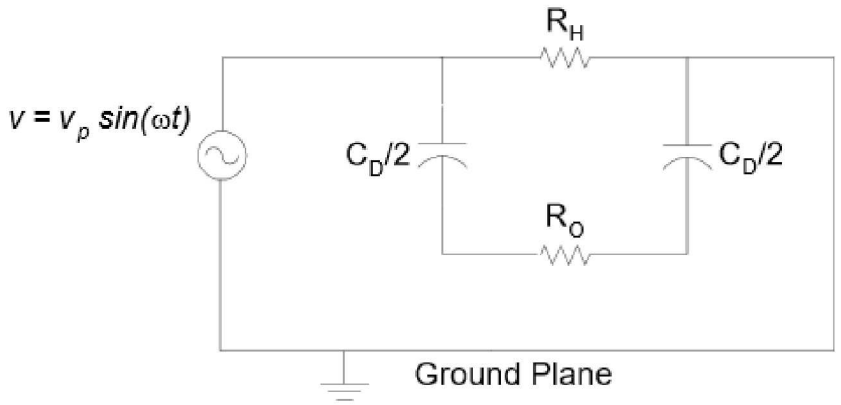
Motivation

- The MJTC substrate can have significant impact on device performance
- **Problem**: Silicon has relatively large permittivity and loss
  - Leads to capacitive coupling between the heater and thermocouples and the obelisk at high frequencies
- **Solution**: use high resistivity substrates
  - NIST – fused silica
  - PTB – quartz
  - Japan – polyimide/alumina
- **Goal**: build upon SNL process developed by Wunsch and fabricate MJTC devices on high resistivity silicon wafers
  - No need to change Si etching steps



NIST; Fujiki (2015)

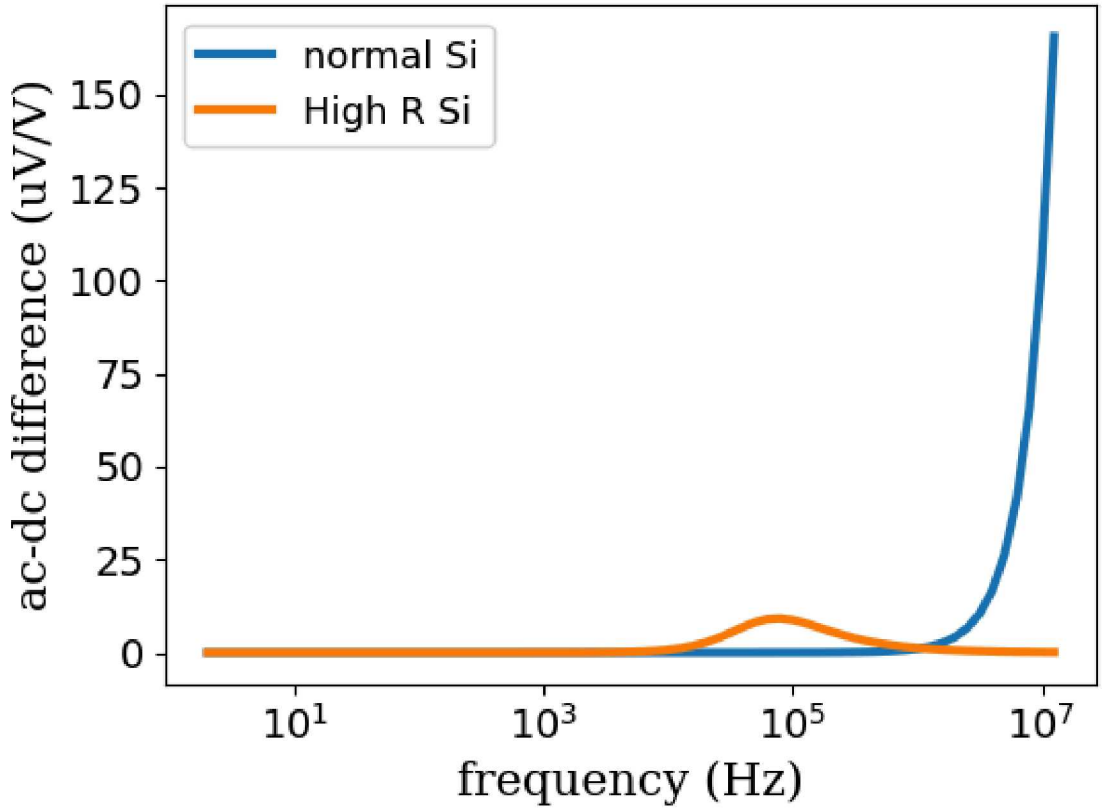
Why high resistivity substrates matter



- Equivalent circuit of MJTC including obelisk
- First principles, simple model of ac-dc behavior

$$\delta = \frac{R_O R_H \chi_D}{(R_O^2 + \chi_D^2)^{3/2}}$$

- ac-dc difference should be lower at high frequencies for substrates with high resistivity
- Looking at loss (tanδ) fundamental equation, see that as substrate resistivity increases, loss decreases



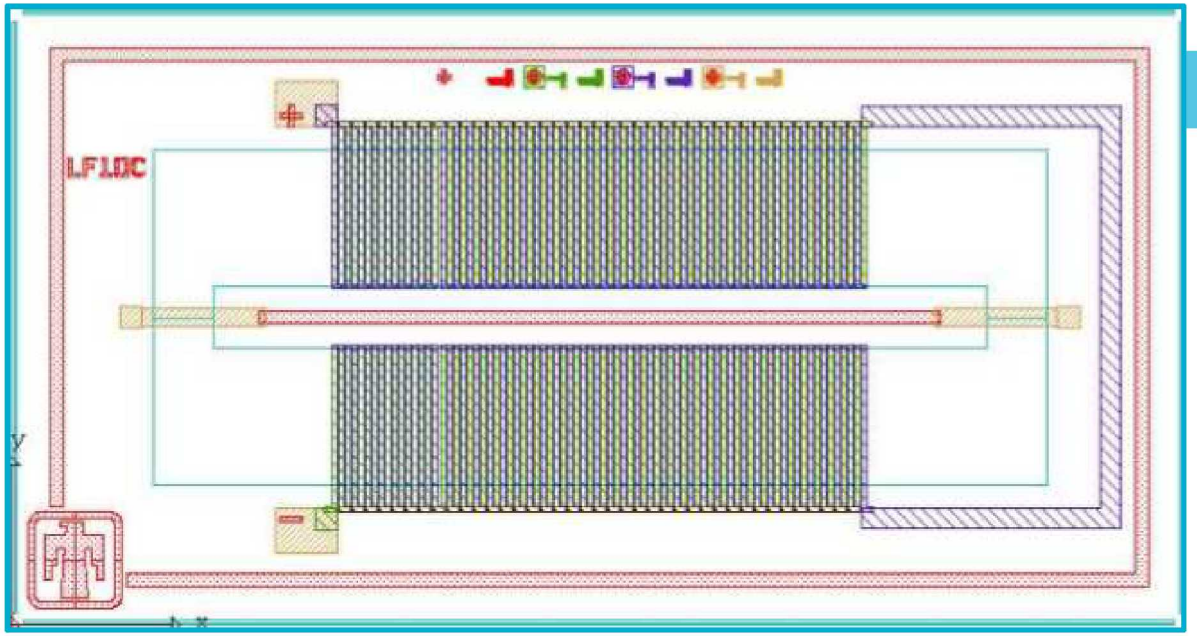
$$tan\delta = \frac{1}{\omega \varepsilon_0 \varepsilon_r \rho_{substrate}}$$

as $\rho_{subsrate}$ ↑, tanδ ↓

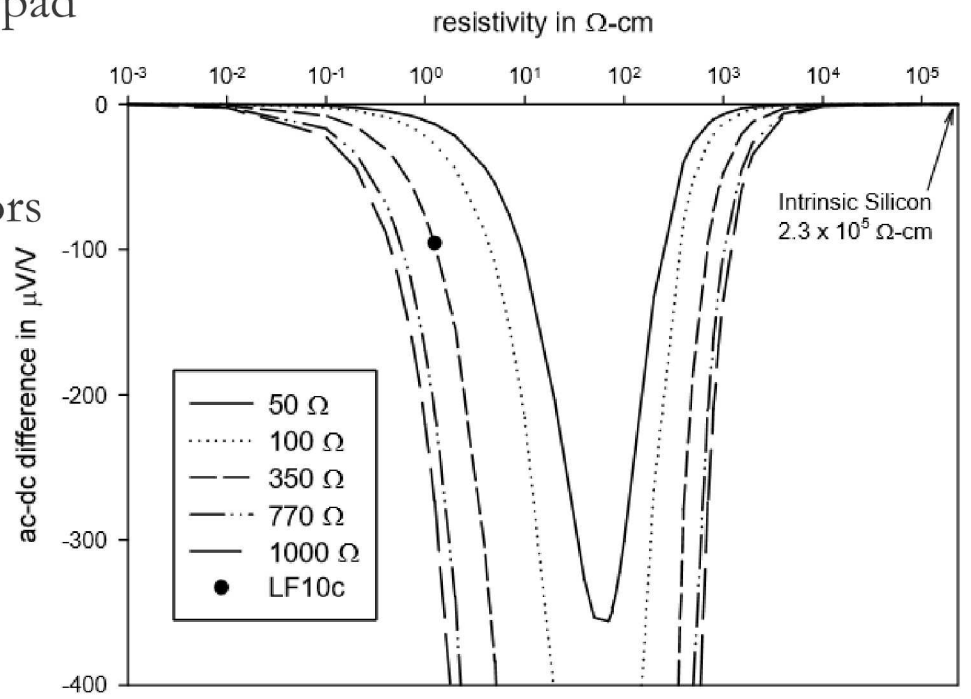
χ_D = capacitive reactance
R_0 = obelisk resistance
R_H = heater resistance
ρ_{si} = Si resistivity

SNL History of MJTC

- MJTC at SNL – late 1990s
  - Primary lead: Tom Wunsch
  - PhD 2001 from UNM
  - MJTC focus:
    - Modification of heater/contact pad design
    - Modeling
    - Sources of ac-dc difference errors above 100kHz



MJTC design by Wunsch, SNL



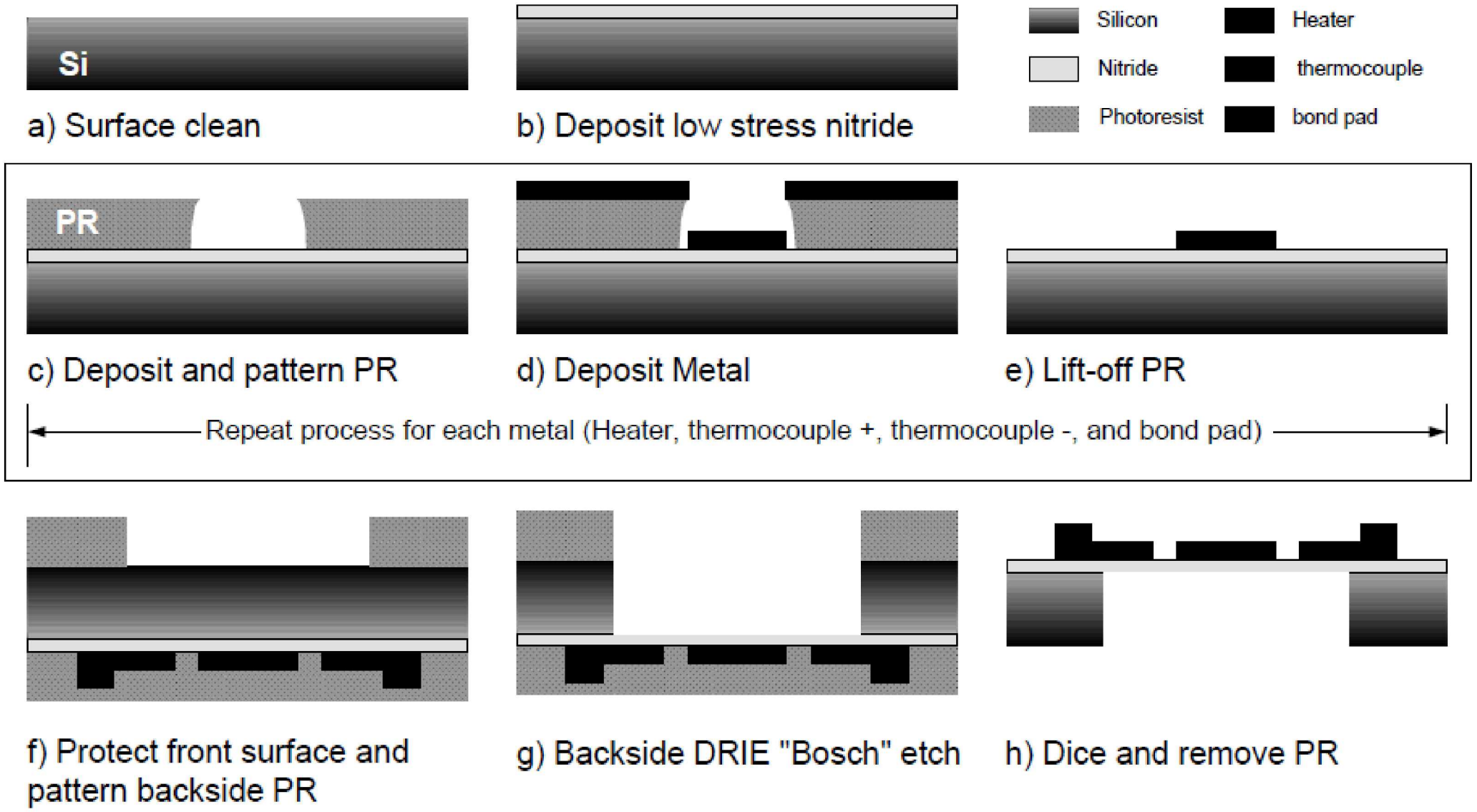
Calculated ac-dc difference vs. substrate resistivity
Wunsch, SNL

SNL MJTC Process

	Wunsch, 2001	SNL today
Substrate	Si ρ = 1-20 Ω·cm Si ρ = 100-200 Ω·cm	~~Si ρ = 1-20 Ω·cm~~ Si ρ = 10000 Ω·cm
Dielectric layer	1 µm low stress Si_3N_4	1 µm low stress Si_3N_4 1 µm SiO_2
Heater	500 nm Evanohm	500 nm Evanohm
Thermocouple +	800 nm NiCr (90/10)	800 nm NiCr (90/10)
Thermocouple -	800 nm NiCu (90/10)	800 nm NiCu (90/10)
Bondpads		20 nm Ti, 1 µm Au

- Start with same fabrication process as used by Wunsch
- Switch to high resistivity Si wafers once original process is established

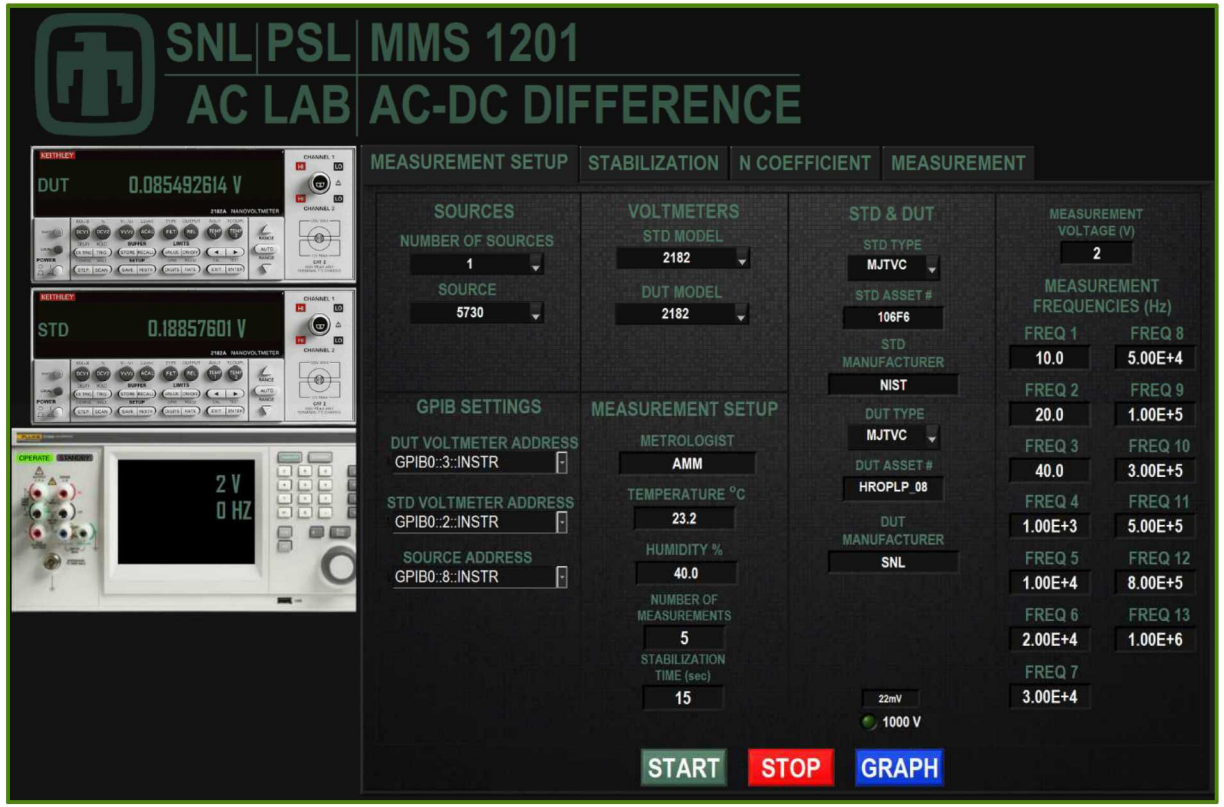
MJTC Fabrication Process



T.Wunsch, PhD Thesis, UNM, 2001

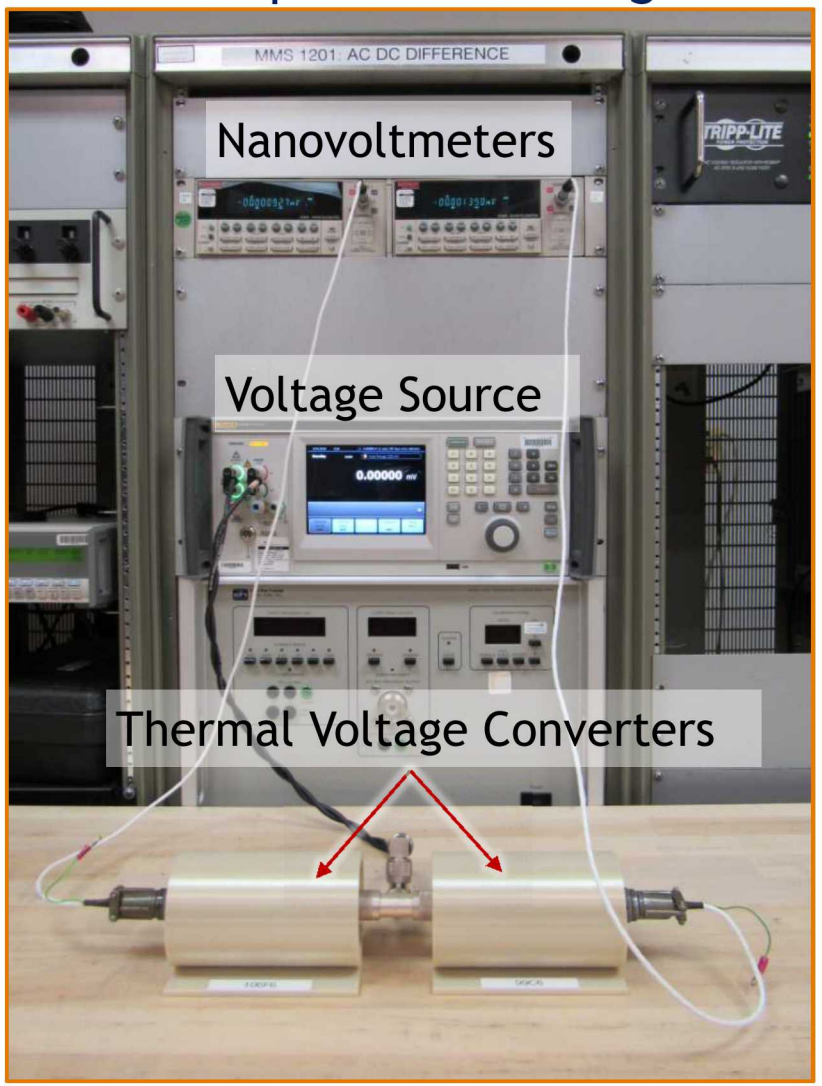
SNL ac-dc setup

- SNL ac-dc difference station
  - Completely automated (LabVIEW) software
  - Software can switch between one and two sources
  - Standards: MJTC (NIST), Fluke 792, Fluke A40B's



AC-DC Difference Software Interface (Josh Stanford)

Experimental setup for calibrating AC voltage



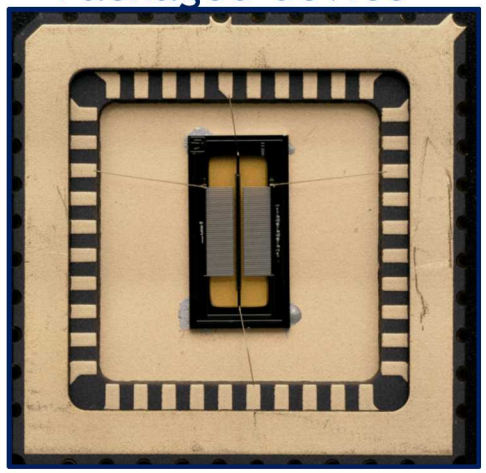
- ~100 calibrations per year
- NVLAP accredited for AC current shunts (1 mA to 100 A up to 100 kHz)
- Soon NVLAP accredited for AC voltage

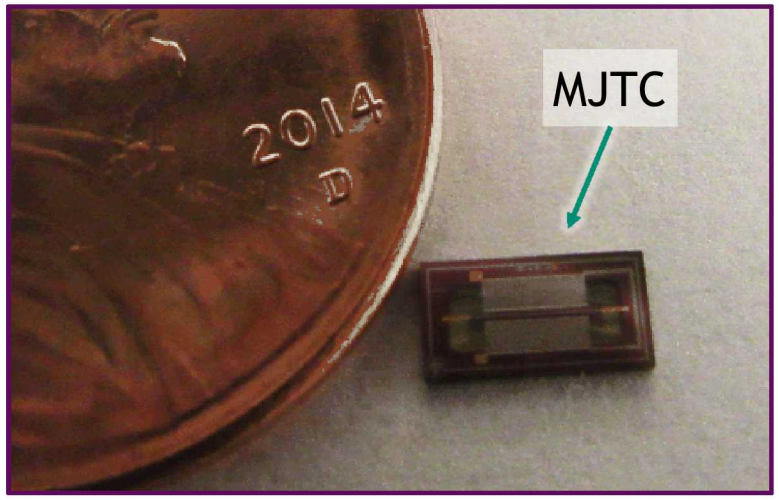
SNL First MJTC device in two decades

All fabrication steps performed at SNL

- Initially repeated steps from Wunsch process
- Metallization, deposition, patterning, etching
- Chips were wire bonded and packaged under vacuum
  - 23 devices initially tested
  - Only 2 failed devices at 1 kHz, 2V

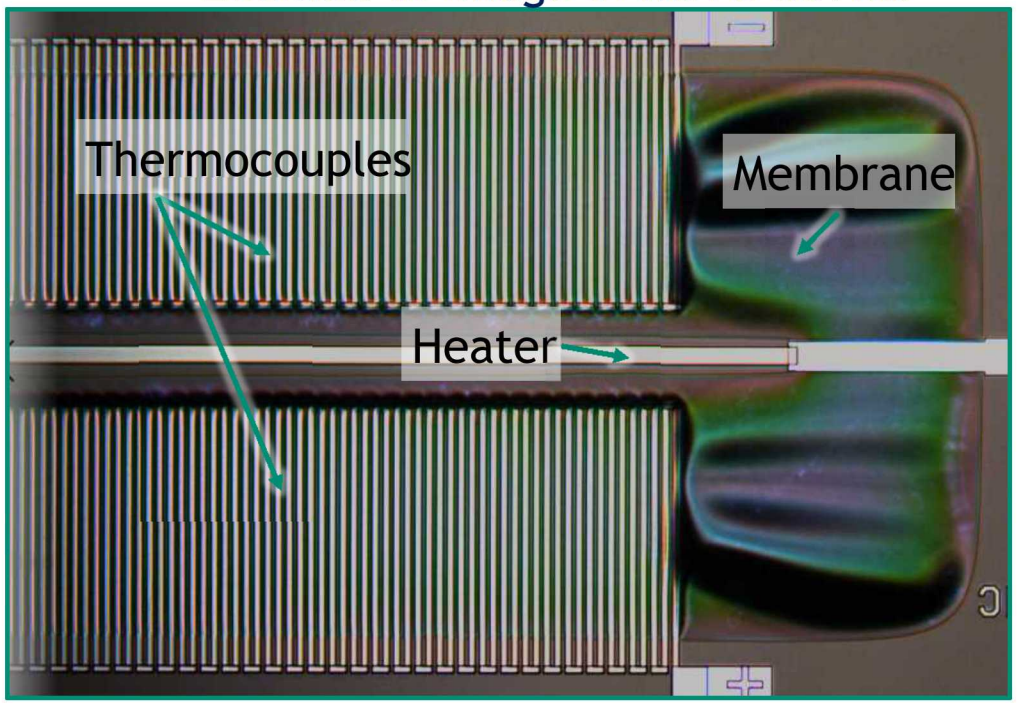
Packaged device





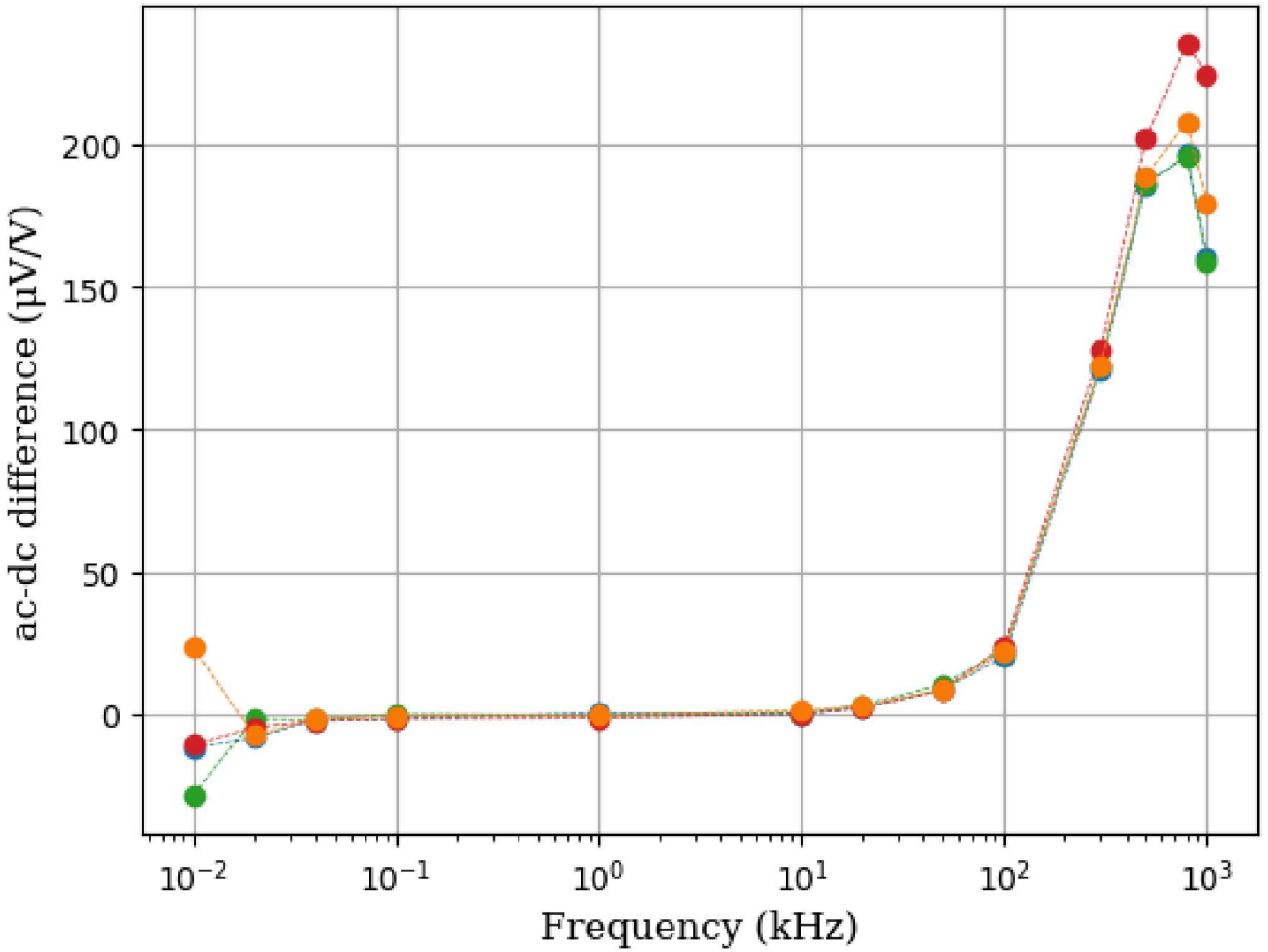
One MJTC device

Zoomed in image of MJTC device



Initial electrical results

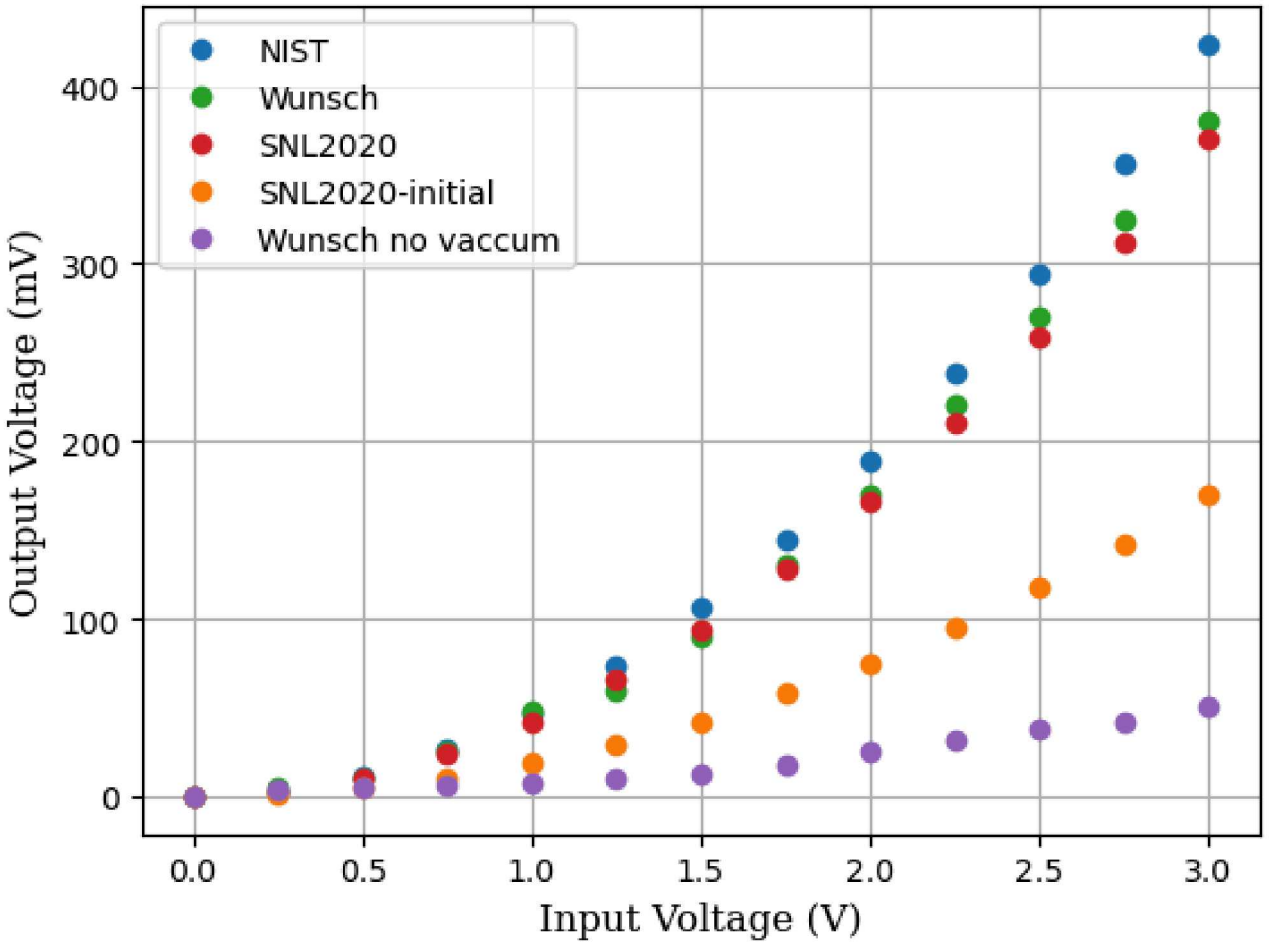
- Very reproducible results
- Sub 2 μV/V ac-dc difference up to ~50 kHz
- As expected, observed larger ac-dc difference at high frequencies
- Comparable results to Wunsch



Heater resistance = 140 Ω - 170 Ω

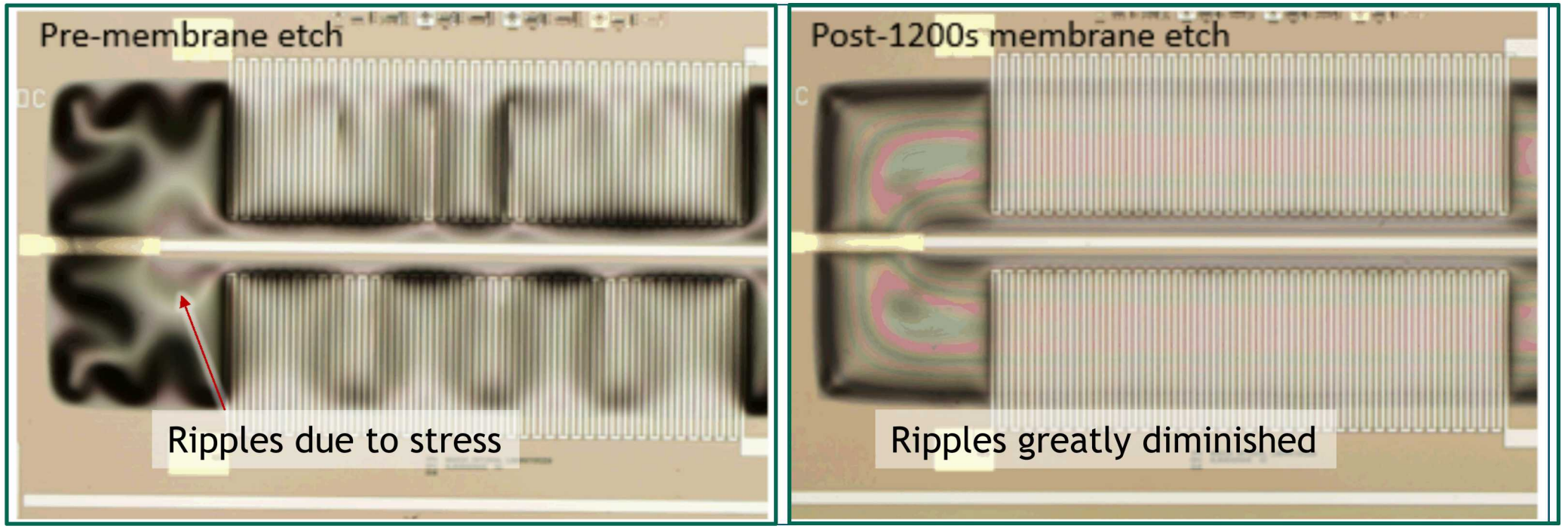
Packaging Results

- Packaging atmosphere can have profound impact on output
  - Reduce heat transfer between chip and chip carrier
  - 1st batch – 1 mtorr pressure
  - 2nd batch – 1 µtorr pressure



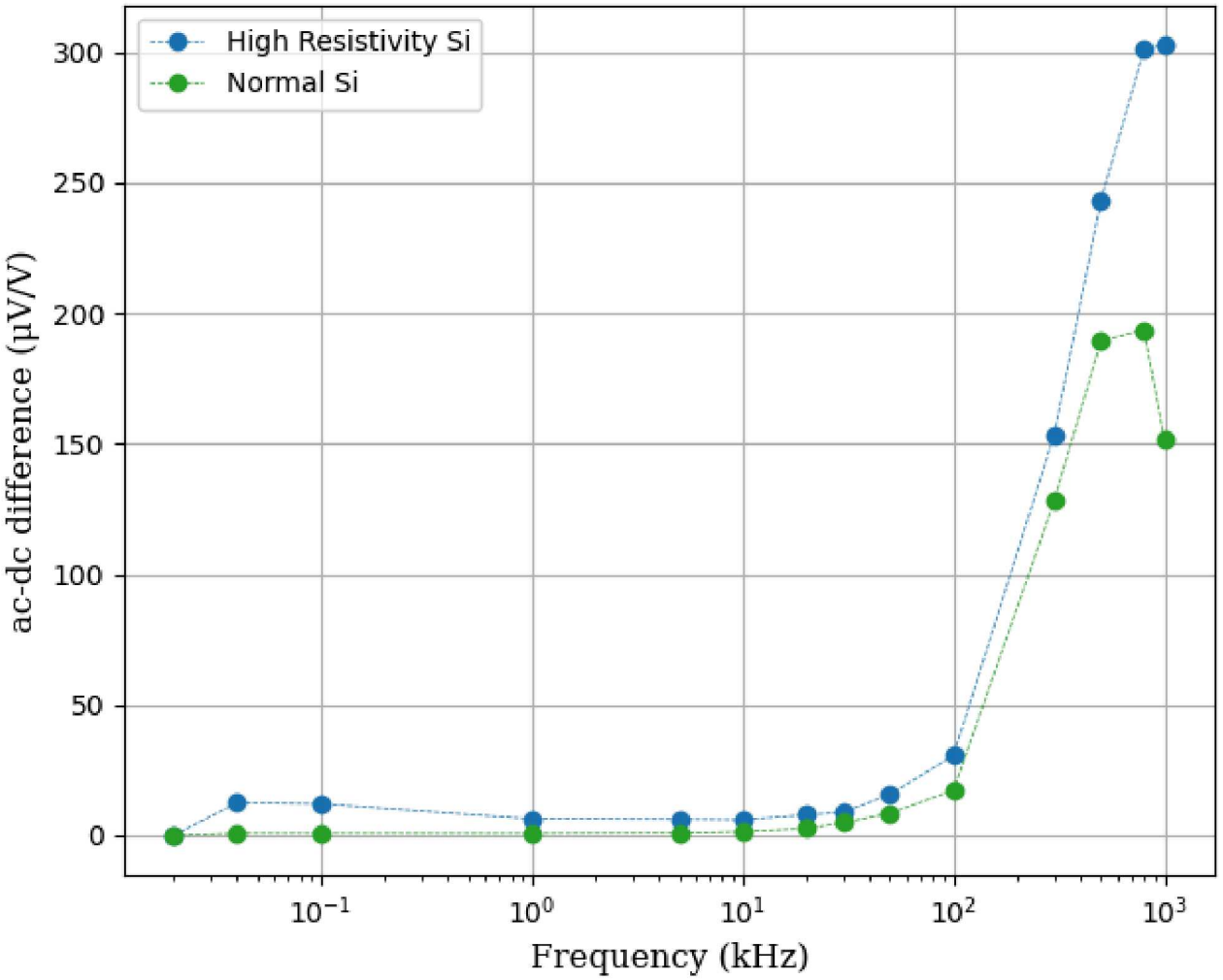
High resistivity silicon results - pictures

- Fabrication of high resistivity silicon wafers had a few issues:
  - Photoresist reticulated during backside Si etch making it very hard to remove
    - Indicates the wafer heated up substantially during Si etch
  - Stress in the silicon nitride membrane (required additional etch step)



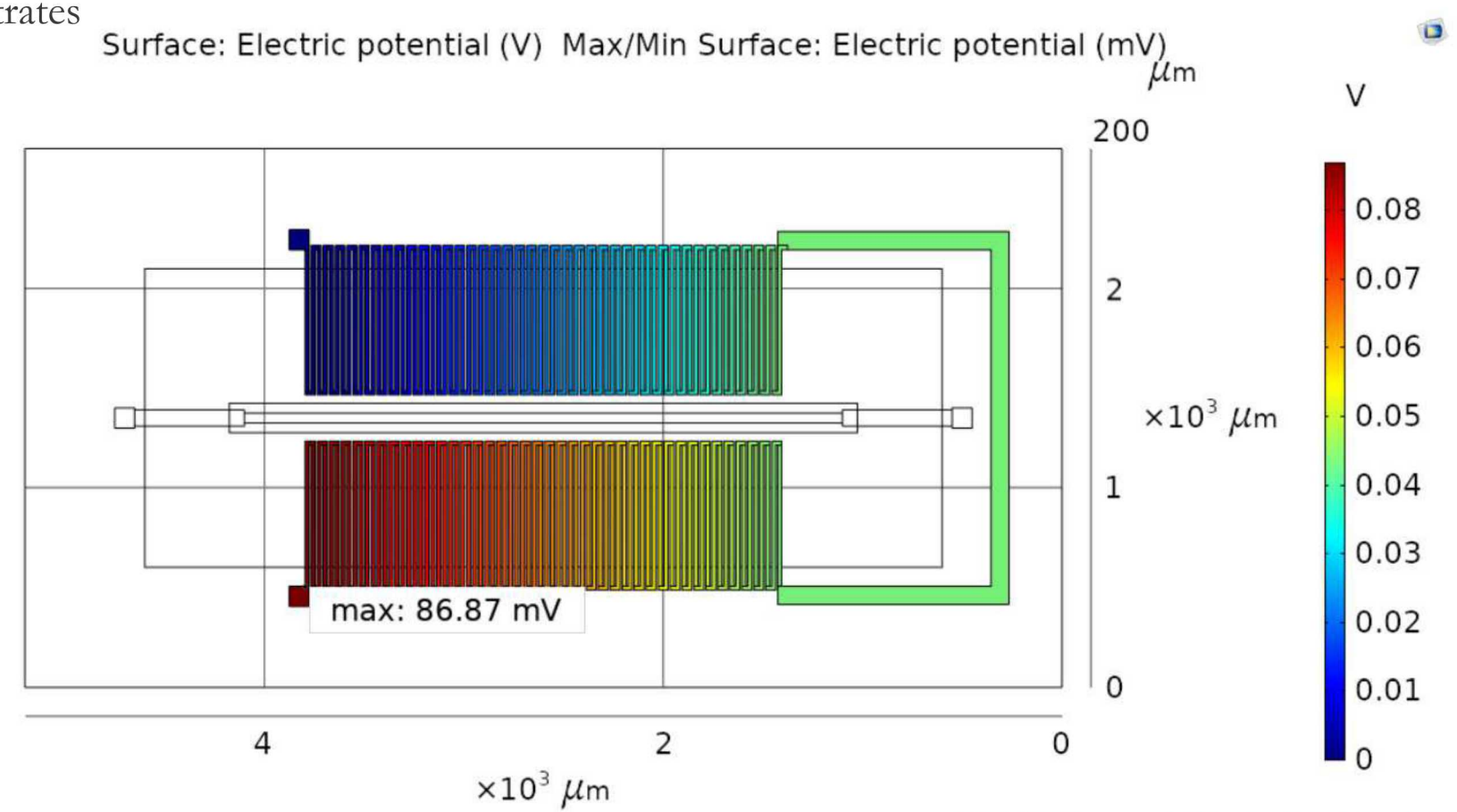
High resistivity silicon results - data

- ac-dc difference results using high resistivity silicon wafer
- Very first wafer!
- ac-dc difference increased at high frequencies rather than decrease
  - Fabrication issues that could have damaged the devices
  - High failure rate indicating devices were damaged during process



Future work

- Continue to fabricate MJTC devices on high resistivity silicon wafers
  - Improve the photoresist reticulation issue during backside etch
  - Look for improved ac-dc difference at high frequencies
  - Investigate other high resistivity substrates
    - SOI
- Measure temperature coefficient of resistivity of heater layer
- COMSOL Modeling
  - Thermal and electrical responses
  - Help decide ideal substrate
- JAWS
  - Cross compare MJTC against JAWS
- Uncertainty analysis of MJTC



COMSOL modeling: Karl Lukes

Conclusions

- Sandia National Laboratories has re-established the process of fabricating MJTC devices for AC voltage calibration applications
- MJTC process was established ~2000 by Tom Wunsch
- Successfully completed an initial wafer using same conditions set by Wunsch
  - ac-dc results are comparable to Wunsch
- Performed initial fabrication of MJTC devices on high resistivity silicon wafer
  - Wafer processing had a few hiccups which lead to low yield and possibly led to unexpected ac-dc difference results
- Additional wafers are in the queue
- COMSOL modeling in initial stages to help determine best substrate and device design

Acknowledgements

- SNL
  - PSL Management: Roger Burton and Meaghan Carpenter
  - PSL AC Lab: Eddie O'Brien, Aaron Meyrick, Karl Lukes, Josh Stanford
  - Tom Wunsch
  - Ron Manginell
  - Jason Dominguez (SNL MESA Fab)
  - Lyle Menk (SNL Packaging)
  - Ed Piekos (SNL Modeling)
- NIST
  - Stefan Cular
  - Joe Hagmann

Thank you!

Questions?

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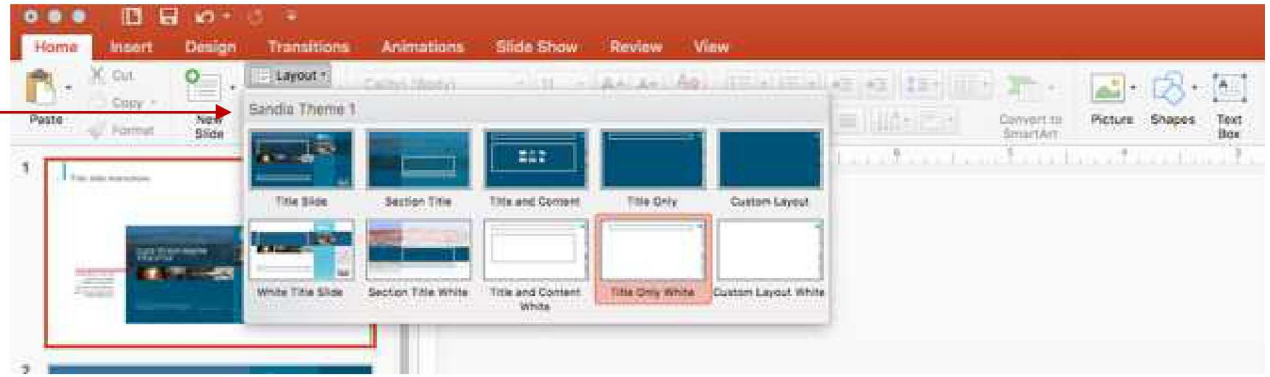

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Adjustable text boxes for adding presenter title and names

Additional program/partner logos can be added here

Add Sand Number to the funding statement within the Master Title slide or add a text box and put it under funding statement paragraph

Ac-dc difference background

- talk about why ac-dc difference
- physics of SJTC and MJTC
- talk about different devices (SJTC, MJTC)
- show ac-dc equation

Packaging Results

- Packaging atmosphere can have profound impact on output
  - Explain why!