SAND2020-8298PE

# ARC-SAFE: Accelerated Response Semiconducting Contactors and Surge Attenuation For DC Electrical Systems


## Sandia National Laboratories and University of New Mexico

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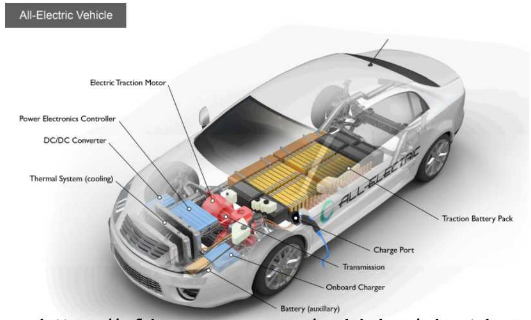
# Opportunity/Application



- Medium Voltage DC systems lack suitable circuit breaker (CB) technologies – limits system performance and adoption
  - Solar and Wind power generation growing rapidly
  - Electric ship and rail power management, electric vehicles

https://www.navsea.navy.mil/Home/Team-Ships/PEO-Ships/Electric-Ships-Office/

https://www.nrel.gov/wind/grid-integration.html




https://afdc.energy.gov/vehicles/electric_basics_ev.html

- Mechanical CBs are large and respond relatively slowly
- Solid State CBs promise <u>faster response times</u>, **smaller form factors**
- Current DC CB available for low voltage/power applications

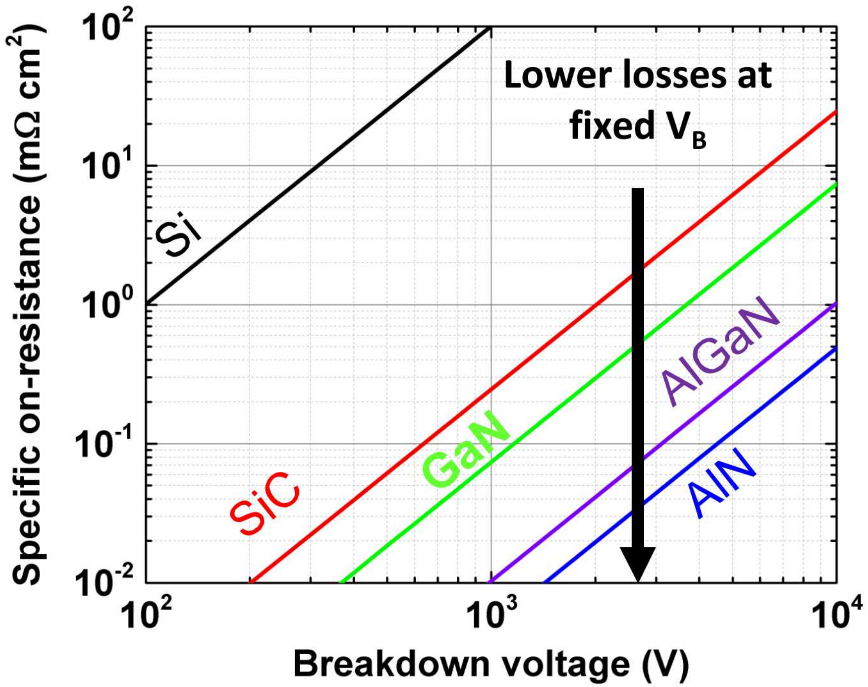
http://www.industrytap.com/wp-content/uploads/2013/02/US-Electrical-Grid.jpg

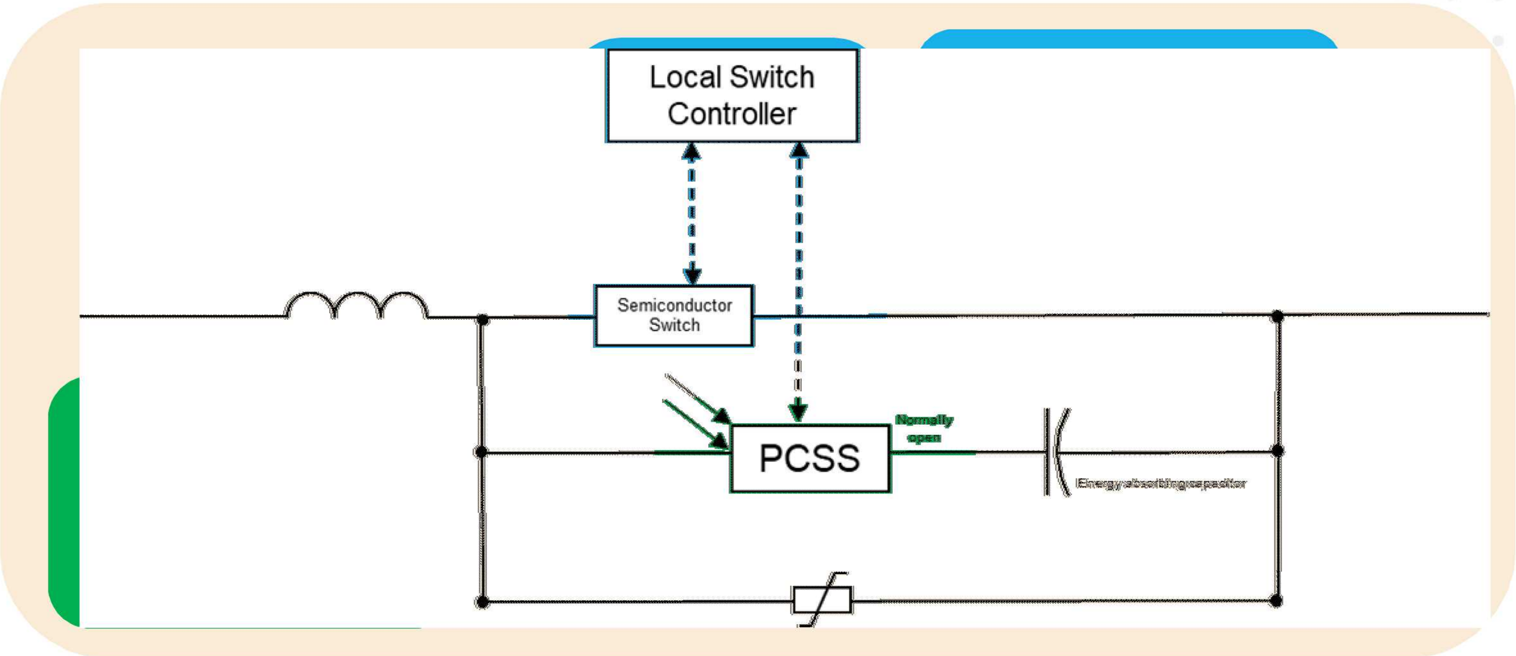
# Uniqueness of Approach



Wide bandgap semiconductors (SiC, GaN) enable lower conduction losses & higher power density

***Targeting 10 kV/100 A CB performance***




- Normally “On” leg to use mature SiC devices with novel circuit architecture
- Normally “Off” leg to use optically-triggered GaN PCSS (good isolation)
- Power Dissipation leg to investigate metal oxide varistors, other technologies

# Key Metrics/Outcomes

Project Objectives

## Year 1+ Milestones

| WBS | Description | Year 1 | | | | Year 2 | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Q1 | Q2 | Q3 | Q4 | Q1 | Q2 | Q3 | Q4 |
| M 1.1 | (G/N) Refine tasks/milestones | | | | | | | | |
| M 2.1 | Design of normally-on leg of CB | | | | | | | | |
| M 2.2 | Design of shunt leg of CB | | | | | | | | |
| M 2.3 | Design of normally-off leg of CB | | | | | | | | |
| M 2.4 | Demonstration of low-voltage CB operation | | | | | | | | |
| M 2.5 | Develop mechanistic understanding of GaN PCSS devices | | | | | | | | |
| M 3.1 | Evaluate high-gain mode operation of vertical GaN PCSS prototypes | | | | | | | | |
| M 3.2 | (G/N) Demonstrate GaN PCSS device with 5 kV operation | | | | | | | | |
| M 5.1 | Initial T2M Plan | | | | | | | | |
| M 5.2 | Impact Sheet | | | | | | | | |

## Key CB Performance Metrics

| Category | Key CB Metrics |
|---|---|
| Rated Voltage | 10 kV DC |
| Power | 1 MW (100 A at 10 kV) |
| Efficiency | 99.97% |
| Response Time | < 500 μs |
| Lifetime | 30,000 cycles, TBC |
| Nuisance Trips | < 0.1% TBC |
| Power Density | 60 $MW/m^3$, TBC |
| Cooling | Passive |

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# Sandia National Laboratories and University of New Mexico Team

## Sandia: System & Circuit Design

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***Power Circuit Laboratories***









## Sandia: GaN Power Devices

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Harry Hjalmarson
Richard Gallegos
Bob Kaplar
Paul Sharps

***MESA Facility (GaN device fabrication)***

## UNM: Pulsed Power, High Voltage, Ultra-Fast Switching (triggers)

Prof. Jane Lehr
Brad Maynard

APERIODIC Laboratory

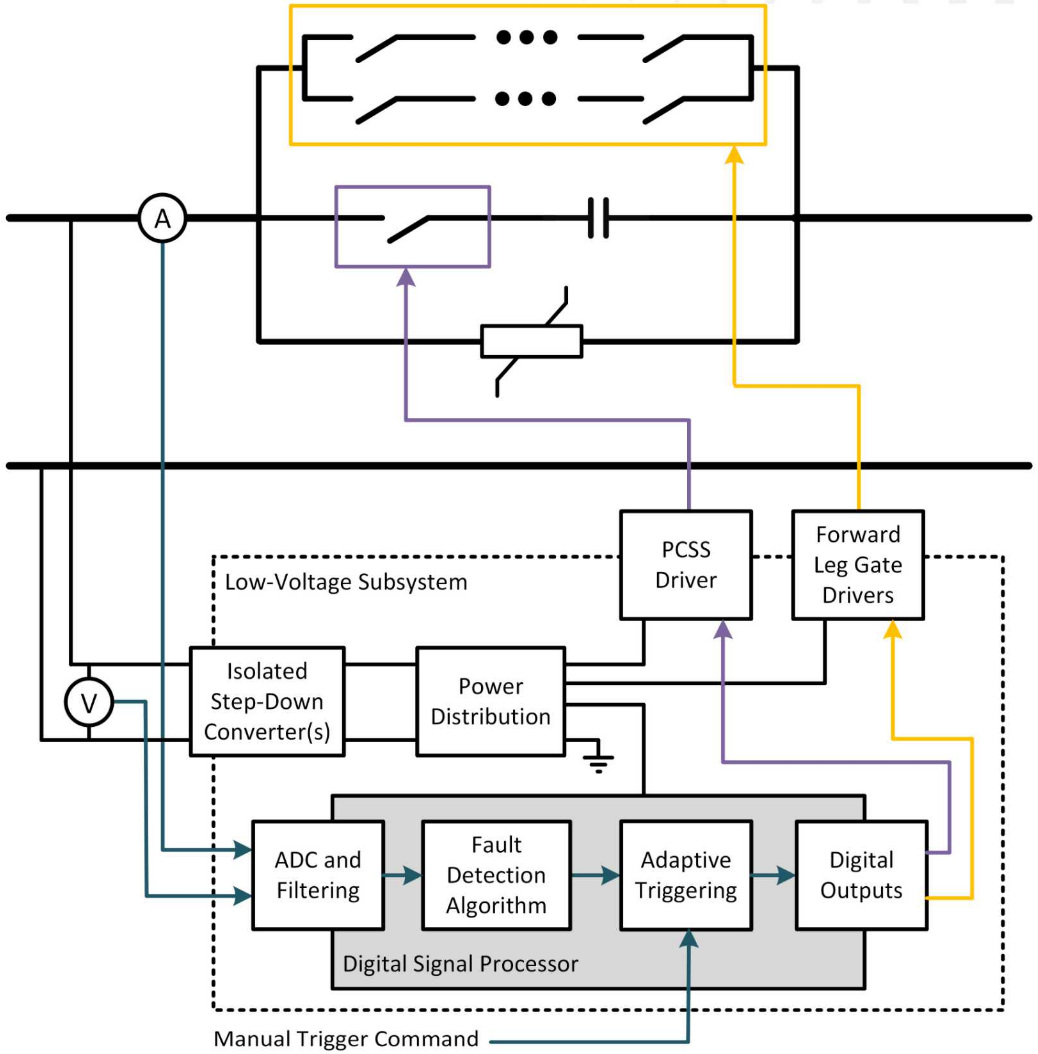
***Advanced Power Electronics Conversion Systems (apex) Laboratory***

***Pulsed Power Laboratories***

# Proposed Solid State Circuit Breaker (SSCB) Architecture

- **Architecture includes**
  - Cascaded JFET HV switch topology
  - Normally-On JFETs have low on-resistance and low auxiliary drive loss
  - Normally-Off Photoconductive semi-conducting switch (PCSS) triggers immediately after a fault to shunt current
  - Capacitor for absorbing + dissipating energy from flyback current
  - Control circuit powered from high-side voltage tap

| Parameter | Requirement |
|---|---|
| Blocking Voltage | 10 kVDC |
| Rated Power | 1 MW |
| Efficiency | 99.97 % |
| Response Time | < 500 μs |
| Life Time | 30,000 cycles |
| Power Density | < 60 $MW/m^3$ |

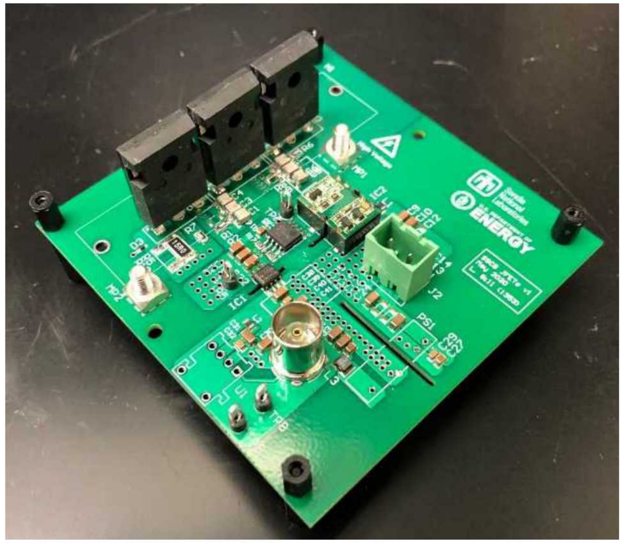


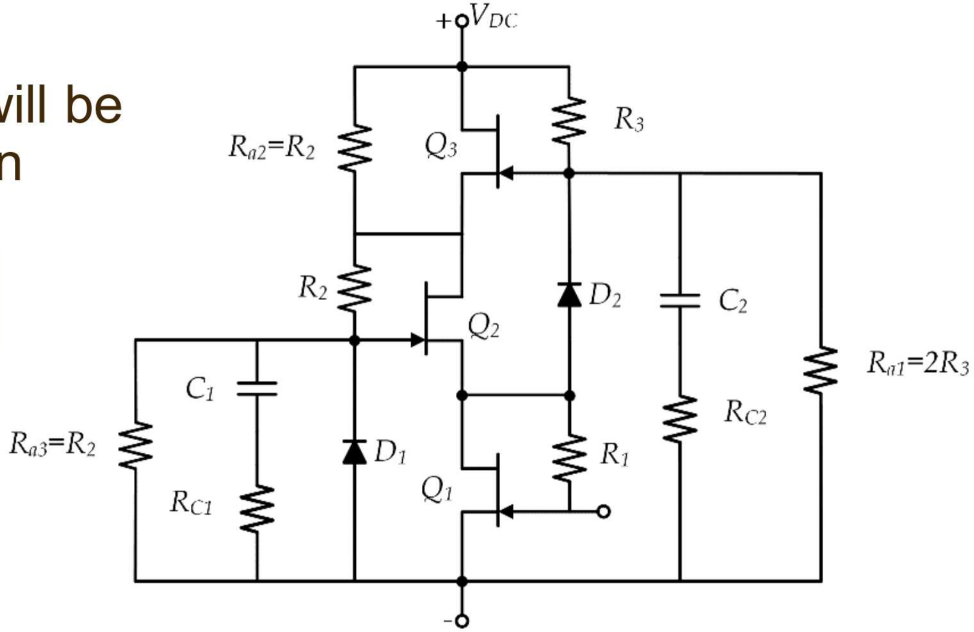
# Initial Prototype is Being Evaluated

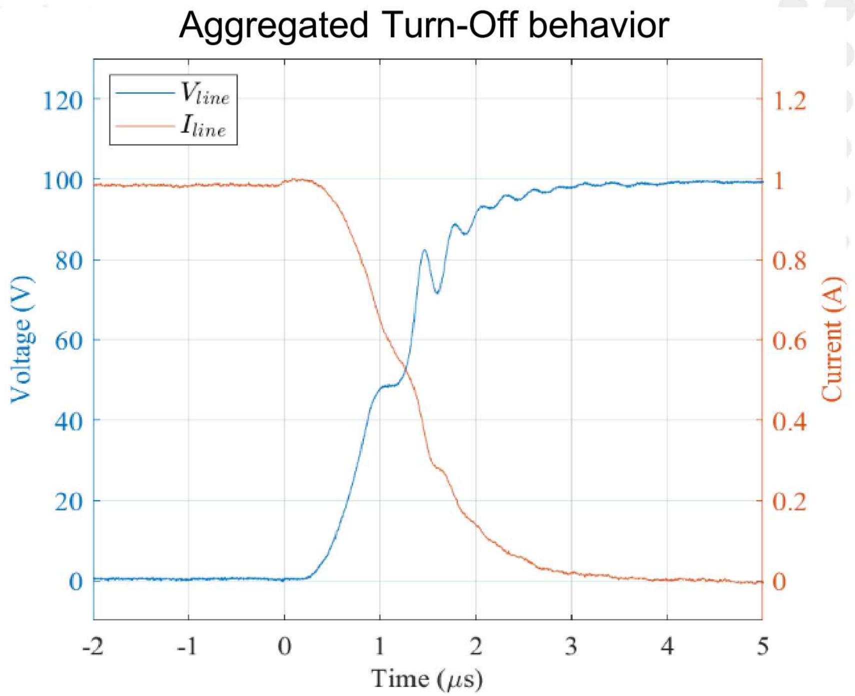
## Initial Forward Leg Prototype

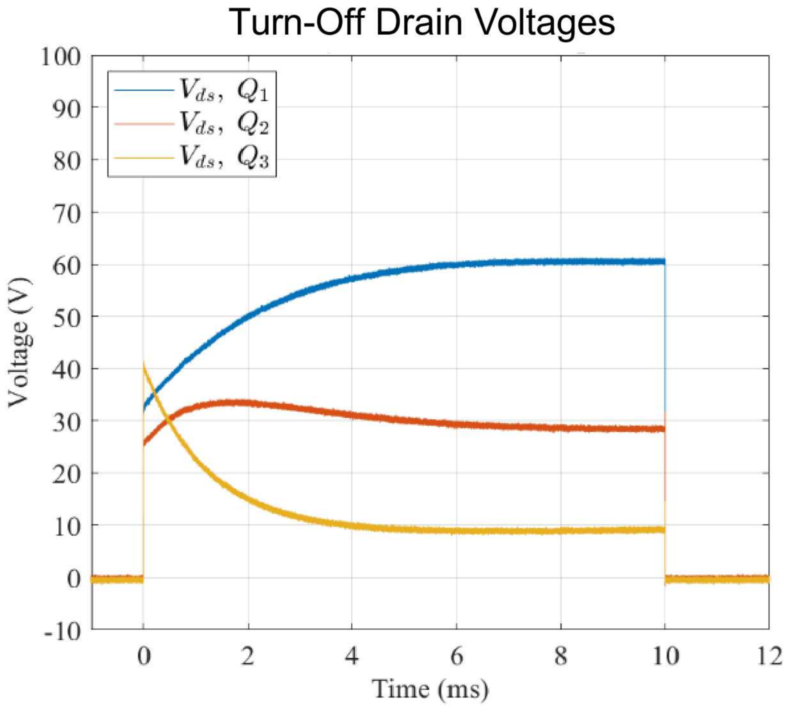
- 1.2 kV prototype has 3 cascaded JFETs
- 3x1.2 kV, 63 A SiC JFETs from United SiC selected for initial prototype; these have 105 mΩ, 10.5W loss at 10 A
- Prototype intended to demonstrate operation and calibrate models
- Subsequent prototype will be rated for 10 kV operation

**M2.4 Demonstration of low voltage CB (ongoing)**



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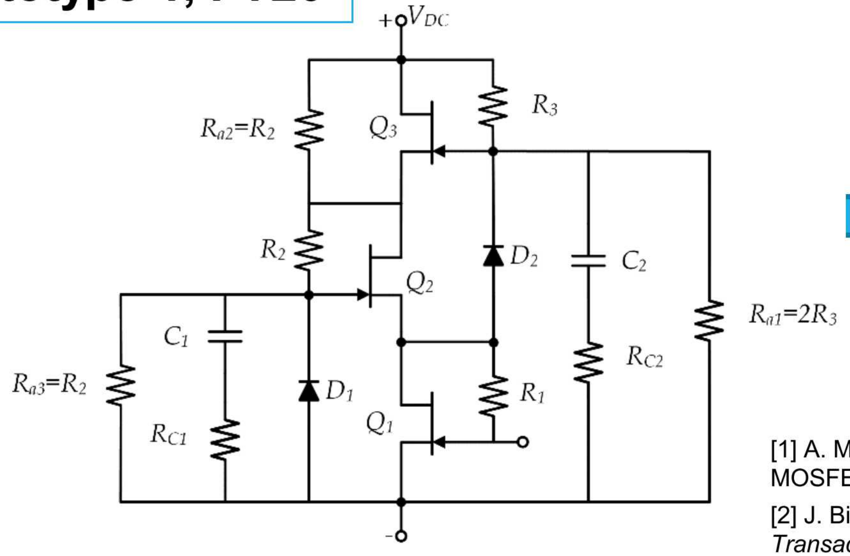
# Cascaded JFET Topology will Scale to >10 kV

## Several approaches were considered in Topology Selection

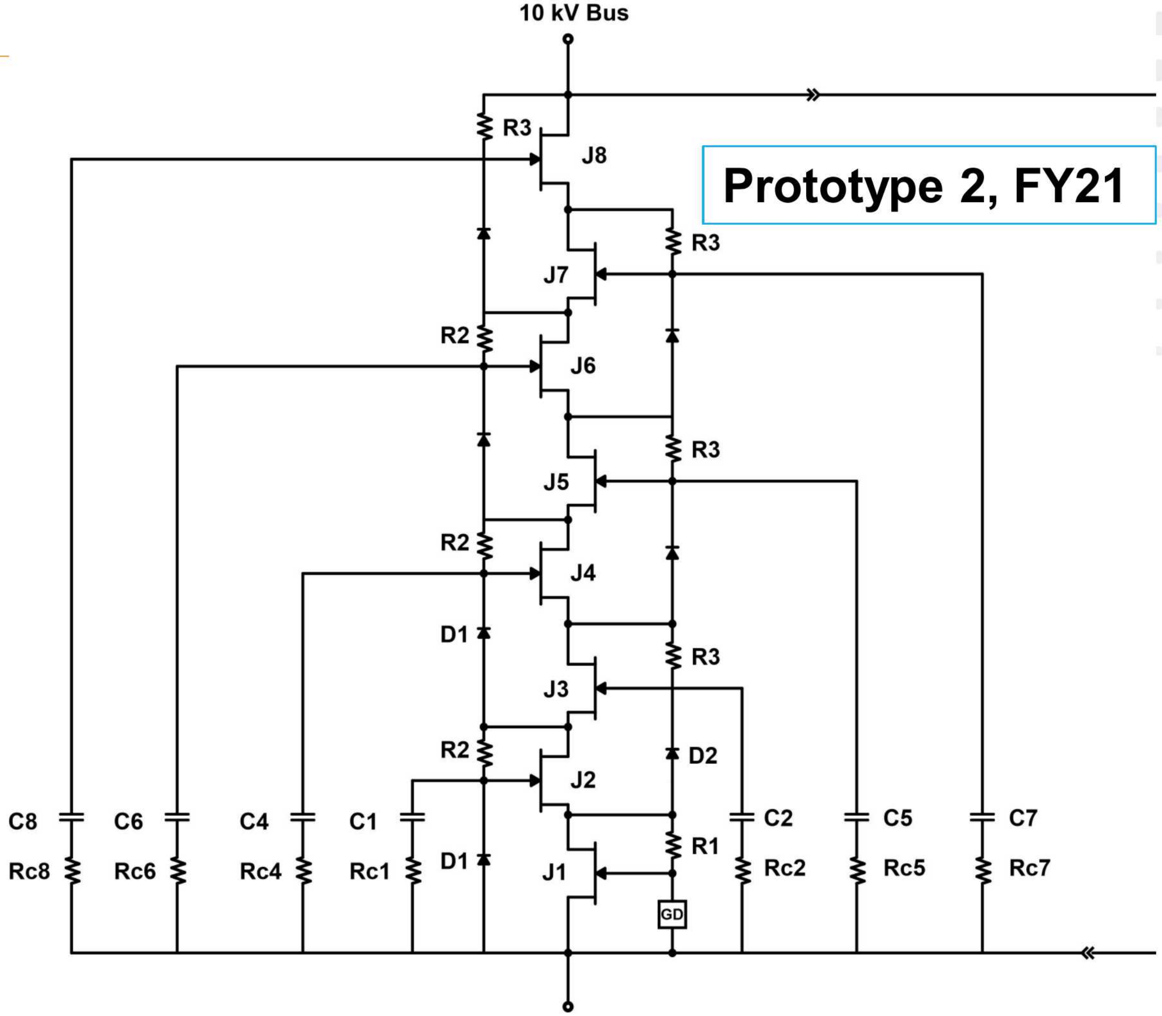
- Active Gate Driving Synchronization [1]
- Supercascode (Kolar) [2]
- Supercascode (Freedom Center) [3]
- Supercascode (United SiC) [4]

**Prototype 1, FY20**




Scalable to

**Prototype 2, FY21**





[1] A. Marzoughi, R. Burgos and D. Boroyevich, "Active Gate-Driver With dv/dt Controller for Dynamic Voltage Balancing in Series-Connected SiC MOSFETs," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 2488-2498, April 2019.

[2] J. Biela, D. Aggeler, D. Bortis and J. W. Kolar, "Balancing Circuit for a 5-kV/50-ns Pulsed-Power Switch Based on SiC-JFET Super Cascode," in *IEEE Transactions on Plasma Science*, vol. 40, no. 10, pp. 2554-2560, Oct. 2012.

[3] X. Song, A. Q. Huang, S. Sen, L. Zhang, P. Liu and X. Ni, "15-kV/40-A FREEDM Supercascode: A Cost-Effective SiC High-Voltage and High-Frequency Power Switch," in *IEEE Transactions on Industry Applications*, vol. 53, no. 6, pp. 5715-5727, Nov.-Dec. 2017.

[4] X. Lyu, H. Li, Z. Ma, B. Hu and J. Wang, "Dynamic Voltage Balancing for the High-Voltage SiC Super-Cascode Power Switch," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1566-1573, Sept. 2019.

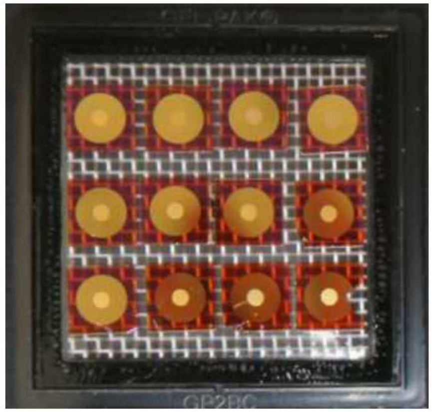
# Normally Off Leg Design – PCSS



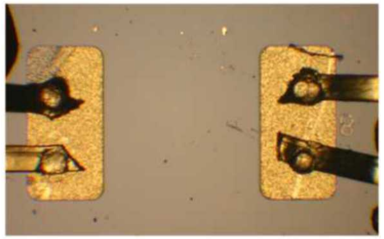
- **Lateral GaN PCSS Key Takeaways**:
  - Persistent conductivity
  - Small trigger laser energy requirement (20 µJ) with sub-bandgap wavelength (532 nm)
  - On-state maintaining field ~3kV/cm
  - Small switching latency and jitter (dependent on voltage and optical trigger energy)
- **Vertical GaN PCSS**:
  - Opportunity for higher bulk field holdoff (~110kV inherent breakdown voltage, assuming

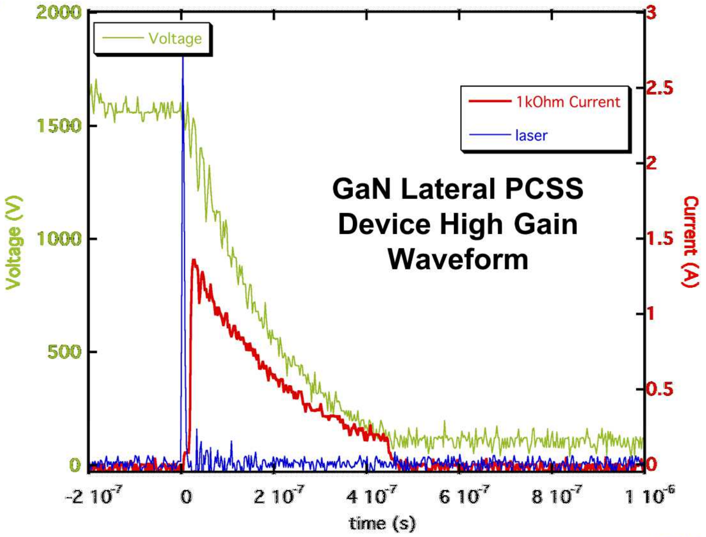
    3 MV/cm for GaN)
- **Vertical GaAs PCSS**:
  - Risk mitigation option from limited results in GaN
  - COTS compact optical triggers

**GaN Vertical PCSS Devices**
**375 µm thickness**

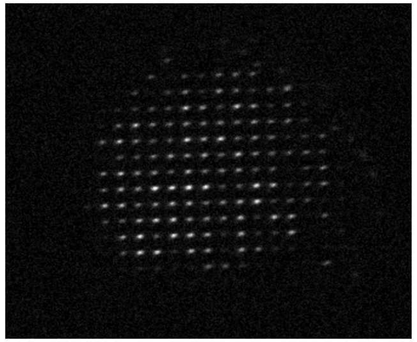


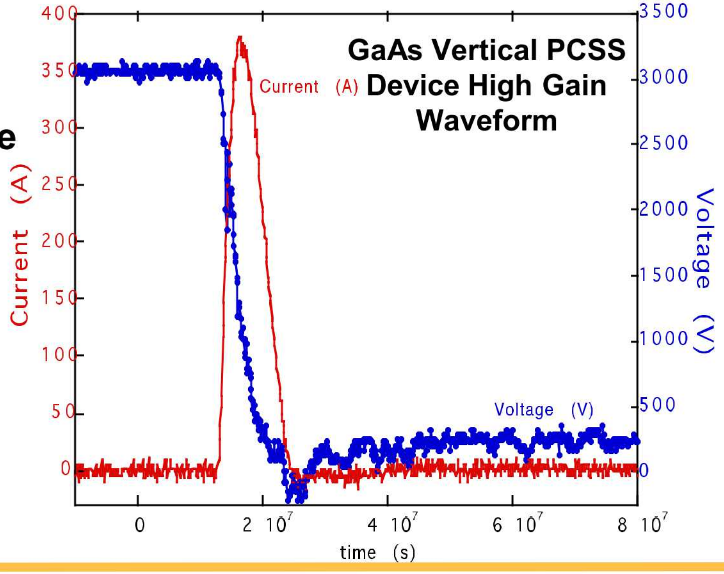
**GaN Lateral PCSS Devi**
**600 µm gap spacing**





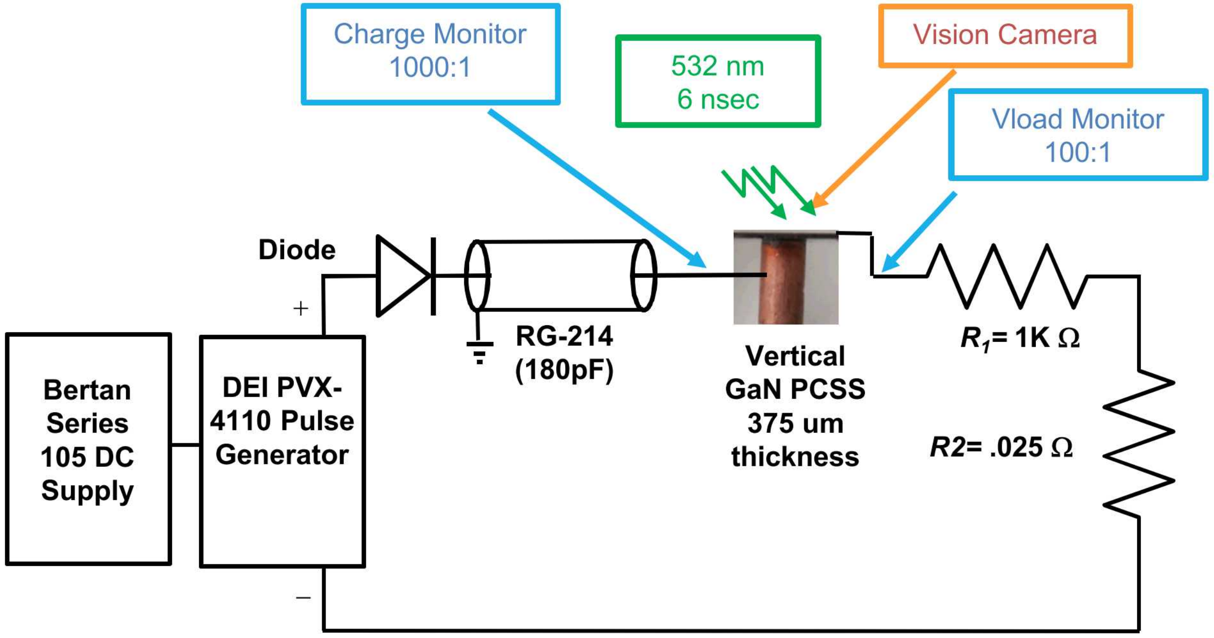

**GaAs Vertical PCSS Device**
**2-D Array of Filaments**

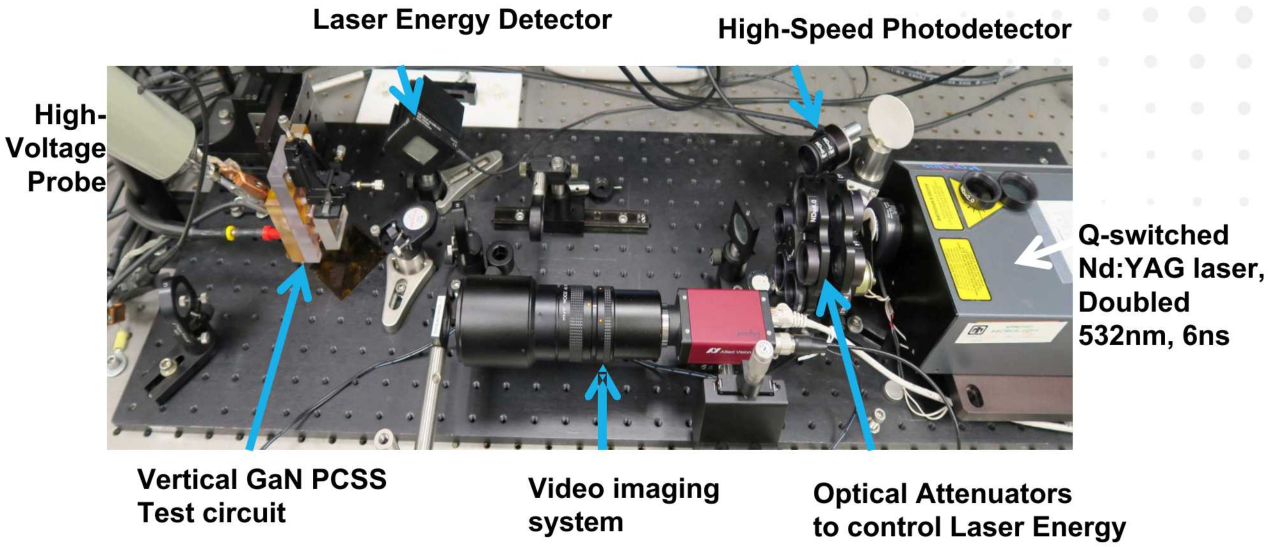




# Vertical GaN PCSS Results – Test Setup





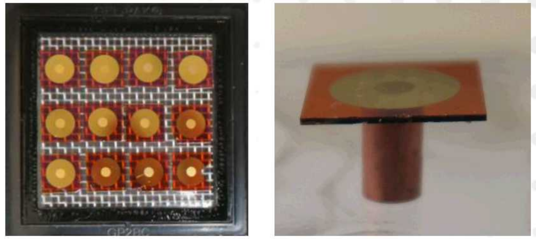

- Frequency doubled Nd:YAG (532 nm) Q-switched laser used as optical trigger
- RG-214 charge storage line pulse charged with ~60ns rise/fall time
- 1 kΩ current limiting resistive load
- Compact optical triggering sources and high-speed circuits are being developed and evaluated at UNM

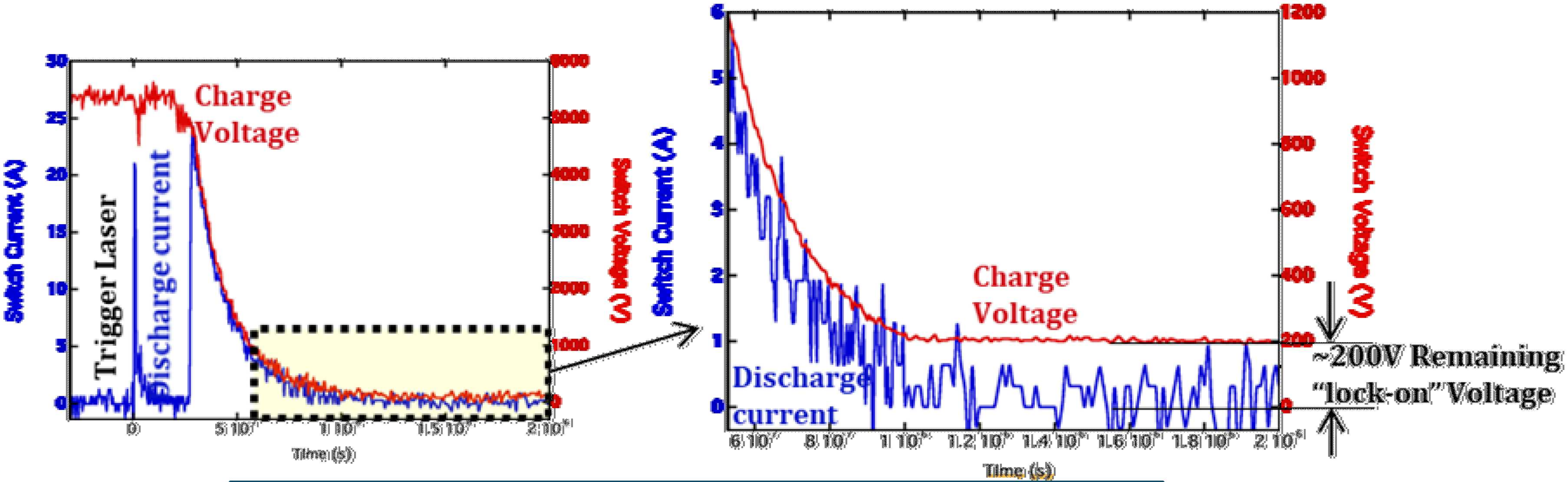
# Vertical GaN PCSS Results



- Switch charged to 5500 V (limited by test setup)
  - Internal field in bulk GaN = 150 kV/cm (Improving test setup for higher voltage)
- On-state persists well after laser pulse duration (high gain mechanism)
- On-state maintained with minimum critical (“lock-on”) field of ~5.3kV/cm
- Non-damaging to GaN (at limited currents)
- Low laser trigger energy required (< 30 μJ) at sub-bandgap (532 nm)
- Next steps: characterization of PCSS at various laser trigger wavelengths, increase voltage to 9 kV, lifetime testing at relevant currents (10 A - 100 A)

**GaN Vertical PCSS Devices**






**M3.1: Evaluate high-gain mode operation of vertical GaN PCSS prototypes.**

**Risks a and c mitigated: Vertical GaN PCSS high-gain mode demonstrated.**

# Mechanism for High Gain in GaN PCSS



- Software
  - REOS: Continuum solution of transport equations including defect reactions
  - EMC: Particle-based solution of the Boltzmann equation
- Previous Research: High gain in GaAs:
  - Lock-on field is similar to the Gunn field in GaAs
  - **GaAs Lock on field ~ GaAs Gunn field ~5kV/cm**
    - Two electron impact ionization
- Development of a New Mechanism for GaN:
  - GaAs theory inapplicable (LO field much lower than Gunn field)
    - **GaN Lock on field ~ 3-5 kV/cm, GaN Gunn field ~ 155 kV/cm**
  - Experimental observations in GaN devices informing development
  - New vertical switch experiments also informing development
  - Theory: Impact ionization of deep levels AND avalanche injection

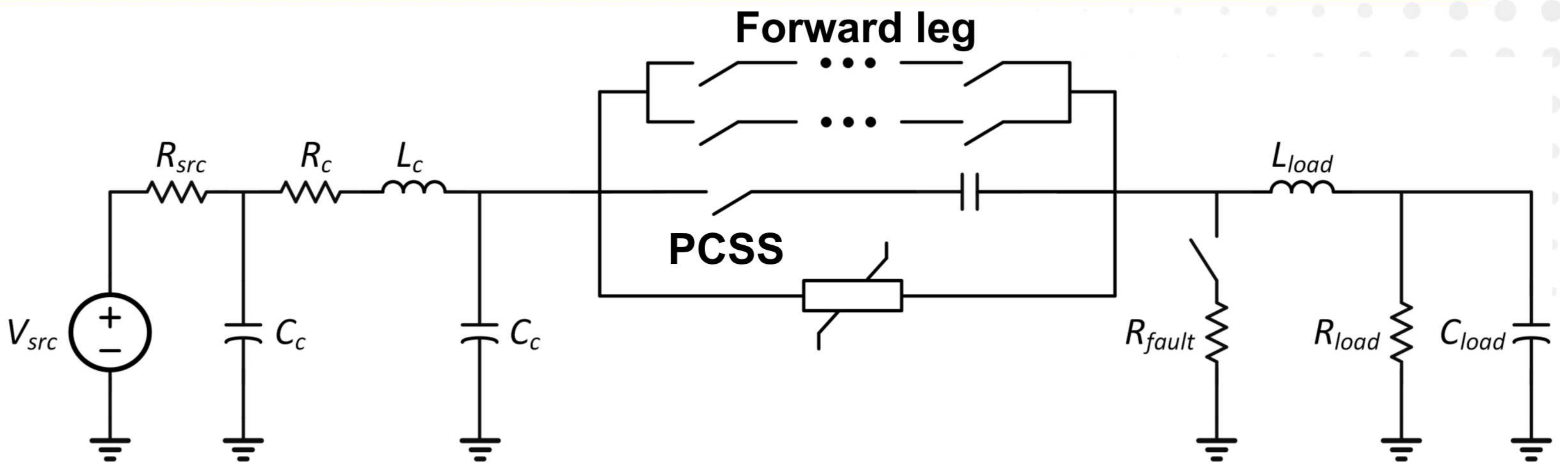


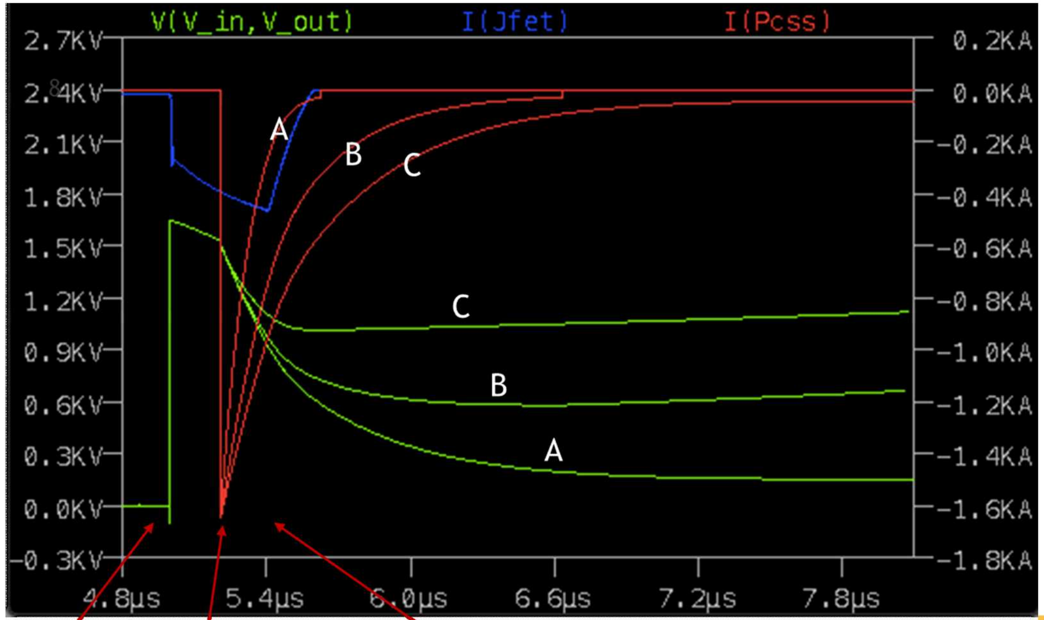
M2.5: Develop mechanistic understanding of GaN PCSS devices.

# System Performance is Being Evaluated in Simulation

**System level simulation model was generated to evaluate performance; includes:**

- Source and cable model
- JFET Cascade circuit model
- PCSS behavioral model
- Load model with adjustable R, L, C, P components




- Simulation shows shunt capacitor values of 0.2 µF, 1 µF, and 500 µF
  - Voltage across Breaker (green)
  - Current through PCSS leg (red)
  - Current through JFET leg (blue)
- Consider 3 cases when coordinating switching
  - A – PCSS conduction ends prematurely
  - B – PCSS and Forward leg well coordinated
  - C – PCSS conduction persists past Turn-Off

M2.1-M2.3: Design of Circuit Breaker.

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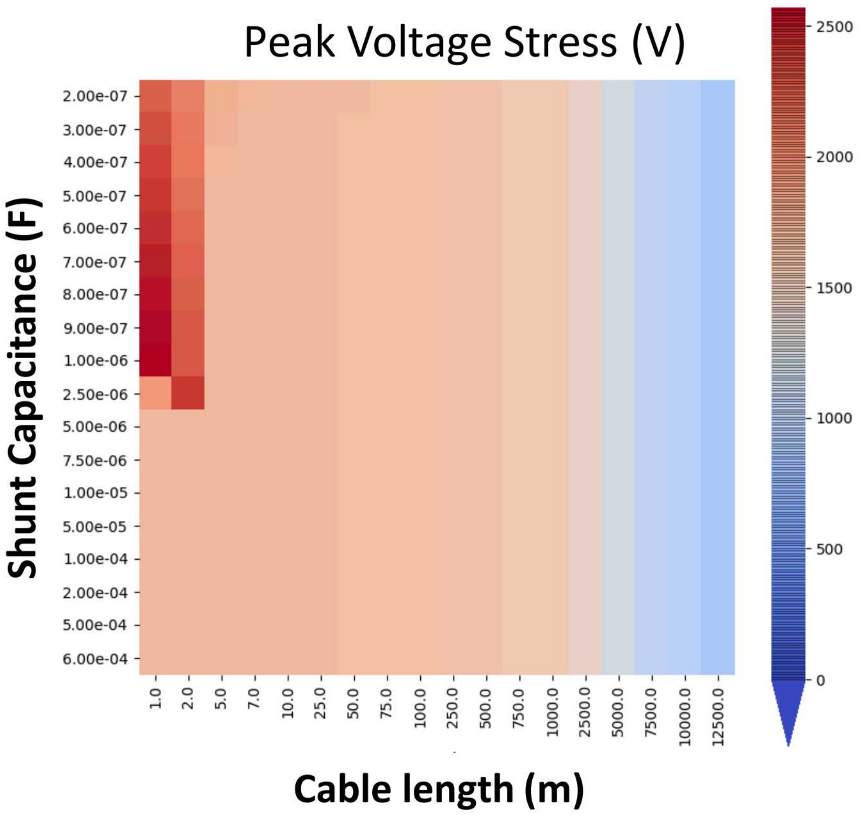
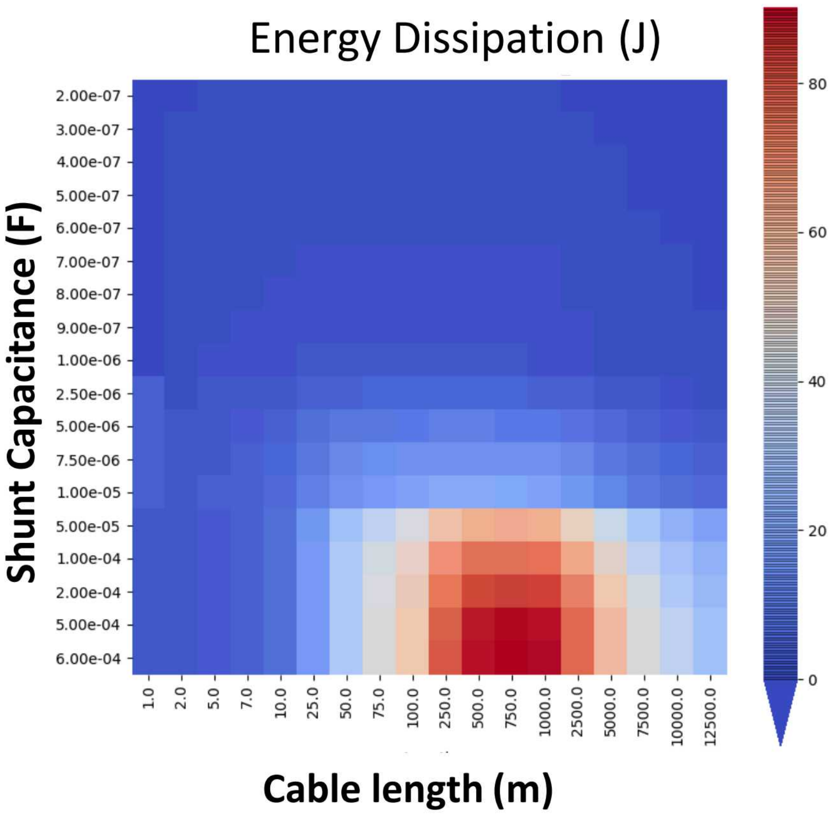
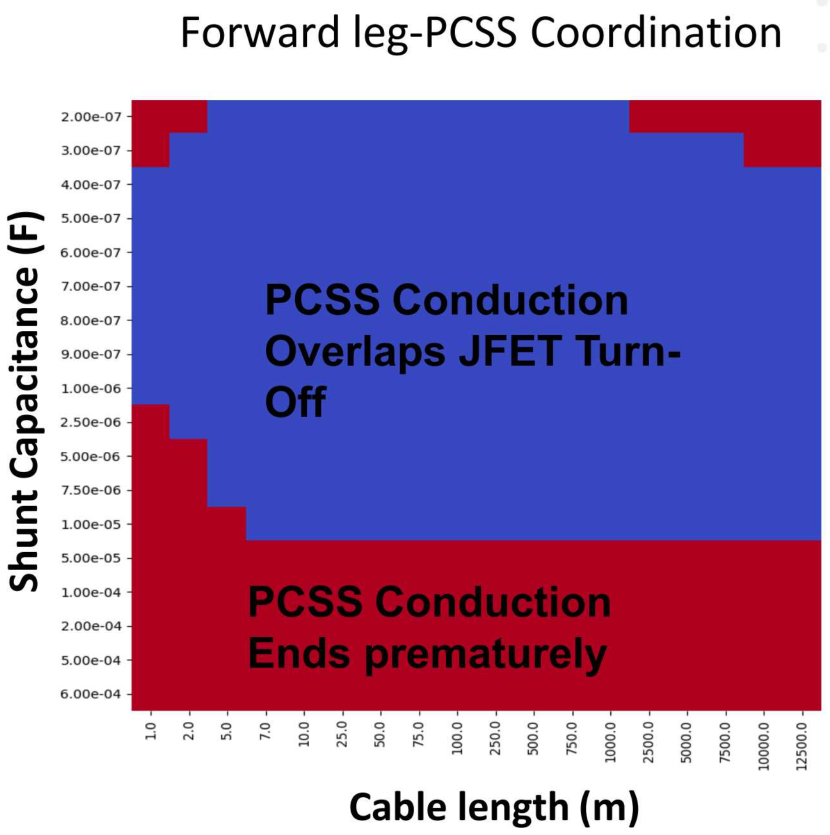
# Simulation Predicts the Sensitivity of Component Stress to System Parameters

- Multiple parameters are evaluated to determine system co-sensitivities to voltage, cable length, shunt capacitor value, switching delays, load characteristics, etc.



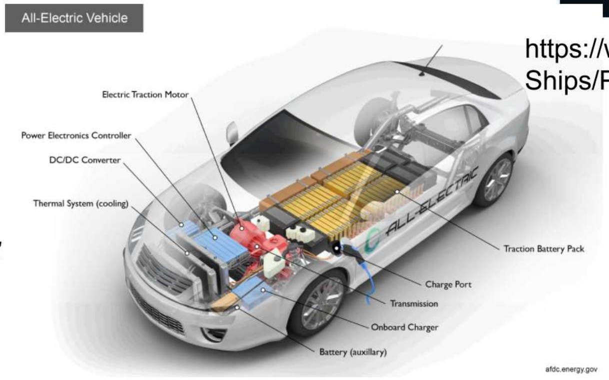



# Commercial Objectives

Technology-to-Market

- As SNL is FFRDC, our primary path for tech to market is licensing
  - Multiple entrepreneurial opportunities through Sandia/DOE programs
- System-level simulations leading to product definition strategies:
  - Reconfigurable CB technology for different system designs?
  - Multiple models for different system designs?
- Focusing on hardware demonstration in first ½ of project before engaging potential customers in:
  - Electric vehicles (ship/rail/car)
  - DC power conversion
  - Renewable energy integration into the grid
- IP being pursued
- Plan to publish and give conference presentations

https://www.navsea.navy.mil/Home/Team-Ships/PEO-Ships/Electric-Ships-Office/




https://afdc.energy.gov/vehicles/electric_basics_ev.html

https://www.nrel.gov/wind/grid-integration.html

# Activities



- **<u>Key Program Risks:</u>**
  – Unknown GaN PCSS performance/reliability
    - Tasks dedicated to this effort – ***looks promising.***
  – Availability of semi-insulating GaN substrates
    - Evaluating multiple vendors (two U.S. and two foreign sources)
  – COTS compact optical triggers at right wavelength and optical power levels
  – Evolving landscape for GaN Foundry services (CB cost)
    - Multiple efforts starting up. Guide cost estimates using SiC foundry models.
  – Alternative competing technologies