Constant Frequency ZVS PWM Converter

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***Abstract*— In this paper, a simple yet novel buck or boost adaptive zero-voltage switching (ZVS) converter topology is proposed for soft switching pulse-width modulation (PWM) dc / dc converters. The converter is designed for the high switching frequency that can achieve high efficiency by reducing switching losses for the entire load range at low and high power. Besides, the output at the load terminals is maintained by a PWM signal at a fixed switching frequency, a phase shift signal between converter ports (legs) controls the system circulating current in order to provide the ZVS condition in all load conditions. With the proposed controller, the converter, thus, is suitable for high switching frequency and high-power applications with the small volume. The proposed dc / dc converter operation is analyzed, designed, and confirmed by simulation results for 240 V input, 400 V / 5 A output, and 200 kHz operating frequency at full load.**

Keywords—ZVS, PWM, converter, high, constant frequency

I. INTRODUCTION

Buck or boost type of pulse-width modulation (PWM) dc–dc converters have been of interest to researchers and industries in a variety of practical energy conversion systems such as renewable energy sources [1]-[2], distributed power generation [3], telecommunication [4], and electrical vehicle applications [5]. In order to obtain a reliable and long-term operation, it is quite necessary to produce a dc / dc converter that has a high-power conversion efficiency minimizing the size and weight for these applications [6]-[9]. With the development of high switching speed of power semiconductors, high frequency power converters can be performable reducing the size of reactive components [10]-[11]. However, the converter power dissipation also increases with the frequency increment that growths dv / dt and di / dt stresses on the switch. Hence, zero voltage switching (ZVS) or zero current switching (ZCS) operation is required for efficient energy conversion. Also, full range soft switching reduces the EMI of the converter from no-load to full load that provides less size and weight of the EMI filter [12].

To improve the switch transition, many research studies have been proposed for the PWM dc-dc converters in the last few decades [7], [13]-[25]. Resonant converter topologies are very convenient achieving the ZVS for the entire load range [14]. However, their resonant component sensitivities to the frequency and temperature and complicated control techniques [15] encounter in a mass scale manufacturing unit. Adding passive components around each power device in the PWM converter [7], [16] can accomplish soft switching; however, it increases the size and cost with more design effort. The PWM converter's primary or secondary side can be designed with active clamp circuits [17]-[19] that allows to discharge the switch output capacitance without increasing conduction losses significantly. Although, it improves the ZVS condition in the converter, the circulating current can be increased resulting the converter efficiency less than expected or duty cycle may be lost effective duty ratio under high load conditions. Also, it upsurges the converter complexity. Three level converters are recommended to reduce the switching losses under low and high load ranges [20]-[21]. However, if the input voltage range is wide, their efficiency is degraded with the increase of circulating current. Furthermore, the circuit parasitic elements cause the severe voltage oscillation across the switches.

This paper proposes a new topology and ZVS approach for the soft switching PWM converters. The converter can be adaptable for buck or boost conversion with the high frequency. With the phase shift between two half-bridges enables the soft switching considering all load conditions. Moreover, the duty cycle manages the output voltage or current at the load terminals. This novel approach requires less complicated circuit topology comparing the other type solutions. The steady state characteristics of the proposed converter is demonstrated by analyzing the circuit operation in detail. The converter design example is derived with the selection of the key components. The theoretical analysis is verified by simulation of 200 kHz, 2 kW converter. Other advantages of the converter will be discussed in the following sections.

II. CIRCUIT DESCRIPTION

In this paper a new approach to fast switching dc / dc converters is introduced. A buck type topology of the proposed converter is shown in Fig. 1.

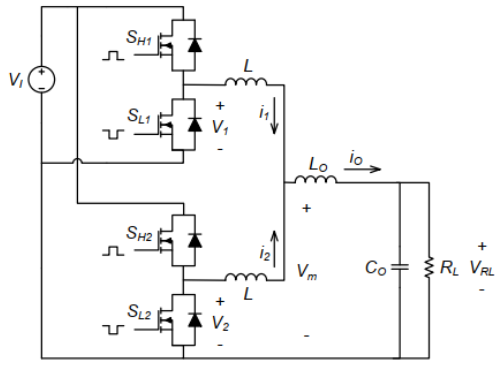

Fig. 1. Proposed topology of a dc / dc converter.

As shown in the figure, the topology consists of two half-bridges paralleled through two inductors L and the connected to the output L - C filter. The main idea in the proposed concept is to use circulating currents to achieve the ZVS condition all the time for all transistors. Then, it is possible to operate the converter at high switching frequency with high efficiency. The novelty introduced in this paper is a use of the phase shift between the two half-bridges to adjust the circulating current. Theoretical waveforms of voltages and currents in the proposed converter are shown in Fig. 2.

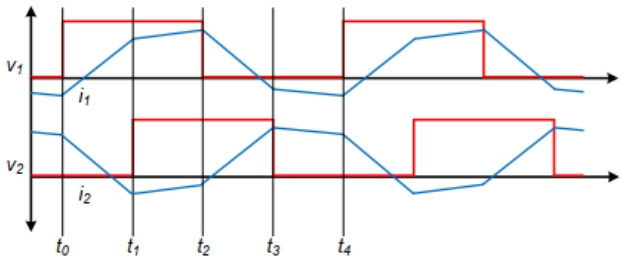

Fig. 2. Proposed topology of a dc / dc converter.

It can be seen, that there is negative current whenever the one of the top transistors (S_{H1} or S_{H2}) is turning-on, which allows recharging the parasitic capacitances during dead-time. Then the ZVS conditions are obtained. The amount of the negative current is adjusted by regulating the circulating currents mentioned before.

III. Circuit Analysis

The proposed dc / dc converter is developed to allow operating at the high switching frequency. As shown in Fig. 1, there are three inductors used in the circuit. Two of them, of inductance L each, are relatively small inductors which allows flow of a significant circulating current. The third inductor, of inductance L_O, is a part of output filter. As the converter operates at a high switching frequency the current ripples in the inductor L_O can be reduced. In order to simplify the theoretical analysis and emphasize the proposed concept it is assumed that the inductance L_O is high enough that the current i_O is constant. Then, the circuit can be simplified and redrawn as shown in Fig. 3.

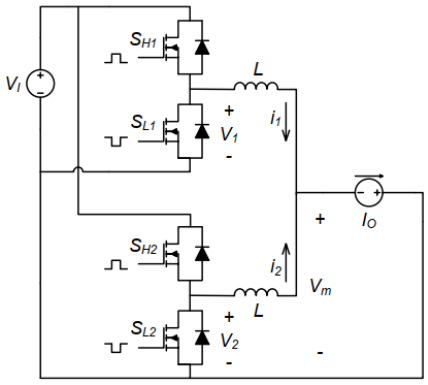

Fig. 3. Simplified topology of the proposed dc / dc converter used for the theoretical analysis.

It can be seen that the output filter with a load resistance R_L is replaced here by the current source I_O. In the simplified circuit, the voltage V_m over the current source I_O can be calculated in general as,

$$V_m = \frac{V_1+V_2}{2} \tag{1}$$

Then, it for various time periods marked in Fig. 2 it is equal to

$$\begin{aligned} t_0 - t_1 &: V_m = \frac{V_I}{2} \\ t_1 - t_2 &: V_m = -V_I \\ t_2 - t_3 &: V_m = \frac{V_I}{2} \\ t_3 - t_4 &: V_m = 0 \end{aligned} \tag{2}$$

Knowing V_1, V_2, and V_m it is possible now to calculate the inductor currents derivative as

$$\begin{aligned} t_0 - t_1 &: \frac{di_1}{dt} = -\frac{di_2}{dt} = \frac{V_I}{2L} \\ t_1 - t_2 &: \frac{di_1}{dt} = \frac{di_2}{dt} = 0 \\ t_2 - t_3 &: \frac{di_1}{dt} = -\frac{di_2}{dt} = -\frac{V_I}{2L} \\ t_3 - t_4 &: \frac{di_1}{dt} = \frac{di_2}{dt} = 0 \end{aligned} \tag{3}$$

From the circuit it is known that

$$I_O = i_1 + i_2 \tag{4}$$

For the analysis it is assumed, that the maximum and the minimum peak values of the currents i_1 and i_2 are equal and their values are i_{max} and i_{min} respectively. The theoretical voltage and current waveforms are shown in Fig. 4.

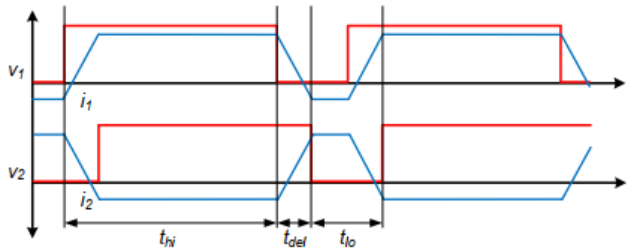

Fig. 4. Voltages and currents in the simplified dc / dc converter model.

Here, t_{hi} is the time period when the upper transistor (SH_x) is turnedon and t_{lo} is the time period when the lower transistor (SL_x) is turned-on, and t_{del} is a time delay between the phases. It can be seen that there is no equal current sharing between two phases. Moreover, the ratio between average switching leg currents depends on duty cycle and phase shift. The average currents can be calculated as follows,

$$i_{1arg} = \frac{i_{max}t_{hi}+i_{min}t_{hi}}{T} \tag{5}$$

$$i_{2arg} = \frac{i_{max}t_{lo}+i_{min}t_{lo}}{T} \tag{6}$$

The average phase currents i_{1arg} and i_{2arg} sum up to the output current I_O. Thus

$$i_{2arg} = i_{1arg} + i_{2arg} = i_{max} + i_{min} \tag{7}$$

In order to obtain the ZVS condition, the minimum amount of the current through the switching leg is required during the transition. The current must flow in a proper direction according to the transition direction. For instance, when the voltage V_I is changing from *0* to V_I, the current i_1 must be negative and when the voltage V_1 is changing from V_I to *0*, the current i_1 must be positive. Same for V_2 and i_2. For the analysis purpose the minimum transition current is introduced as I_{tmin}.

The output current and the minimum transition current defines the necessary current swing. Knowing that i_{min} must be equal to $-I_{tmin}$, i_{max} can be calculated as

$$i_{max} = I_O + I_{tmin} \tag{8}$$

The peak-to-peak value of the phase current is

$$i_{max} - i_{min} = I_O + 2I_{tmin} \tag{9}$$

Knowing the necessary current swing, the related phase-shift between the two half-bridges can be calculated. It is more practical to define this phase-shift as a time delay t_{del} as shown in the Fig. 2. Then, by rearranging (3) and (9) the time delay t_{del} can be calculated as

$$t_{del} = \frac{2L(I_O+2I_{tmin})}{V_I} \tag{10}$$

It can be concluded, that above equation is valid only if V_1 is not equal to V_2 during that time period. Thus, the limitations on the duty cycle are introduced. It is straightforward that

$$\begin{aligned} t_{hi} &\geq t_{del} \\ t_{lo} &\geq t_{del} \end{aligned} \tag{11}$$

Rearranging equations (10) and (11) results with equation for inductor value

$$\begin{aligned} L &\leq \frac{t_{hi}V_I}{2(I_O+2I_{tmin})} \\ L &\leq \frac{t_{lo}V_I}{2(I_O+2I_{tmin})} \end{aligned} \tag{12}$$

It can be furthermore rearrange by introducing the maximum output current I_{Omax}, and the minimum and the maximum duty cycles D_{min} and D_{max}. As the proposed topology is a buck type converter the duty cycle is defined as

$$D = \frac{t_{hi}}{t_{hi}+t_{lo}} \tag{13}$$

where t_{hi} + t_{lo} is a period T. Then, the equation (12) can be rewritten as

$$\begin{aligned} L &\leq \frac{V_I T(1-D_{max})}{2(I_{Omax}+2I_{tmin})} \\ L &\leq \frac{V_I T D_{min}}{2(I_{Omax}+2I_{tmin})} \end{aligned} \tag{14}$$

In order to estimate the inductor value L using above equations value of I_{tmin} must be known. It can be estimated based on the total output capacitance of the particular half-bridge C_{oss}. The charge stored in that capacitance is equal to

$$Q_{oss} = C_{oss}V_I \tag{15}$$

This capacitance needs to be recharged during the dead-time t_d when both of half-bridge transistors are turned-off. To simplify the calculations it is assumed, that the current through the switching leg is linearly decreasing during dead time from I_{tmin} down to zero. Thus, the average value of this current during the dead time is equal to $I_{tmin}/2$. Then, this current can be estimated as

$$I_{tmin} = \frac{2C_{oss}V_I}{t_d} \tag{16}$$

In the original circuit shown in Fig. 1 the current i_o is not constant but has some ripples. As long the inductance L_O is significantly larger than inductance L these ripples are relatively small and can be neglected. Taking them into account however

can improve efficiency of the converter especially when operating with duty cycle equal $D = 0.5$ when these ripples are highest. Then, the equation (10) can be rewritten as

$$t_{del} = \frac{2L(I_O + 2I_{tmin} - I_{ripple})}{V_I} \quad (17)$$

where I_{ripple} is the peak-to-peak value of current ripples on the inductor L_O. This value can be measured directly or estimated based on the inductor and operation point values.

IV. Design Example

To illustrate the proposed in this paper dc / dc converter the example design is shown. As the proposed topology is developed especially for high power applications, thus as an illustrative example 8 kW buck converter is used. The parameters of the converter are shown in Table I.

TABLE I - THE PROPOSED CONVERTER PARAMETERS

Symbol	Parameter	Values
f_o	operating frequency	145 kHz
V_I	dc input voltage	400 V
I_{Omax}	maximum output current	40 A
V_O	output voltage	200 V
C_{oss}	FET output capacitor	1800 pF
t_d	dead time	200 ns
D_{max}	maximum duty cycle	0.85
D_{min}	minimum duty cycle	0.15

The operating frequency f_o is selected to be 145 kHz to put the first harmonic outside of the conducted EMI measurement range, which usually starts at 150 kHz. The half-bridge output capacitance C_{oss} is estimated based on two IPW65R041CFD MOSFETs transistors with added parallel capacitance (1 nF) to reduce *dv / dt* when turning of at high current. As the first step of the design process, the minimum transition current I_{tmin} is calculated using (16)

$$I_{tmin} = \frac{2C_{oss}V_I}{t_d} = 7.2\ A \quad (18)$$

Then, the inductor L value is calculated using (14). As in this example $D_{min} = 1 - D_{max}$, then

$$L \le \frac{V_I T D_{min}}{2(I_{Omax} + 2I_{tmin})} = 3.8\ \mu H \quad (19)$$

The 3.3 µH inductor is selected. As the output filter inductor value L_O must be significantly larger than L, it is selected to be 220 µH.

V. Simulation Results

To validate the presented concept and its theoretical analysis circuit simulations are performed. In the simulation the circuit schematic shown in Fig. 1 is used with parameters specified and calculated in Section IV. As switches, IPW65R041CFD MOSFETs are used as they have outstanding performance in terms of r_{dson} and switching speed. For the purpose of verifying the proposed concept, the circuit is operating at the constant duty cycle $D = 0.5$ until reaching the steady state. The load resistance used in simulation is $R_L = 5\ \Omega$ which results in output power of 8 kW at 200 V output voltage. The time delay t_{del} between the half-bridges is obtained from 17 as

$$t_{del} = \frac{2 \times 3.33\ \mu H\ (40\ A + 2 \times 7.2\ A)}{400\ V} = 898\ ns \quad (20)$$

In the simulation, gate signals have trapezoidal shape with rise and fall time equal to 50 ns. To compensate it deadtime t_d and time delay between the two half-bridges t_{del} are extended by 100 ns. All the components used in simulation are ideal except for the switches for which actual models from manufacturer are implemented. Thus, only switch losses are analyzed. The obtained from simulation waveforms are shown in Fig. 5(a) and Fig. 5(b). It can be seen that the ZVS conditions are obtained for all the switches. Thus, switching losses are minimized, which is confirmed by the high efficiency equal to 98.4 %. The output voltage is 196.8 V, which results with output power of 7746 W. Thus, switches losses are equal to 126 W.

Then, the duty cycle was increased to $D = 0.75$ in order to illustrate operation with no equal average phase currents. The load resistance was set to $R_L = 7.5\ \Omega$ in order to maintain the same output current as in the previous case. The obtained from simulation waveforms are shown in Fig. 5(c) and Fig. 5(d) As before the ZVS conditions are obtained for all the switches. The efficiency for this case is equal to 98:8%. The output voltage is 296.5 V, which results with output power of 11722 W. Thus, switches losses are equal to 143 W.

For the comparison, same circuit with removed additional parallel capacitance on the half-bridge outputs and $t_{del} = 0$ is simulated. The measured efficiency in this case is 92.5 % for $D = 0.5$ and 95.2 % for $D = 0.75$. The simulated output voltages are 186.5 V and 286.5 V. The related output power is 6956 W and 10944 W. Thus, the switches losses are equal to 564 W and 552 W respectively. The simulation results summary is presented in Table II.

TABLE II - THE PROPOSED CONVERTER SIMULATION SUMMARY

D	R_L	t_{del}	η	P_o	P_{loss}
0.5	5 Ω	1 µs	98.4 %	7746 W	126 W
0.5	5 Ω	0 µs	92.5 %	6956 W	564 W
0.75	7.5 Ω	1 µs	98.8 %	11722 W	143 W
0.75	7.5 Ω	0 µs	95.2 %	10944 W	552 W

In the above table, the P_o is the output power and P_{loss} is power loss in the switches. The presented comparison clearly shows that by using proposed technique the switches losses are reduced more the four times. Thus, the converter can operate at high frequency with a high efficiency.

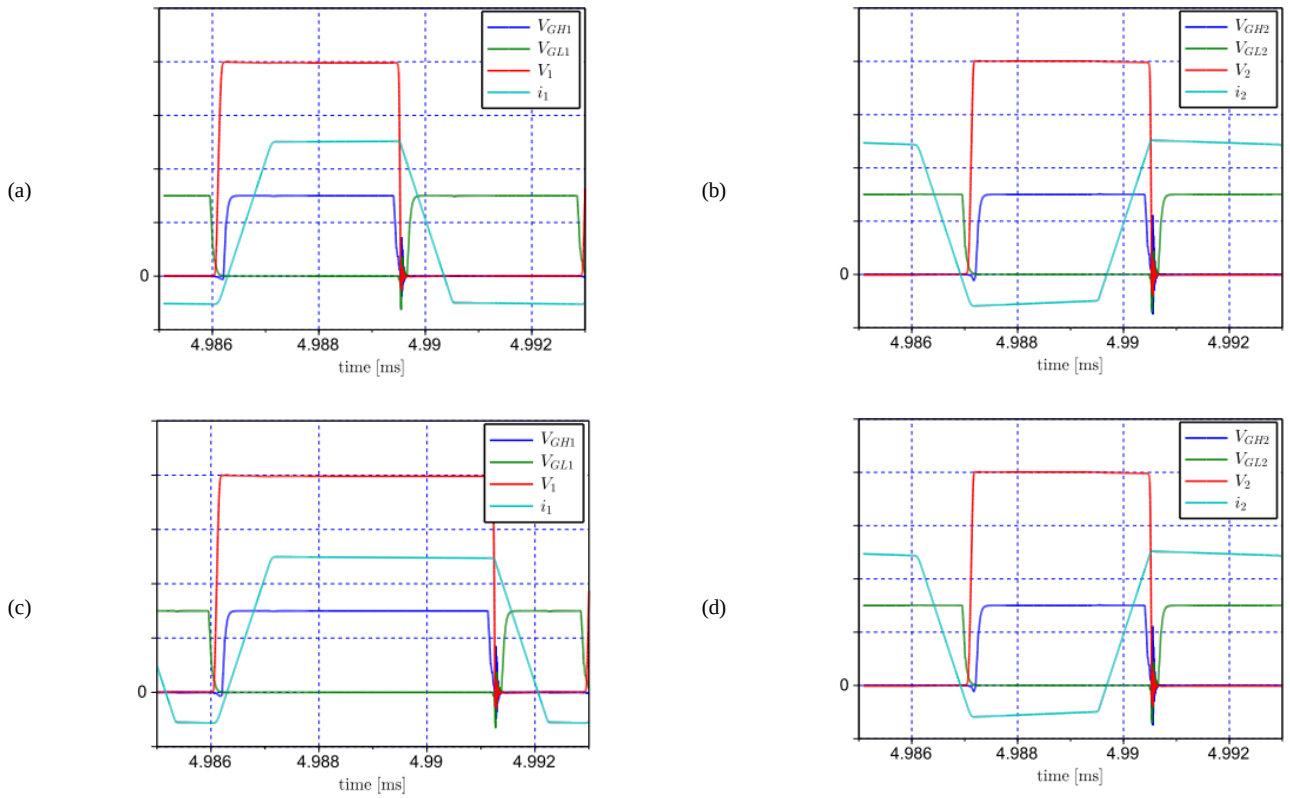

Fig. 5. Voltages and current in the proposed dc / dc converter, a) leading leg for $D = 0.5$, b) lagging leg for $D = 0.5$, c) leading leg for $D = 0.75$, d) lagging leg for $D = 0.75$. The V_{GH1}, V_{GH2} and V_{GL1}, V_{GL2} are gate to source voltages and are shown on 10 V / div scale. The V_1 and V_2 are half-bridge output voltages and are shown on 100 V / div scale. The i_1 and i_2 are half-bridge output currents and are shown on 20 A / div scale.

VI. Topology Variants

The proposed concept is based on the half-bridge topology. Thus, it can be used as a drop-in replacement in many applications where half-bridge topology is applicable. For instance, it can be used as boost converter, dc / ac inverter, or ac / dc converter like PFC. The boost variant of the proposed topology is shown in Fig. 6.

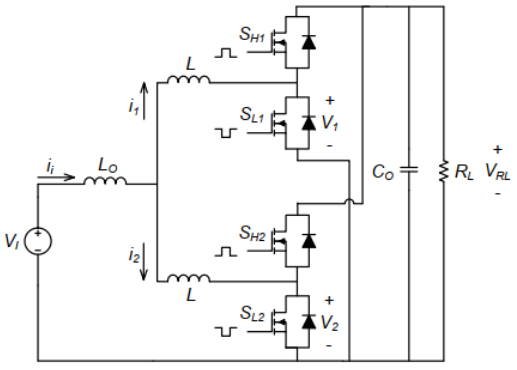

Fig. 6. Boost variant of the proposed converter topology

It can be observed that boost variant is very similar to the buck variant. The differences are reversed current direction and swap of the input and output. For the boost variant the equations for the minimum transition current I_{tmin} and the time delay t_{del} needs to be updated. Thus, the equation (16) is rewritten as

$$I_{tmin} = \frac{2C_{oss}V_O}{t_d} \tag{21}$$

and the equation (17) is rewritten as

$$t_{del} = \frac{2L(I_i+2I_{tmin}-I_{ripple})}{V_O} \tag{22}$$

It can be observed, that in the boost topology variant the minimum transition current I_{tmin} and the time delay t_{del} depends on the output voltage. Thus, it needs to be considered in the control loop design. The dc to ac inverter variant of the proposed topology is shown in Fig. 7.

It can be observed that boost variant is almost identical with the buck variant. The only difference is that the load is connected here to the middle point of the input voltage. Thus, output current i_O can have both positive and negative values. As the output current can have negative values, the equation for calculating the time delay t_{del} needs to be updated. Thus, the equation (17) is rewritten as

$$t_{del} = \frac{2L(|I_O|+2I_{tmin}-I_{ripple})}{V_I} \tag{23}$$

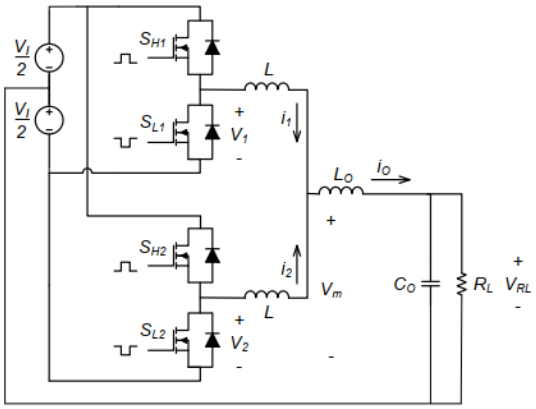

Fig. 7. dc to ac inverter variant of the proposed topology

VII. Conclusions

A novel soft switching ZVS PWM converter has been designed using a phase shift strategy for the buck or boost energy conversion systems. The structure of the converter is simpler than the other ZVS PWM converters that requires numerous components. The performance of the proposed converter is presented by analyzing the system. The design example is established with the component values to show the practicability of the converter. The simulation results are obtained and validated with theoretical calculation. The converter has the advantages of ZVS soft switching under the all load conditions and increasing the energy conversion efficiency with reducing the switching losses. The output voltage is managed by adjusting the duty cycle with the fixed switching frequency. The simulation results are presented for 400 V output voltage, 2 kW output power, and 200 kHz switching frequency at the full load.

References

[1] M. S. Ortmann, S. A. Mussa, M. L. Heldwein, "Three-Phase Multilevel PFC Rectifier Based on Multistate Switching Cells," IEEE Transactions on Power Electronics, vol.30, no.4, pp.1843-1854, April 2015.

[2] S. Bal, A. K. Rathore, D. Srinivasan, "Modular Snubberless Bidirectional Soft-Switching Current-Fed Dual 6-Pack (CFD6P) DC/DC Converter," IEEE Transaction on Power Electronics, vol.30, no.2, pp.519-523, February 2015.

[3] J. Holtz, M. Holtgen, J. O. Krah, "A Space Vector Modulator for the High-Switching Frequency Control of Three-Level SiC Inverters," IEEE Transactions on Power Electronics, vol.29, no.5, pp.2618-2626, May 2014.

[4] P. Das, M. Pahlevaninezhad, A. S. Kumar Singh, "A Novel Load Adaptive ZVS Auxiliary Circuit for PWM Three-Level DC–DC Converters," IEEE Transactions on Power Electronics, vol.30, no.4, pp.2108-2126, April 2015.

[5] K. Colak, M. Bojarski, E. Asa, D. Czarkowski, "A constant resistance analysis and control of cascaded buck and boost converter for wireless EV chargers," IEEE Applied Power Electronics Conference and Exposition (APEC), 2015, pp. 3157-3161.

[6] A. Mousavi, G. Moschopoulos, "A New ZCS-PWM Full-Bridge DC–DC Converter with Simple Auxiliary Circuits," IEEE Transactions on Power Electronics, vol.29, no.3, pp.1321-1330, March 2014.

[7] E. Asa, K. Colak, D. Czarkowski, B. Ozpineci, "Analysis of High Frequency AC Link Isolated Three Port Resonant Converter for UAV Applications," IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 1679-1684.

[8] B. Gu, J. Dominic, B. Chen, L. Zhang, J. S. Lai, "Hybrid Transformer ZVS/ZCS DC–DC Converter With Optimized Magnetics and Improved Power Devices Utilization for Photovoltaic Module Applications," IEEE Transactions on Power Electronics, vol.30, no.4, pp.2127-2136, April 2015.

[9] E. Asa, K. Colak, M. Bojarski, D. Czarkowski, "Asymmetrical Duty-Cycle and Phase-Shift Control of a Novel Multiport CLL Resonant Converter," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 3, no. 4, pp. 1122-1131, Dec. 2015.

[10] M. Rodriguez, Y. Zhang, D. Maksimovic, "High-Frequency PWM Buck Converters Using GaN-on-SiC HEMTs," IEEE Transactions on Power Electronics, vol.29, no.5, pp.2462-2473, May 2014.

[11] P. F. Miaja, A. Rodriguez, J. Sebastian, "Buck-Derived Converters Based on Gallium Nitride Devices for Envelope Tracking Applications," IEEE Transactions on Power Electronics, vol.30, no.4, pp.2084-2095, April 2015.

[12] D. Hamza, M. Pahlevaninezhad, P. K. Jain, "Implementation of a Novel Digital Active EMI Technique in a DSP-Based DC–DC Digital Controller Used in Electric Vehicle (EV)," IEEE Transactions on Power Electronics, vol.28, no.7, pp.3126-3137, July 2013.

[13] C. W. Tsang, M. P. Foster, D. A. Stone, D. T. Gladwin, "Analysis and Design of LLC Resonant Converters with Capacitor–Diode Clamp Current Limiting," IEEE Transactions on Power Electronics, vol.30, no.3, pp.1345-1355, March 2015.

[14] E. Asa, K. Colak, D. Czarkowski, "Analysis of a CLL Resonant Converter With Semi-Bridgeless Active Rectifier and Hybrid Control," in IEEE Transactions on Industrial Electronics, vol. 62, no. 11, pp. 6877-6886, Nov. 2015.

[15] M. Momeni, H. M. Kelk, H. Talebi, "Rotating Switching Surface Control of Series-Resonant Converter Based on a Piecewise Affine Model," IEEE Transactions on Power Electronics, vol.30, no.3, pp.1762-1772, March 2015.

[16] A. Parastar, J. K. Seok, "High-Gain Resonant Switched-Capacitor Cell-Based DC/DC Converter for Offshore Wind Energy Systems," IEEE Transactions on Power Electronics, vol.30, no.2, pp.644-656, February 2015.

[17] C. Liu, B. Gu, J. S. Lai, M. Wang, Y. Ji, G. Cai, Z. Zhao, C. C. Liang, C. Zheng, P. Sun, "High-Efficiency Hybrid Full-Bridge–Half-Bridge Converter With Shared ZVS Lagging Leg and Dual Outputs in Series," IEEE Transactions on Power Electronics, vol.28, no.2, pp.849-861, February 2013.

[18] U. R. Prasanna, A. K. Rathore, "Small-Signal Modeling of Active-Clamped ZVS Current-Fed Full-Bridge Isolated DC/DC Converter and Control System Implementation Using PSoC," IEEE Transactions on Industrial Electronics, vol.61, no.3, pp.1253-1261, March 2014.

[19] B. Gu, C. Y. Lin, B. Chen, J. Dominic, J. S. Lai, "Zero-Voltage-Switching PWM Resonant Full-Bridge Converter With Minimized Circulating Losses and Minimal Voltage Stresses of Bridge Rectifiers for Electric Vehicle Battery Chargers," IEEE Transactions on Power Electronics, vol.28, no.10, pp.4657-4667, October 2013.

[20] J. L. Duarte, J. Lokos, F. B. M. V. Horck, "Phase-Shift-Controlled Three-Level Converter With Reduced Voltage Stress Featuring ZVS Over the Full Operation Range," IEEE Transactions on Power Electronics, vol.28, no.5, pp.2140-2150, May 2013.

[21] Y. Shi, X. Yang, "Wide-Range Soft-Switching PWM Three-Level Combined DC–DC Converter Without Added Primary Clamping Devices," IEEE Transactions on Power Electronics, vol.29, no.10, pp.5157-5171, October 2014.