SAND2020-8161C

3.3-kV SiC MOSFET Performance and Short-Circuit Capability

Diang Xing, Chen Xie, Ke Wang, Tianshi Liu, Boxue Hu, Jin Wang, and Anant Agarwal
Center for High Performance Power Electronics (CHPPE)
The Ohio State University
Columbus, OH, USA
xing.174@osu.edu, agarwal.334@osu.edu

Ranbir Singh
GeneSiC Semiconductor Inc.
Dulles, VA, USA
ranbir.singh@genesicsemi.com

Stanley Atcitty
Sandia National Laboratories
Albuquerque, NM, USA
satcitt@sandia.gov

***Abstract*— This paper compares the long-channel and short-channel 3300-V, 5-A silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) manufactured by GeneSiC regarding static characteristics and short-circuit (SC) sustaining capability. Their saturation currents were measured up to 2200-V drain bias at different gate voltages. The SC withstand times of two types of devices were measured at 2200-V drain voltage and 18-V gate voltage. Their SC test results were compared with 1200-V SiC MOSFETs from four different manufactures, which suggested that SiC MOSFETs with longer channel length should have longer sustaining times in a SC event. In addition, the device dynamic characteristic was evaluated. A comprehensive simulation program with integrated circuit emphasis (SPICE) model was developed based on the device test results.**

Keywords—Silicon carbide (SiC), MOSFET, channel length, short-circuit, Double pulse test (DPT), modeling.

I. INTRODUCTION

Medium voltage (MV) semiconductors greater than 3000 V are attractive for power conversion applications to avoid the complex voltage stacking structure and achieve a simplified control strategy. However, commercial silicon (Si) based MV devices suffer from one or more limitations including high hard-switching loss, high specific on resistance and lower maximum junction temperature. Wide-bandgap (WBG) semiconductors have shown improved performance compared with Si devices [1] - [3]. Though most of MV WBG devices are still emerging with relatively high cost, devices are readily available from some manufacturers including GeneSiC. These devices need to be evaluated for performance and reliability for the market pull they will have in the future.

The targeted devices in this paper are 3300-V, 5-A, TO-268 packaged SiC metal–oxide–semiconductor field-effect transistor (MOSFET) samples from GeneSiC. Some papers have already reported the older generation of this series of devices in terms of static and dynamic performances [4], [5]. The test samples in this paper are relatively one or two years old, and they contain two types of designs with different channel lengths. In this paper these two kinds of devices were tested to analyze the relationship between the short-circuit (SC) withstanding capability and channel length for the first time. Their SC withstand times (SCWTs) were also compared with 1200-V commercial SiC MOSFETs from four different manufacturers at the same gate voltage and 2/3 of rated drain-source voltages. All the measurements were conducted at room temperature. Furthermore, a SPICE model for the 3300-V device was developed based on the evaluation results.

In this paper, the static characteristics comparisons of long-channel and short-channel devices are presented in the Section II. The SC tests are shown in the Section III. Section IV shows the device dynamic performance through double-pulse test (DPT). Finally, the device SPICE modeling including first quadrant I-V curves, body/integrated Schottky diode I-V curve, drain-source leakage current, and parasitic capacitances is presented in Section V.

II. CHANNEL-LENGTH RELATED STATIC CHARACTERISTICS

Agilent curve tracer B1505A was used to measure the device static characteristics except the saturation current at high drain voltage. The saturation current was measured through a custom setup shown in Fig.1. The current was measured through the voltage drop across the 0.1-Ω shunt resistor. Decoupling capacitors were used to achieve low loop stray inductance. External 20-Ω gate resistor was used to achieve slow turn-off speed. For each point, 1-μs turn-on gate voltage pulse was applied at different drain bias, and the saturation current was extracted after 500 ns when the device was turned on.

The first quadrant I-V curves of both short-channel and long-channel devices are plotted in Fig.2. A higher current is observed in the short-channel device at the same V_{ds} and V_{gs} condition compared with the long-channel device. When V_{gs} =

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

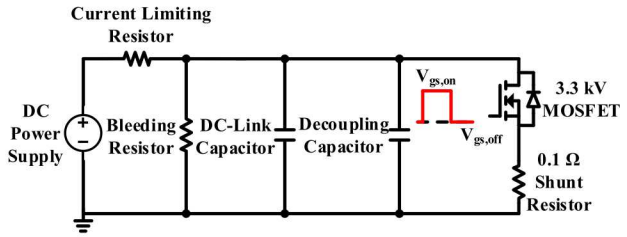


Fig.1 Circuit diagram for saturation current/SC tests.

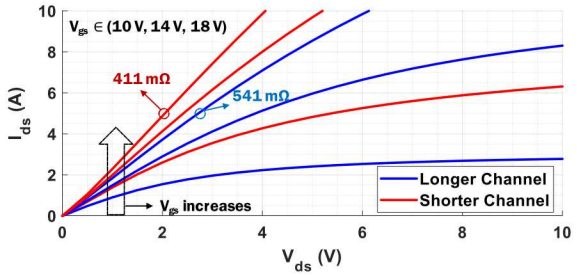


Fig.2 First quadrant I-V curves of short-channel and long-channel devices.

18 V and I_{ds} = *5 A*, long-channel device has 541-mΩ $R_{ds(on)}$ and short-channel device has 411-mΩ $R_{ds(on)}$. In Fig.3, I_{ds} and transconductance (g_m) are plotted at 0.1-V V_{ds} with V_{gs} increasing form 0 V to 20 V. The short-channel device shows higher maximum value of g_m. The threshold voltage was extracted through the linear extrapolation method. The short-channel device has threshold voltage of 3.32 V, and the long-channel MOSFET has threshold voltage of 3.79 V. The saturation currents were measured up to a drain voltage of 2/3 of the rated voltage (2200 V) at three different gate voltages as shown in Fig.4. Both saturation currents increased with higher drain bias and the short-channel device showed higher currents at the same gate voltage condition compared with the long-channel device. In terms of other static features, no significant difference was found in their drain-source leakage current, gate-source leakage current, and terminal capacitances.

The static characteristics show that the device with long channel have worse conductance when fully turned-on. The higher resistance is related to the poor inversion layer mobility of SiC MOSFETs, resulting from the high density of SiC/SiO_2 interface traps (Dit) [6], [7]. Even for MV MOSFETs with thick drift layer and large drift layer resistance, channel resistance can be a large fraction of total resistance. Another factor resulting a lower conductance for a long-channel device could be its larger threshold voltage caused by the longer channel [8], [9]. Both disadvantages make the long-channel devices less attractive in terms of performance compared to the short-channel one. However, the device with short-channel has lower barrier between source and channel, which results in higher output current when a high drain bias is applied [10]. This can make the short-channel device have higher saturation current and be less reliable when SC events happen. With higher drain bias, a significant increase in saturation current can be observed for both devices as shown in Fig.4. As temperature rises during SC, the effective inversion layer electron mobility also increases [11] resulting in higher channel conductance for both cases.

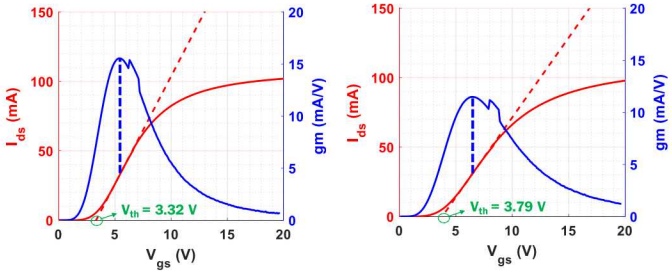


Fig.3 Measurement of threshold voltages for short-channel (a) and long-channel (b) devices.

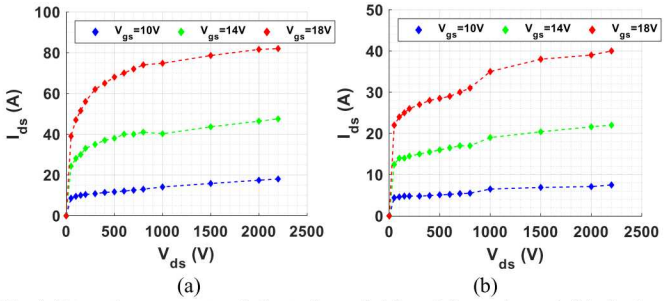


Fig.4 Saturation currents of short-channel (a) and long-channel (b) devices with different gate voltages up to V_{ds} of 2.2 kV.

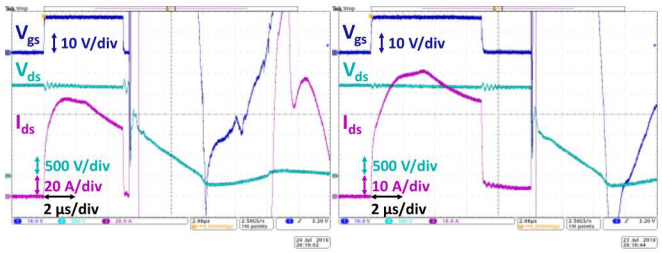
III. Channel-Length Related Short-Circuit Capability

The SCWTs of both short-channel and long-channel devices were measured at 2200-V drain voltage and 18-V turn-on / 0-V turn-off gate voltages. The tests started with a 1-μs SC pulse and then followed by continuous single pulses with increment of 1 μs until the device failed. The interval between each test point was longer than 1 min to make sure the device fully cooled down. The device drain-source voltage, gate-source voltage, and drain-source current were recorded in the tests.

Fig.5 shows the waveforms when the tested devices failed. The short-channel device dissipated 900 mJ energy within 5 μs, while the long-channel device dissipated 799 mJ energy within 7 μs. Both devices failed catastrophically after the gate voltage was turned off. These SC failures are caused by temperature related physical changes [12], [13]. The long-channel device survived for longer time due to lower SC current.

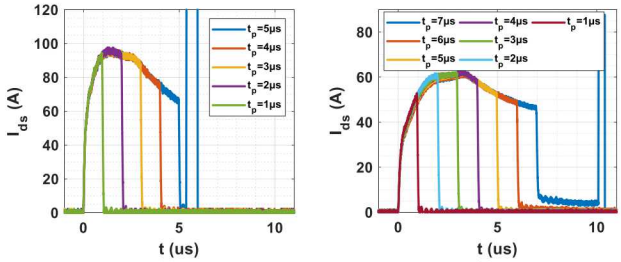
Fig.6 plots SC current waveforms with increasing pulse length. Current tails after device turn-off can be found in the 5-μs-pulse waveform for the short-channel device, and the 6-μs and longer pulses for the long-channel device. Negative threshold voltage at high temperature, or largely thermal generated electron-hole pairs in hot spots could be the reasons observed current tails [13], [14].

Due to the lack of enough 3300-V SiC MOSFETs from other vendors in the market, the SCWTs of targeted devices were compared with four 1200-V SiC MOSFETs from different commercial manufacturers at normalized conditions (2/3 of rated drain voltage and 18-V gate voltage). The results are shown in Fig.7. On average, the SCWT of 3300-V devices (6 μs) is longer than the SCWT of 1200-V devices (4.4 μs).



(a) (b)

Fig.5 The SC tests waveforms (a) The short-channel device failed at the 5-µs pulse after switching off; (b) the long-channel device failed at the 7-µs pulse after switching off.



(a) (b)

Fig.6 SC currents for each SC pulse: (a) short-channel device, (b) long-channel device.

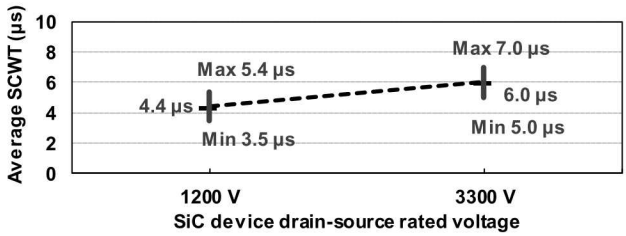


Fig.7 1.2-kV & 3.3-kV devices SCWTs comparisons. Four 1.2-kV devices have 3.5, 4.0, 4.8, and 5.4-µs SCWTs respectively.

This is expected as the 3300 V devices with thicker drift layer, offer lower SC current density (normalized to die area) and larger thermal capacitance of the die.

IV. Dynamic Evaluation

A custom DPT setup was built to investigate the device switching performance, and its circuit diagram is shown in Fig.8. The lower switch was driven by 18-V turn-on voltage and – 4-V turn-off voltage. Its turn-on external gate resistor was 20 Ω and the turn-off gate resistor was 10 Ω. The upper switch was kept in an off position to act as a freewheeling diode. Active Miller clamping circuit was used in both upper and lower switches to stabilize the gate signals. Considering both long-channel and short-channel devices have almost the same parasitic capacitances, only the test results of the device with short channel are presented.

The DPT waveforms of lower switch are shown in Fig.9. The dc bus voltage is 2400 V and the inductive switching current is 6 A. The fall time of V_{ds} from 90% to 10% is 95 ns with dV/dt of 20.2 kV/µs during turn-on, and the rise time of V_{ds} from 10% to 90% is 45 ns with dV/dt of 42.7 kV/µs during turn-off. The total switching loss is around 1 mJ including 850 µJ switching-on loss and 150 µJ switching-off loss.

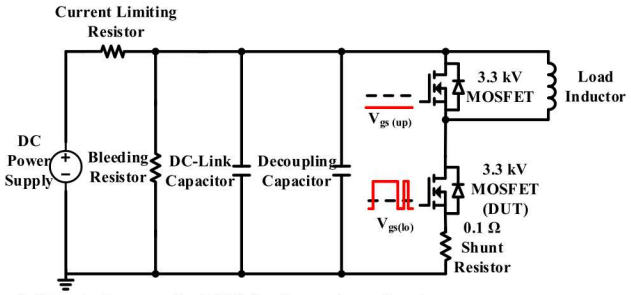
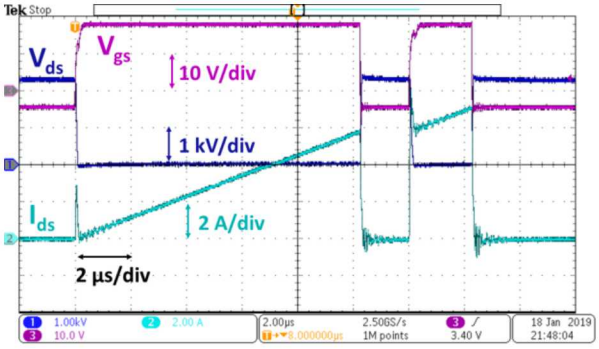
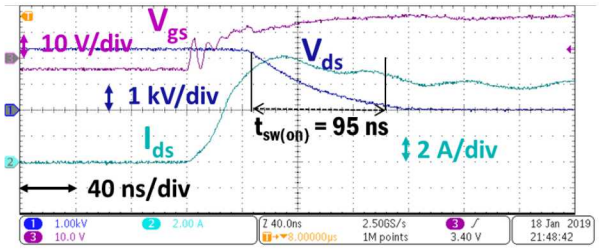


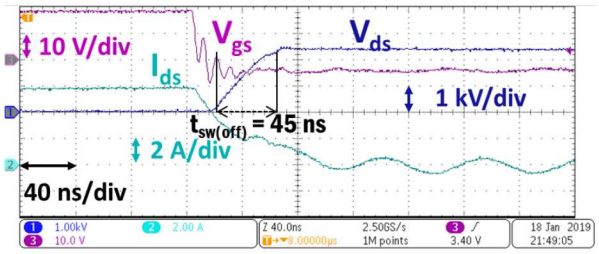
Fig.8 Circuit diagram for DPT for dynamic evaluation.



(a)



(b)



(c)

Fig.9 (a) Device DPT waveforms; (b) zoomed in on switching-on transient; (c) zoomed in on switching-off transient.

V. SPICE Modeling

The SPICE modeling method for the short-channel 3300-V device is discussed next. Based on static characteristics, the models for first quadrant I-V curves, body diode I-V curves in third quadrant, drain-source leakage current, and three parasitic capacitances (C_{dg}, C_{ds}, C_{gs}) were developed.

A. Modeling of First Quadrant I-V Curves

Classic MOSFET SPICE voltage controlled current source models are labeled and known as level-1, level-2, and level-3 models, which are analytical or semi-empirical models with

parameters and equations derived from physics [15], [16]. The level-1 model with channel length modulation was built in this paper. The model was improved by adding a bulk charge variation parameter [15], which is considered as a constant in the traditional level-1 model equations. The complete formula is shown as:

$V_{gs} \le V_{th}$ (cutoff region)

$$I_{ds} = 0 \tag{1}$$

$0 < V_{ds} \le (V_{gs} - V_{th}) / \alpha$ (linear region)

$$I_{ds} = \beta \times (V_{gs} - V_{th} - 0.5 \times \alpha \times V_{ds}) \times V_{ds} \times (1 + \lambda \times V_{ds}) \tag{2}$$

$0 < (V_{gs} - V_{th}) / \alpha < V_{ds}$ (saturation region)

$$I_{ds} = (\beta / 2 / \alpha) \times (V_{gs} - V_{th})^2 \times (1 + \lambda \times V_{ds}) \tag{3}$$

where β is the current gain factor and $\beta = \mu_s \times C_{ox} \times W / L$, of which μ_s is the effective charge-carrier mobility, C_{ox} is the gate oxide capacitance, L is the channel length, and W is the channel width. In addition, V_{th} is the threshold voltage, λ is the channel length modulation parameter, and α is the bulk charge variation parameter.

The values of β, V_{th}, α and λ were determined through Matlab curve fitting tool. Specifically, $\beta = 0.1455$, $V_{th} = 3.808$, $\alpha = 0.2848$, and $\lambda = 0.0005946$. The comparisons of measurement data, level-1 models with and without bulk charge are shown in Fig.10. The drain voltage ranges from 0 V to 2000 V in Fig.10 (a) and from 0 V to 50 V in Fig.10 (b). Gate voltages are 10-V, 14-V, and 18-V for both V_{ds} ranges. The curve fitting error sum of squares (SSE) of level-1 model had a 92.2% reduction after adding the bulk charge parameter, which indicates that the bulk charge parameter significantly improved the fitting accuracy.

B. Modeling of Body/Integrated Schottky Diode I-V Curve

A piecewise function is used to describe the MOSFET intrinsic body diode or integrated Schottky diode forward feature when the switch is working in the third quadrant region and inversion layer is fully suppressed. The modeling formula according to [17] is shown as:

$V_{sd} \le V_{er1}$ (low-level injection region)

$$I_{sd} = I_{sl} \times [\exp(V_{sd} / V_l) - 1] \tag{4}$$

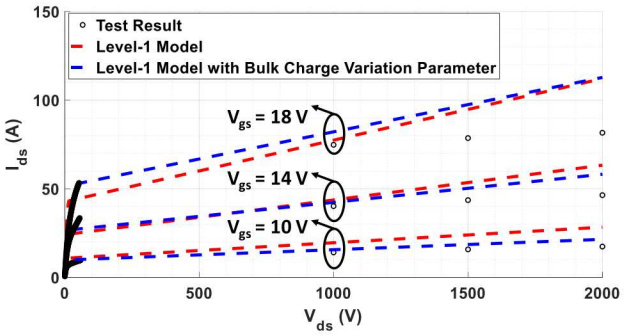
$V_{er1} < V_{sd} \le V_{er2}$ (high-level injection region)

$$I_{sd} = I_{sh} \times [\exp(V_{sd} / V_h) - 1] - I_{sd1} \tag{5}$$

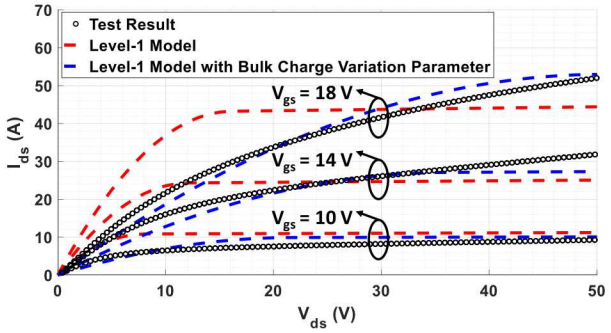
$V_{er2} < V_{sd}$ (linear region)

$$I_{sd} = V_{sd} / R_s - I_{sd2} \tag{6}$$

where V_{er1} is the threshold voltage between low-level injection region and high-level injection region; and V_{er2} is the threshold voltage between high-level injection region and linear region. I_{sl} and V_l are saturation current and emission parameter for the low-level injection region, respectively; and I_{sh} and V_h are saturation current and emission parameter for the high-level injection region, respectively. R_s is the series resistance in the linear region, and I_{sd1} and I_{sd2} are the star-up currents calibrations values for high-level injection and linear regions.



(a)



(b)

Fig.10 Comparisons of models and measurement data for first quadrant I-V curves: (a) V_{ds} from 0 V to 2000 V; and (b) V_{ds} from 0 V to 50 V.

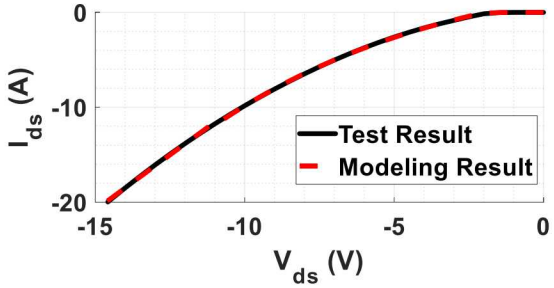


Fig.11 Comparisons of modeling results and measurement data for body/integrated Schottky diode I-V curve.

The parameter values were extracted through Matlab curve fitting tool: $V_{er1} = 2.1$, $V_{er2} = 11$, $I_{sl} = 0.000216$, $I_{sh} = 12.7$, $V_l = 0.2653$, $V_h = 8.208$, $R_s = 0.4319$, $I_{ds1} = 5.936$, and $I_{ds2} = 13.91$. Fig.11 plots the measurement data at V_g of -5 V and the modeling result curve.

C. Modeling of Drain-source Leakage Current

The drain-source leakage current was measured from 0 V drain bias to 3000 V drain bias with gate voltage at -5 V. Referring to [17], a superposition of a linear function and an exponential function were applied to fit the device drain-source leakage current, which is shown as:

$$I_{dss} = I_0 \times \exp[g_1 \times (V_{ds} - V_{br})] + g_2 \times V_{ds} \tag{7}$$

where I_0 is the coefficient of avalanche breakdown current, V_{br} is the avalanche breakdown voltage, g_1 is the coefficient of avalanche breakdown conductance, and g_2 is the leakage conductance coefficient.

Based on the parameter optimization calculation, $I_0 = 5e\text{-}8$, $V_{br} = 3500$, $g_1 = 0.005$, and $g_2 = 1.355e\text{-}13$. Then the fitting result is shown in Fig.12.

D. Modeling of Terminal Capacitances

The parasitic capacitances were measured and modeled as C_{dg} vs. V_{ds} that from 0 V to 2000 V, C_{ds} vs. V_{ds} that from 0 V to 2000 V, and C_{gs} vs. V_{gs} that from -5 V to 20 V. According to [17], [18], the modeling formula for C_{dg} can be expressed as:

C_{dg} vs. V_{ds}

$$C_{dg} = C_{oxd} \times C_{dg0} / sqrt(1 + V_{ds} / V_{td}) / (C_{oxd} + C_{dg0} / sqrt(1 + V_{ds} / V_{td})) \quad (8)$$

where C_{oxd} is the gate-drain oxide capacitance, C_{dg0} is the zero-bias capacitance of C_{dg}, and V_{td} is the drain threshold voltage. After data optimization, these values were extracted as follows: $C_{oxd} = 9.995e\text{-}8$, $C_{dg0} = 8.796e\text{-}10$, and $V_{td} = 0.0799$. For the C_{ds} model:

C_{ds} vs. V_{ds}

$$C_{ds} = C_{ds0} / (1 + V_{ds} / V_{bi})^m \quad (9)$$

where C_{ds0} is the zero-bias capacitance of C_{ds}, C_{bi} is the built-in potential, and m is the order coefficient. The following values were obtained: $C_{ds0} = 5.14e\text{-}10$, $V_{bi} = 1.34$, and $m = 0.4754$. As for C_{gs}, a pure empirical model is applied:

C_{gs} vs. V_{gs}, when $V_{gs} \leq -1.2$

$$C_{gs} = -9.951e\text{-}11 \times V_{gs} + 8.936e\text{-}10 \quad (10)$$

C_{gs} vs. V_{gs}, when $-1.2 < V_{gs} \leq 2.3$

$$C_{gs} = 9.463\text{-}10 \quad (11)$$

C_{gs} vs. V_{gs}, when $2.3 < V_{gs}$

$$C_{gs} = 2.368e\text{-}9 \quad (12)$$

Fig.13 plots the measurement data and modeling results of all three capacitances.

VI. Conclusion

The on-resistance and threshold voltage differences of 3300-V long-channel and short-channel devices are presented. The SC withstand capabilities of these two devices are also discussed. In summary, the long-channel device has larger on-resistance, higher threshold voltage but longer SCWT compared with the short-channel device. Compared with 1200-V commercial devices, the 3300-V devices from GeneSiC showed better average SCWT at 2/3 of their rated voltages and 18-V V_{gs}. The dynamic evaluation and SPICE modeling method of the short-channel device are presented as an example. The DPT results show a 1 mJ switching energy loss, with 20.2 kV/μs turn-on dV/dt and 42.7 kV/μs turn-off dV/dt, at 2400-V dc bus voltage and 6-A switching inductive current. At the end, the modeling results including first quadrant I-V curves, body diode I-V curve, drain-source leakage current, and three parasitic capacitances are presented.

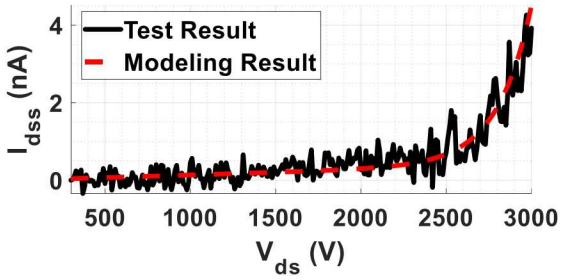


Fig.12 Comparisons of modeling results and measurement data for drain-source leakage current.

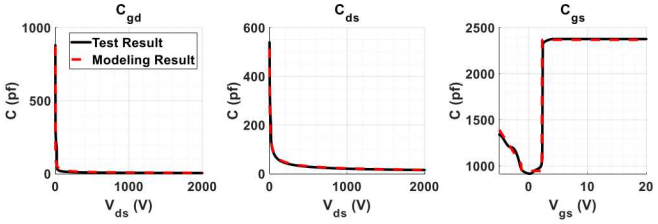


Fig.13 Comparisons of modeling results and measurement data for: (a) C_{gd}; (b) C_{ds}; and (c) C_{gs}.

Acknowledgment

The authors would like to thank GeneSiC for providing 3300-V SiC device samples.

The authors gratefully acknowledge support for this work from Dr. Imre Gyuk and the Energy Storage Program in the Office of Electricity Delivery and Energy Reliability at the U.S. Department of Energy. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia LLC, a wholly owned subsidiary of Honeywell International Inc. for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. SAND2020-XXXX C.

References

[1] J. A. Cooper and A. Agarwal, "SiC power-switching devices-the second electronics revolution?," in Proceedings of the IEEE, vol. 90, no. 6, pp. 956-968, June 2002, doi: 10.1109/JPROC.2002.1021561.

[2] S. Madhusoodhanan et al., "Comparison study of 12kV n-type SiC IGBT with 10kV SiC MOSFET and 6.5kV Si IGBT based on 3L-NPC VSC applications," 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 310-317, doi: 10.1109/ECCE.2012.6342807.

[3] L. Schrittwieser, J. W. Kolar and T. B. Soeiro, "99% Efficient three-phase buck-type SiC MOSFET PFC rectifier minimizing life cycle cost in DC data centers," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 1, pp. 47-58, 2017, doi: 10.24295/CPSSTPEA.2017.00006.

[4] B. Hu et al., "A Survey on Recent Advances of Medium Voltage Silicon Carbide Power Devices," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 2420-2427, doi: 10.1109/ECCE.2018.8558451.

[5] H. Wen, J. Gong, Y. Han and J. Lai, "Characterization and Evaluation of 3.3 kV 5 A SiC MOSFET for Solid-State Transformer Applications," 2018 Asian Conference on Energy, Power and Transportation Electrification (ACEPT), Singapore, 2018, pp. 1-5, doi: 10.1109/ACEPT.2018.8610709.

[6] D. Xing et al., "Design Strategies for Rugged SiC Power Devices," 2019 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2019, pp. 1-5, doi: 10.1109/IRPS.2019.8720557.

[7] S. Yu et al., "Bias-Induced Threshold Voltage Instability and Interface Trap Density Extraction of 4H-SiC MOSFETs," 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 2019, pp. 420-424, doi: 10.1109/WiPDA46397.2019.8998931.

[8] K. Tachiki, T. Ono, T. Kobayashi, H. Tanaka and T. Kimoto, "Estimation of Threshold Voltage in SiC Short-Channel MOSFETs," in IEEE Transactions on Electron Devices, vol. 65, no. 7, pp. 3077-3080, July 2018, doi: 10.1109/TED.2018.2837028.

[9] Yadav, M. K., Pradhan, K. P., & Sahu, P. K. (2016), "A complete analytical potential based solution for a 4H-SiC MOSFET in nanoscale," Advances in Natural Sciences: Nanoscience and Nanotechnology, 7(2), 025011. doi:10.1088/2043-6262/7/2/025011.

[10] T. A. Fjeldly and M. Shur, "Threshold voltage modeling and the subthreshold regime of operation of short-channel MOSFETs," in IEEE Transactions on Electron Devices, vol. 40, no. 1, pp. 137-145, Jan. 1993, doi: 10.1109/16.249436.

[11] A. Pérez-Tomáset al., "Field-effect mobility temperature modeling of 4H-SiC metal-oxide-semiconductor transistors," Journal of Applied Physics, vol. 100, no. 11, p. 114508, 2006.

[12] J. Sun et al., "High-Temperature Characterization of a 1.2-kV SiC MOSFET Using Dynamic Short-Circuit Measurement Technique," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 215-222, March 2020.

[13] G. Romano et al., "A Comprehensive Study of Short-Circuit Ruggedness of Silicon Carbide Power MOSFETs," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 978-987, Sept. 2016.

[14] S. Sundaresan, V. Mulpuri, S. Jeliazkov and R. Singh, "Avalanche and Short-Circuit Robustness of 4600 V SiC DMOSFETs," 2019 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2019, pp. 1-7.

[15] Arora, N. (2007), "Mosfet modeling for VLSI simulation: Theory and practice," New Jersey: World Scientific.

[16] P. Twesha, (2014) "Comparison of Level 1, 2 and 3 MOSFET's" 10.13140/RG.2.1.1616.3442.

[17] X. Fang. *Characterization and Modeling of SiC Power MOSFETs THESIS*. [Online]. Available: https://etd.ohiolink.edu/pg_10?0::NO:10:P10_ACCESSION_NUM:osu1354687371

[18] N. Phankong, T. Yanagi and T. Hikihara, "Evaluation of inherent elements in a SiC power MOSFET by its equivalent circuit," Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, 2011, pp. 1-8.