Cascaded logic using clocked domain wall devices

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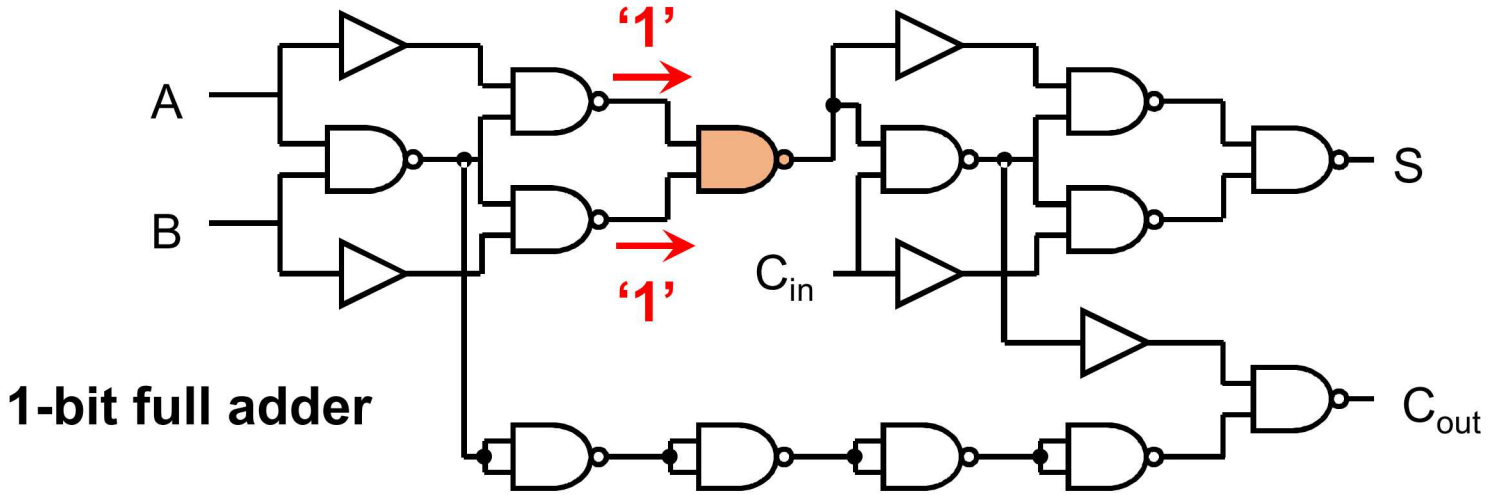
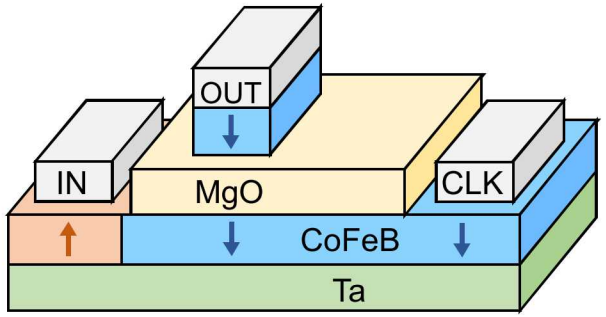


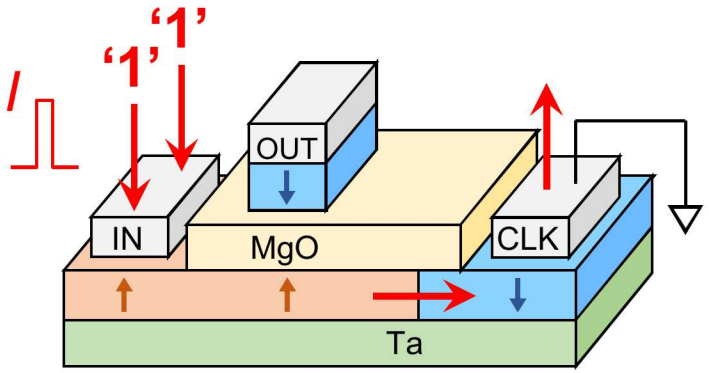
1-bit full adder

Clock phase 1:
standby
State: '1' (P)



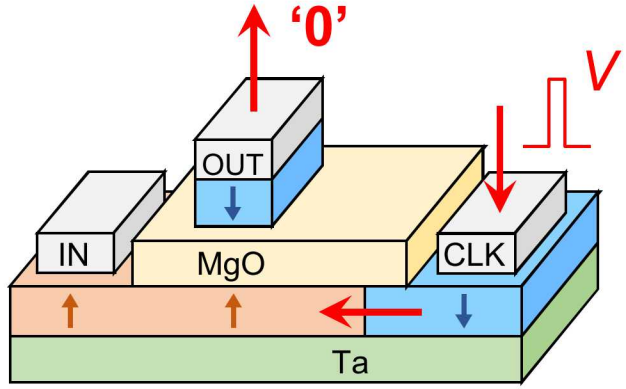
DW NAND gate

Clock phase 2:
receive input & compute
State: '1' (P) → '0' (AP)



DW NAND gate

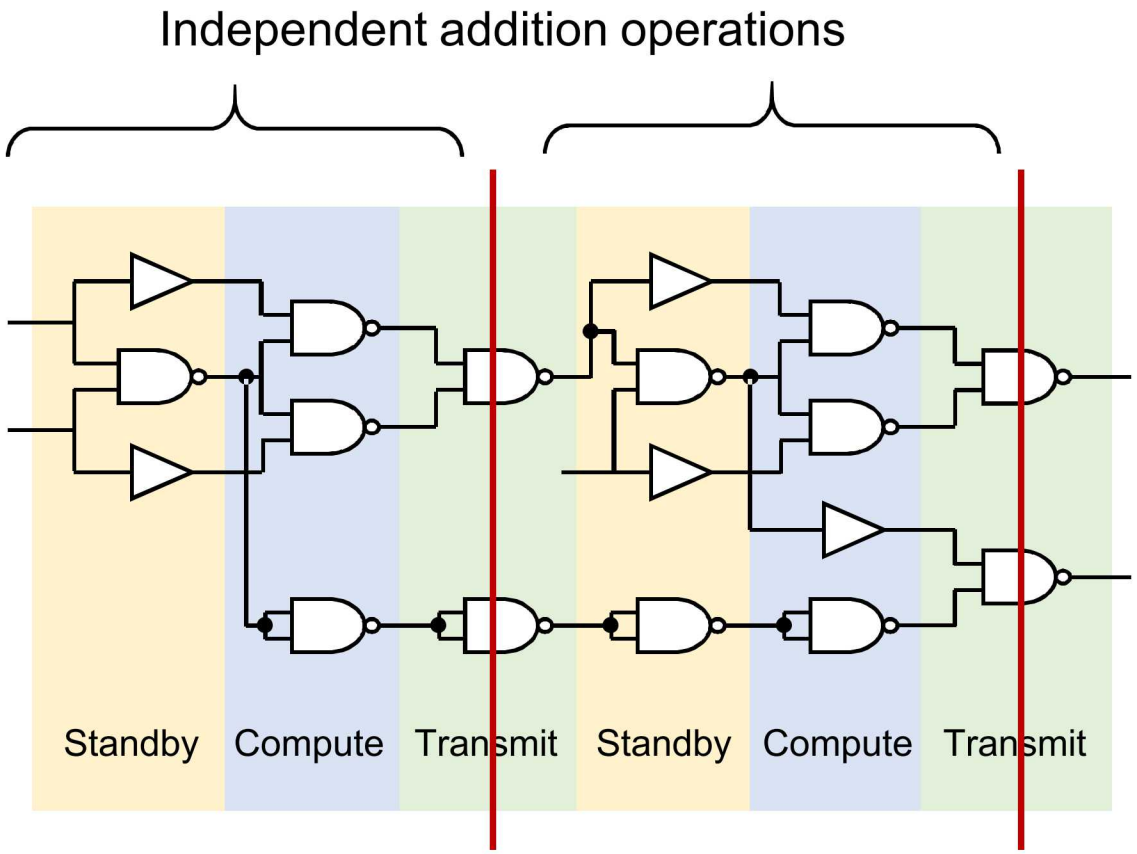
Clock phase 3:
transmit & reset
State: '0' (AP) → '1' (P)



DW NAND gate

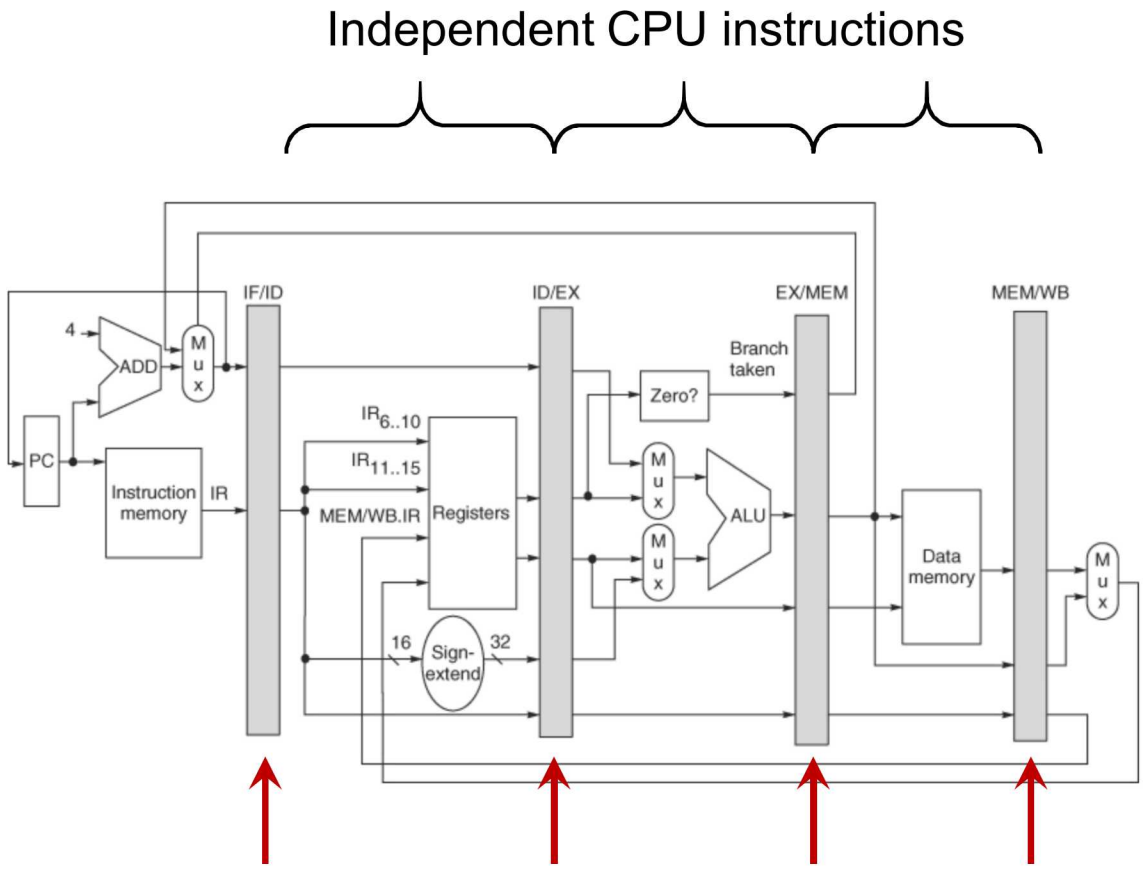
Domain wall devices serve double duty as processing elements and non-volatile data buffers

Micro-pipelined domain wall logic



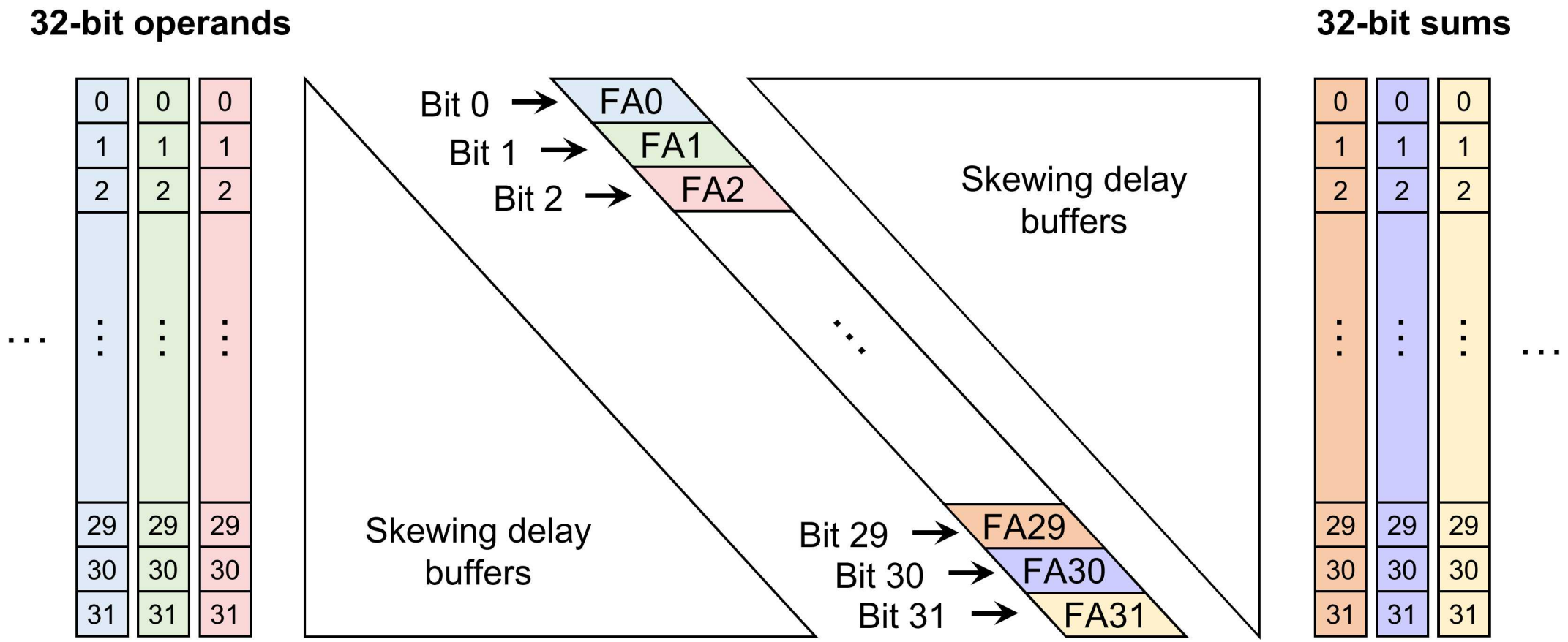
Domain wall data buffering
(consumes no static power)

Pipelined CMOS processor



MIPS architecture, from Hennessy & Patterson, *Computer Architecture*, 2011

Bit-level micro-pipelining enables high-throughput arithmetic operations

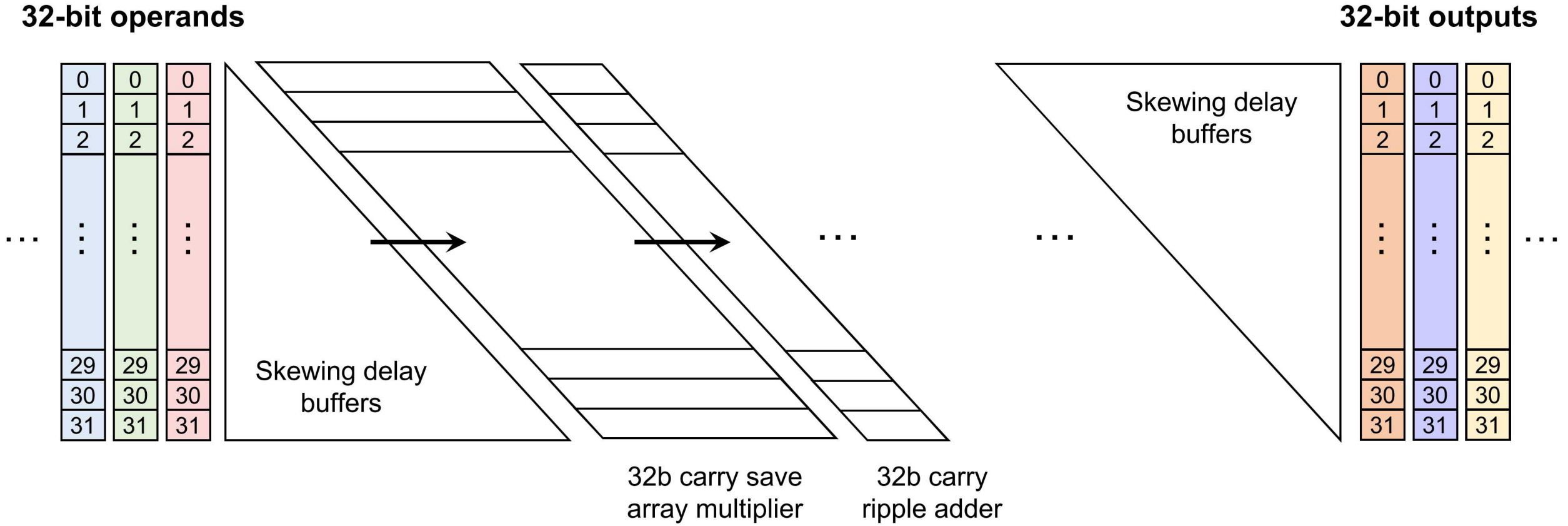


32-bit ripple carry adder

Delay per add: 32 cycles (1 clock cycle = 1 gate delay)

Throughput: 1 sum / gate delay

Bit-level micro-pipelining enables high-throughput systolic processing



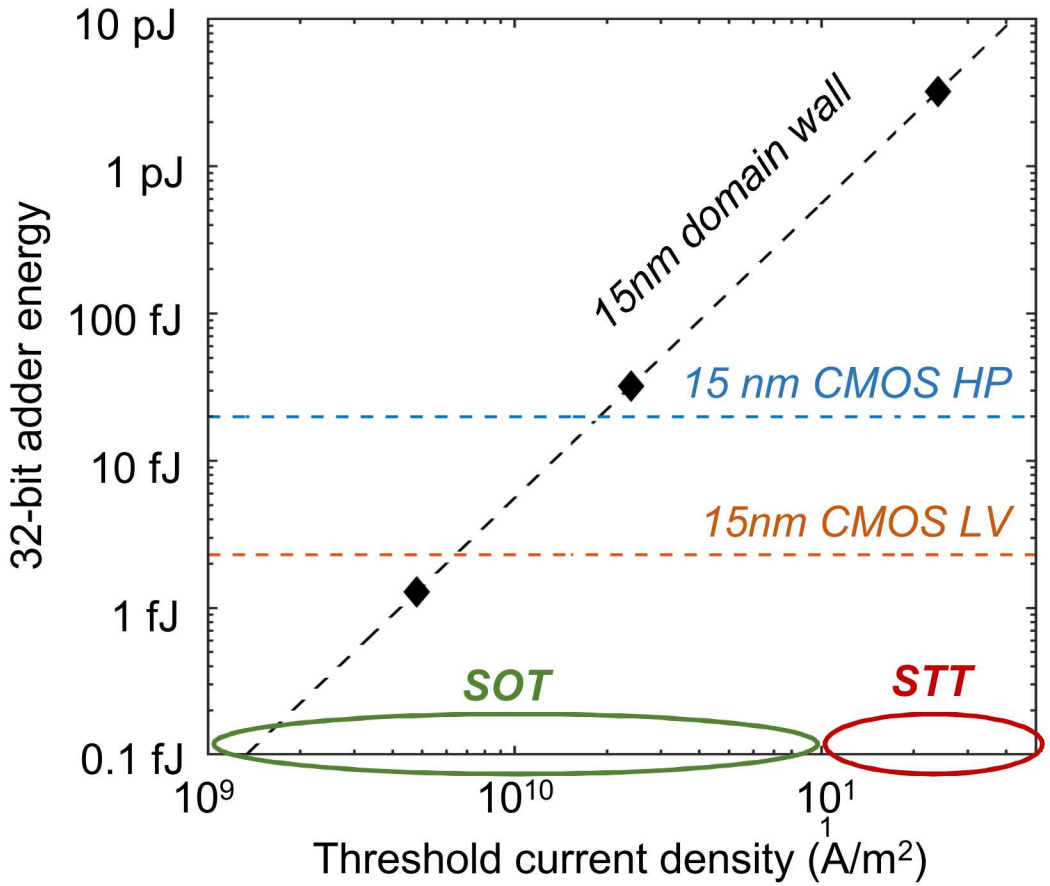
Chain of arithmetic operations (e.g. matrix multiplication)

Delay per operation: *X* cycles (1 clock cycle = 1 gate delay)

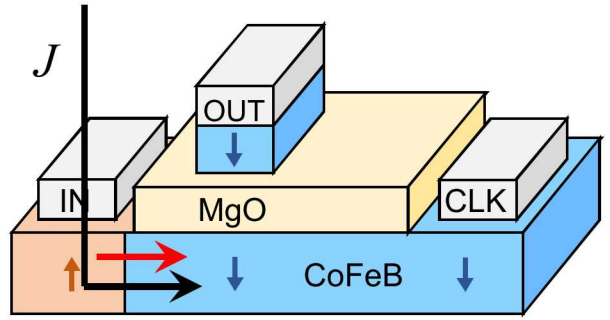
Throughput: 1 output / gate delay

Domain wall logic energy consumption below scaled CMOS

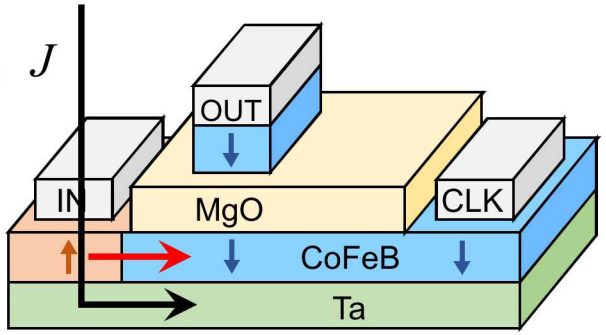
Domain wall circuit simulation using
micromagnetics-validated SPICE compact models:



Spin transfer torque (STT)



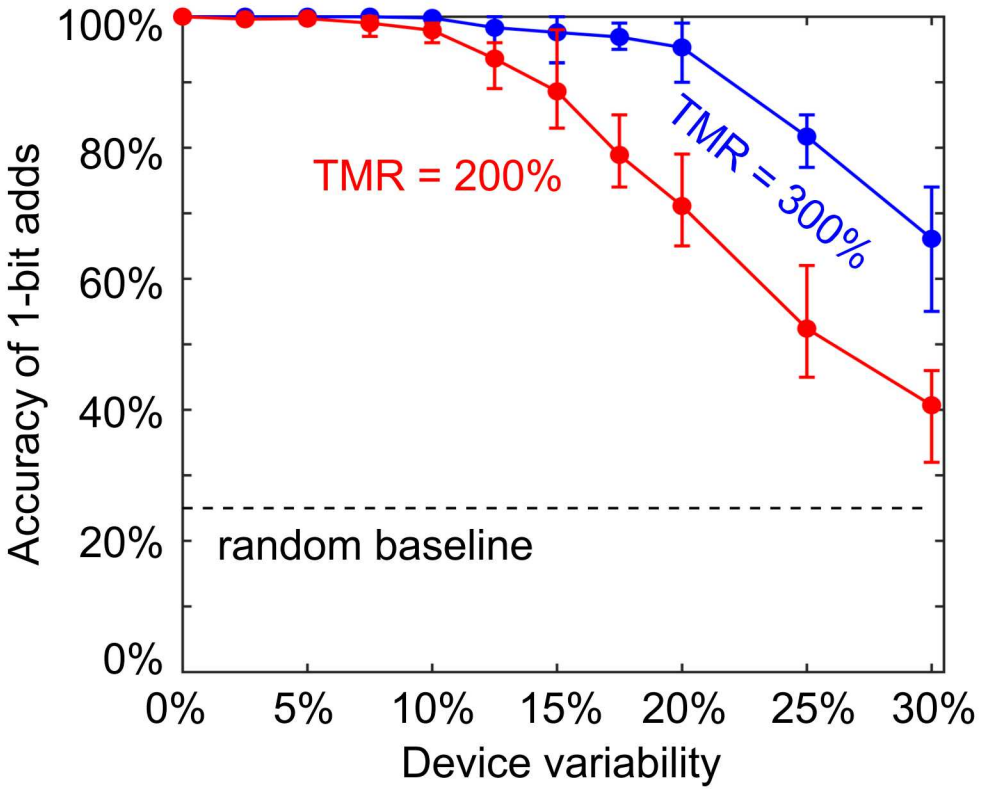
Spin orbit torque (SOT)

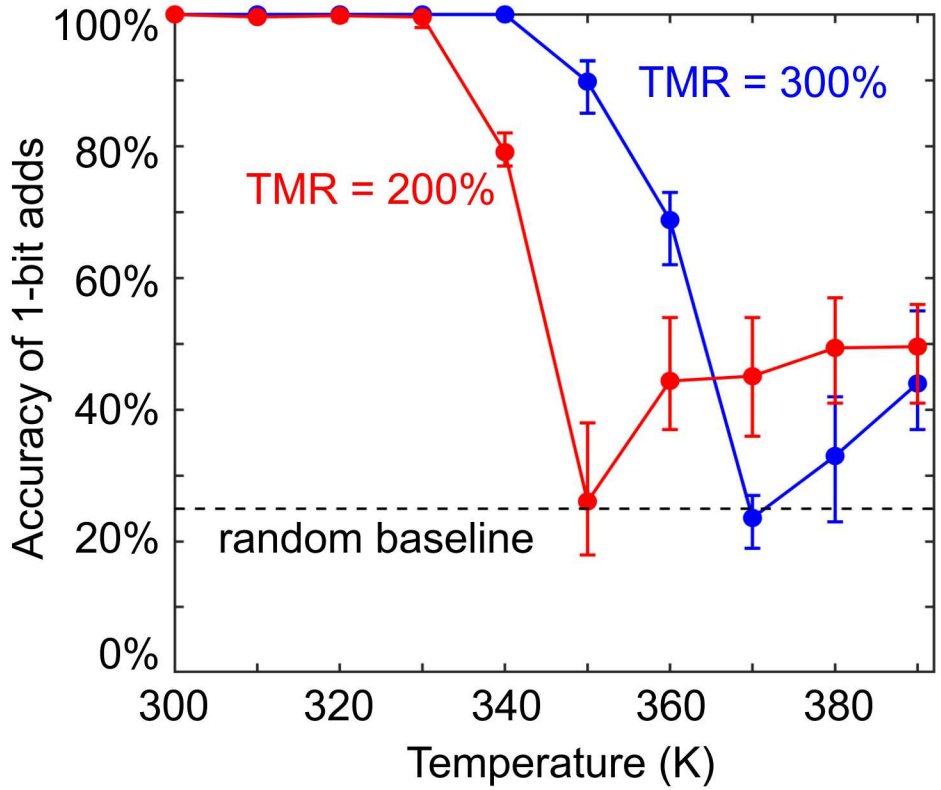


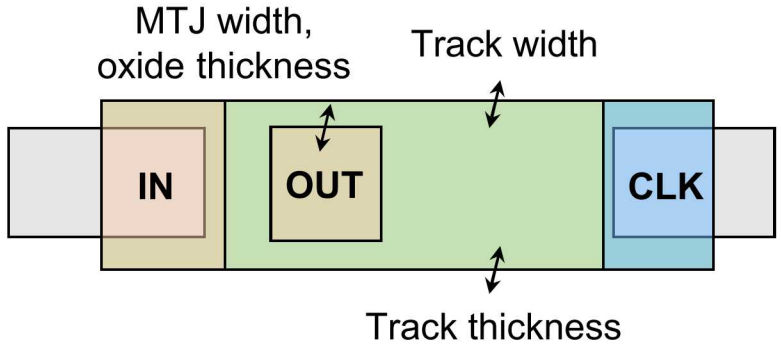
CMOS: D. Nikonov, I. Young, IEEE JXCDC 2015

Compact device model: X. Hu et al, IEEE Trans Elec Dev 2019
Circuit benchmarking: T. Xiao et al, IEEE JXCDC 2019

Robust to process variations and high temperature







Higher TMR → Higher current On/Off ratio
→ Higher robustness to noise/variations