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FPGA Reliability Test Design Using Parametric Degradation Analysis

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Introduction

Reliability Testing

Definition of reliability: "The probability that a system, vehicle, machine, device, and so on will perform its intended function under operating condition, for a specified period of time."[1]

Standard reliability testing approach:

- Pass/Fail – either a device has failed or it has not.
- Uses binomial statistics
- Easy but requires large sample sizes

Parametric degradation analysis approach:

- Observe a parameter which degrades towards some critical level, at which point the device will fail. (stops performing within device specifications)
- Provides model insight into the health of the device
- Requires smaller test sample size because more data is generated per unit

Field Programmable Gate Arrays (FPGAs)

FPGAs are integrated circuit semiconductor devices "based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects"[2], with a key advantage over similar devices being that they can be reprogrammed after manufacturing.

- Can be customized for specific design tasks allowing them to fill a wide variety of needs in many industries
- Ideal for prototyping and debugging
- Ideal for reliability testing:
  - Lots of I/O for getting info out of device
  - Well-understood failure modes (based on MOSFET transistors)

The Problem

As microelectronics continue to shrink in size, failure analysis, debugging, and other evaluations are increasingly difficult to perform meaning more precise methods are needed to get information out of the devices. One proposed solution is to thin the device silicon substrate so that tools and instruments could then get localized information out of the device at the submicron level.

We are trying to answer two main questions:

1. How does thinning of the silicon substrate impact device performance?
2. How does thinning of the silicon substrate affect the device lifetime and degradation rate?

Planned Approach

Thin the silicon substrate to various thicknesses and compare parameter degradation to that of full thickness devices before and after after accelerated stress conditions (temperature, voltage, frequency, etc.).

Use the comparison data to understand the differences in performance and lifetime (based on degradation) resulting from thinning the substrate. We'll focus on functional circuit timing delay degradation using Ring Oscillators and Static Random Access Memory functional bit failure rate monitors as critical degradation parameters.

Some of the challenges:

- Accounting for the stochastic device-to-device manufacturing variance
- Small sample size
- Several failure modes to account for

Goal and Hopeful Results

Goal:

To be able to say with some amount of confidence (>50%) that there is or isn't a difference between device degradation rates caused by substrate thinning.

Intended uses of results:

- Inform future work in FPGA microelectronic failure analysis, debugging, etc.
- Provide greater understanding about limitations of FPGAs with regards to substrate thinning
- Apply results to other microelectronics because building blocks of FPGAs are common to many other logic devices

Next Steps

- Increase confidence in results (hopefully to ≈90%)
- Quantify difference between unmodified and modified devices at different levels of substrate thinning
- Quantify degradation acceleration factors

References

1. Meeker, William Q., Jr., et al. Statistical Methods for Reliability Data, John Wiley & Sons, Incorporated, 1998. ProQuest Ebook Central, https://ebookcentral.proquest.com/lib/sandia/detail.action?docID=588896.
2. https://www.xilinx.com/products/silicon-devices/fpga/what-is-an-fpga.html

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