

POSITION PAPER FOR THE CCC WORKSHOP ON
PHYSICS & ENGINEERING ISSUES IN ADIABATIC/REVERSIBLE CLASSICAL COMPUTING

Priority Research Challenges in the Physics and Engineering of Classical Reversible Computing Systems

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In this position paper, we briefly outline a number of major outstanding research challenges in relation to the development of practical computing systems that utilize logically and physically reversible computing techniques to achieve improved energy efficiency on general purpose digital application. These challenges span all levels of the computing stack, from fundamental physics up through systems engineering and application algorithms, although the lower levels have a more immediate importance at this time.

1 Fundamental Physics Challenges

Although the validity of Landauer's Principle (which provides the motivation for reversible computing) follows almost trivially from basic statistical physics and information theory [1], more work needs to be done to apply recent developments in non-equilibrium quantum thermodynamics and quantum information to the fundamental physics of mechanisms for carrying out classical reversible operations. In particular, we can ask questions such as the following:

- (1) Do there exist (and can we formulate) fundamental (technology-independent) lower bounds on important quantities such as the entropy generation (energy dissipation) required to carry out generalized logically reversible operations, as a function of generic physical parameters such as the time allowed to perform the operation, the local temperature, the size of the device, etc.?
- (2) Do there exist exotic quantum mechanical phenomena (e.g., decoherence-free subspaces, topological invariants, generalized quantum Zeno effects, etc.) that can potentially be utilized in realistically buildable physical mechanisms for carrying out reversible computation to allow those mechanisms to more closely approach the fundamental limits from (1), whatever those are?

Answering the above questions may lead to the discovery of entire new *classes* of physical implementation technologies for reversible computing, with improved scaling characteristics which may allow them to vastly outperform existing technologies in the long run.

Answering the above questions in a sufficiently general way may also yield important insights into the thermodynamic limits of engineering implementations of *quantum* computing technologies as well [2].

2 Challenges in Device- and Circuit-Level Technologies

2.1 Challenges for Asynchronous Ballistic Reversible Computing (ABRC)

One novel category of implementation approaches to reversible computing are the *asynchronous ballistic* reversible technologies [3][4]; these could potentially offer improved scaling of dissipation-delay characteristics compared to more conventional adiabatic technologies. However, these techniques are relatively new, so, many open questions remain about them, including:

- (1) In available implementation technologies, such as fluxon-based superconducting circuits [4], what is a simple set of primitives that suffices for universal computation, using economical constructions?
- (2) What are the limits on energy efficiency of physical implementations of those primitives? Is it possible for the energy efficiency of implementations to scale better than in the case of adiabatic technologies?

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2.2 Challenges for Adiabatic approaches to Reversible Computing

Classic adiabatic approaches to reversible computing (including both semiconducting and superconducting approaches) are relatively well-developed, in comparison with other approaches discussed above. However, important questions remain in this area, including:

- (1) How can we design high-Q resonant energy-recovering clock-power supplies and clock distribution networks that can recover *arbitrarily large* fractions of the energy delivered to an adiabatic circuit? Are there limits on the degree of energy recovery that is ultimately achievable?
- (2) Are there fundamental limits to the energy savings that is achievable through cryogenic operation, in both semiconducting and superconducting implementations of reversible adiabatic circuits?
- (3) How can semiconducting devices be optimized for maximum energy efficiency when operated adiabatically at cryogenic temperatures? Are there limits to the energy savings achievable using this approach?

3 Challenges for Reversible Processing Architectures

For the adiabatic and (even more so) the ballistic case, much more work is still needed to develop efficient and effective hardware architectures for both general-purpose (programmable) and more special-purpose digital computation. This includes work at a number of different levels:

3.1 Hardware Description Languages (HDLs) and Design Tools for Reversible Computing

There is a great need for descriptive and effective Hardware Description Languages (HDLs) that can appropriately handle both the adiabatic and asynchronous forms of reversible circuits, and accompanying tools for both synthesis and analysis of detailed designs.

3.2 Effective Designs of Reversible Functional Units (FUs)

Obviously, efficient designs are needed for all manner of functional units, both for general-purpose processor microarchitectures, and more special-purpose IP blocks. Designs will vary in their degree of reversibility, and in the assumed performance characteristics of the underlying hardware.

3.3 Reversible Processor Architectures and Programming Languages

As reversible hardware approaches ever-higher degrees of reversibility, there will be an increasing need for reversibility at the programmer-visible level in processor design, and for reversible programming languages.

3.4 Systems Engineering for Reversible Machines

A great deal of work will be needed at the level of computer systems engineering to appropriately balance tradeoffs in the degree of reversibility, energy efficiency, cost, speed, and compactness of system designs.

3.5 Reversible Application Algorithms

In the far future, when very high degrees of reversibility are attained at the hardware level, crafting good reversible parallel algorithms for a variety of important application problems will become more important. There is relatively little work on reversible algorithms so far [5][6].

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References

- [1] Frank, M. P., "Physical Foundations of Landauer's Principle," in J. Kari, I. Ulidowski, eds., *Reversible Computation. RC 2018*, Lecture Notes in Computer Science (LNCS), vol. 11106, Springer, Cham, pp. 3–33, 2018. [doi:10.1007/978-3-319-99498-7_1](https://doi.org/10.1007/978-3-319-99498-7_1) (see also [arXiv:1901.10327](https://arxiv.org/abs/1901.10327))
- [2] Shukla, K. and M. P. Frank, "Pathfinding Thermodynamically Reversible Quantum Computation," presentation, NSF QLCI Workshop on the Identification and Control of Fundamental Properties of Quantum Systems, Jan. 2020.
- [3] Frank, M. P., "Asynchronous ballistic reversible computing," in *2017 IEEE International Conference on Rebooting Computing (ICRC)*, Washington, DC, 2017, pp. 1-8, [doi:10.1109/ICRC.2017.8123659](https://doi.org/10.1109/ICRC.2017.8123659).
- [4] Frank, M. P., R. M. Lewis, N. A. Missert, M. A. Wolak, and M. D. Henry, "Asynchronous ballistic reversible fluxon logic," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 5, pp. 1–7, 2019. [doi:10.1109/TASC.2019.2904962](https://doi.org/10.1109/TASC.2019.2904962)
- [5] Frank, M. P., *Reversibility for Efficient Computing*, Ph.D. thesis, MIT, June 1999. <https://dspace.mit.edu/handle/1721.1/9464>
- [6] Demaine, E. D., J. Lynch, G. J. Mirano, N. Tyagi, "Energy-Efficient Algorithms," in *ITCS '16: Proceedings of the 2016 ACM Conference on Innovations in Theoretical Computer Science*, pp. 321–332, Jan. 2016. [doi:10.1145/2840728.2840756](https://doi.org/10.1145/2840728.2840756)