

Exceptional service in the national interest

Update: FPGA Trust/Assurance Study

USG/DIB FPGA Assurance Community of Interest Meeting

Mike Johnson, Sr Scientist/Engineer
Sandia National Laboratories

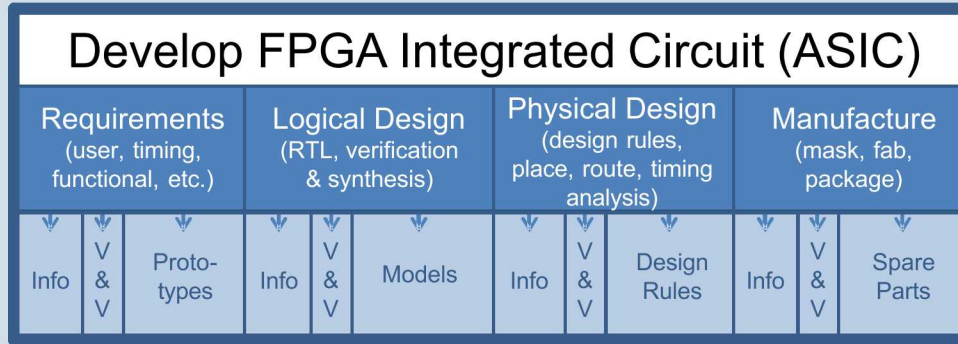
BACKGROUND

- 2014 “Trust in FPGAs” Study – what was it?
 - In-depth review of the design, development, provisioning, and system considerations of FPGAs and the tools, information, and processes supporting this
 - Focused on US-based FPGA vendors, design tool developers, and end-users/system integrators of FPGA-based systems for the DoD and IC
 - Assessed relative risk across the FPGA lifecycle based upon postulated attacks weighed against their difficulty to conduct and consequence if successful
 - Highlighted areas where USG investment could address highest risk elements of the lifecycle – some of which are being worked today

FPGA Assurance: Lifecycle Considerations

FPGA Vendor

Acquire
Materials
Tools
Hard IP

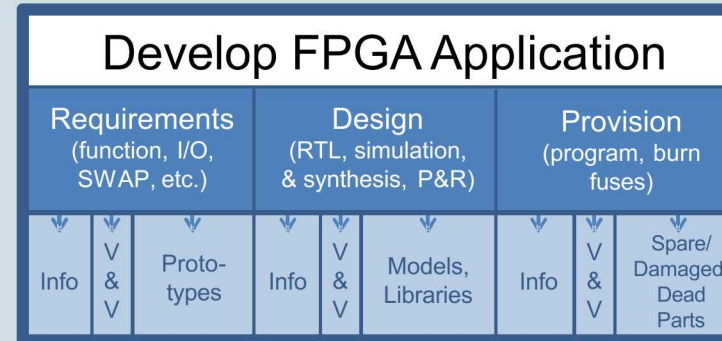
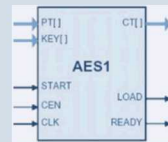
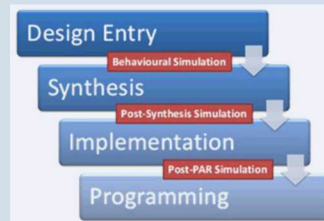


unprogrammed
devices



System Developer

Acquire
FPGAs
Tools
Soft IP



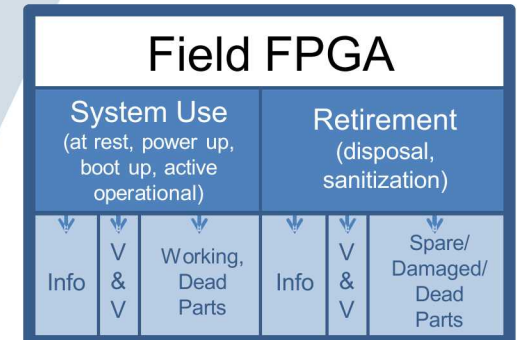
bitstream

Deploy
System

upgrade/
re-purpose



Field FPGA



Why Update the 2014 Study?

- Review and document relevant technical improvements and trust & assurance developments in the FPGA market since 2014
 - Updates from the 4 major US-based FPGA Vendors: Xilinx, Intel, Microchip and Lattice
 - Updates pertinent to FPGA EDA tools, IP, and end-user application development
- Help develop FPGA Assurance resources more readily available to leadership, stakeholders, program managers, and engineers
 - Up-to-date technical information
 - Practical best practices and guidance
 - Assurance and verification approaches
 - Investment, partnership, and research opportunities

What's New Since 2014?



Industry Shifts

- Altera → **Intel PSG**; Actel → Microsemi → **Microchip**
- **Lattice** → ~~Canyon~~ **Bridge**
- Trusted Foundry: IBM → **GF US2**; access to SOTA?

▪ eFPGA

Tech Advancements

- 14nm/16nm → 7nm; novel NV memory technologies
- Complex SoC-FPGA architectures → becoming the “norm” versus “traditional” FPGA
- 2.5D/3D and Heterogenous Integration solutions
 - Research into new methodologies / approaches / tools (game theory)

▪ Bitstream authentication, PUFs, secure boot (SoCs), SCA mitigation, etc.

USG Initiatives

- NDIA Electronics Division: FPGA Sub-Committee; Device Mfr Working Group

▪ JFAC, T&AM, MINSEC

- 5200.44 Update; Section 224 of 2020 NDAA

▪ AF, Navy FPGA programs

▪ FPGA Assurance Strategy



2020 FPGA Study Update: What's Happening?

- Primary motivation is to update the 2014 study with assurance-related technical and market developments since the original study concluded
 - the intention is not to revisit each 2014 topic from scratch
 - assurance considerations pertaining to development and usage of system-on-chip devices will be of special interest – emergent area since 2014 study concluded
- Developing updated Requests for Information (RFIs)
 - RFI Focus Areas: FPGA Vendors, IP Vendors, EDA Tool Vendors (FPGA design + verification), End-user developers
- Assembling a USG Advisory Panel
 - DoD and IC SMEs and Stakeholders to review RFI material and study team results
- Results are intended to consider and complement other ongoing USG FPGA efforts as appropriate
 - Title III FPGA effort, DoD FPGA Assurance Strategy, Rad Hard FPGAs, eFPGA initiatives, other...
- Small Sandia team working preparatory tasks → expect kickoff in August 2020
 - As work progresses and sponsor requests, updates provided to USG groups and to this community

QUESTIONS?