

Co-Optimization of Boost Converter Reliability and Volumetric Power Density Using Genetic Algorithm

Lee Gill, Jason C. Neely, Lee J. Rashkin, Jack D. Flicker, Robert J. Kaplar

Sandia National Laboratories

Albuquerque, NM 87185

lgill@sandia.gov

Abstract—In power electronic applications, reliability and power density are a few of many important performance metrics that require continual improvement in order to meet the demand of today's complex electrical systems. However, due to the complexity of the synergy between various components, it is challenging to visualize and evaluate the effects of choosing one component over another and what certain designs impose on the overall reliability and lifetime of the system. Furthermore, many areas of electronics have realized remarkable innovation in the integration of new materials of passive and active components; wide-bandgap semiconductor devices and new magnetic materials allow higher operating temperature, blocking voltage stress, and high switching frequency, all of which would allow much more compact power converter designs. However, uncertainty remains in the overall electronics reliability in different design variations. Hence, in order to better understand the relationship of reliability and power density in a power electronic system, this paper utilizes genetic algorithm (GA) to provide pareto optimal solution sets in a multi-variant trade space that relates the Mean Time Between Failures (MTBF) and volumetric power density for the design of a 5 kW synchronous boost converter. Different designs of the synchronous boost converter based on the variation of the electrical parameters and material types for the passive (input and output capacitors, the boost inductor, and the heatsink) and active components (switches) have been studied. A few candidate designs have been evaluated and verified through hardware experiments.

Keywords—genetic algorithm, optimization, boost converter, reliability, failure rate, MTBF, power density

I. INTRODUCTION

The performance requirements of power electronic products are increasingly becoming more stringent, driven by higher demand of power, requiring certain form-factors, and diverse load profiles. Moreover, many end users of the power conversion systems are demanding much higher performance improvement in the areas regarding cost, efficiency, power density, reliability, and manufacturability [1]-[2]. A need for greater improvement in these performance factors, especially the reliability factor is amplified in certain industries, such as automotive, aerospace, and railway traction as more electronic parts are required to realize the future trends of the transportation electrification while ensuring safety, life-cycle cost, and lifetime in these applications [3].

Optimization techniques addressing cost, efficiency, power density, and manufacturability performance factors have been exploited in [4]-[6]. However, ensuring and increasing reliability are faced with stark challenges when one or more of

these performance factors are to be co-optimized, especially with increasing complexity of the future electronic systems. Such efforts to fulfil future reliability requirements, multidisciplinary collaboration with expertise in material sciences, semiconductor devices, power electronics, system engineering and reliability engineering are paramount in not only bridging the gap of evaluating the five performance metrics altogether, but also in increasing the adoption of compact and reliable electronics integration in many industrial sectors, such as renewable energy, electric vehicles, and more electric aircrafts.

Mean-Time-to-Failure (MTTF) and Mean-Time-Between-Failures (MTBF) are the two classical metrics to evaluate or estimate the expected lifetime of non-repairable items or repairable items, respectively. MTBF is related to reliability, which is defined as the probability of an individual unit of interest, operating with full functionality for a specific length of time, t , under specific tests or stress conditions. The standards for the reliability of electronic systems are presented in [7]-[9].

The statistical model of reliability can be expressed in (1) where λ is the intrinsic failure rate of a component and the inverse of the failure rate, $1/\lambda$ specifies the MTBF. The reliability of a system composed of n components is equal to the sum of all the reliabilities of the individual component's failure rate as expressed in (2).

$$R(t) = e^{-\lambda t} \quad (1)$$

$$\lambda = \sum_{i=1}^n \lambda_i \quad (2)$$

For a given system, there are multiple failure mechanisms at the component level, packaging level, and printed circuit board (PCB) level. In power electronic systems, various failure mechanisms need be identified in order to determine the robustness and the life cycle of the application. This requires identifying a number of models that are associated with the system as well as appropriate parameters critical to dictating MTBF.

In addition, recent emerging technology in magnetic materials and semiconductor devices, such as wide bandgap based devices has introduced opportunities contributing to the development of power conversion products with higher efficiency and power density compared to the traditional designs [10]. However, scientific understanding of interaction between different components, especially uncertainties with the use of novel materials, causing different dynamics in thermal and

electrical stress on a system, is continuing to evolve. This is because of highly dependent parameters between components impacting one or more performance factors, including reliability.

With the direct results of the opportunities exploited in both passive and active components, there have been active research efforts in the optimization of one or more performance factors in many applications, such as efficiency, power density, and cost of PV converter systems [11], power density and efficiency for DC-DC converters for telecom applications [12], and multicell power supply for data centers [13]. To enhance the understanding of failure mechanisms of power electronic components as a whole and ultimately to further advance the electrification of transportation, multi-objective optimization trade-off design studies among reliability, expected service time, and cost relating power density of power electronic systems must be realized.

All in all, this research effort seeks to provide insight in minimizing MTBF while maximizing volumetric power density of a 5 kW synchronous boost converter. Due to the characteristics of a multi-variant trade space, an evolutionary algorithm is implemented to obtain a set of optimal solutions based on the reliability of the boost inductor, transistors, capacitors, and heatsinks. Section II provides an explanation of the multi-objective optimization scheme using the genetic algorithm (GA) with the evaluation models for the boost inductor, capacitor, transistors, and heatsink. Section III presents the optimal boundary space, the pareto frontier, that realizes optimum MTBF and volumetric power density of the boost converter based on different types of component materials and types. Several candidate designs have been selected and hardware experimental results are presented in Section IV. Section V concludes the paper with a summary of findings and analysis of the multi-objective optimization.

II. MULTI-OBJECTIVE OPTIMIZATION

A. Genetic Optimization Algorithm

The genetic algorithm is a probabilistic method for optimizing multi-input systems. The approach is based on the principles of natural selection, but applied to a user defined fitness function [14]. A GA begins with an initial population of individuals spread over the design space where each parameter of interest represents a gene on a chromosome. These genes may represent a key dimension, a capacitance value, a switching frequency, or other design parameters. In each generation, new individuals are created by algorithms that mimic mating and gene crossover. The fitness of each individual in the new population is then determined by some user defined function and the individuals with the best fitness are selected for the next generation. By repeating this process over several generations, optimal solutions can be found. Additionally, the algorithm can be adapted to multi-objective fitness functions to find a pareto frontier.

For the multi-objective optimization in this work, the analysis was done using the Genetic Optimization System Engineering Tool (GOSET) developed by Purdue University [15]. This MATLAB® based software package consists of several scripts for implementing the genetic algorithm

optimization problem and producing candidate solution sets. The GA starts by initializing the genes used in the optimization, which herein are the switching frequency (f_{sw}), input voltage (V_{in}), output voltage (V_o), boost inductor current ripple factor (k_L), input and output voltage ripple factor (k_C), maximum allowable semiconductor junction temperature rise (T_j), and target efficiency (η). Then it is followed by a sequential succession of fitness evaluation, selection, crossover, mutation steps.

B. Co-Optimization of Synchronous Boost Converter

For the purposes of evaluating GOSET to realize multi-objective optimization for potential applications, such as EVs and more electric aircrafts that weight heavily on both reliability and power density of power converters, a 5 kW synchronous boost converter, shown in Fig.1, is selected as the converter of interest. The passive and active elements highlighted in Fig.1 are the main components that make up the majority of the volume of the converter, and hence, the genetic optimization tool takes in the parameters listed in Table 1 as the genes for the computation. The variables in Table I are important factors that influence both the volume and the reliability of the boost converter, depending on the combination of the parameter values.

Another objective of the multi-objective optimization studies is to draw relationships between different material types of the elements of the boost converter. For example, the pareto optimization between different magnetic core material types, which in this study iron powder cores from Magnetics Inc.[16], such as High Flux, MPP, and Kool μ have been chosen for the comparison. For the switching transistor comparison,

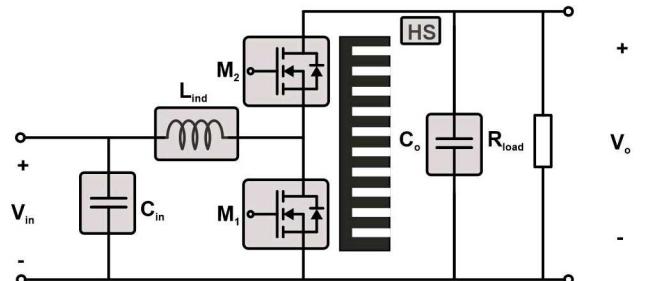


Fig.1 Schematic of the synchronous boost converter with the passive and active elements to be optimized highlighted.

TABLE I. GENE DATA TYPE AND DESCRIPTION TO GOSET

Gene	Description	Data Range /Min...Max/	Data Sweep Type
V_{in}	Input Voltage	[200 V...400 V]	Logarithmic
V_o	Output Voltage	[500 V...1000 V]	Logarithmic
f_{sw}	Switching Frequency	[10 kHz...1MHz]	Logarithmic
k_L	Inductor Current Ripple Factor	[5%...200%] ^a	Linear
k_C	Input/Output Voltage Ripple Factor	[5%...10%] ^a	Linear
η	Target Efficiency	[95%...100%]	Linear

^a Peak-to-peak value

semiconductor devices based on silicon (Si) and silicon carbide (SiC) materials (e.g. IGBTs vs. SiC MOSFETs) are evaluated for the optimal designs of the boost converter. For the input and output capacitors, multilayer ceramic chip (MLCC) capacitors and film capacitors are investigated. Lastly, natural cooling, forced air cooling, and liquid cooling are studied for the juxtaposition of MTBF and volumetric power density relationship.

Fig.2 shows the simplified flowchart of the multi-objective optimization scheme that maps each potential design combination into a trade-space that eventually morphs into a pareto frontier with competing objectives between MTBF and power density. Note that the flowchart is indeed the fitness evaluation function of the GA. In the fitness evaluation step, the cost function that determines the selection or the design of each component assigns the combination of a solution set with appropriate fitness value. The following briefly describes and explains the component selection procedures that pass on the proper values to the pareto analysis function.

1) Initialization Function

In the initialization step, chromosomes are generated with randomly selected individuals based on the user input of gene types and data ranges. In this step, varying degrees of comparison studies can be considered based on the selection of specific passive and active elements under scrutiny.

2) Magnetic Selection Function

The magnetic selection function compares many possible boost inductor designs that satisfy the operating conditions and electrical requirements of the synchronous boost converter. There are two main constituents of a boost inductor: the core and the windings. Fig. 3 illustrates the magnetic selection function in a more detailed manner. The wire gauge size (AWG) is selected based on the operating frequency of the converter. The wire sizes have been selected with greater than 100% skin depth to prevent the effect of skin effect on the conductors. The smallest possible number of conductors required for the inductor current while allowing the conductor temperature to rise to 70 °C is calculated using the Neher-McGrath theory [17]-[18]. The AWG sizing and the wire bundle information based on the ampacity calculation is passed along to the core selection function. To limit the scope of the input parameters, the maximum conductor temperature is set to 70 °C while the ambient to 20 °C. The material selection for the conductors is limited to the properties of copper material, though similar approach can be taken for different material types, like aluminum.

The core design selection function considers every possible core size manufactured by Magnetics Inc., but the selection is limited to iron powder cores (High Flux, MPP, and Kool M μ) and toroidal shape to restrict the scope as well as to reduce the computation time of the optimization. The manufacturer's core data, including the cores' physical and magnetic characteristics are imported to the GA core design selection function. Moreover, stacked core designs with combining the same cores up to five times have increased the number of potential candidate designs by a factor of five. This is to provide realistic design scenarios practiced by many designers.

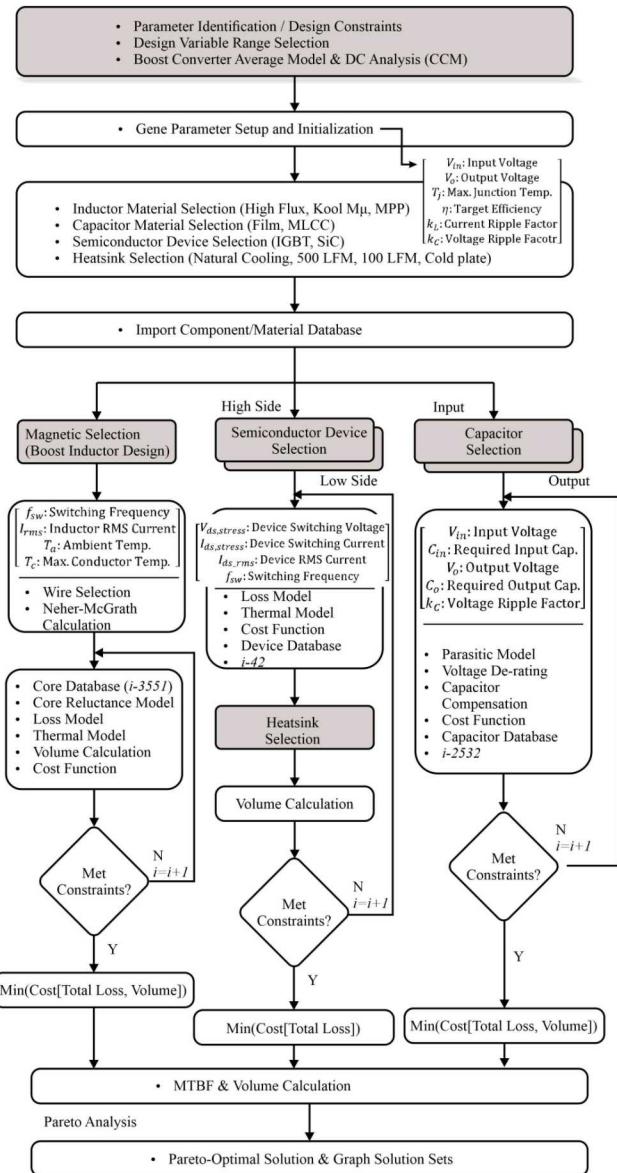


Fig.2 Simplified flowchart of the multi-objective optimization procedure to generate pareto optimal solution sets comparing a variety of material type of passive and active components.

To determine and to eliminate cores that are not large enough to meet the energy storage requirement of the boost converter, the area product principle referenced in [19] is used to calculate the core's energy handling capability, which is expressed in (3).

$$A_p = \frac{LI^2(10^4)}{B_m \times J \times K_u} \quad (3)$$

where

B_m is the flux density in teslas

J is the current density in amps-per-cm²

K_u is the window utilization factor

L is the inductor

I is the peak current through the inductor

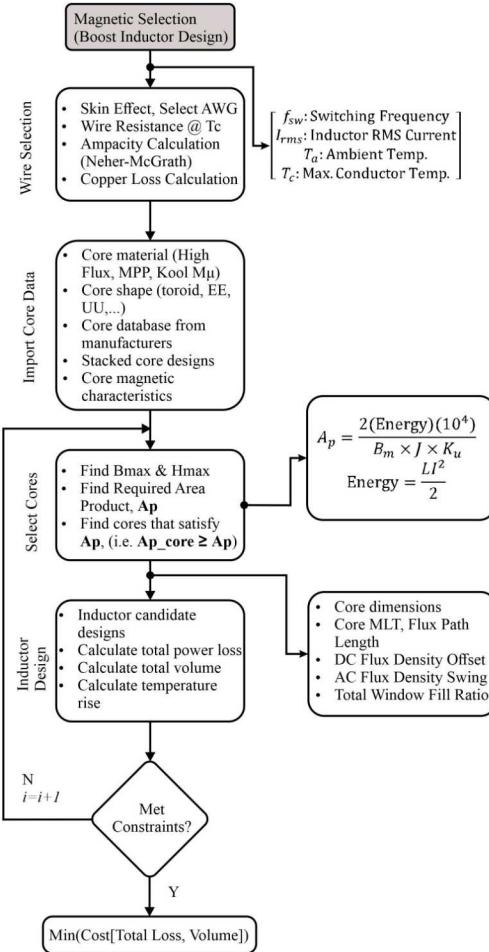


Fig.3 Flowchart illustrating the magnetic selection function that optimizes the boost inductor design based on the input parameter sets.

$$n^2 = \frac{L \times L_e}{\mu_r \mu_0 A_e} \quad (4)$$

where

L_e is the flux mean path length

A_e is the core cross sectional area

μ_r is the relative permeability

μ_0 is the permeability of the free space

n is the number of turns

Among the cores that have met the energy handling requirement, appropriate number of turns is determined based on the flux path length, cross sectional area, and the inductance as denoted in (4). The final total volume of the boost inductor for each design set of parameters is calculated. The core loss is then estimated using the curve fit data provided by the manufacturer [20]. The total volume along with the total loss of the inductor for each design is compared with a simple cost function to provide a competitive selectin of the boost inductor from a large pool of potential numerous magnetic designs.

The total core loss affects the temperature rise of the core in a direct manner along with the switching frequency. The core temperature calculation based the empirical formula that

employs convection and thermal radiation has been used in (5) according to [21].

$$T_{core} [^{\circ}\text{C}] = T_{amb} [^{\circ}\text{C}] + \left(\frac{P_{core} + P_{cu} [\text{mW}]}{A_s [\text{cm}^2]} \right)^{0.833} \quad (5)$$

where A_s is the total surface area of the inductor including the core and the windings.

3) Semiconductor Device Selection Function

The switching and conduction losses of the semiconductor transistors remain one of the main energy loss contributors in switch mode power supplies. When high switching frequency is evaluated, the switching losses impose a significant impact on the overall stress and reliability of the system, but also on the volume of the cooling system. Therefore, it is critical that an accurate model based on empirical data and theoretical calculation of the switching losses is imperative to optimal design of converter systems.

With changing values of the voltage stress, current stress, switching frequency, and varying device characteristics across different devices and materials, the switching losses are calculated based on the MOSFET device model proposed in [22]. The model is based on the charge equivalent representation of the parasitic capacitances of a MOSFET to determine the voltage fall and rise times as well as drain-source current rise and fall times in a half-bridge configuration. The rise and fall times are based on the energy stored in the parasitic capacitances and inductances. Piecewise estimation of the device energy losses is computed with an iterative process and can accurately determine the turn-on and turn-off losses with varying degrees of electrical stress factors.

Many commercially available devices, such as CREE/Wolfspeed, Rohm, Infineon, LittleFuse, and Fuji Electric, have been evaluated and the datasheet values are appropriately extracted to derive distinct loss equations for any qualifying devices with proper voltage and current rating for specific set of genes. The cost function determines the device with the smallest losses for each population and the process is repeated for both the low side (LS) and the high side (HS) device of the synchronous boost converter.

4) Heatsink Selection Function

The cooling system in a power electronic system tends to be bulky and takes up the majority of the volume budget of the system density requirement. In highly efficient converter systems, the size of the cooling is optimized based on the loss of the power dissipation source, mainly the switching devices. With different junction-to-case thermal resistance of the devices selected, the heating dissipation requirement varies across different solution sets.

There are several cooling systems considered in the optimization scheme – natural cooling, forced air cooling with an option of a fan speed allowing 500 Linear Feet per Minute (LFM) and 100 LFM in an air duct, and liquid cooling approach. The sizing equation for each mechanism is based on the estimation provided in [23]-[24]. The approximated sizing equations provided allow a better visualization of the trends with a continuous function, rather than exhaustive methodology

employed in other elements like the capacitor and inductor selection.

5) Capacitor Selection Function

A wide variety of capacitors with different characteristics is available for designers. In power electronic systems, the DC link capacitor is implemented using PCB mounted chip or leaded capacitors. For the most part, the capacitance and rate voltage are in an opposing relationship and such a relationship is more prominent in MLCC whereas film capacitors pose a good balance between the two characteristics. Temperature and frequency play a critical role in the de-rating of the capacitance of MLCC and, thus there are class 1 and class 2 type of ceramic materials to compensate the temperature factor and maintain a high dielectric constant, respectively [25].

The parasitic behaviors due to the ESR and ESL from these capacitors must be recognized and taken into the design consideration. For high voltage DC link capacitor designs, film capacitors provide much larger capacitance with high enough voltage rating, though several capacitors might be needed in parallel to reduce the effect of the series resistance of the film capacitors caused by the dielectric losses. An alternative to film capacitors are MLCC capacitors; however, a large number of MLCC capacitors need to be combined to compensate the lower capacitance characteristic over increasing in withstand voltage [26].

Furthermore, due to the inherent material characteristic differences in reliability between polymer based capacitors and ceramic based capacitors, reliability has been a major focus of research comparison studies among various material types for capacitors. For instance, initial studies have shown a clear trade-off between volume and component lifetime. As volume reduces, more electrical stress is concentrated into a smaller DC link capacitor, and the rate of failure is predicted to increase [27]. This research further explores the relationship in a power electronic system, namely the synchronous boost converter.

6) MTBF Calculation

Failure rate for each component with an exception of the heatsink is calculated using the procedures and equations laid out in [18]. For each component, λ_p expressed in failures/ 10^6 hours and the system MTBF is calculated with the inverse of the total summation of the components' failure rates as described in (8) where $i = 1$ is the capacitor, $i = 2$ is the inductor, $i = 3$ is the semiconductor device.

$$MTBF_{boost} = \frac{1}{\sum_{i=1}^3 \lambda_{p,i}} \quad (8)$$

Appropriate multipliers are selected based on the appropriate applications. The inductor failure rate is determined by the equation described in [18] with inductor type of fixed inductor or choke (i.e. $\lambda_b = 0.00003$) and the hotspot temperature factor is based on the temperature rise calculated previously. The MLCC capacitor calculation is based on the CDR (i.e. $\lambda_b = 0.002$) and the film, CH (i.e. $\lambda_b = 0.00037$). Lastly, the semiconductor device is based on MOSFET base failure rate of $\lambda_b = 0.012$.

7) Computing Resources

Due to the nature of the modeling complexity along with a number of parameters involved in the optimization algorithm, the computation time can be significant. Thus, parallel processing with the aid of High Performance Computing (HPC) clusters at Sandia National Laboratories [28] was employed to reduce the run-time of the optimization computation and analysis.

III. PARETO OPTIMAL SOLUTIONS AND ANALYSIS

Based on the optimization procedure and the models described in the previous sections, the multi-objective optimization analysis has been executed for several comparison studies. In the subsequent subsections, different cooling mechanisms, semiconductor device types, capacitor material types, and inductor material types in relations to MTBF and power density are investigated and analytical results are explained.

A. Heatsink Cooling Type Pareto Optimization

Fig.4 shows the pareto optimal solution sets between four different cooling systems for the 5 kW synchronous boost converter: natural cooling, forced air cooling with fan speed of 500 LFM and 1000 LFM, and liquid cooling. Note that the polymer-based film capacitor type is chosen for both the input and output capacitors. SiC-based semiconductor devices are selected for both the HS and LS switching transistors. High flux material based cores are selected for the boost inductor design. Therefore, the cooling system pareto fronts are limited and specific to the material types selected. However, the trends seen in the figure align with the general insight and the fundamental of physics that the thermal resistance of the heat exchanger can be controlled by the medium surrounding it. While keeping $MTBF > 20,000$ hours, the power density of the 5 kW boost converter can be increased from 30 kW/L with natural convection to 70 kW/L with 100 LFM of forced air cooling, and to 260 kW/L with liquid cooling mechanism. Though liquid cooling provides an effective medium for the heat exchanger, the rest of the pareto optimization analysis hereafter will be based off the forced air cooling with 100 LFM case.

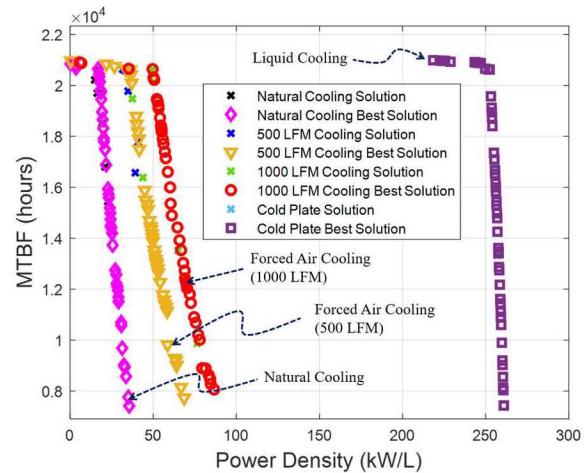


Fig.4 Pareto optimization of cooling system comparison between natural convection, forced air cooling with a fan speed of 500 LFM, 1000 LFM and liquid cooling mechanism

B. Semiconductor Device Type Pareto Optimization

With the recent advancement in the integration of a new generation of power devices like the wide bandgap based semiconductor transistors into power electronic applications, the development of power conversion systems has seen increased in performance in terms of efficiency and power density due to the superior material properties, higher temperatures, higher blocking voltages, and faster switching speeds than current Si technology. This results in the development of power converters with much higher power density [29].

For purposes of evaluating SiC-based semiconductors compared to IGBT transistors, the optimization scheme considered these two competing power devices to investigate for the 5 kW synchronous boost converter. Fig. 5 shows the results of the co-optimization pareto frontiers between SiC MOSFETs and IGBT transistors. There is a clear trend for both transistors that higher power density can be achieved at the expense of reliability. The difference between the two becomes prominent as higher power density is required; the theoretical maximum power density gain with the employment of SiC MOSFETs is approximately 37 kW/L. The analysis is based on the selection of film capacitors for input and output capacitors and forced air cooling of 100 LFM.

C. Input and Output Capacitor Type Pareto Optimization

Another aspect of the optimization analysis is to compare the effect of different capacitor material type; for input and output capacitors, MLCC and polymer-based film capacitors are compared in regard to power density and reliability. Due to its inherent characteristics, MLCC capacitors allow much higher power density designs in a power electronic system. However, the advantage becomes ambiguous when the voltage rating increases due to the trend in decreasing in capacitance over voltage.

Fig.6 illustrates the pareto optimization fronts when MLCC capacitors and film capacitors are used for the 5 kW synchronous boost converter. A gain of 50 kW/L in power density can be realized when MLCC capacitors are selected. Though MLCC performs superior in increasing power density over the film capacitor solution, large number of capacitors needed to achieve the required capacitance suffers MTBF factor. Thus, it can be deduced from the graph that there's a theoretical limit to 5,000 hours when MLCC capacitors are used in this electronic system.

D. Magnetic Inductor Material Type Pareto Optimization

Fig. 7 depicts pareto optimal solutions for the 5 kW boost converter based on Kool Mu, High Flux, and MPP core materials. The optimal solution sets provide a performance metric tool between different inductor material types. With varying magnetic characteristics across different core types, it can be challenging to evaluate the trade-off between core material types, especially when multi-objective optimal designs are sought after.

The general trend is similar between the three core types; higher power density designs can be realized at the expense of decreased MTBF. For the highest power density designs, MPP and High Flux are preferred. Compared to Kool Mu, using MPP can bring about a potential gain of 10 kW/L for the boost

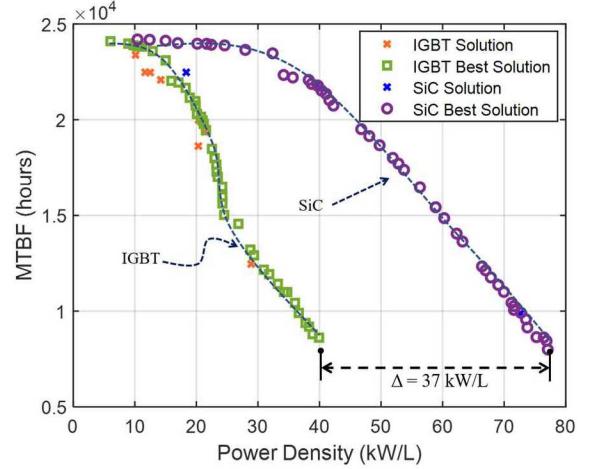


Fig.5 Pareto fronts comparing the co-optimization results between SiC MOSFETs and IGBT transistors for the HS and LS switching devices.

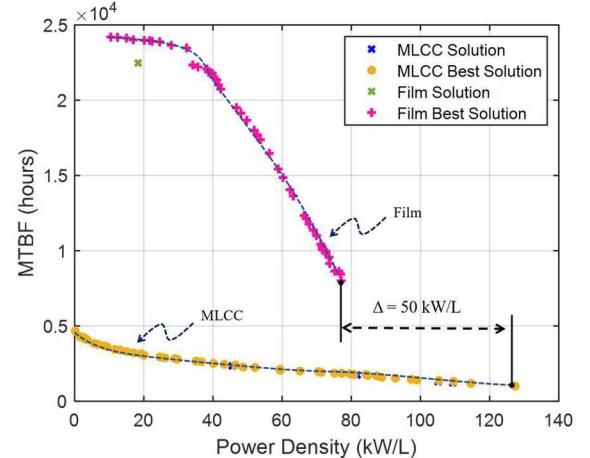


Fig.6 Pareto optimization solution sets with MLCC capacitors and film capacitors for input and output capacitors.

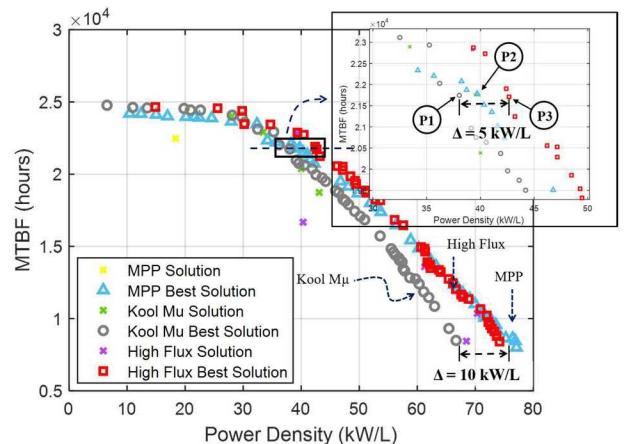


Fig.7 Pareto optimization solution evaluating Kool Mu, High Flux, and MPP and the prototypes with different inductors denoted as P1, P2, and P3, respectively.

converter. High Flux cores allow high power density designs for high power and high DC bias applications because of its high saturation flux density (1.5 T). However, when such a design is necessary, high switching frequency is required and hence, switching losses through the devices along with the core loss can have a significant impact on the reliability factor.

IV. EXPERIMENTAL RESULTS AND VERIFICATION

To validate the analysis provided in this work, three separate prototype designs have been developed and tested. Fig.7 shows the candidate design marked P1, P2, P3 for Kool Mu, MPP and High Flux, respectively. With the High Flux design compared to the design using Kool Mu at MTBF of 22,000 hours, additional 5 kW/L of power density gain is expected.

A. Optimal Solutions for Different Magnetic Materials

Fig.8 shows the 5 kW inductor design example for each prototype. From the optimization results of the prototypes, a single core of C058110A2 is used for P3 whereas two stacked cores of 0077717A7 for P2 and C055716A2 for P3 are used. Table II shows the details and specifications of the candidate designs; boost converter operating points, predicted losses, MTBF, and power density are summarized.

Looking at the optimized solution sets for the different magnetic materials, some of the variables seem to be converging to specific values; the optimized input voltage tends to be around 400 V whereas the output voltage is approximately 500 V. Most of the switching frequency selections vary between 30 kHz to 70 kHz. The junction temperature is selected to be the lowest, at 75 °C for higher MTBF designs and at 175 °C for higher power density designs. For all design considerations, the semiconductors selected for both the HS and LS are C2M0040120D, which is assumed to have the best balance between the switching and conduction losses based on the switching frequency, voltage, and current conditions. Though the device current rating is much higher than the anticipated current through the device, its small junction-to-case thermal resistance of the device, largely driven by the physical size of the die contributes to a reduced heatsink size. Moreover, the input and output capacitors are selected for all cases are B32641B6682J and B32774X8305K000, respectively as the voltage selection gene was fixed at 5% of the voltage ripple.

B. Hardware Prototype and Verification Experiment Results

The prototypes for the selected designs noted as P1, P2 and P3 have been developed and their operating conditions have been demonstrated in order to verify the validity of the design procedure and the optimization scheme. Fig.9 shows an image of the prototype, P3 with the High Flux solution. The components have been selected based on the parts in Table II and the same procedure is used to build the Kool Mu (P1) and MPP prototype (P2).

The magnetic designs have been validated using the saturable core model and the winding model in PLECS. The core physical and magnetic characteristics, including the dimensions, permeability, flux density saturation, and number of turns are considered to confirm the desired inductance values. Finally, each core is hand wound to its calculated turns number and the inductance values are measured using a network analyzer.

TABLE II – SELECTED PROTOTYPE SPECIFICATIONS

Operating Condition			
Variable	P1 (Kool M μ)	P2 (MPP)	P3 (High Flux)
Input, Vin	400V	400V	400V
Output, Vo	500V	500V	500V
$I_{in,min} - I_{in,max}$	7.47-17.78A	9.9-15.35A	10.74-14.57A
f_{sw}	47.37 kHz	48.7 kHz	47.87 kHz
Duty Cycle	20.81%	20.8%	21.4 %
T_j	78.8°C	75.19°C	75°C
Inductance	169 μ H	310 μ H	462 μ H
Input Capacitors			
Model #	B32641B6682J	B32641B6682J	B32641B6682J
Capacitance	3×6.8 nF	3×6.8 nF	3×6.8 nF
Total Volume	0.936 mL	0.936 mL	0.936 mL
Output Capacitors			
Model #	B32774X8305	B32774X8305	B32774X8305
Capacitance	4×3 μ F	4×3 μ F	4×3 μ F
Total Volume	29.11 mL	29.11 mL	29.11 mL
Boost Inductor			
AWG/Strands	23 AWG/10	23 AWG/10	23 AWG/10
Model #	0077717A7	C055716A2	C058110A2
Window Fill Factor	20%	17.7%	24%
Turns Number	52	46	78
Loss (W/C)	10.53W/10.89 W	10.89W/7.09W	7.84 W/8.8 W
Temp. Rise	48.6 °C	35 °C	90 96 °C
Total Volume	0.045L	0.043 L	0.0365 L
Low Side Semiconductor Device			
Model #	C2M0040120D	C2M0040120D	C2M0040120D
Rating (V,I)	1200 V, 60 A	1200 V, 60 A	1200 V, 60 A
Rds(on)	40 m Ω	40 m Ω	40 m Ω
R _{jc}	0.38 °C/W	0.38 °C/W	0.38 °C/W
Packaging Type	TO-247	TO-247	TO-247
Loss (Ton/Toff/Cond)	2.09W/3.45W/1 .33W	2.69W/3.13W/1 .33W	2.88 W/2.98 W/1.37W
Volume	1.71 mL	1.71 mL	1.71 mL
High Side Semiconductor Device			
Model #	C2M0040120D	C2M0040120D	C2M0040120D
Rating (V,I)	1200 V, 60 A	1200 V, 60 A	1200 V, 60 A
Rds(on)	40 m Ω	40 m Ω	40 m Ω
R _{jc}	0.38 °C/W	0.38 °C/W	0.38 °C/W
Packaging Type	TO-247	TO-247	TO-247
Loss (Ton/Toff/Cond)	5.82W/2.28W/5 .05W	4.68W/2.5W/5. 05W	2.88 W/2.98 W/1.37 W
Volume	1.71 mL	1.71 mL	1.71 mL
Total Efficiency	99.16%	99.2%	99.2 %
Heatsink			
Volume	0.054L	0.057L	0.056 L
Power Density	38.04 kW/L	39.74 kW/L	42.67 kW/L
MTBF	~21,800 hrs	~21,800 hrs	~21,800 hrs

Fig.10(a)-(c) illustrate the experimental results of the input voltage, output voltage, input current, and output current waveforms in comparison with the theoretical or simulated data from each SPIC model. Fig.10(a) accounts for P1, Fig.10(b) for P2, and Fig.10(c) for P3. It is concluded that each prototype conforms to the expected requirements and performs with high efficiency of the desired operating condition of boosting the input voltage of 400 V to output voltage of 500 V; the efficiencies for P1, P2, and P3 are 97%, 98.8%, and 98.9%, respectively.



Fig.8 5 kW boost inductor design comparison between P1 (Kool Mu), P2 (MPP), and P3 (High Flux) prototypes.



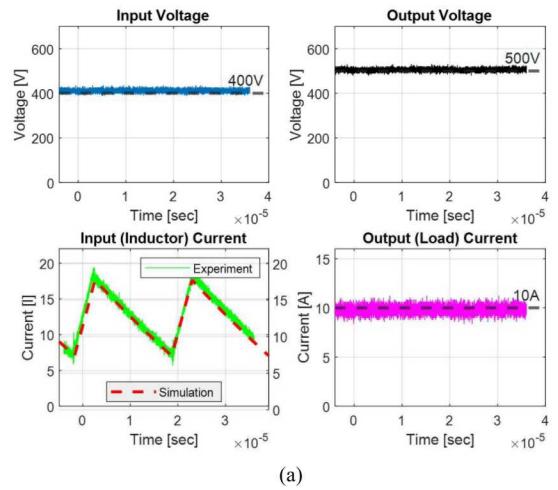
Fig.9 Picture of hardware prototype with the High Flux core design, P3.

V. CONCLUSION AND FUTURE WORK

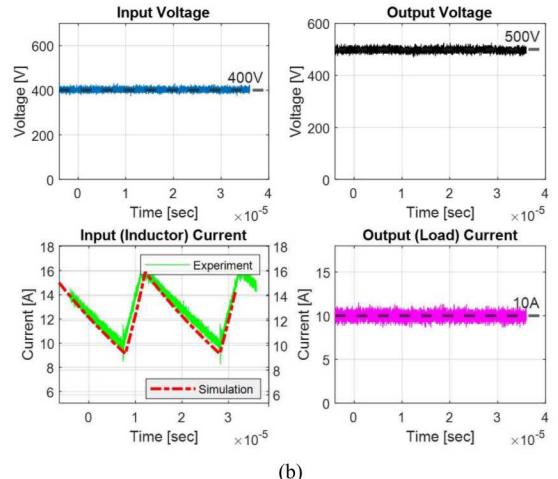
This research effort seeks to investigate multi-objective optimization between MTBF and volumetric power density of the 5 kW synchronous boost converter. A detailed selection model for each component of the boost converter under optimization objectives is developed with a high level of fidelity. Optimal solution sets are identified for varying degrees of component material type variation. Several candidate designs are selected and developed to validate the viability of the optimized output solutions computed from the model. The operating conditions using the prototypes have been verified with a good fit to the anticipated results from the simulation.

In future work, the authors suggest various improvements and variations that can be added to the current optimization work. First, the fitness function used to evaluate the fitness value of each gene set can be improved with different genetic operators, such as elitism, migration, and random search. Furthermore, each model can be expanded to other materials; there are several other iron powder core types in Magnetics Inc., such as XFlux, and Kool Mu Max and ferrite cores from different core manufacturers can be used to compare its performance metric against iron powder cores. Core shapes can be extended to other shapes, like EE, UU, EI, etc.

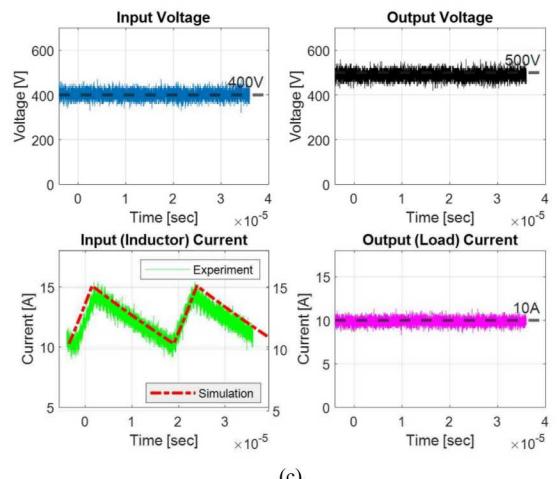
In this work, only the main components of the boost converters have been modeled for the multi-objective optimization. However, there are many other components that have not been analyzed in the optimization studies, such as the gate driver, auxiliary power supply and other ancillary ICs and circuits. Though it is important to include a model for every



(a)



(b)



(c)

Fig.10 Measured waveforms of the 5 kW boost converter operation with input of 400 V and output of 500 V for each candidate boost converter design – P1, Kool Mu shown in (a), P2, MPP shown in (b), and P3, High Flux shown in (c). The efficiencies are 97% for (a), 98.8% for (b) and 98.9% for (c).

possible electronic and mechanical component that degrade over time in a system, it remains a keen challenge to evaluate the overall system's reliability that's inclusive of the system constituents in its entirety.

Lastly, there's an on-going research effort using similar design multi-objective design optimization scheme to model an inverter system for electric vehicle traction drive system [30].

ACKNOWLEDGMENT

The authors would like to thank Nicholas Baker and Raymond Martinez at Sandia National Laboratories for the development of the testbed for the hardware prototype experiments and measuring accurate data for testing.

Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology & Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. The views expressed in the article do not necessarily represent the views of the U.S. Department of Energy or the United States Government. This research was supported by the US Department of ENERGY (DOE) Vehicle Technologies Office (VTO) under the Electric Drivetrain Consortium.

REFERENCES

- [1] H. S.-hung Chung, H. Wang, F. Blaabjerg, and M. Pecht, *Reliability of power electronic converter systems*. London: Institution of Engineering and Technology, 2016.
- [2] J. D. van Wyk and F. C. Lee, "On a Future for Power Electronics," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59-72, June 2013.
- [3] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran and P. Tavner, "An Industry-Based Survey of Reliability in Power Electronic Converters," in *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1441-1451, May-June 2011.
- [4] L. Schrittweiser, J. W. Kolar and T. B. Soeiro, "99% Efficient three-phase buck-type SiC MOSFET PFC rectifier minimizing life cycle cost in DC data centers," in *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 1, pp. 47-58, 2017.
- [5] P. Papamanolis, F. Krämer and J. W. Kolar, "Minimum loss operation of high-frequency inductors," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 1756-1763.
- [6] F. C. Lee, S. Wang and Q. Li, "Next Generation of Power Supplies—Design for Manufacturability," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.
- [7] IEEE, *IEEE standard framework for the reliability prediction of hardware*, IEEE Std. 1413, New York, 2009..
- [8] ANSI/VITA 51.2 Standard, *Physics of failure reliability predictions*, Oklahoma City, OK: VEMbus International Trade Association, 2011.
- [9] Military Handbook: *Reliability prediction of electronic equipment*, MIL-HDBK-217F, Washington, DC, Dec. 2, 1991.
- [10] J. Biela, M. Schweizer, S. Waffler and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2872-2882, July 2011
- [11] R. M. Burkart and J. W. Kolar, "Comparative Life Cycle Cost Analysis of Si and SiC PV Converter Systems Based on Advanced η - ρ - σ Multiobjective Optimization Techniques," in *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4344-4358, June 2017.
- [12] J. Biela, U. Badstuebner and J. W. Kolar, "Impact of Power Density Maximization on Efficiency of DC-DC Converter Systems," in *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 288-300, Jan. 2009.
- [13] M. Kasper, D. Bortis, G. Debay and J. W. Kolar, "Design of a Highly Efficient (97.7%) and Very Compact (2.2 kW/dm³) Isolated AC-DC Telecom Power Supply Module Based on the Multicell ISOP Converter Approach," in *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7750-7769, Oct. 2017.
- [14] Edwin K. P. Chong and Stanislaw H. Żak, *An Introduction to Optimization*, 2nd ed. New York, New York, USA: John Wiley & Sons, Inc., 2001.
- [15] Scott D. Sudhoff, GOSET: *Genetic Optimization System Engineering Tool: For Use with MATLAB®*, version 2.6, (January 1, 2014) [Online] Available:<https://engineering.purdue.edu/~sudhoff/Software%20Distribution/GOSET%202.3%20manual.pdf>.
- [16] Powder Cores Catalog, Magnetics, Pittsburgh, PA, 2017. [Online]. Available:<https://www.mag-inc.com/Design/Technical-Documents/Powder-Core-Documents>.
- [17] J. H. Neher and M. H. McGrath, "The calculation of the temperature rise and load capability of cable systems," in *Transactions of the American Institute of Electrical Engineers. Part III: Power Apparatus and Systems*, vol. 76, no. 3, pp. 752-764, April 1957.
- [18] P. Pollak, "Neher-McGrath Calculations for Insulated Power Cables," in *IEEE Transactions on Industry Applications*, vol. IA-21, no. 5, pp. 1319-1323, Sept. 1985.
- [19] C. W. T. McLyman, *Transformer and inductor design handbook*. CRC Press, 2017.
- [20] Curve Fit Equation Tool, Magnetics, Pittsburgh, PA, 2017. [Online]. Available:<https://www.mag-inc.com/Design/Design-Tools/Curve-Fit-Equation-Tool>.
- [21] T. Nussbaumer, K. Ragg and J. W. Kolar, "Design Guidelines for Interleaved Single-Phase Boost PFC Circuits," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2559-2573, July 2009.
- [22] D. Christen and J. Biela, "Analytical Switching Loss Modeling Based on Datasheet Parameters for mosfets in a Half-Bridge," in *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3700-3710, April 2019.
- [23] D. Christen, M. Stojadinovic and J. Biela, "Energy Efficient Heat Sink Design: Natural Versus Forced Convection Cooling," in *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8693-8704, Nov. 2017.
- [24] Ohmite, *Heatsink Sizing Guide*, 2017. Available: <https://www.ohmite.com/assets/docs/pdf-files/Product%20Guide%20Thermal%20print.pdf?r=false>.
- [25] TDK, *Guide for Replacing Film Capacitors with MLCC, Version 4*, 2011. Accessed: 5/12/2020. [Online]. Available: <https://passive-components.eu/tdk-guide-for-replacing-of-film-capacitors-with-mlcc/>
- [26] J. Stewart, J. Neely, J. Delhotal and J. Flicker, "DC link bus design for high frequency, high temperature converters," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 809-815.
- [27] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters—An Overview," in *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569-3578, Sept.-Oct. 2014.
- [28] Y. Denning, *2019 HPC Annual Report*. Report No. SAND2019-11345 O, Sandia National Laboratories, 2019.
- [29] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155-2163, May 2014.
- [30] L. Rashkin, J. Neely, L. Gill, J. Flicker, and R. Darbali-Zamora, "Optimal Power Module Design for High Power Density Traction Drive System," *IEEE Transportation Electrification Conference (ITEC 2020)*, June 23-26, 2020.