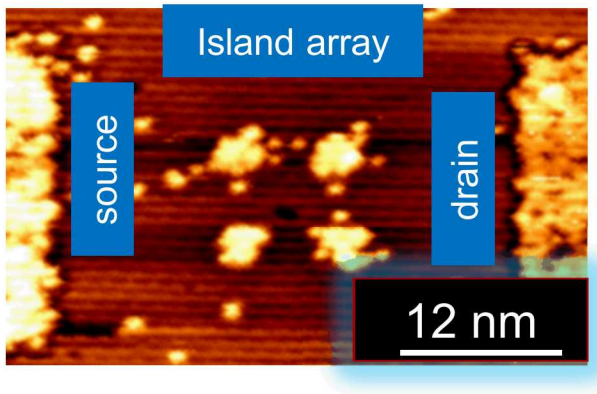
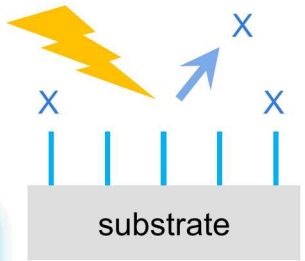
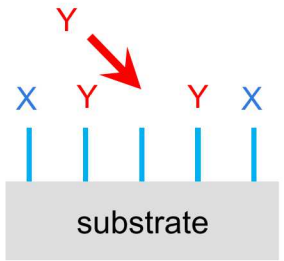
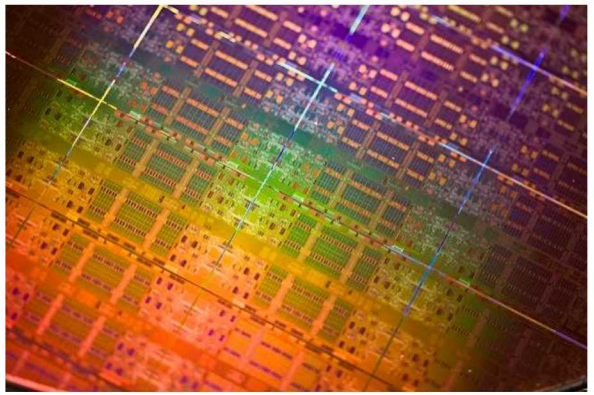
SAND2020-7035PE









FAIR DEAL GC Thrust 1 : APAM devices

Shashank Misra, Scott Schmucker, Tzu-Ming Lu, Lisa Tracy, Aaron Katzenmeyer

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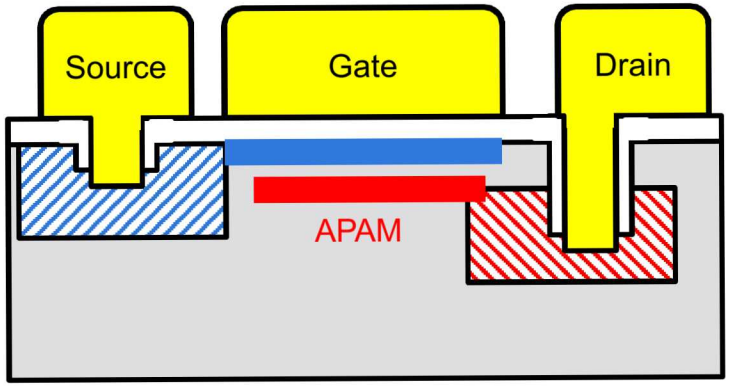
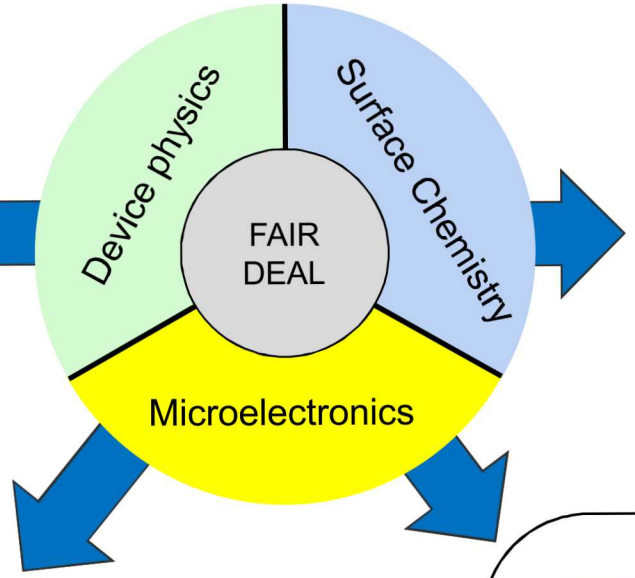
Digital electronics at the atomic limit (DEAL)

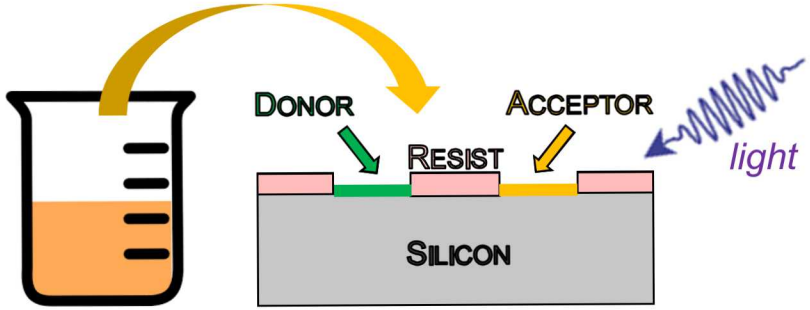
Sandia National Laboratories

Thrust 1: APAM-enabled Devices

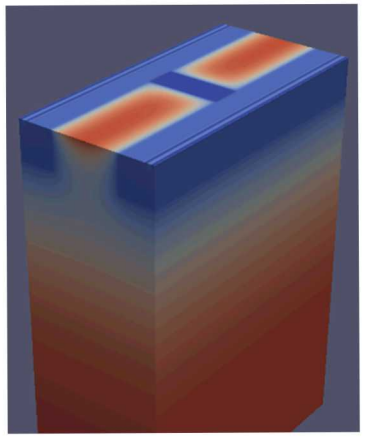




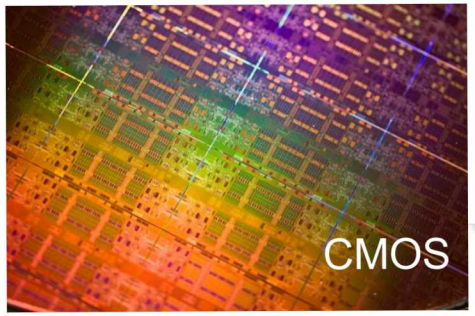
Thrust 4: Application Platform

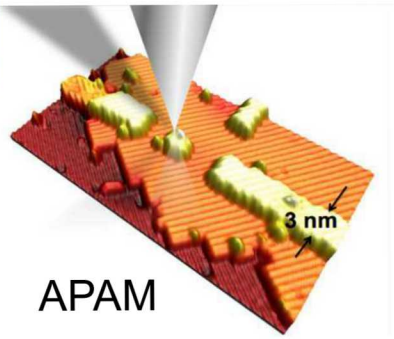


Thrust 2: APAM Modeling

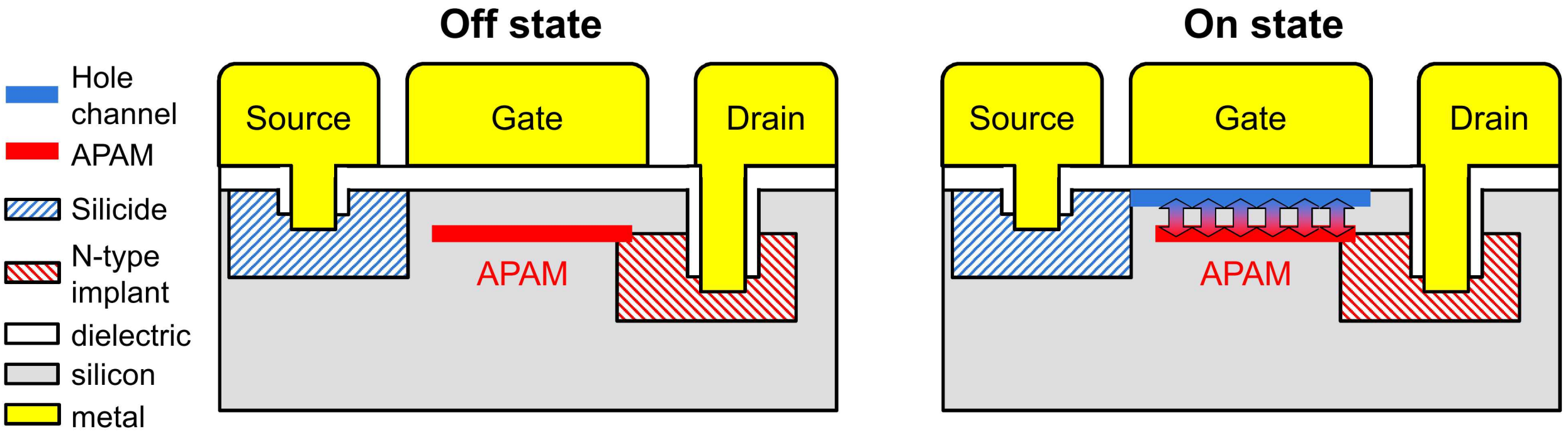


Thrust 3: CMOS Integration





Capstone goal: TFET



Requires highly-doped, atomically-sharp layer

Why is it hard to make an APAM transistor?

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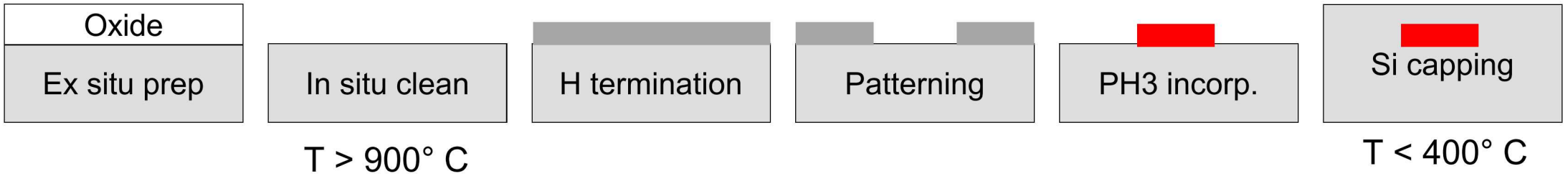
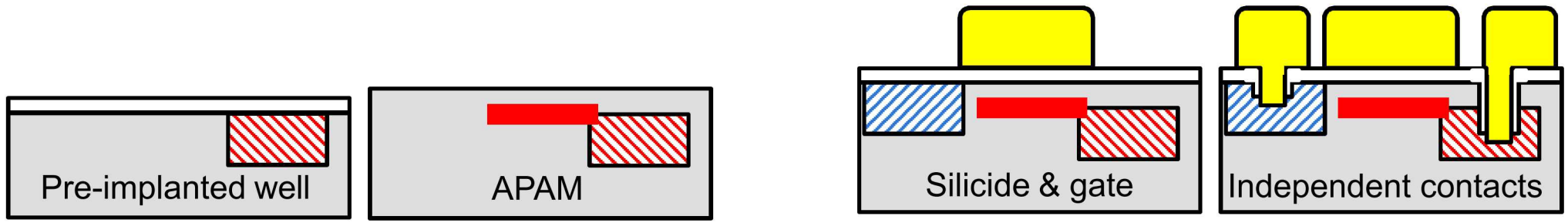
APAM flow



TFET flow

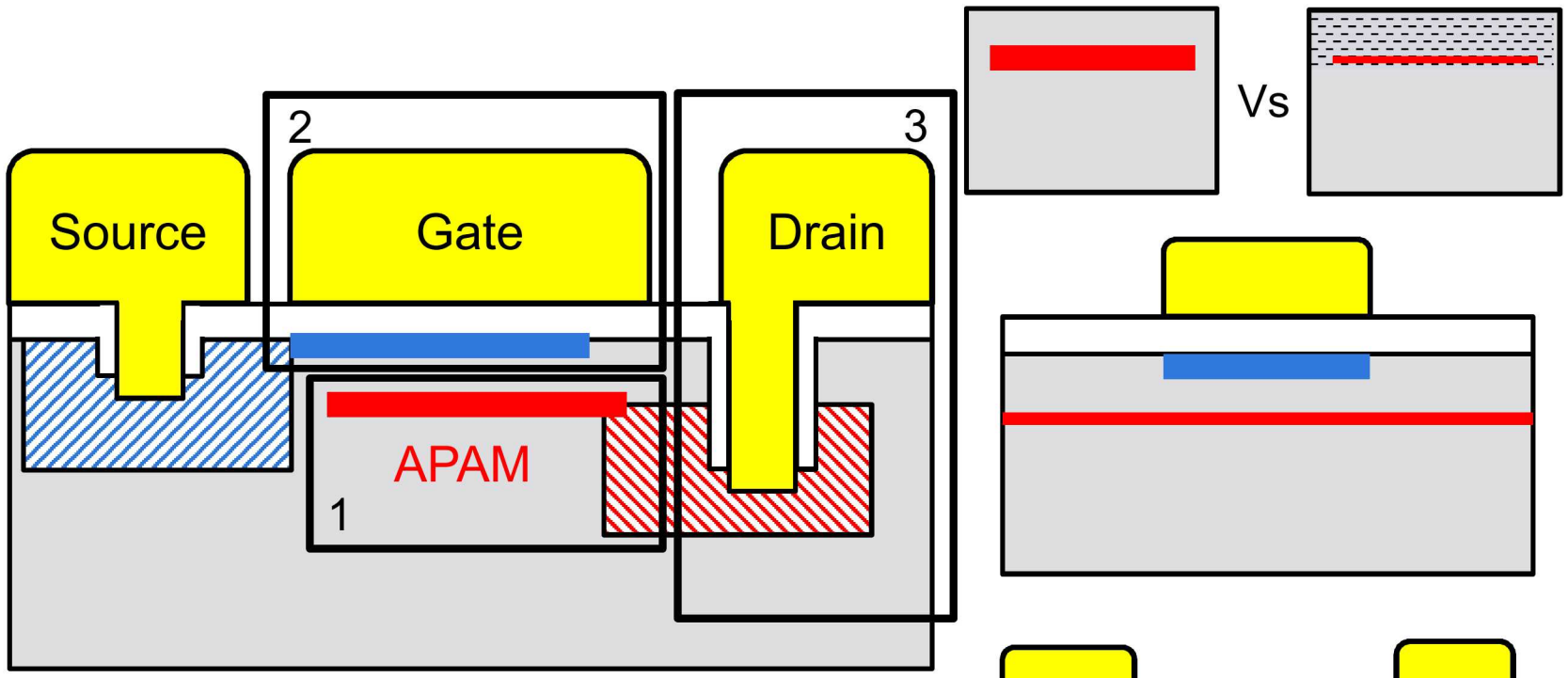


APAM prep must keep pre-APAM steps intact

All post-APAM steps must keep APAM layer intact

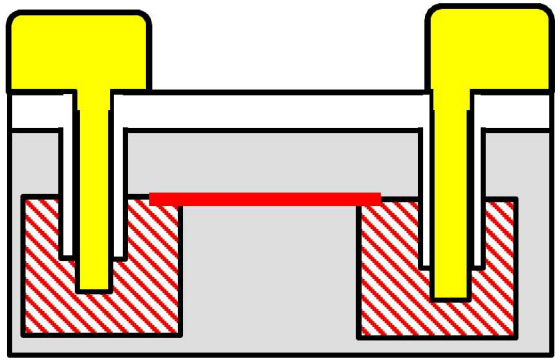
Must ensure thermal and process compatibility!

Thrust 1 – task layout



Task #1. Channel engineering

Task #2. Surface gates

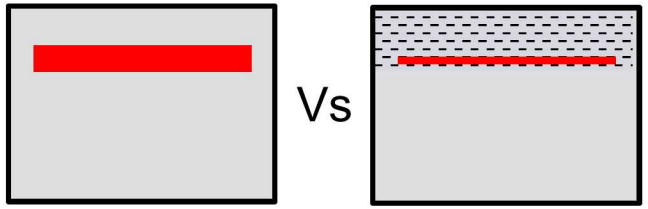


Task #3. Room temperature operation

The elemental components of ANY transistor, including the TFET

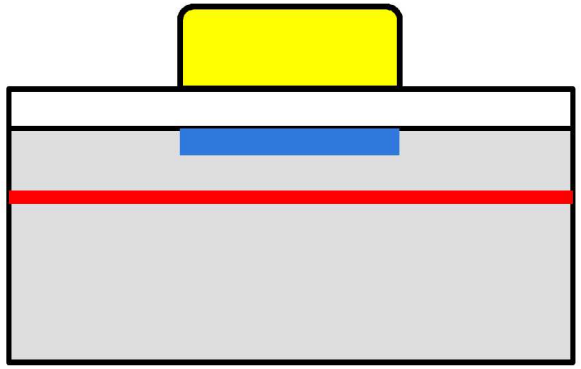
FY 20 accomplishments

Complete set of tools to evaluate APAM and silicon cap



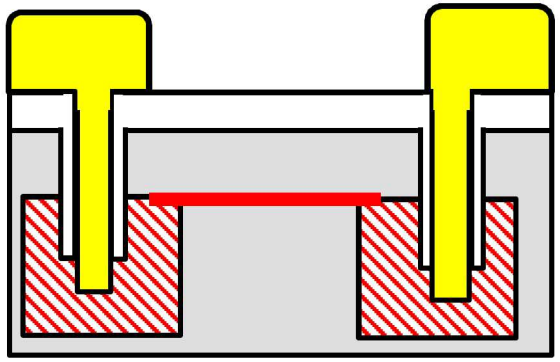
Task #1. Channel engineering

1st: APAM-compatible, transistor-grade gate stack



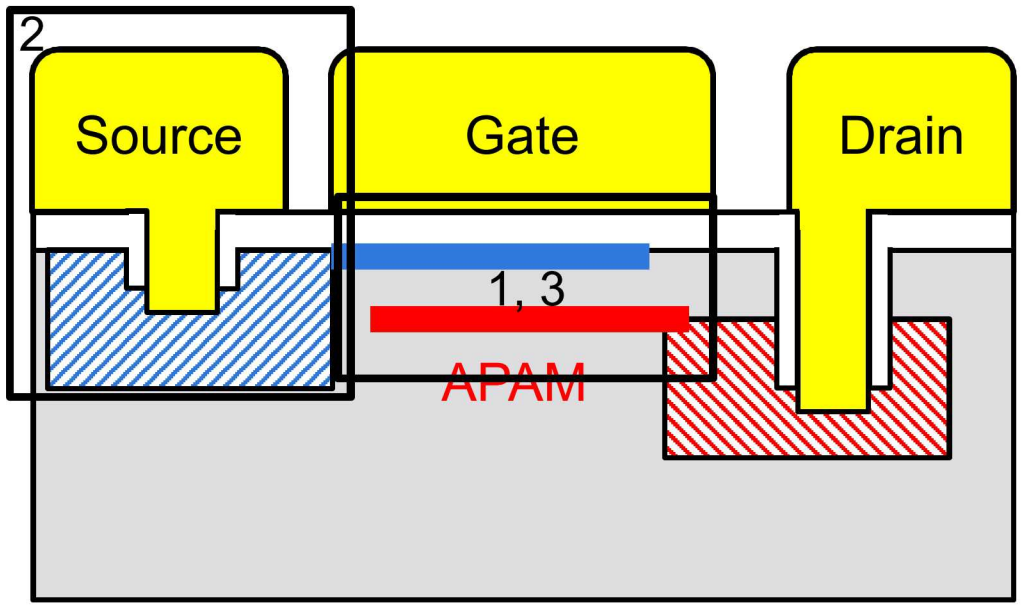
Task #2. Surface gates

1st: Room temperature APAM device



Task #3. Room temperature operation

FY 21 goals



Task #1. Channel engineering

Understand APAM process
→ electrical characteristics

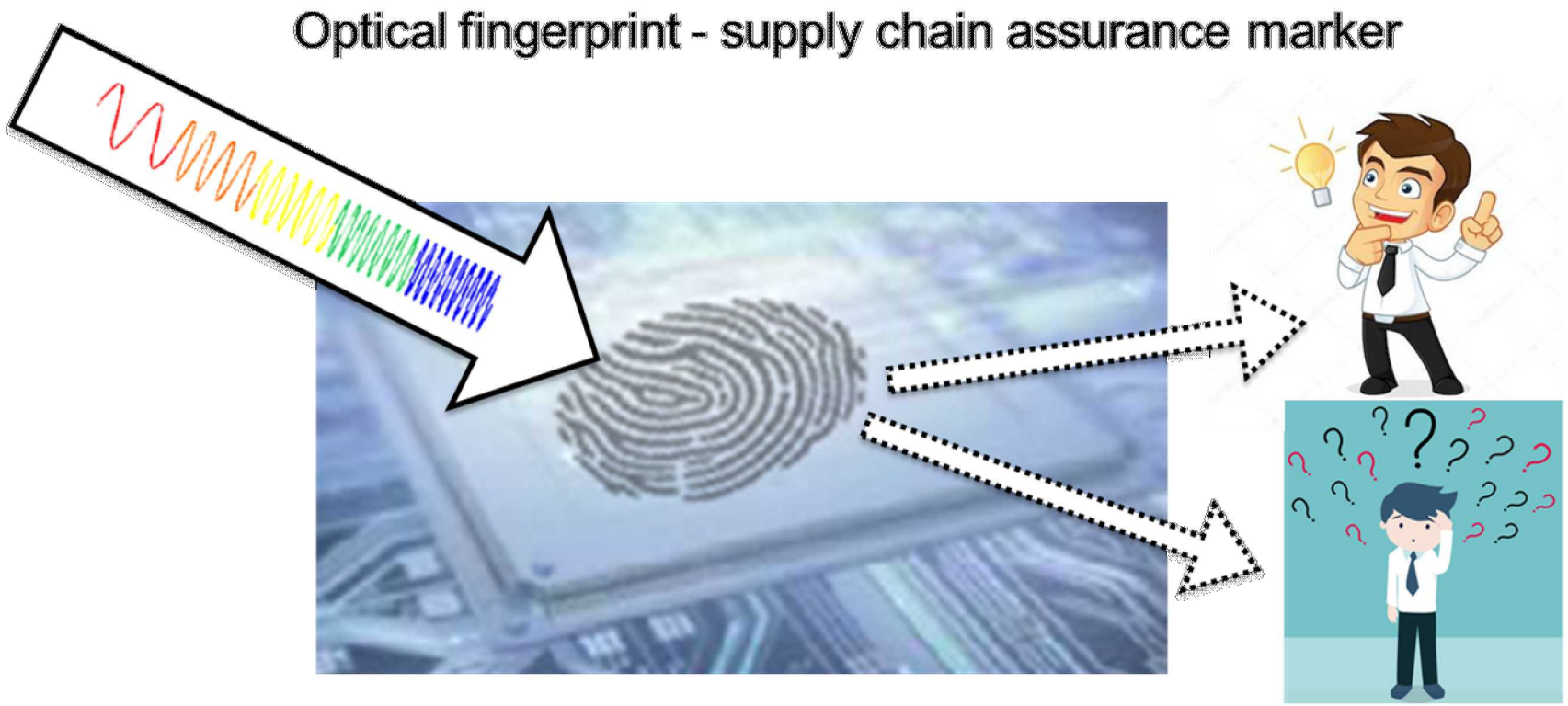
Task #2. APAM Transistor

Develop silicide
Construct transistor

Task #3. Room temperature operation

Understand physics of APAM layer

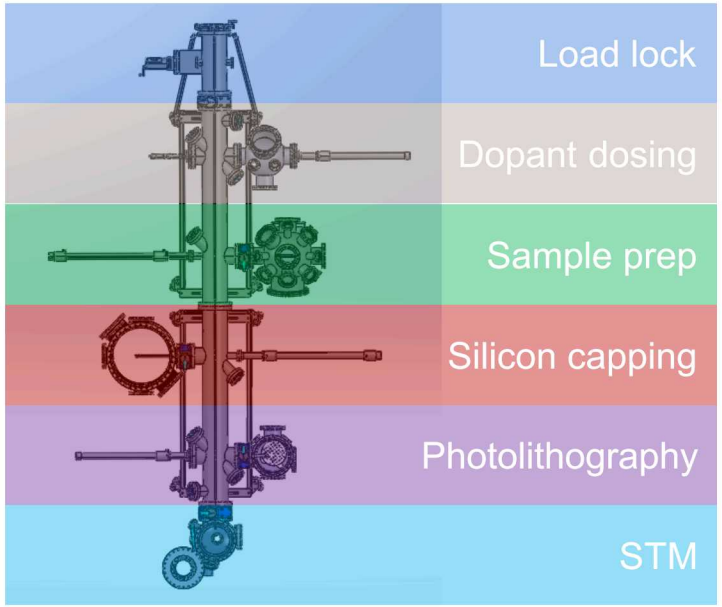
Task #4 – Optical fingerprint



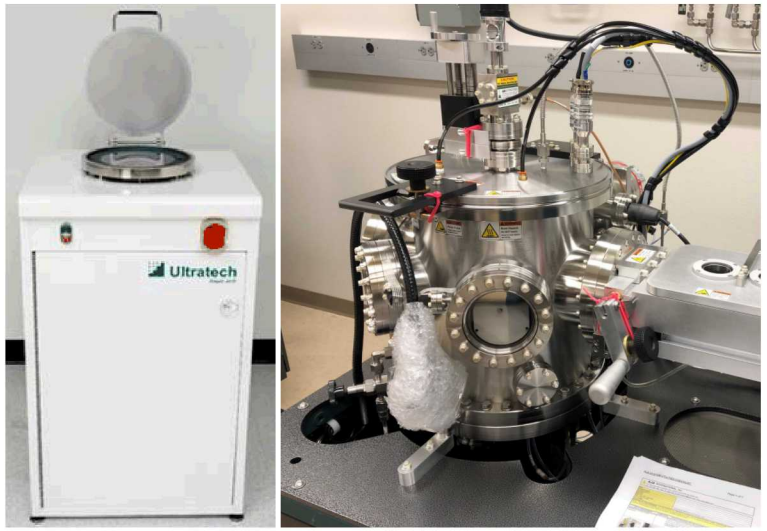
FY 20 Accomplishment: Understand fundamental optical properties of APAM layers

Discontinuing in FY 21: Unclear path to unique marker, more need for electrical fingerprints

Thrust 1 – Capabilities



APAM system that separates parts of the process



Oxide ALD and metal PVD – we own our gate stack

Variable temperature measurement 1 – 420 K

Equipment purchases directly feed speeding up cycles of learning

FY 20 Impact

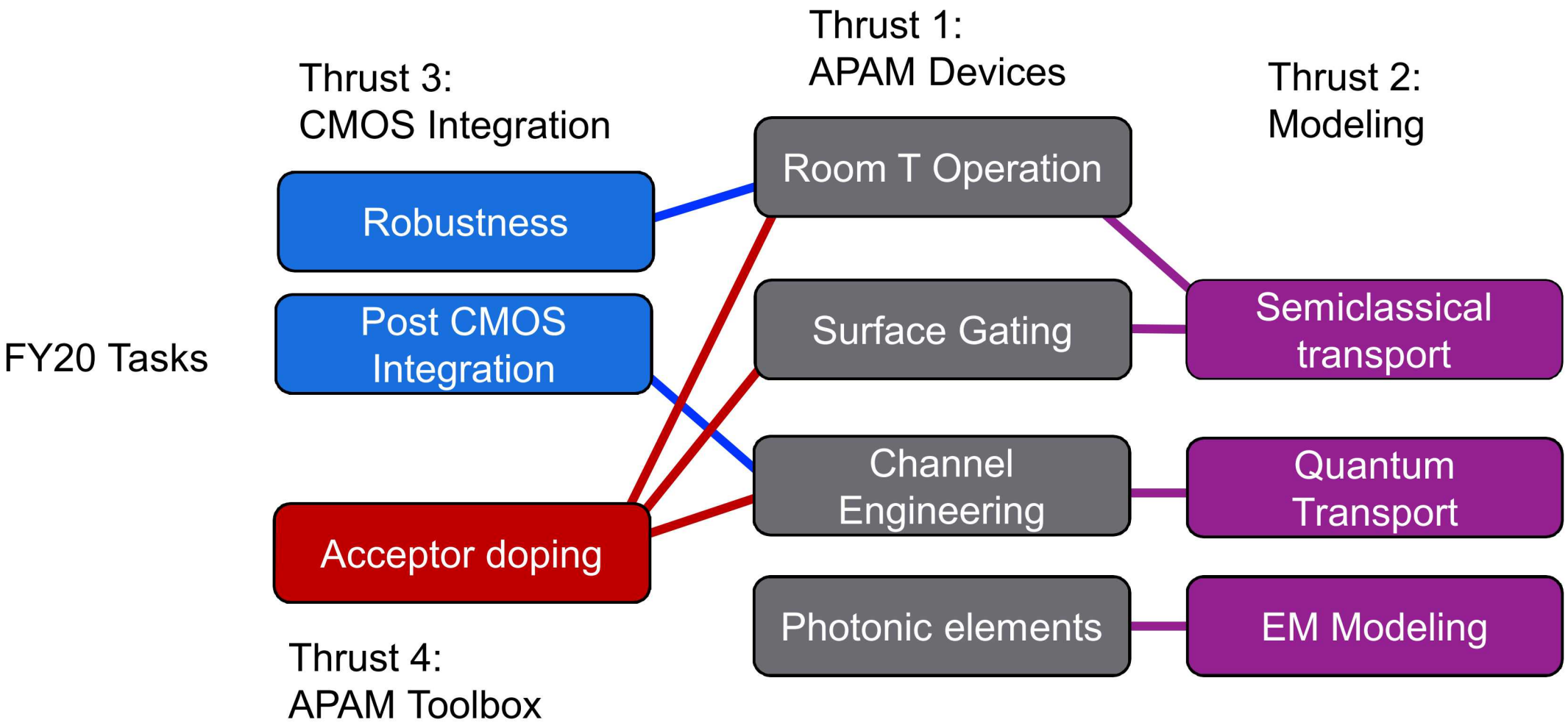
1st: Gated APAM device
1st: Room temperature APAM device

Attempting outreach to IEEE audiences, on their terms

Articles			
Task	**Topic**	**Journal**	**Status**
Surface Gating	Cryogenic gated SET	Journal of Physics: Materials	Accepted
Optical fingerprint	Optical response of APAM layer	Journal of Materials Research	Accepted
Surface Gating	APAM TFET	Technical Advance	In preparation

Invited talks	
Talk topic	**Event**
Quantum devices	NSF workshop on “Quantum Simulators”
APAM digital devices & CMOS integration	Invited seminar at LPS
APAM digital devices & CMOS integration	Invited seminar at NIST (canceled)
APAM digital devices	Invited talk at APS March Meeting (canceled)
APAM digital devices	Workshop on AP fabrication of solid-state quantum devices (canceled)
APAM digital devices	SOS24 – “Will HPC survive the cloud, and in what form?” (canceled)

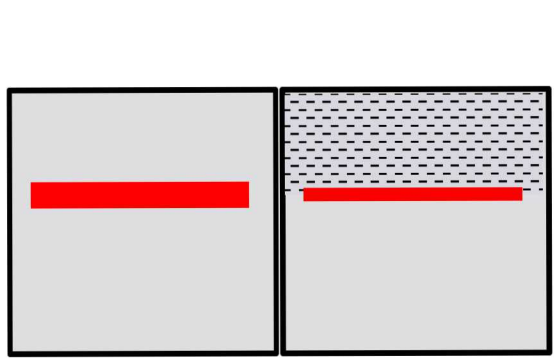
Integration with other tasks

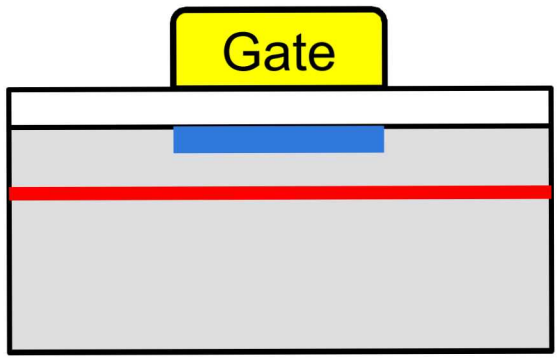


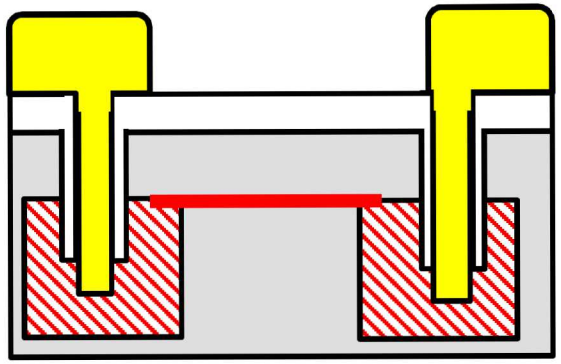
Outline

Sandia National Laboratories

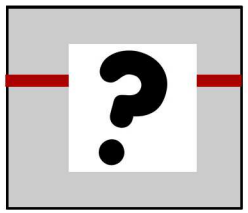
Channel Engineering	Surface gating	Room temp operation	Optical fingerprint
Scott Schmucker	**Tzu-Ming Lu**	**Lisa Tracy**	**Aaron Katzenmeyer**

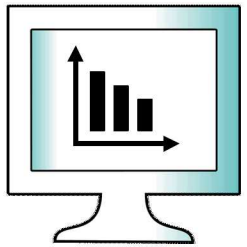






What are the Goals of Channel Engineering?





APAM Processes

- Temperature
- Time
- Dose
- Precursor

APAM Characteristics

- Defects
- Dopant Distribution
- Dopant Density

Device Performance

- Current Density
- Capacitance
- Contact Resistance

Materials Characterization

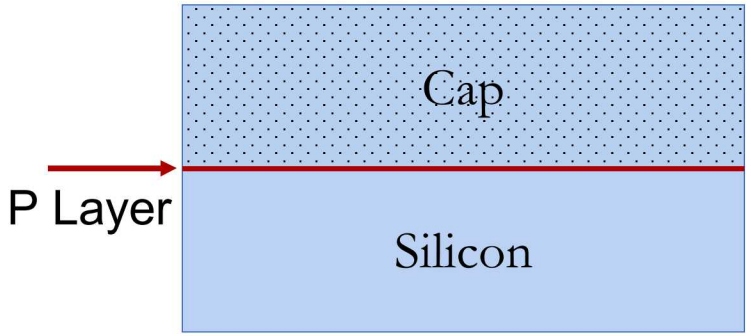
How do you know when all of the right atoms are in the right place?

Device Performance

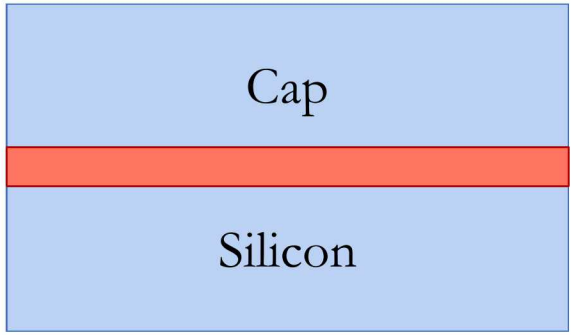
What are the key variables and metrics?

This is discovery science – we are developing underlying understanding

Temperature → Materials → Devices

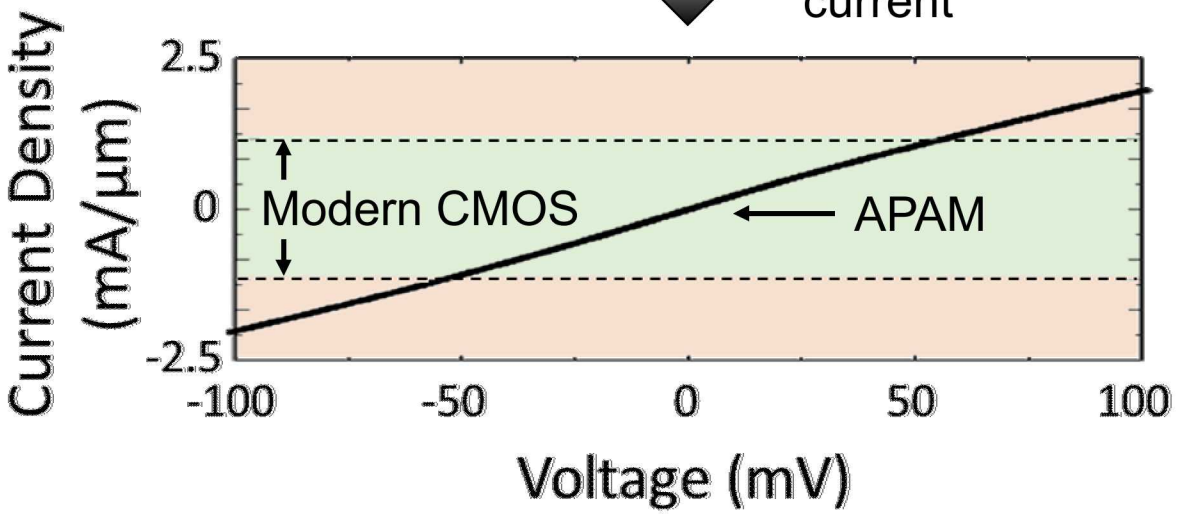


Confined P layer, defects in cap



P layer has diffused, few cap defects

High drive current



Reduced current density?

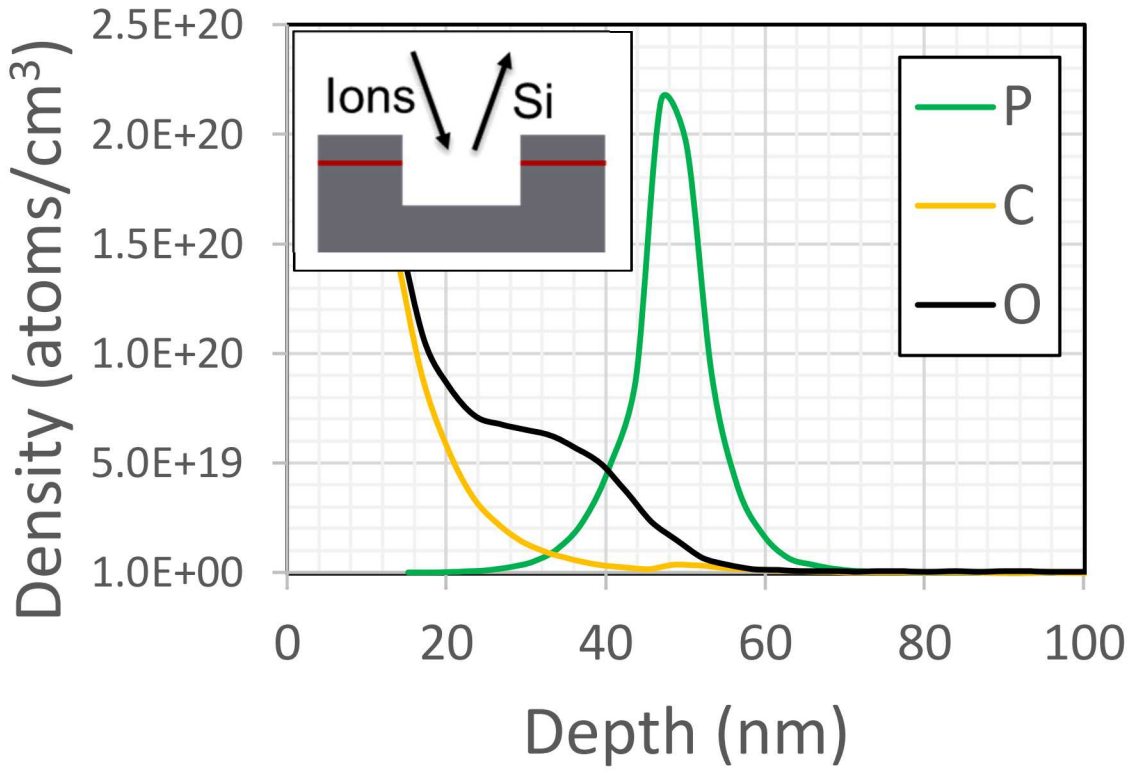
Temperature changes APAM materials → How does this effect performance?

Mapping Recipes to Depth Profiles

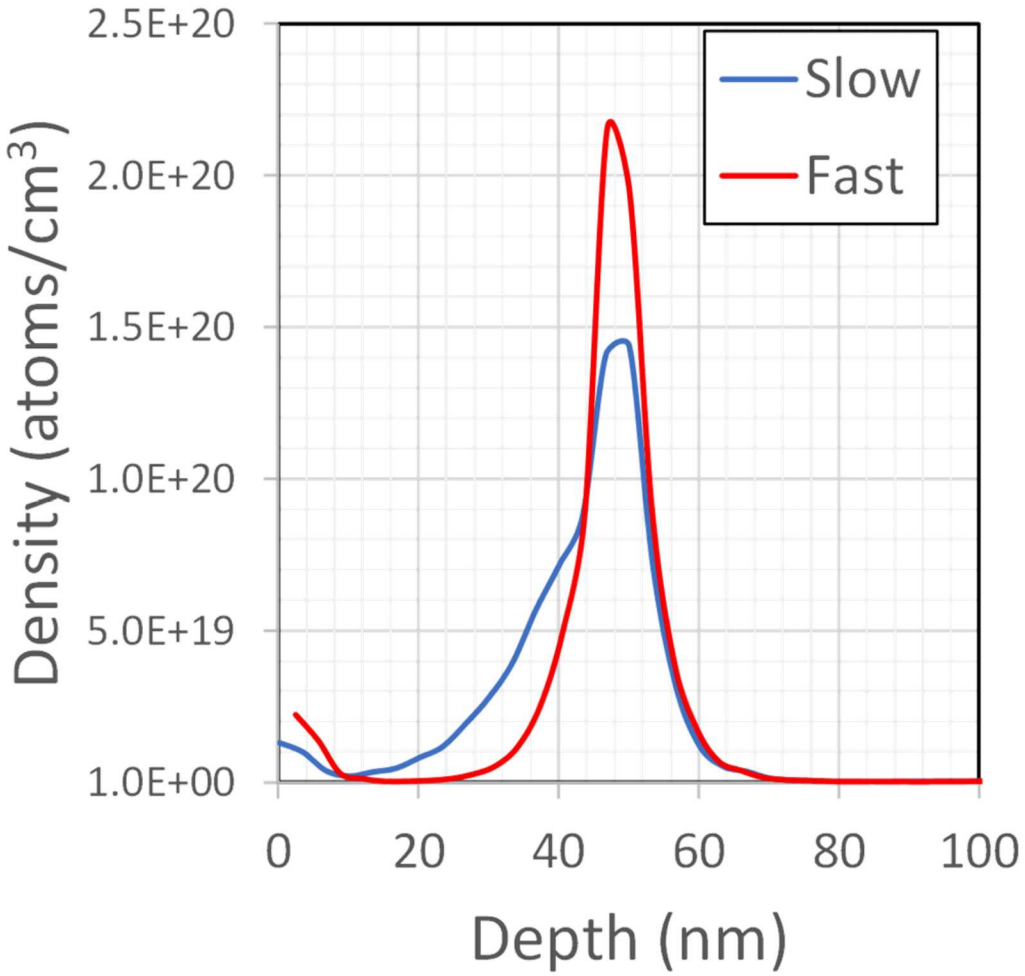
Secondary Ion Mass Spectrometry (SIMS)

→ Location of Dopant Atoms

→ Density of Some Defects



Varying Growth Rate of Si Cap



SIMS identifies depth of dopant atoms and composition of cap

Assessing Electrical Activity in Device Caps

Spreading Resistance Profiling (SRP)

→ Assess electrical activity in cap
→ Spreading of APAM delta layer can be a limiting factor

Resistivity as a Function of Depth

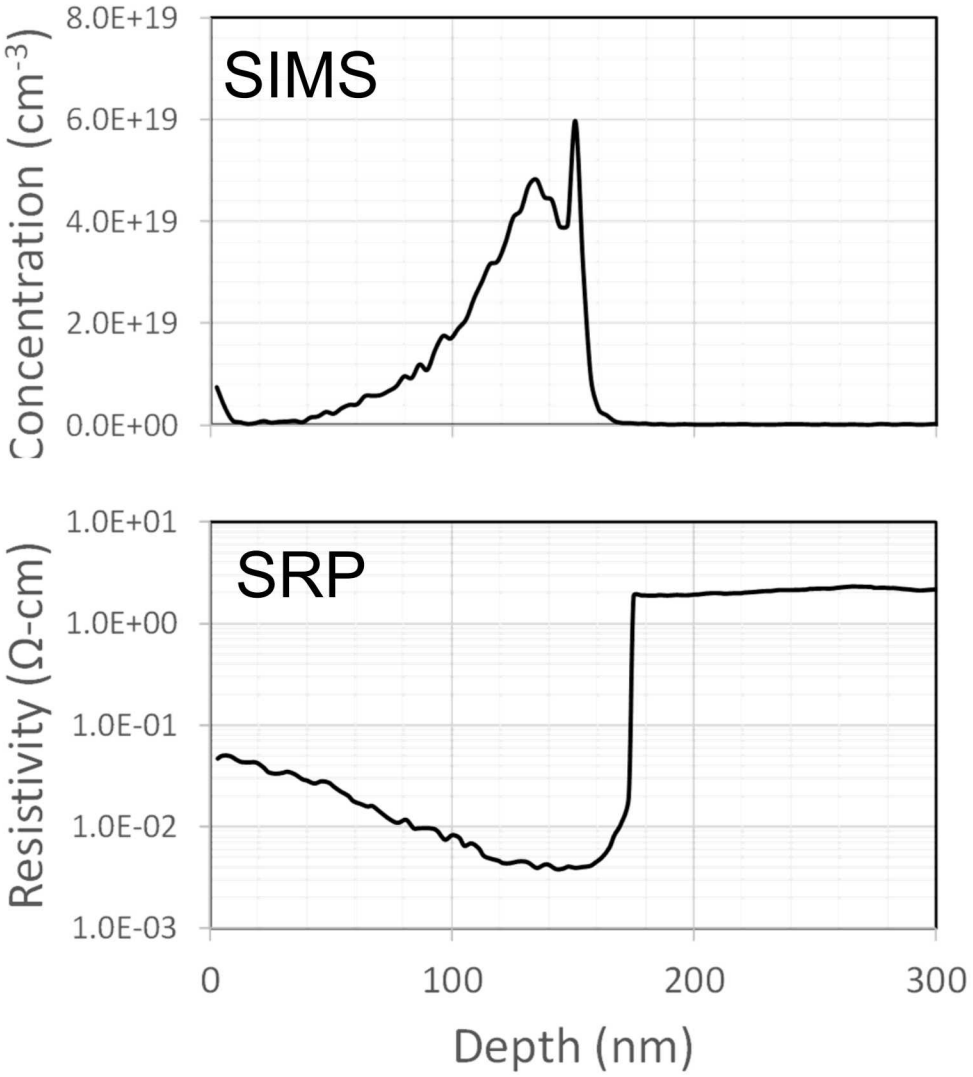
↓

Carrier Density and Polarity as a Function of Depth

↙ ↘

Electrical Activation of APAM Dopants

Electrical Activity of Contaminants in Cap



SRP tells us about electrical activity of dopants in Si cap

Mapping Recipes to Gated Devices

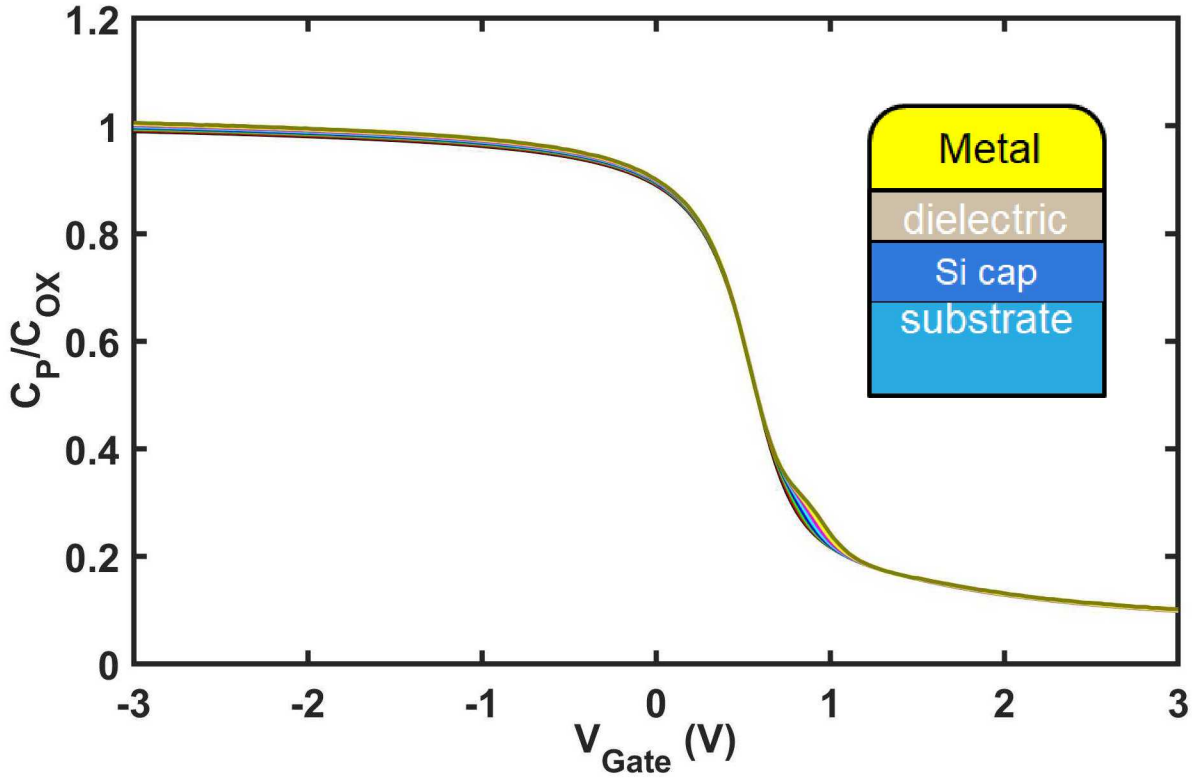
High quality material stack for capacitor:

→ Newly enabled, key measurement technique

→ Intrinsic quality of device is high

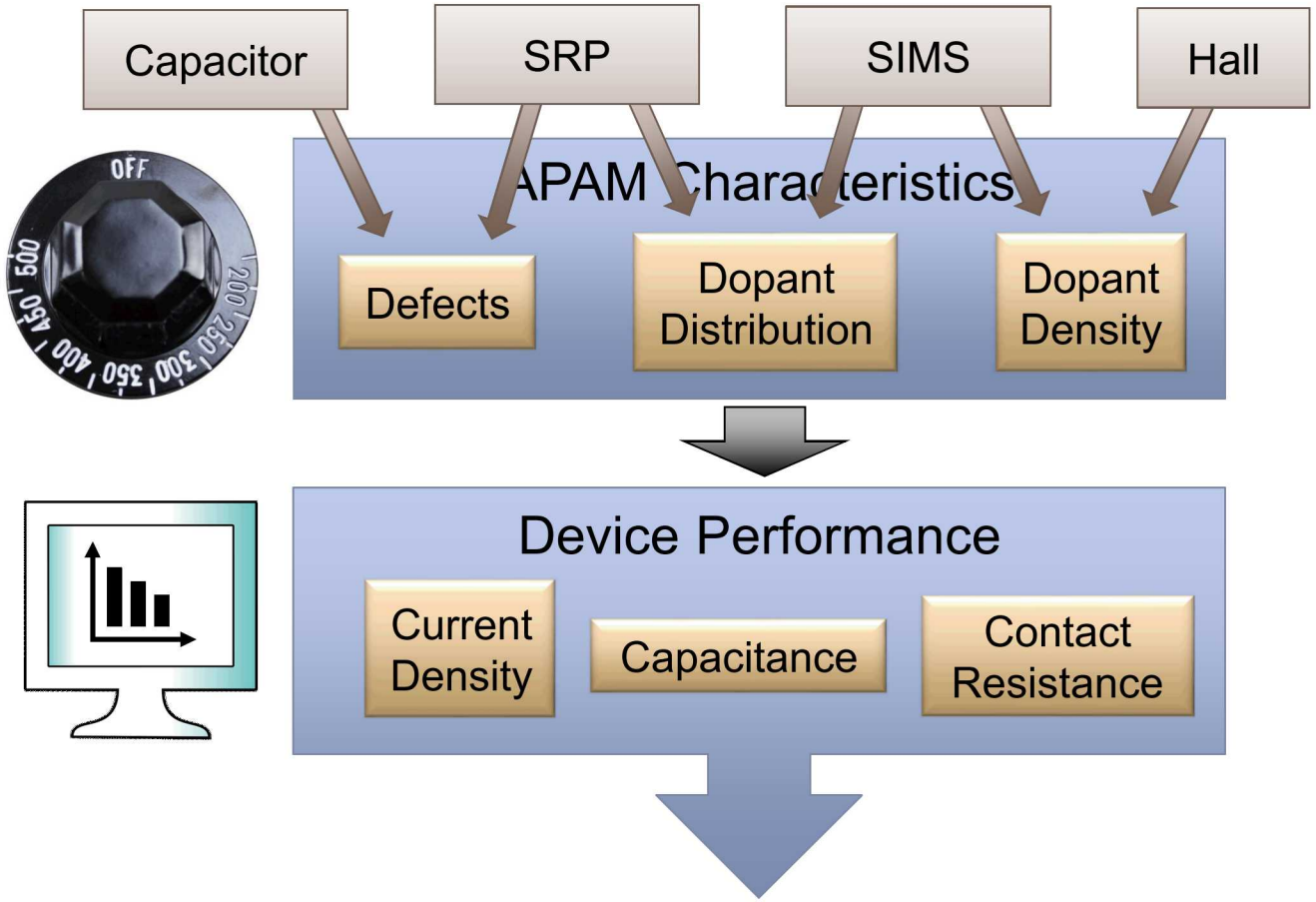
- Can see defects in the cap, not just in the gate stack

→ Detailed later in this session



A high quality capacitor enables characterization of defects in the Si cap

APAM Characteristics to Device Performance

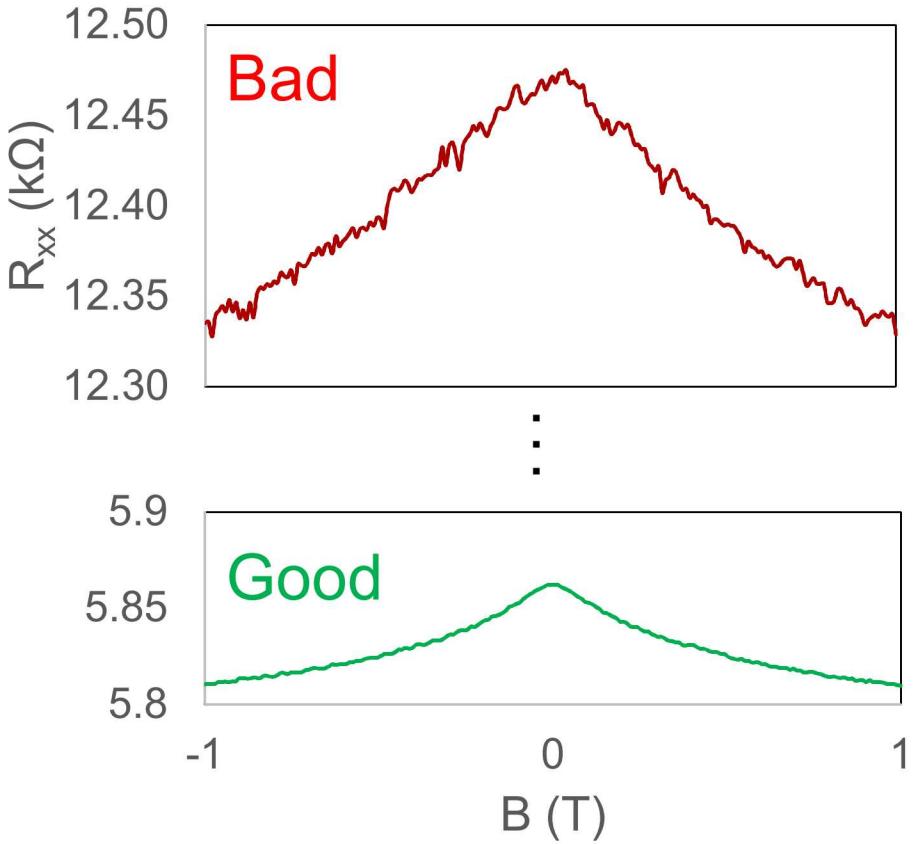


These are observables!

- Suites of tools to **access formerly hidden APAM characteristics**
- Now **one-step removed from performance metrics** (observables)
- Next: For key performance metrics (e.g. contact resistance), **turn APAM Characteristics knobs and optimize for desired metric**

Control of APAM characteristics → removes hidden variables

Problems with Reproducibility in FY20



- Influence seen in device performance
- What APAM characteristic is the cause?
- Dopant distribution? Defects in cap? Unknown hidden variable?

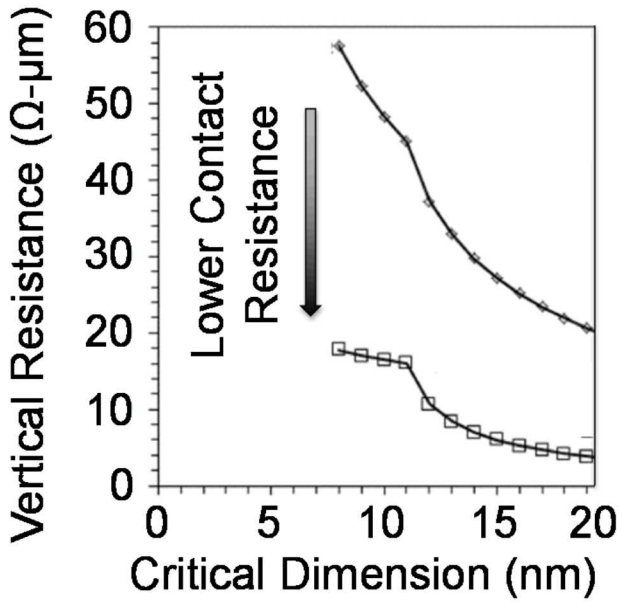
FY20 Q3 – STM team 'sprint'

- Full team synchronizes on results every day
- Independent test and validation of each process step

The machinery is in place, but irreproducibility has restricted progress

Looking Forward – Contact Resistance

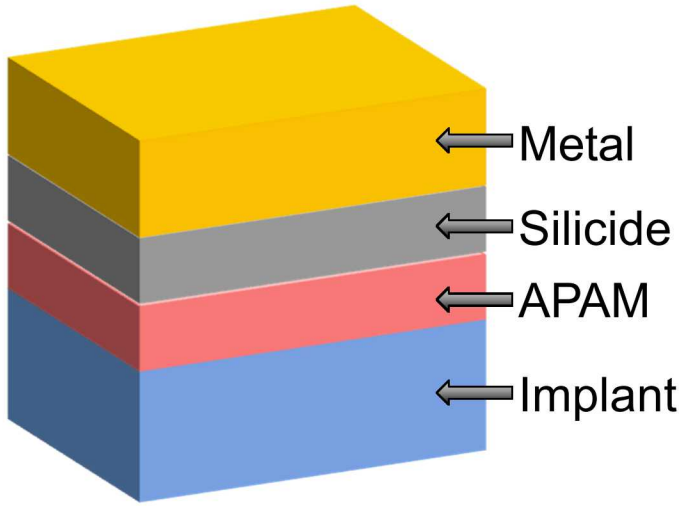
Contact Resistance
→ Commercial Interest



V. Kamineni et al., IEEE IITC (2018)

Size of CMOS transistor determined by contact resistance

APAM → Reduce Resistance



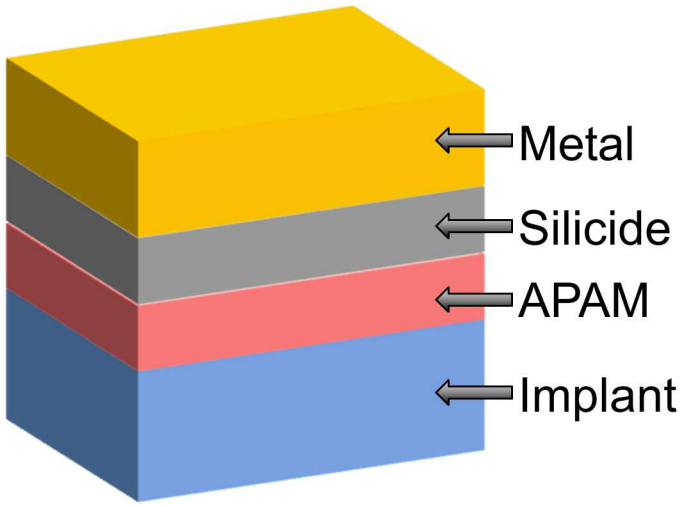
Applied Materials: APAM could decrease contact resistance

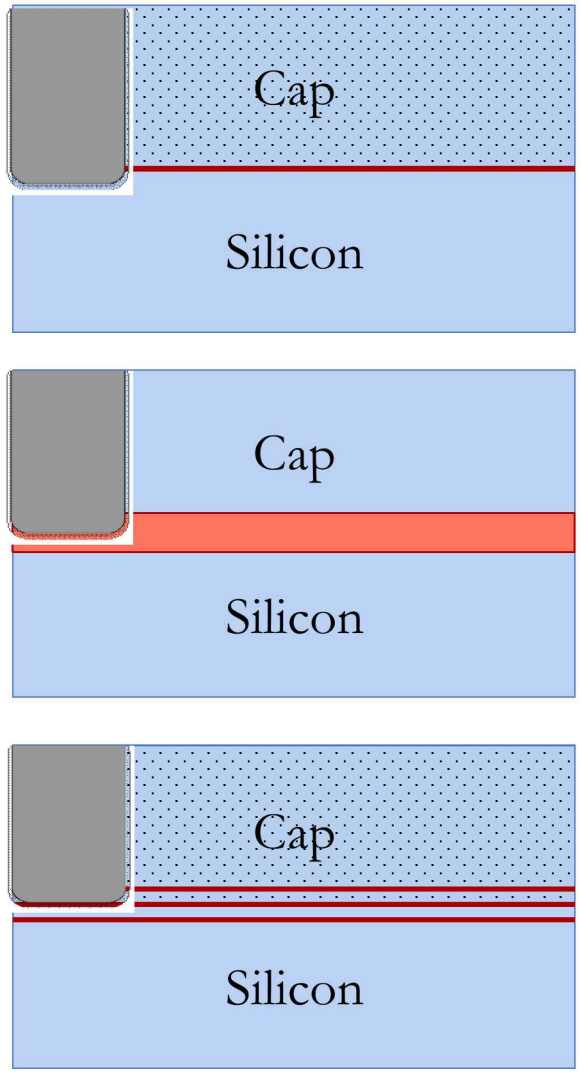
Reducing barrier to electron transport with **APAM ultradoping**

Have asked for plus-up to pursue this to Applied Materials' specifications.

APAM may offer new method to improve contact resistance in CMOS devices

How to engineer the channel for optimization?

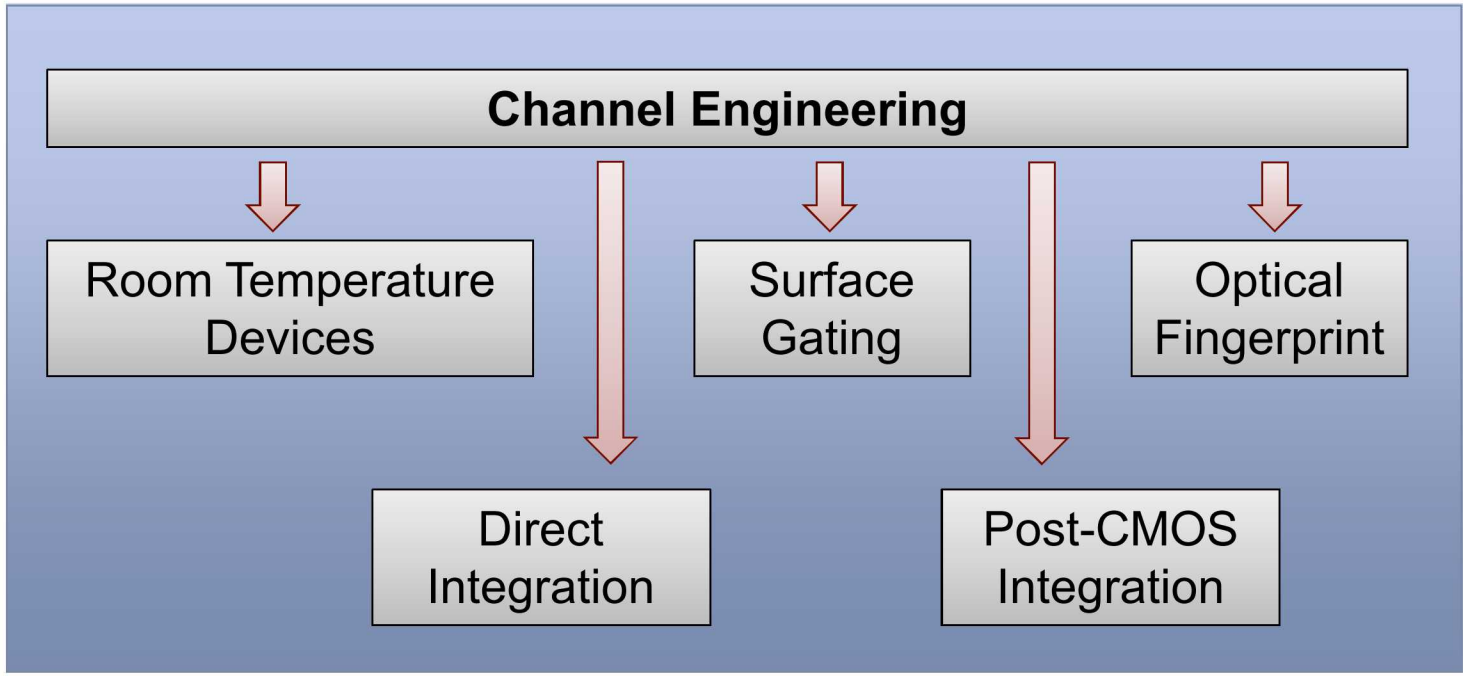




- How should APAM materials be **engineered to optimize contact resistance**?
- Expand existing machinery with Univ. Florida & Appl. Mater. collaboration

Existing capabilities leveraged to assess implications of contact tuning

Broader impact



- **Channel Engineering is a key enabling step in the development of every APAM application**
- **Discovery Science: Developing fundamental understanding** of APAM processes and their impact on the channel
- **Assessment of impact** that channel characteristics have on key devices

Channel Engineering = Key enabling step for every APAM application

Surface gating/APAM transistor

Sandia National Laboratories

FY20 Accomplishments

- Characterization of APAM composition and electrical activation
- High-quality gate stack for device characterization

FY 21 Goals

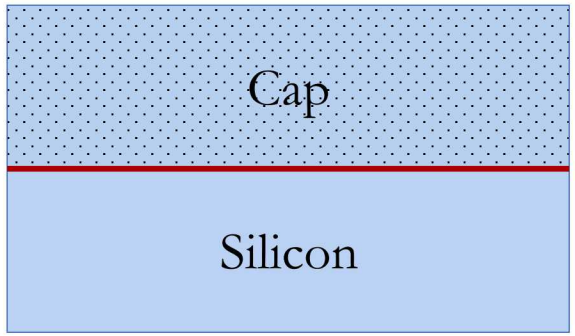
Connect characteristics to device performance

Assess impact of APAM on contact resistance

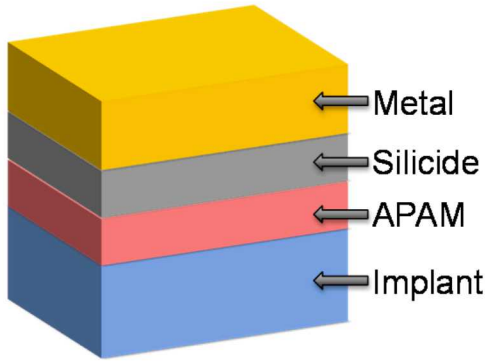
Beyond GC

Channel Engineering → Key enabling technology for all APAM technologies

Key implications for future CMOS technology



Materials Characterization
FY 20



Device Performance
FY 21

Outline

Sandia National Laboratories

Channel Engineering

Scott Schmucker

Surface gating

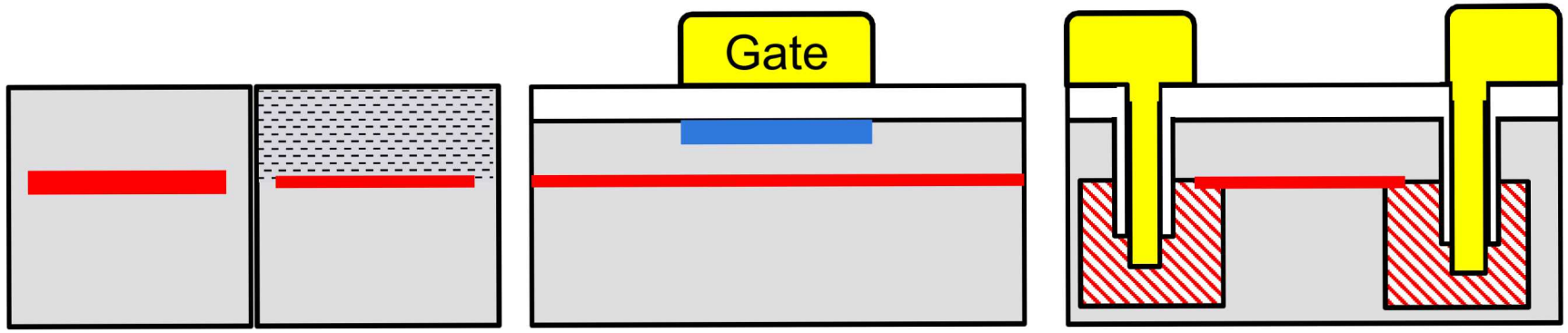
Tzu-Ming Lu

Room temp operation

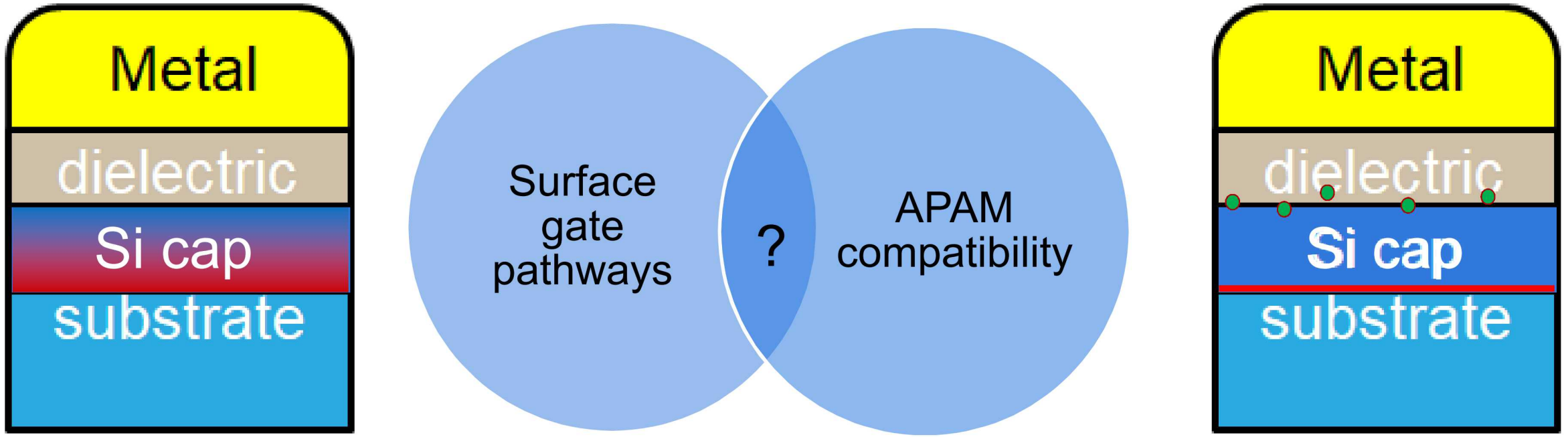
Lisa Tracy

Optical fingerprint

Aaron Katzenmeyer



Surface Gating / APAM Transistor

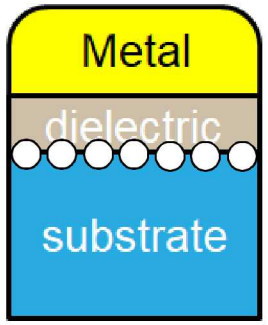


Accomplishments in FY20:

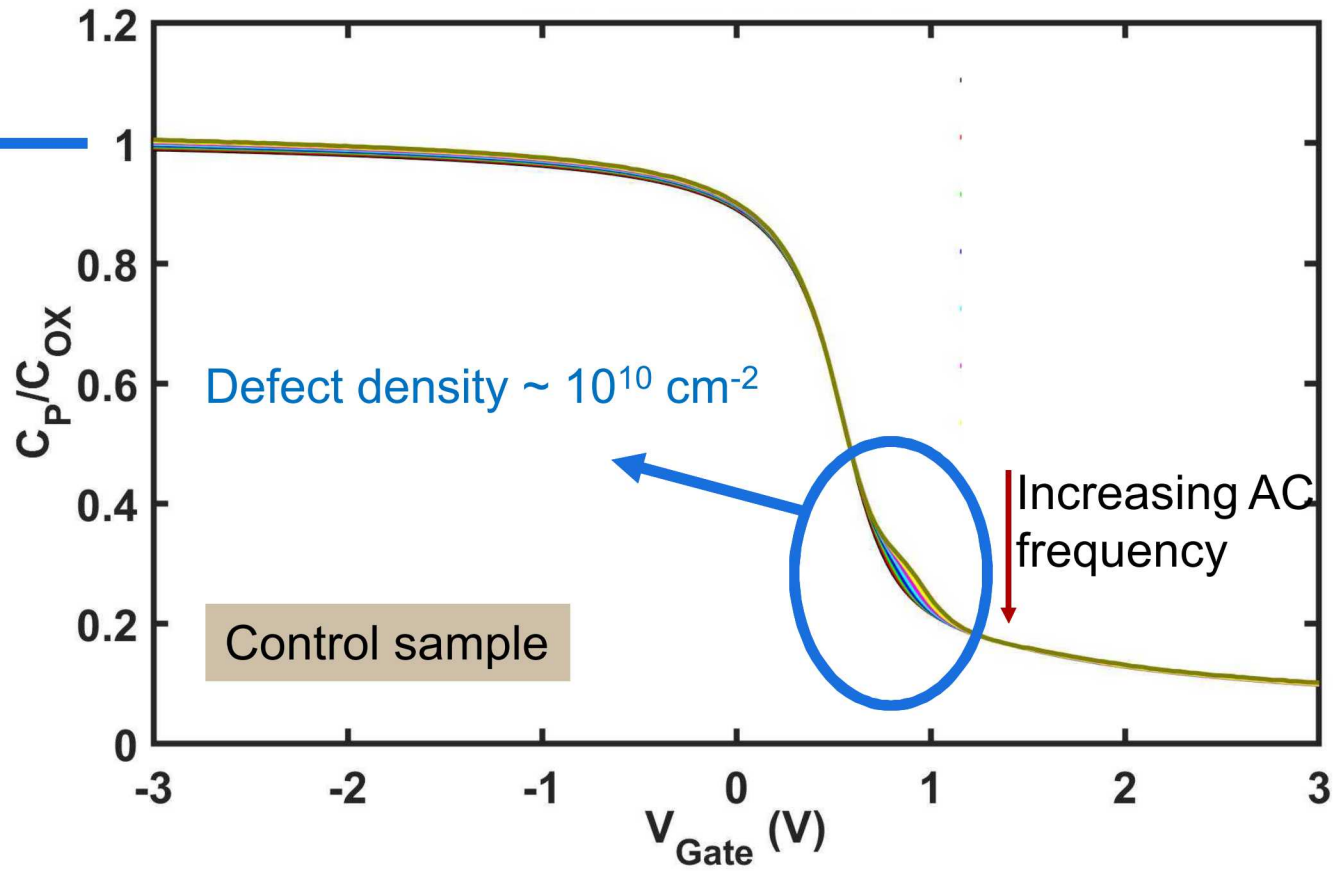
- **C-V characteristics show sufficiently good interface quality <u>for exploring device ideas</u>**

Baseline low-temperature gate stack works

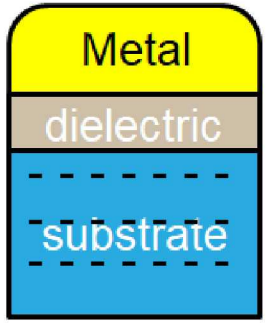
Accumulation of holes at negative gate voltages



Control p-Si substrate



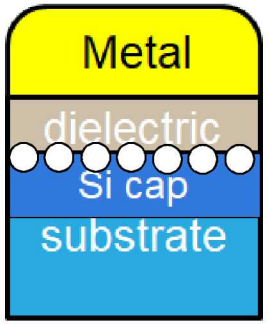
Depletion of holes at positive gate voltages

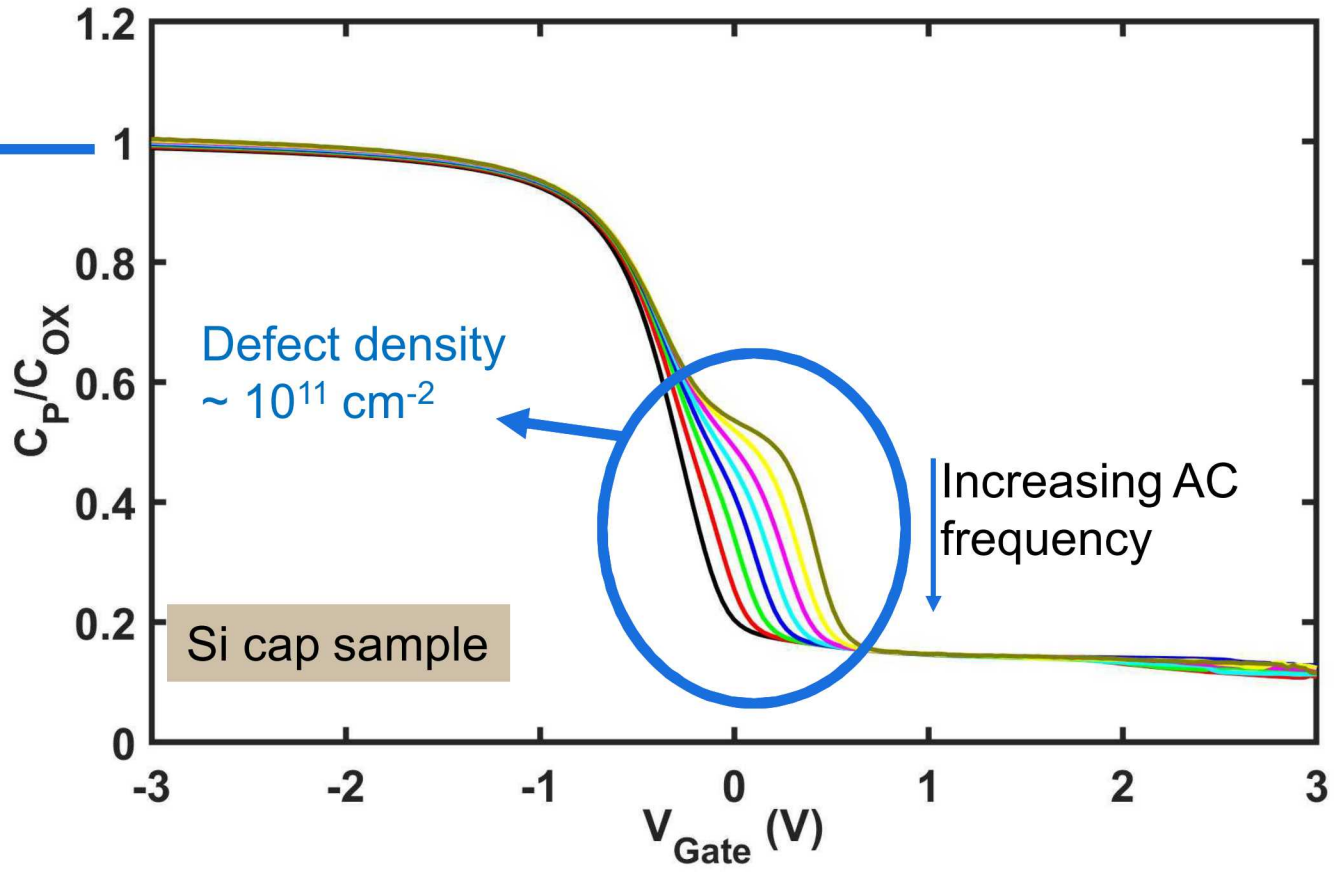


- **The low-T stack yields a high quality interface for assessing epi and interface quality.**

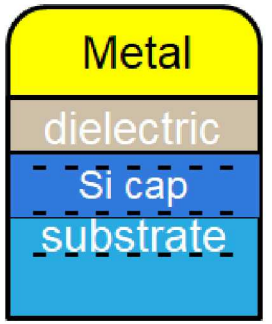
Low-T stack/APAM Si cap works

Accumulation of holes at negative gate voltages





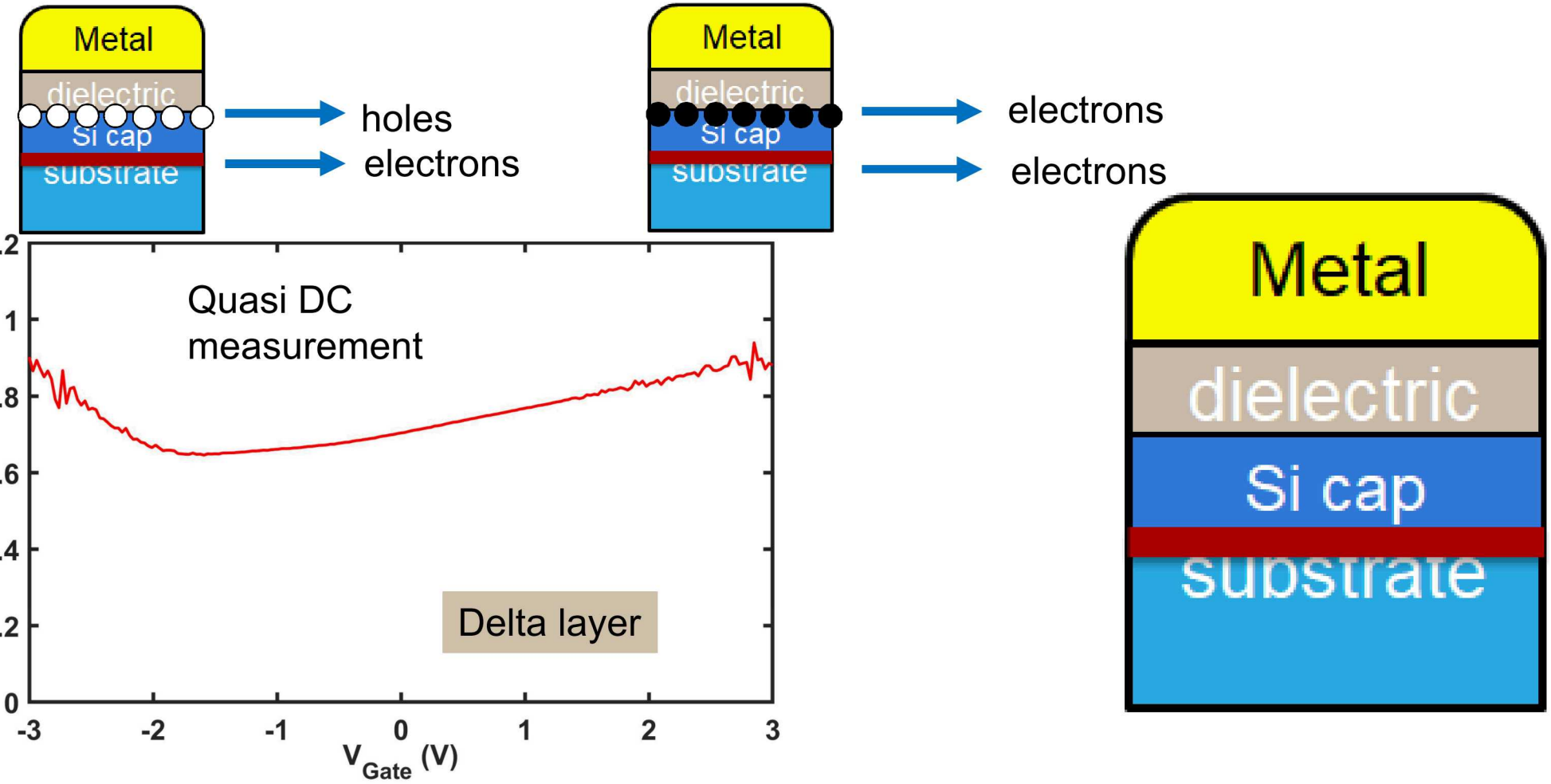
Depletion of holes at positive gate voltages



Si cap, no delta layer

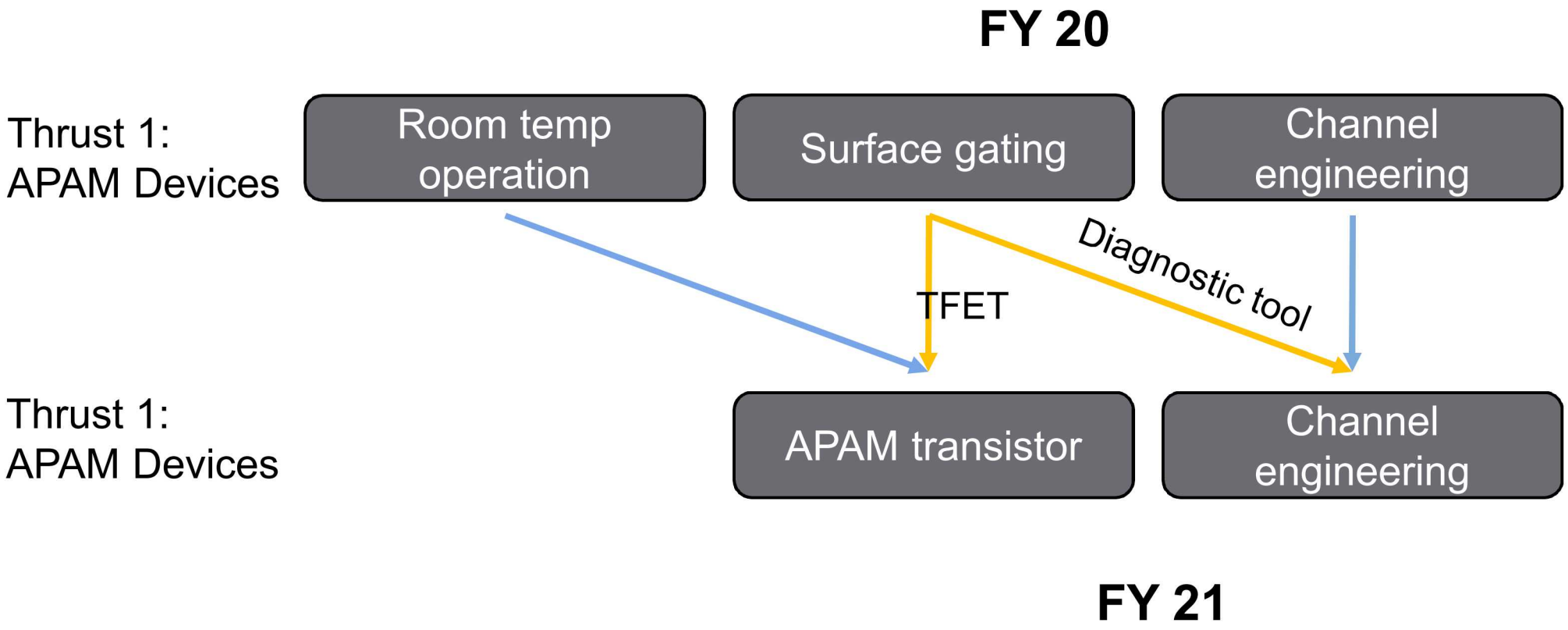
- **The dielectric/Si cap interface is of sufficient quality for exploring device ideas**

- **Vertically stacked h-e bilayers possible when gate is biased negative**



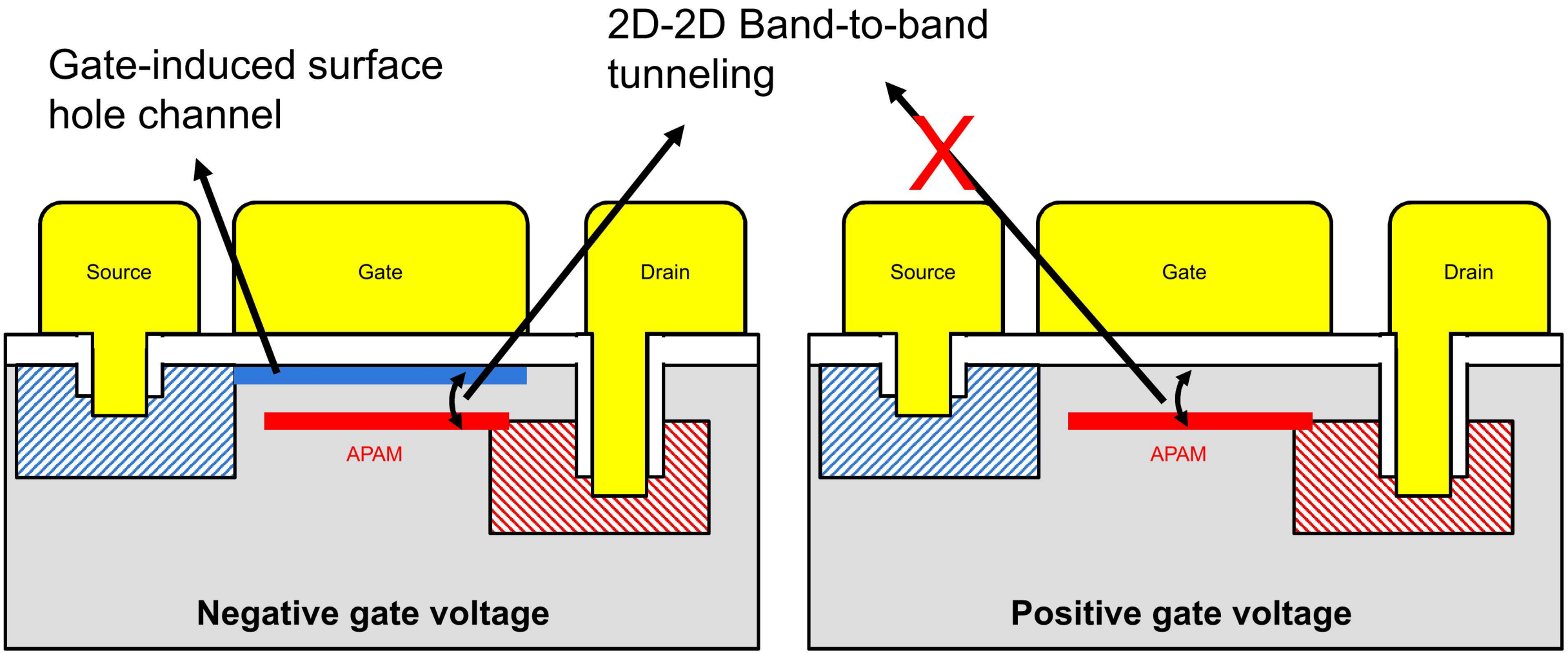
- **This stack enables the vertical tunnel FET architecture we are going to explore.**

Evolution of Surface Gating Task



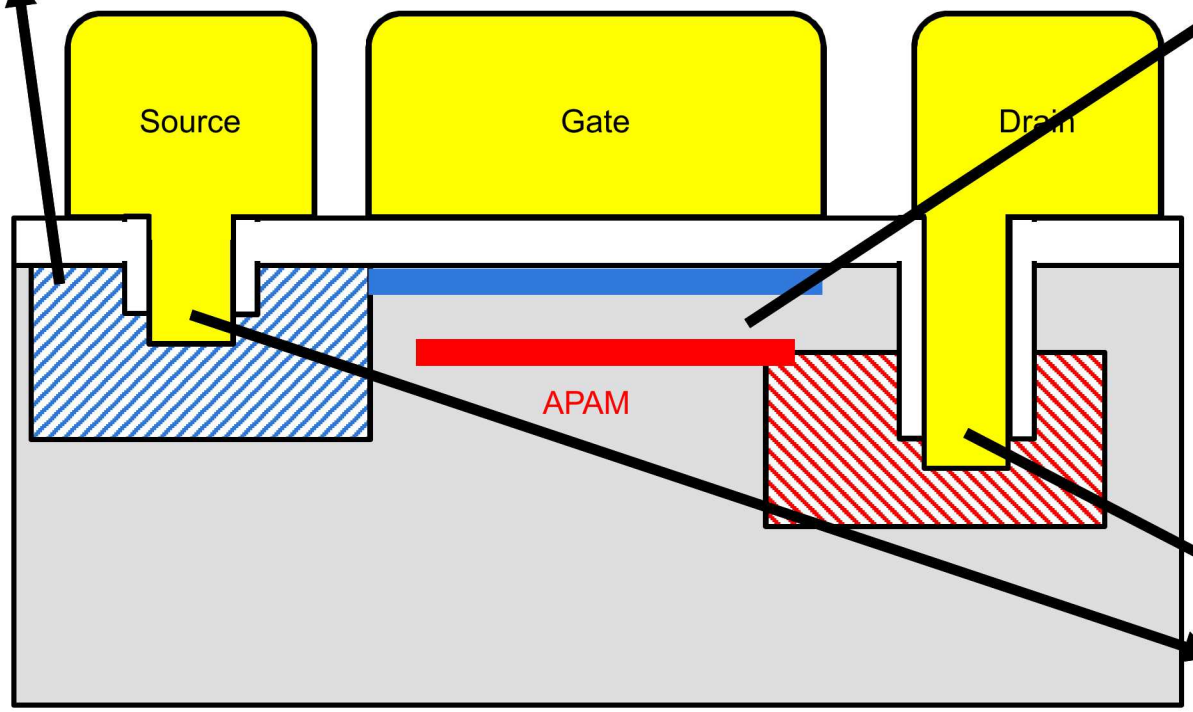
- **Surface gating is a fundamental building block for many development efforts.**

FY21 Goal: Vertical Tunnel FETs



FY21 Goal: Vertical Tunnel FETs

Low-T silicide contact:
APAM Transistor
CMOS Integration



Controlled epi thickness/quality/doping for BTB tunneling:
Channel engineering
Semiclassical transport
Quantum transport

Via process to avoid contacting substrate:
Room temp operation

- **The development of a vertical TFET requires integration of many thrust areas in the GC**

Surface gating/APAM transistor

Sandia National Laboratories

FY20 Accomplishments

- Transistor-grade gate stacks
- CV as a diagnostic tool for low-T epitaxy

FY 21 Goals

Develop silicide contact for surface hole channel

Design and model device IV curve

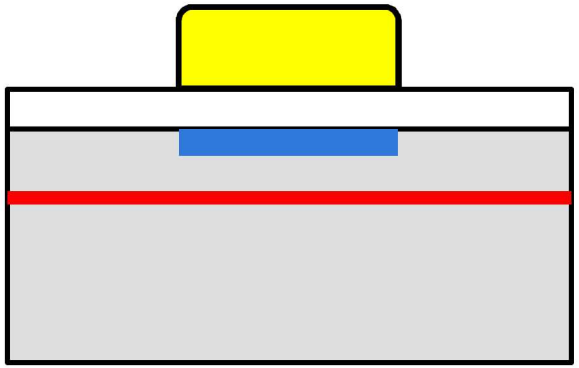
Demonstrate TFET operation

Beyond GC

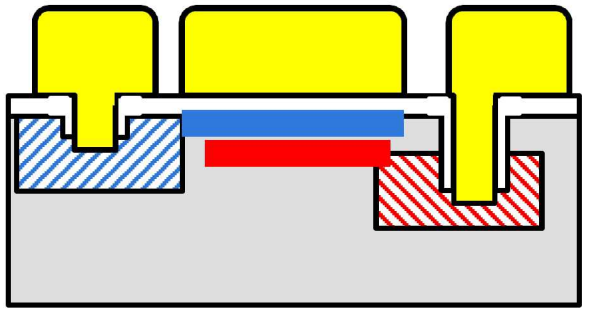
Surface gating is a fundamental building block for future APAM technology

Optimize device performance

Internal/External support to further develop the device architecture



FY 20



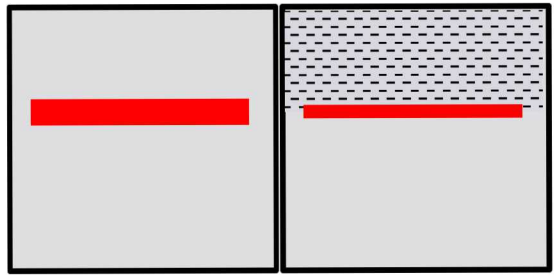
FY 21

Outline

Sandia National Laboratories

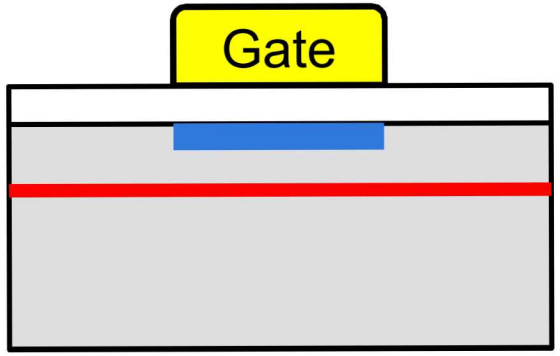
Channel Engineering

Scott Schmucker



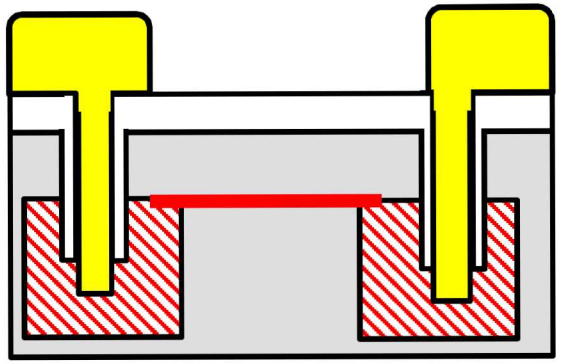
Surface gating

Tzu-Ming Lu



Room temp operation

Lisa Tracy



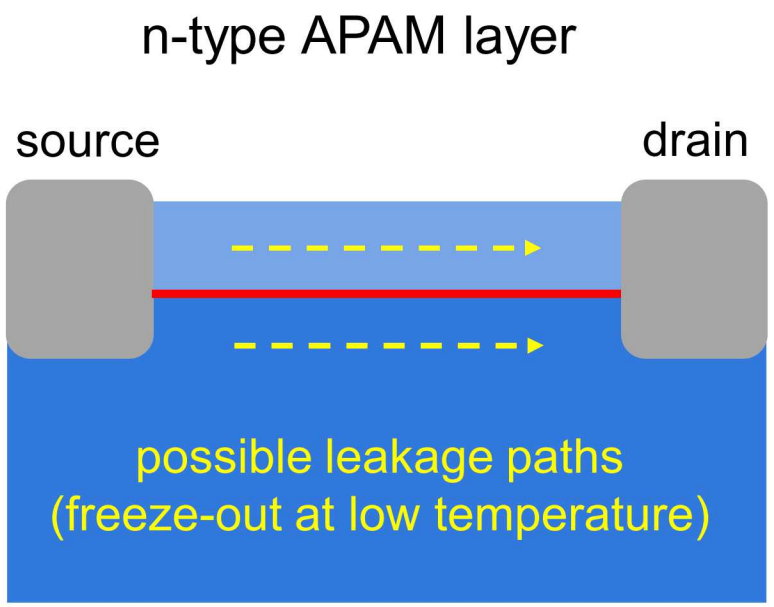
Optical fingerprint

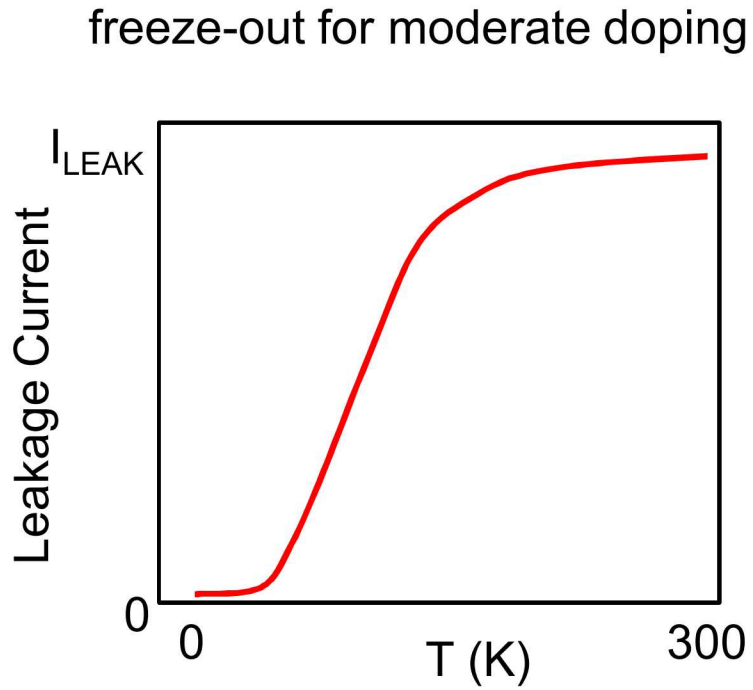
Aaron Katzenmeyer

Goal: Room Temperature Device Operation

- Existing devices operate at cryogenic temperatures
- End target: 150°C operation of APAM devices

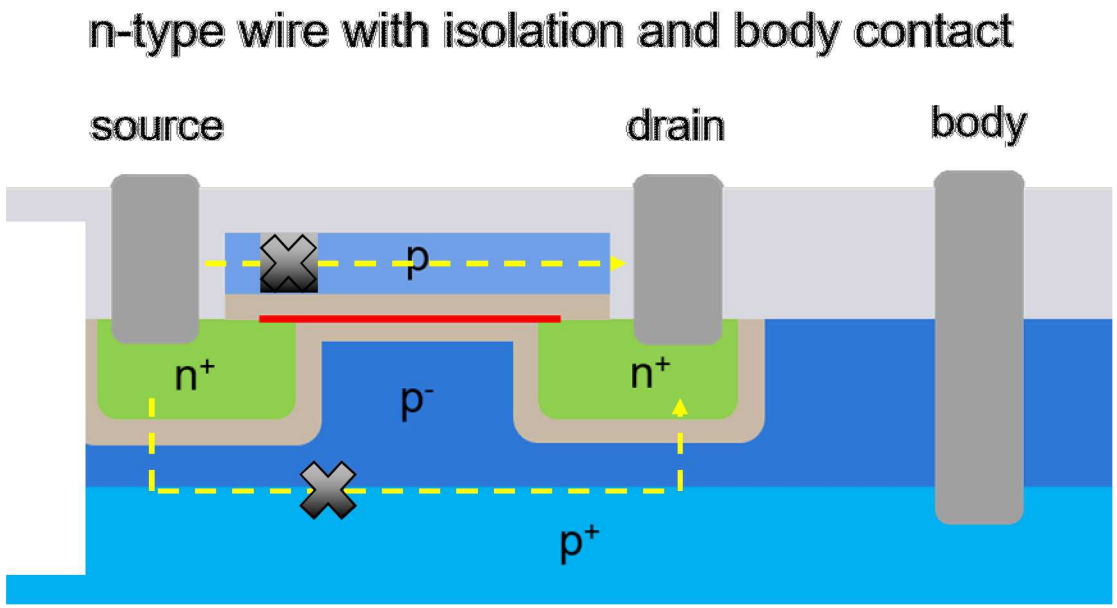
Aluminum
Silicon cap
Phosphorus
Silicon substrate





Device Isolation at Room Temperature

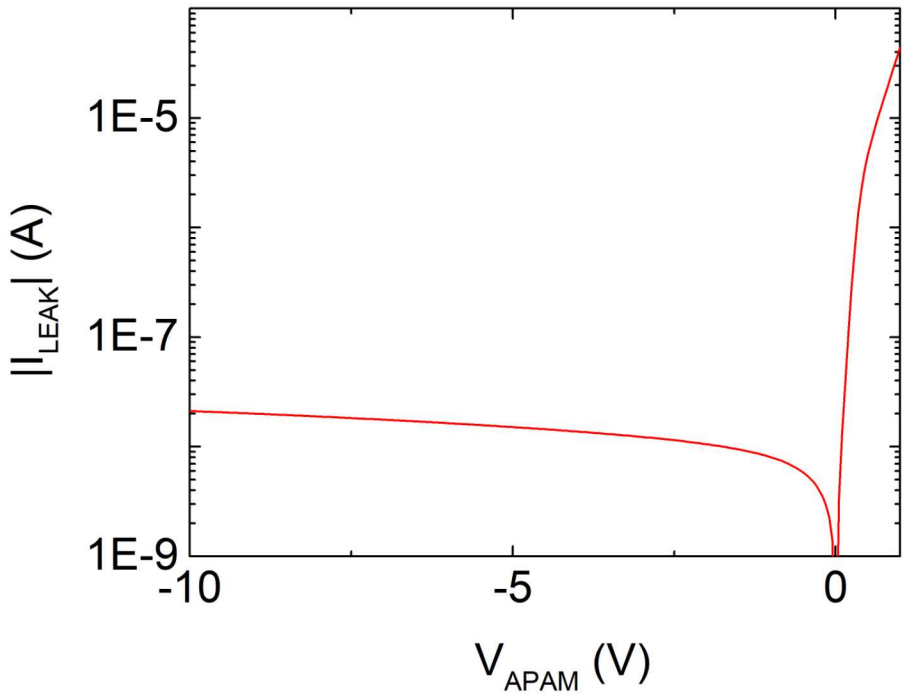
- Fabricated APAM devices with new design and process flow for isolation contacts and additional body contact
- Semi-classical modeling informed design

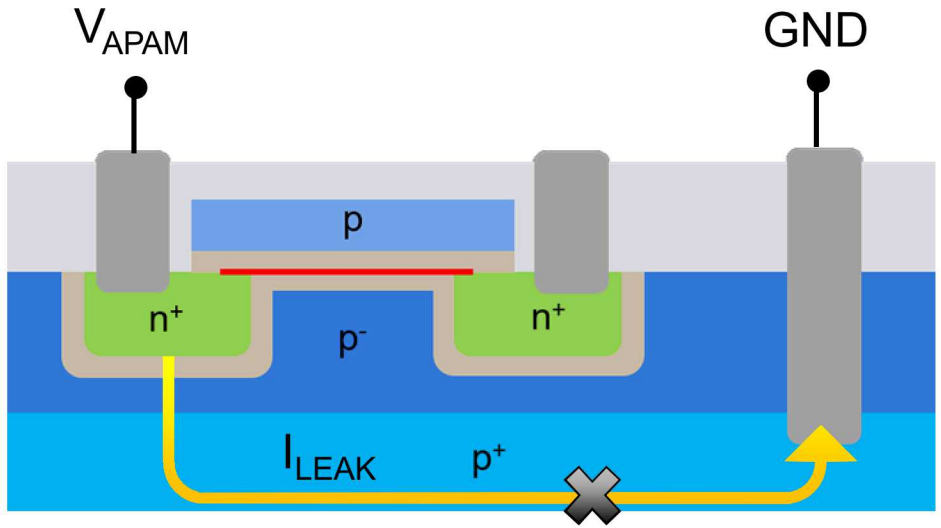


Solution for control over leakage paths

Substrate Isolation

- Room temperature leakage from APAM layer to substrate contact is low for reverse bias





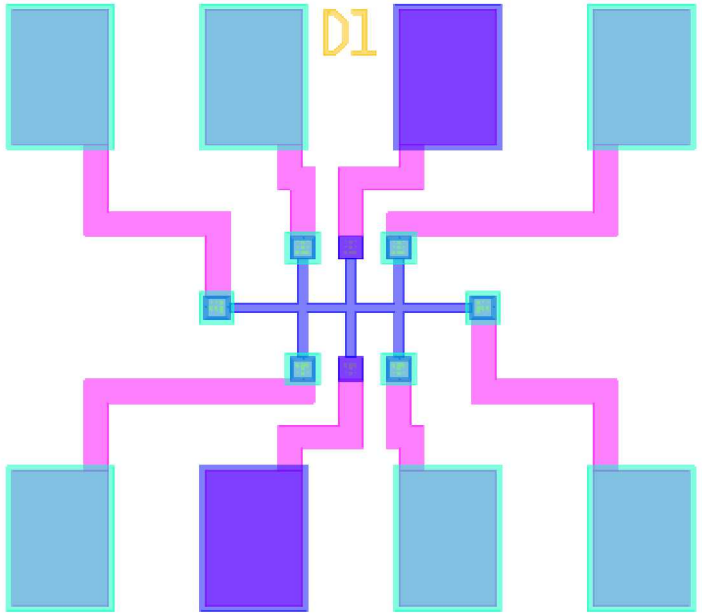
Room temperature substrate leakage now minimal

Electrical Transport Results

- Hall measurement of delta layer at room temperature

Measurement	Density (cm^{-2})	Resistivity (W/sq.)	Mobility (cm^2/Vs)
4 K Hall	9×10^{13}	570	120
RT Hall – NEW!	8.1×10^{13}	1,070	72

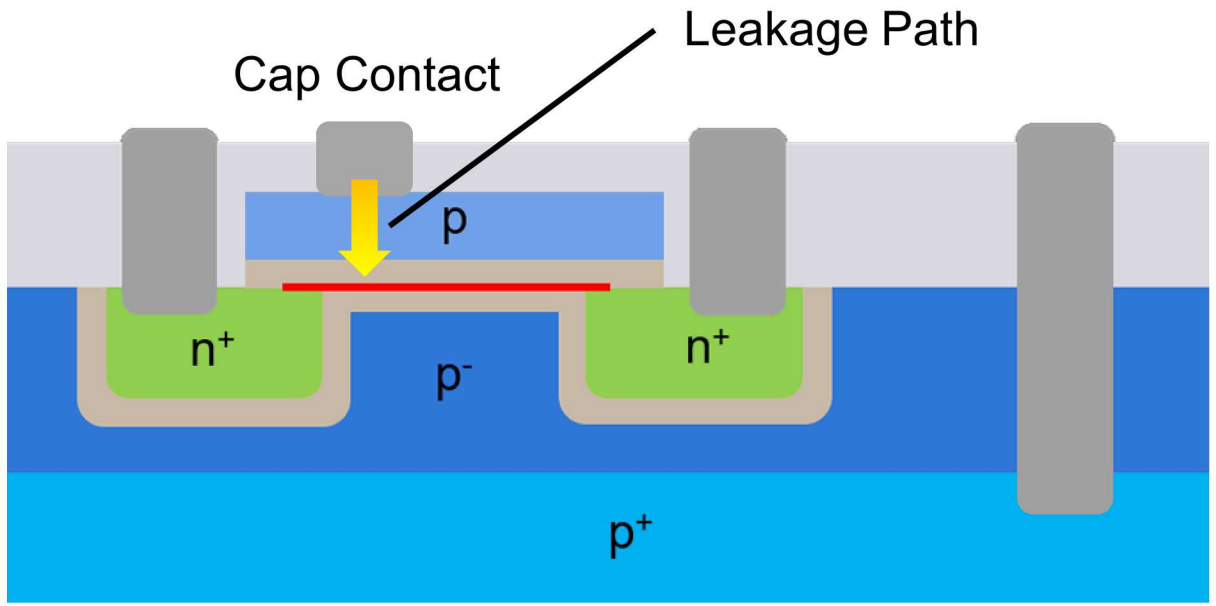
APAM layer Hall bar geometry



First Hall measurement of APAM device at RT!

Si Cap Isolation

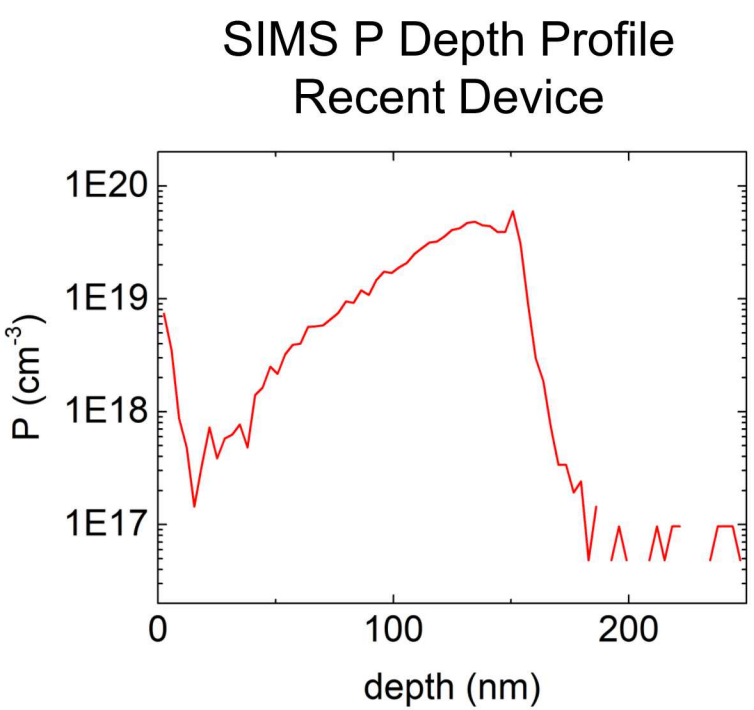
- Device design allows for “cap contact” – metal contact landing on Si cap
- Measurements show low resistance Ohmic transport between cap contact and APAM contacts

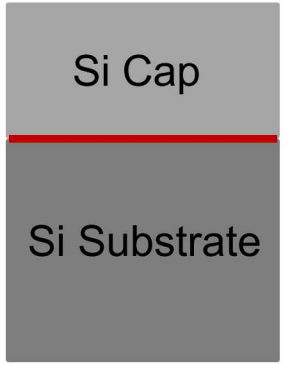


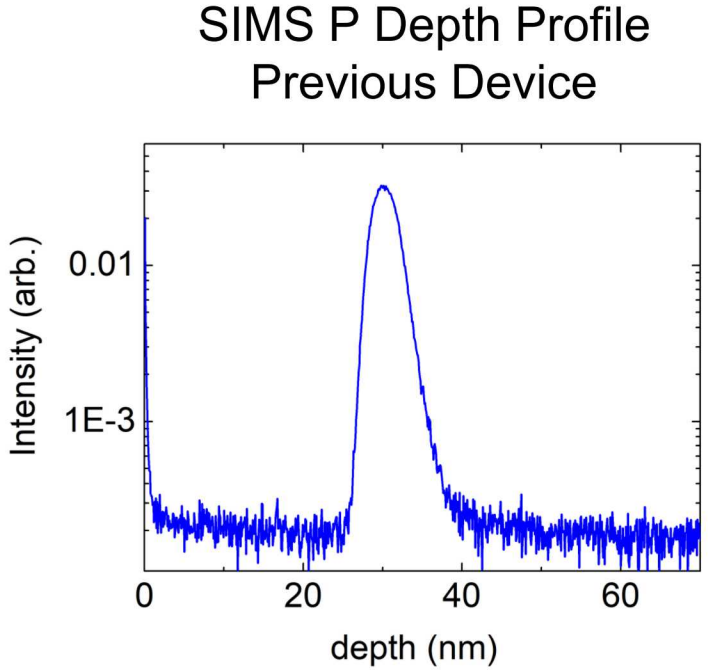
Origin of leakage path?

Cap Isolation - Solution

- APAM layer diffusion - explains leakage in cap layer
- We have previously show minimal diffusion by modifying cap growth

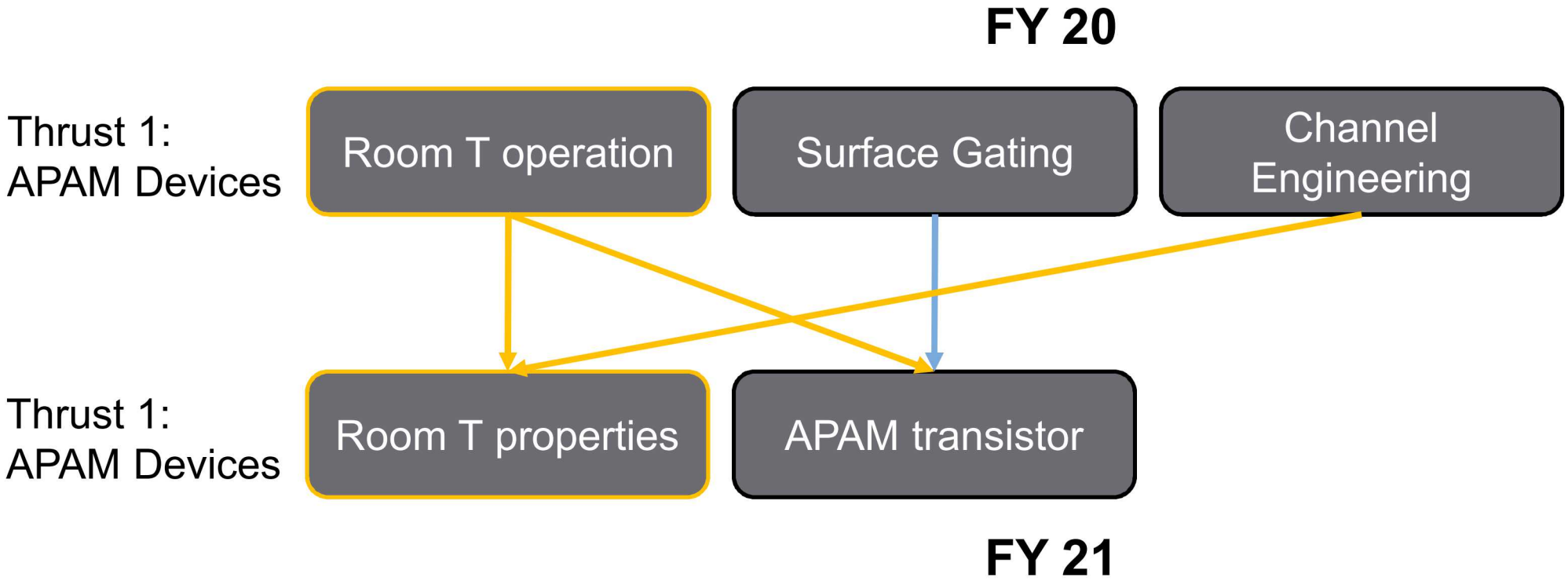






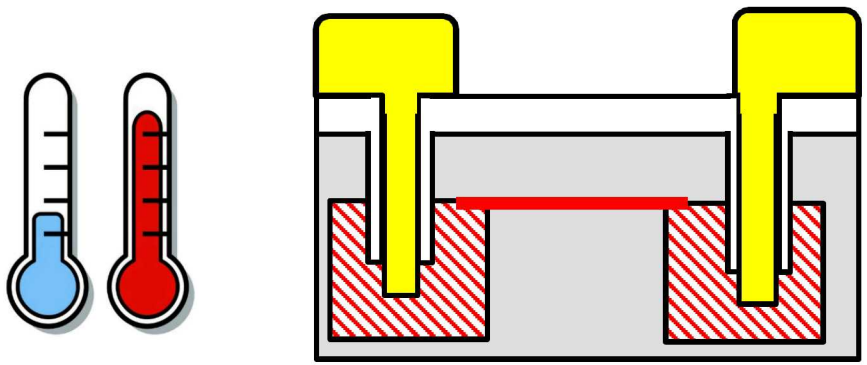
Need to re-tune process to minimize diffusion

Evolution of RT Operation Task



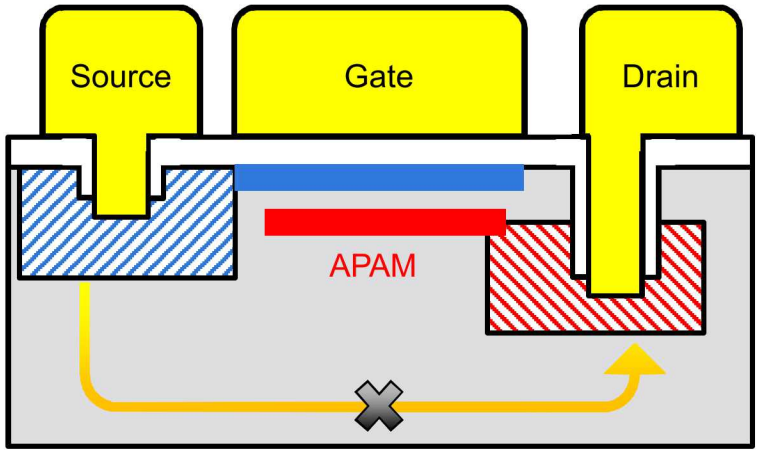
FY21 Plan – Characterize RT Properties

- Measure transport properties from 1 to 420 K.
  - Team with robustness task – test up to 300 C
- Characterize gating of room temperature device in transport (Hall)
- Investigate limitations on current density at elevated temperatures
- Use modeling to interpret results

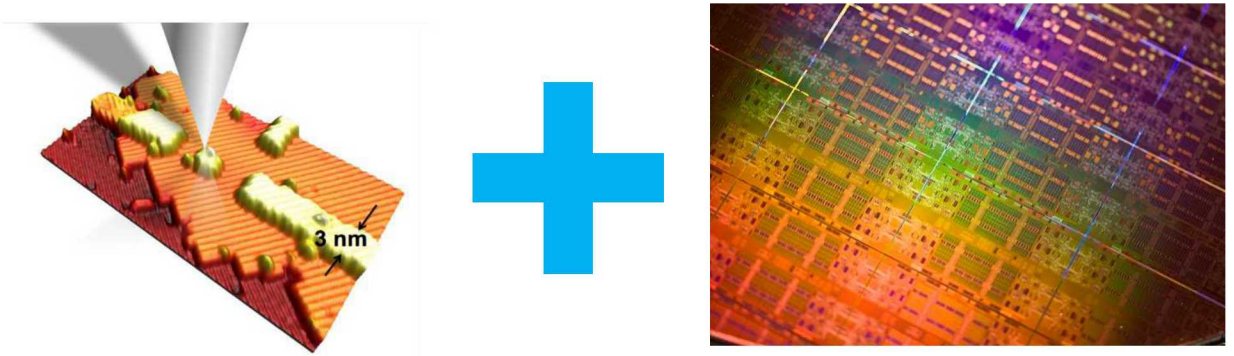


Impact

Capstone goal #1: APAM transistor



Capstone goal #2: APAM-CMOS integration



- **Understanding of APAM properties at RT (and above) provides foundation for capstone goals**
- **Opens new opportunities for Robustness Task – Failure analysis during device operation**

Room temperature operation

Sandia National Laboratories

FY20 Accomplishments

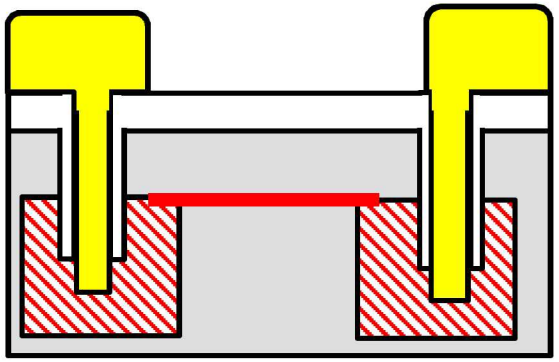
- Isolation of APAM layer from substrate
- Room temperature Hall measurement

FY 21 Goals

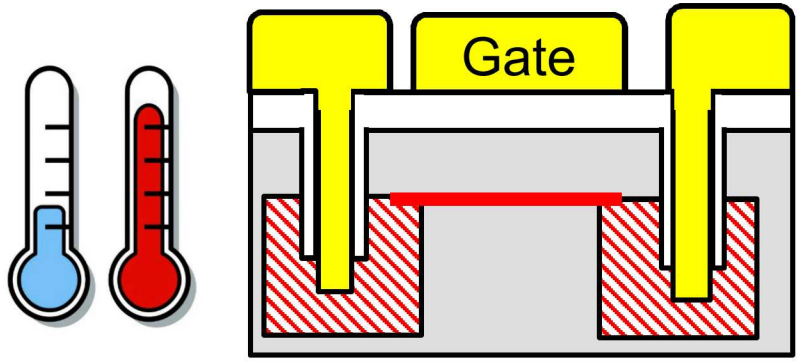
Measure transport properties from 1 to 420 K.

Beyond GC

Failure analysis during device operation



FY 20



FY 21

Outline

Sandia National Laboratories

Channel Engineering

Scott Schmucker

Surface gating

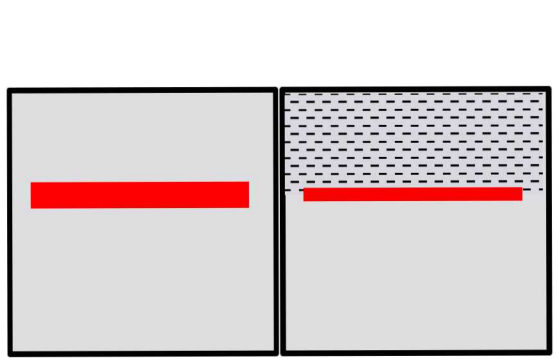
Tzu-Ming Lu

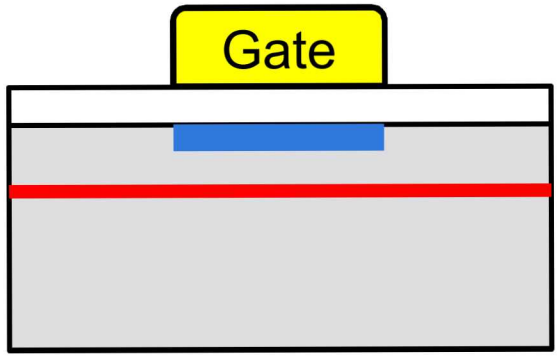
Room temp operation

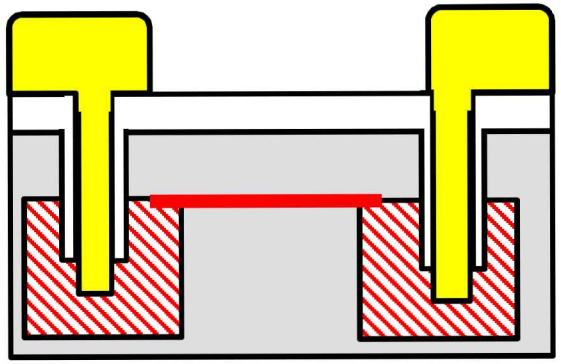
Lisa Tracy

Optical fingerprint

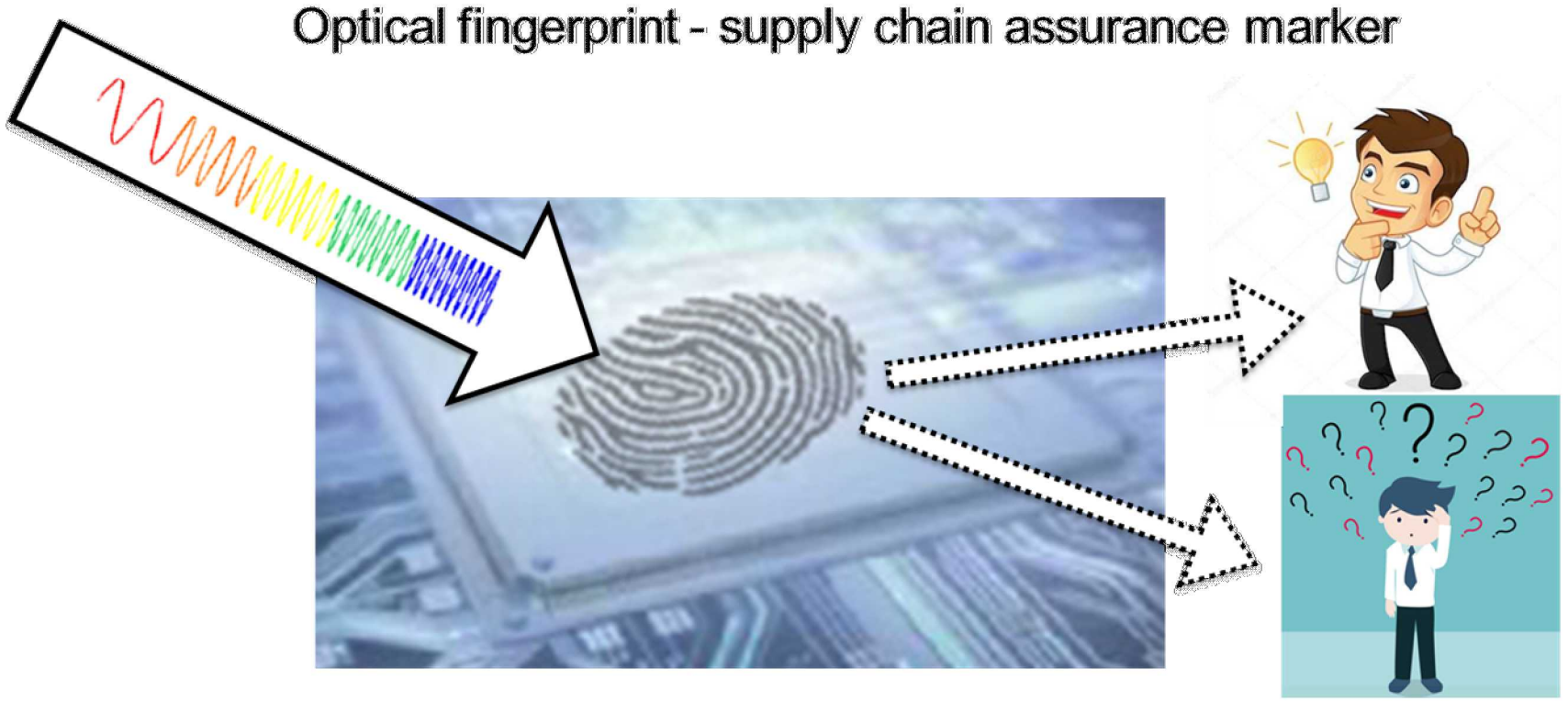
Aaron Katzenmeyer







APAM Photonics - Fingerprint

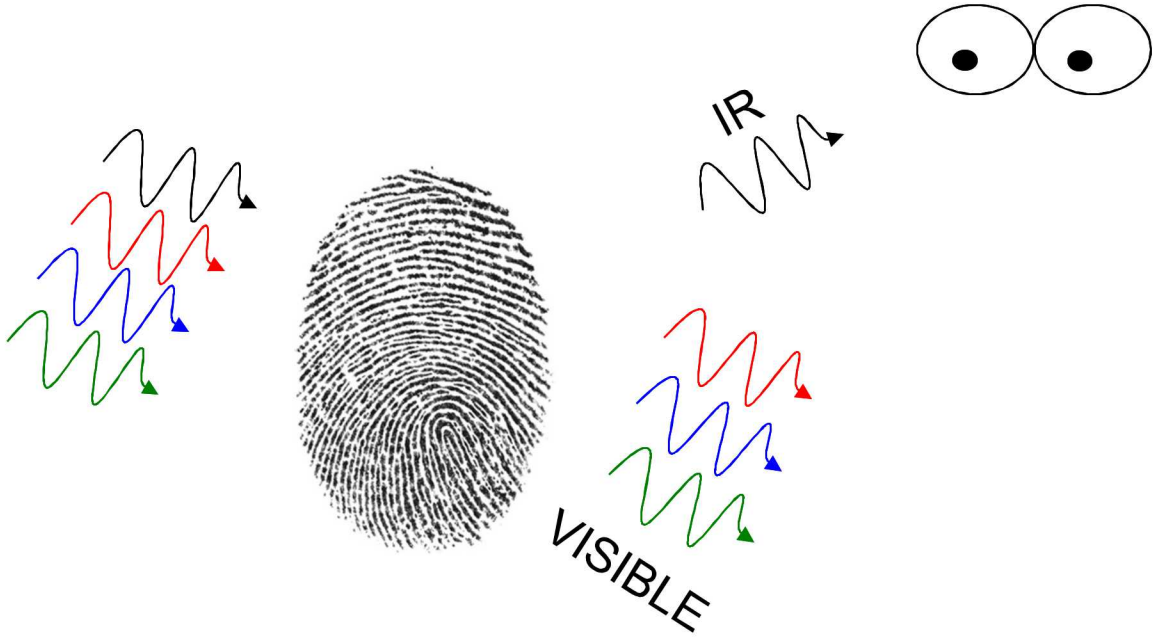


Challenge – Fingerprint

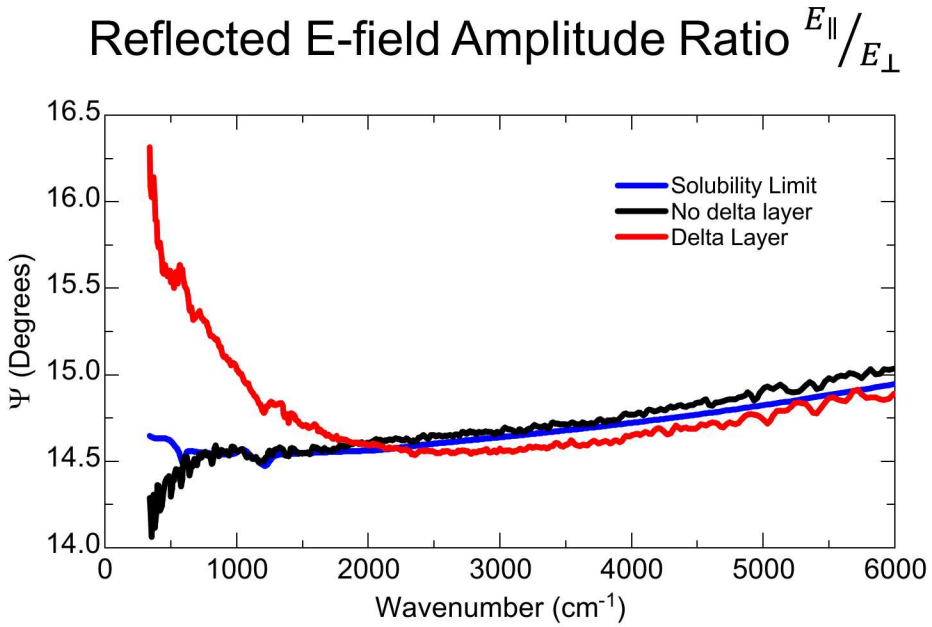
Engineer a patterned delta-layer (metasurface) for device identification

Need to know where, what to look for

- ***Wavelength***
- ***Polarization***
- ***Angle of Incidence***
- ***Phase***



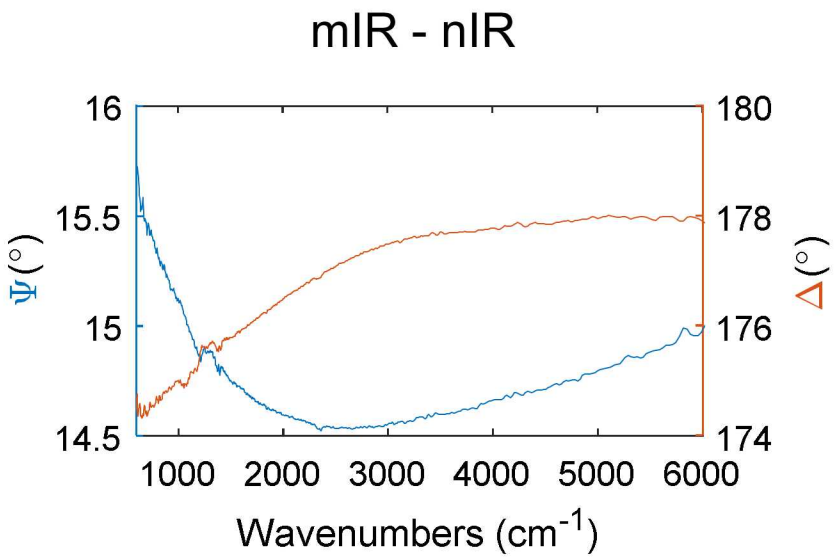
δ-layer optical response

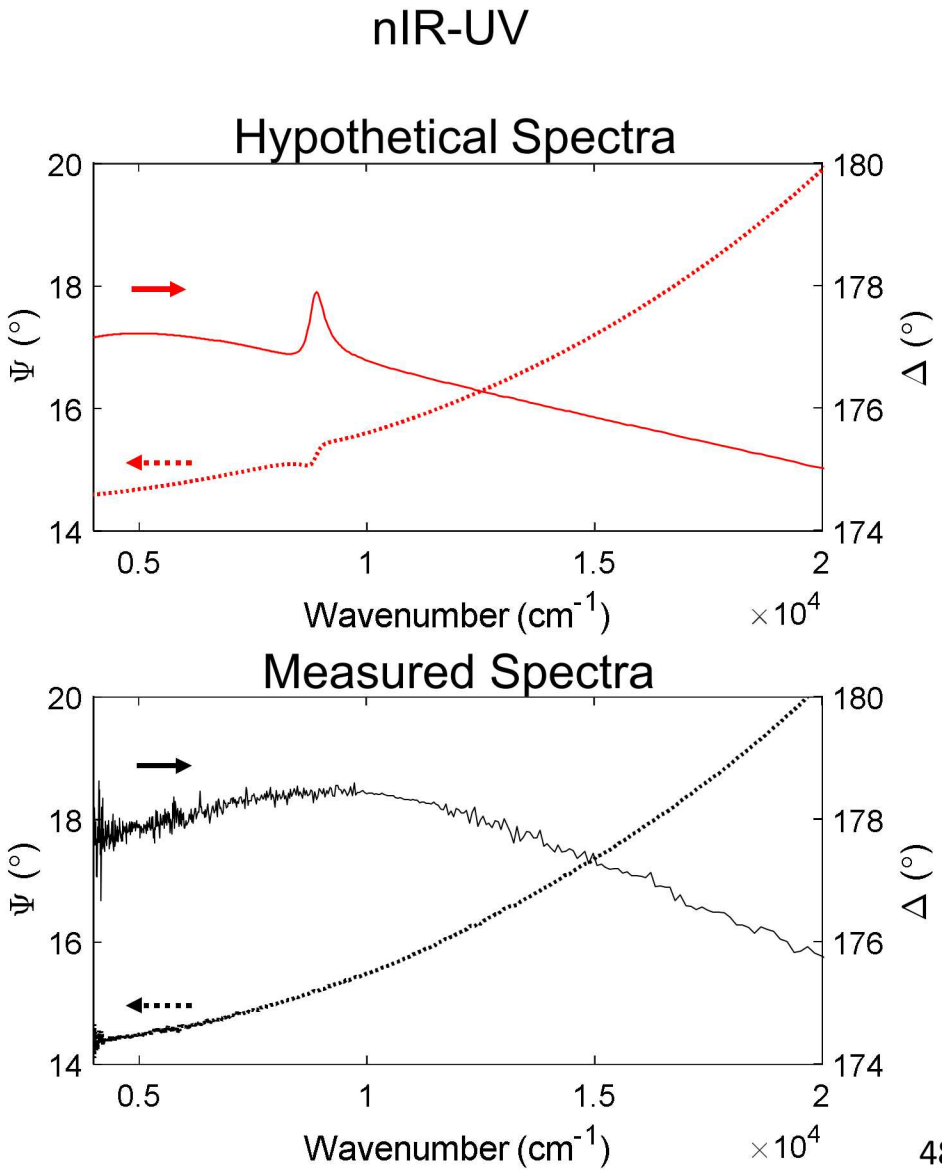


Atomically thin layer has notable mIR response

Where is the plasma resonance?

State-of-the-art design relies on epsilon near-zero





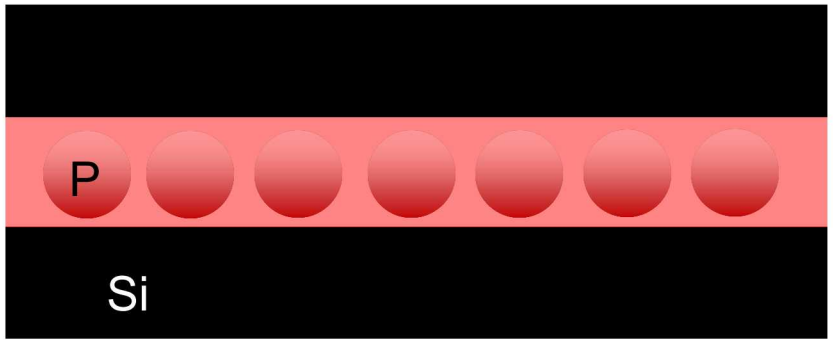
"**Assessing atomically-thin delta-doping of silicon using mid-IR ellipsometry**,"

A. Katzenmeyer, T.S. Luk, E. Bussmann, S. Young, E. Anderson, M. Marshall, J. Ohlhausen, P. Kotula, P. Lu, D. Campbell, T.-M. Lu, P. Liu, D. Ward, S. Misra, *Journal of Materials Research* (accepted, DOI: 10.1557/jmr.2020.155)

The plasma resonance is…absent!

New material, new model

- Drude model appears incomplete
- Not a III-V 2DEG!
- Derive delta-layer permittivity from scratch
  - Two-dimensional, anisotropic



The future of APAM photonics relies on more accurate permittivity

Summary

Sandia National Laboratories

FY20 Accomplishments

- First optical measurement of single delta-layer
- ID a new science problem – dielectric response of 2D disordered alloy

No-Go

No clear way to design a unique optical marker

Electrical fingerprint more desirable for customers

Beyond GC

New description of permittivity will guide photonic applications