Gate Drive Technology Evaluation and Development to Maximize Switching Speed of SiC Discrete Devices and Power Modules in Hard Switching Applications

Handong Gui, *Student Member, IEEE*, Zheyu Zhang, *Senior Member, IEEE*, Ruirui Chen, *Student Member, IEEE*, Jiahao Niu, *Student Member, IEEE*, Leon M. Tolbert, *Fellow, IEEE*, Fei (Fred) Wang, *Fellow, IEEE*, Daniel Costinett, *Senior Member, IEEE*, Benjamin J. Blalock, *Senior Member, IEEE*, and Benjamin B. Choi

***Abstract*- To understand the limitation of maximizing the switching speed of SiC low current discrete devices and high current power modules in hard switching applications, double pulse tests are conducted and the testing results are analyzed. For power modules, the switching speed is generally limited by the parasitics rather than the gate drive capability. For discrete SiC devices, the conventional voltage source gate drive (VSG) is not sufficient to maximize the switching speed even if the external gate resistance is minimized. The limitation of existing current source gate drives (CSG) are analyzed, and a CSG dedicated for SiC discrete devices is proposed, which can provide constant current during the switching transient regardless of the high Miller voltage and large internal gate resistance. Compared with the conventional VSG, the proposed CSG achieves 67% faster turn-on time and 50% turn-off time, and 68% reduction in switching loss at full load condition.**

I. Introduction

Silicon carbide (SiC) MOSFETs have shown superior characteristics such as lower conduction loss, higher switching speed, higher maximum junction temperature, and lower specific capacitance compared to Si IGBTs [1]-[3]. However, it is difficult to apply SiC MOSFETs to hard switching converters with switching frequency of hundreds of kHz and achieve high efficiency (e.g., >99%) [4]-[6], and researchers have found that SiC MOSFETs show slower switching speed compared to Si CoolMOS [7]-[9]. To design converters with high efficiency and power density, it is desired to understand whether the switching characteristics of SiC MOSFETs have been fully utilized, or if there is still potential to improve the switching speed and reduce the switching loss.

Several factors have been summarized that impact the switching speed of SiC MOSFETs such as gate drives, parasitics, loads, and thermal management systems [10], [11]. Among them, gate drives control the behavior of SiC MOSFETs and can significantly affect their switching performance. The requirements of gate drives for discrete devices and power modules can be different. Fig. 1 plots the comparison between some SiC discrete devices and power modules from different manufacturers. One critical difference between them is the current rating. Generally, power modules built with multiple SiC dies in parallel have higher current as well as higher parasitic capacitance and lower internal gate resistance compared to discrete devices with a single die. With the same gate drive technology, the switching performance of discrete devices and power modules can be different due to the above parameters difference. Therefore, to find the proper gate drive technology for SiC MOSFETs and increase the switching speed, discrete devices with low current rating and power modules with high current rating should be separately evaluated.

In terms of gate drive technology, it can be grouped into three fundamental categories: voltage source gate drives (VSGs), current source gate drives (CSGs), and resonant gate drives (RGs) [12], [13]. The advantage of the RG is its ability to reduce

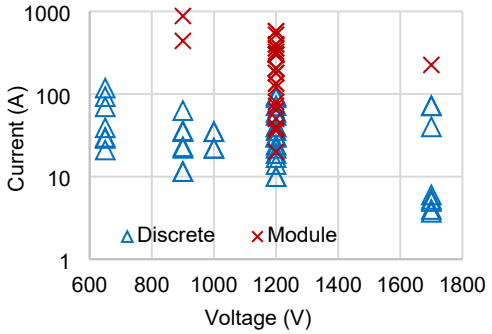


Fig. 1. Voltage and current rating of SiC discrete devices and power modules from several manufacturers.

This work was supported by The Boeing Company and NASA. This work also made use of the Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and DOE under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

H. Gui, R. Chen, J. Niu, L. M. Tolbert, F. Wang, D. Costinett, and B. J. Blalock are with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996 USA (e-mail: hgui@vols.utk.edu; rchen14@vols.utk.edu; jniu3@vols.utk.edu; tolbert@utk.edu; fred.wang@utk.edu; daniel.costinett@utk.edu; bblalock@tennessee.edu).

Z. Zhang is with the Zucker Family Graduate Education Center, Clemson University Restoration Institute, North Charleston, SC 29405 USA (e-mail: zheyu.zhang@ieee.org).

B. B. Choi is with the NASA Glenn Research Center, Cleveland, OH 44135 USA (e-mail: benjamin.b.choi@nasa.gov).

the gate drive loss [14]-[16]. However, for SiC MOSFETs in high voltage and high power applications, the gate drive loss is small compared to other losses due to their superior intrinsic gate charge characteristic, which makes RGs less attractive because of their more complicated structure.

The VSG is the most common technology for semiconductor power devices because of the simple structure and control. For SiC MOSFETs, some manufacturers provide guidance about the design of VSGs [17], [18], and researchers have proposed more advanced controls and topologies to improve the performance of VSGs, which mainly includes crosstalk and overvoltage suppression [19]-[23], current and voltage balancing [24]-[27], and dynamic gate impedance control [28]-[32]. However, it is still not clear whether the switching speed of the SiC discrete devices and power modules have been maximized with the existing VSG technology.

If the VSG is not sufficient to maximize the switching speed of SiC MOSFETs, then the CSG could be a candidate in spite of its more complex hardware circuit and control strategy. With the same gate charge, CSGs can provide constant current during switching transients and hence reduce switching time. Not much research has been conducted to develop CSGs for SiC MOSFETs, and most of them are based on linear circuits, which are difficult for applications requiring large gate current [33], [34]. More CSGs have been proposed for Si MOSFETs and Si IGBTs. In [35]-[39], CSGs with inductors are adopted for low voltage Si MOSFETs in voltage regulator applications to reduce the gate drive loss. In [40]-[44], CSGs based on voltage controlled current source with BJTs are used to adaptively tune the *dv*/*dt* and *di*/*dt* and improve the switching loss of Si IGBTs. Nevertheless, these CSGs are not designed for SiC MOSFETs. Compared to Si MOSFETs and Si IGBTs, there are some unique characteristics of SiC MOSFETs like lower gate source voltage rating, lower transconductance, and higher internal gate resistance. Therefore, existing CSGs may not be suitable for SiC MOSFETs.

Based on the above review and analysis, the main focus and contributions of this paper are: 1) identifying whether existing gate drive technologies are sufficient for maximizing the switching speed of low current discrete devices and high current power modules respectively with double pulse tests, 2) analyzing the limiting factors of existing VSGs and CSGs and summarizing the requirements for gate drives to maximize the switching speed of SiC MOSFETs, and 3) proposing a CSG that can enhance the gate current, overcome the intrinsic deficiencies of SiC discrete device like high Miller voltage and large internal gate resistance, and reduce the switching time and loss.

This paper is organized as follows. Section II presents the switching characterization for SiC discrete devices and power modules. Based on the testing results, Section III analyzes the requirements of the gate drive for discrete devices and power modules, respectively. Section IV demonstrates the design and benefits of the proposed CSG for discrete devices. Section V gives the experimental results of the proposed CSG, and Section VI provides a conclusion.

II. Switching Testing for Discrete Devices and Power Modules

A. Typical Switching Transient Analysis

A typical phase-leg configuration and the switching transient waveforms with two MOSFETs as well as its parasitics are plotted in Fig. 2. Theoretically, there is no speed limitation for a MOSFET as long as the gate drive can provide enough gate current. However, in reality, the parasitics have significant impact on the switching transient of the switch and limit the switching speed.

First, MOSFETs have internal gate resistance that is intrinsic to the device. With the traditional VSG, the maximum gate current is limited since the gate voltage cannot exceed the maximum value, namely around 20 V for SiC MOSFETs. As shown in Fig. 2, the gate current charging the lower side MOSFET's input capacitance equals to $(V_{dr}-v_{gs\_L})/(R_{g(int)\_L}+R_{g(ext)\_L})$, where V_{dr} is the amplitude of the gate drive output voltage, $R_{g(int)\_L}$ and $R_{g(ext)\_L}$ are internal and external gate resistance. Larger internal gate resistance results in lower gate current, which further decreases as the gate voltage rises. Therefore, switches with larger internal gate resistance are harder to improve the switching speed with the same gate drive technology.

Furthermore, the *di*/*dt* and *dv*/*dt* of the MOSFET during a switching transient increase when the switching speed increases. As a result, the overvoltage across the switch increases due to the influence of the output capacitance and the loop inductance [45], [46]. With multiple dies in parallel, power modules with higher current rating have higher *di*/*dt* than discrete devices if the gate drives have enough driving capability. On the other hand, if the applied DC bus voltage is the same, the *dv*/*dt* of the power module and the discrete device is similar because of the net effect between the reduced gate resistance and the increased transfer capacitance. Therefore, it is more difficult for the power module with higher power rating to increase the switching speed because of the higher *di*/*dt*.

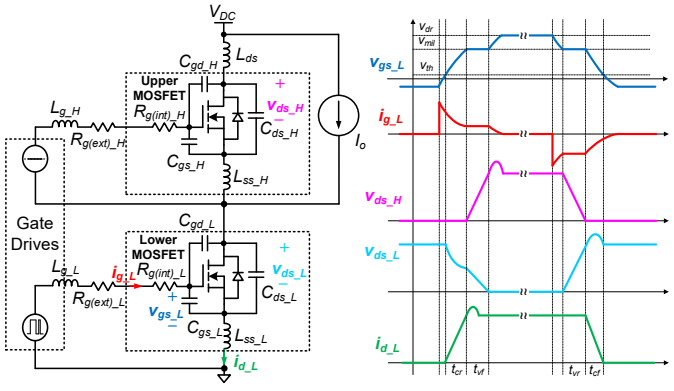


Fig. 2. Phase-leg configuration and switching transient waveforms including switches and circuit parasitics.

B. Testing Setup

To identify the limitations that determine the switching speed of SiC discrete devices and power modules respectively, one discrete device and one power module utilizing the state-of-the-art die and packaging technology are selected to be tested, and the parameters are listed in Table I. As shown, the power module has much higher current rating as well as lower on-resistance and internal gate resistance. The classical VSG is applied, and the switching speed is increased by reducing the external gate resistance value.

Double pulse test (DPT) is a widely employed method to evaluate the switching behavior of power semiconductor devices. A DPT circuit is illustrated in Fig. 2, where V_{DC} is the applied DC bus voltage and L is the load inductor to generate load current I_o. A detailed methodology of conducting DPT for wide band-gap devices has been provided in [47] and is followed in this paper.

Fig. 3 shows the DPT boards and the testing platform developed for discrete device characterization. The drain current of the device is measured by a current shunt. The bulky DC-link capacitors are located on a dedicated board and connected with the device under test (DUT) through short wires. The tested loop inductance is 18 nH.

Fig. 4 shows the DPT boards and the testing platform developed for power module characterization. The gate drive boards are directly plugged into the terminals of the module. A dedicated DC-link capacitor board is attached to the top of the module. Because load current is high in this case, a current shunt is not used, and three Rogowski coils are attached to the bolts that connect the power pad with the DC-link capacitor board to measure the drain current. The tested loop inductance is 10 nH.

C. Testing Results and Analysis

Fig. 5 illustrates the tested switching waveforms of the discrete device at 30 A with no external gate resistance. The overvoltage of the upper MOSFET during turn-on is 106 V above the DC bus voltage (500 V) while that of the lower MOSFET during turn-off is 101 V. Since the voltage rating of the device is 1.2 kV, it means that even with the lowest external gate resistance, there is still large room to accelerate the switching speed without exceeding the breakdown voltage when operating at lower DC bus voltages.

On the other hand, it is shown in Fig. 6 that with 1.4 Ω external gate resistance, the overvoltage is much larger for the power module, namely 438 V for the upper MOSFET and 362 V for the lower MOSFET when the load current is 800 A. In such case, the drain-source voltage of the MOSFETs approaches the voltage rating (900 V). Therefore, the switching speed cannot be further increased.

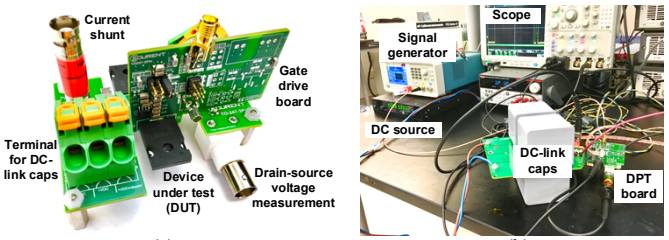


Fig. 3. DPT for discrete device. (a) DPT boards. (b) Testing platform.

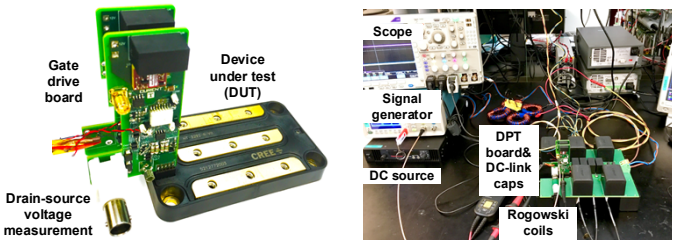


Fig. 4. DPT for power module. (a) DPT boards. (b) Testing platform.

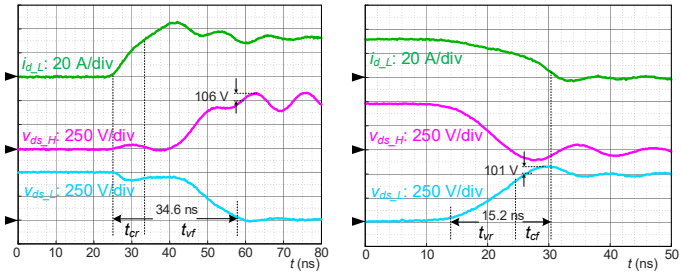


Fig. 5. Tested switching waveforms of discrete device when V_{DC}=500 V, I_o=30 A and $R_{g(ext)\_L}$=0 Ω. (a) Turn-on transient. (b) Turn-off transient.

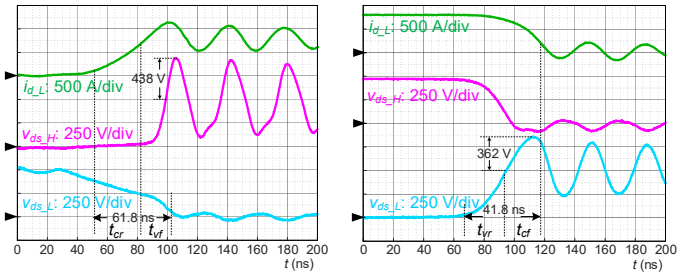


Fig. 6. Tested switching waveforms of discrete device when V_{DC}=500 V, I_o=30 A and $R_{g(ext)\_L}$=1.4 Ω. (a) Turn-on transient. (b) Turn-off transient.

Fig. 7 plots the relationship between the overvoltage during the switching transient and the applied external gate resistance of the discrete device and the power module at full load

Table I. Parameters of tested discrete device and power module.

Type	Manufacturer	Packaging	Die Tech.	Voltage	Current	$R_{ds(on)}$	$R_{g(int)}$	C_{oss} @ 500 V
Discrete	Wolfspeed	TO-247 4-pin	3rd GEN	1.2 kV	30 A	75 mΩ	10.5 Ω	2800 pF
Module	Wolfspeed	High Performance 62 mm	3rd GEN	900 V	880 A	1.25 mΩ	0.2 Ω	65 pF

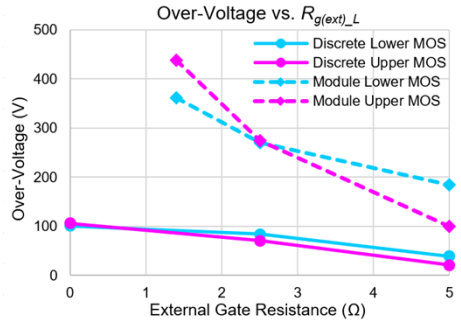


Fig. 7. Comparison of tested overvoltage between discrete device and power module.

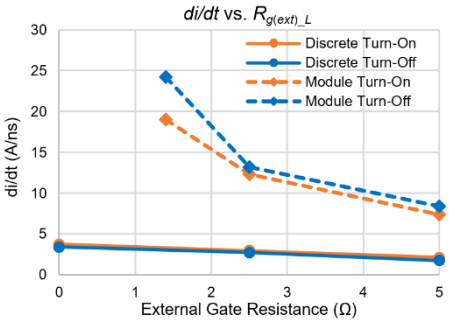


Fig. 8. Comparison of tested *di/dt* between discrete device and power module.

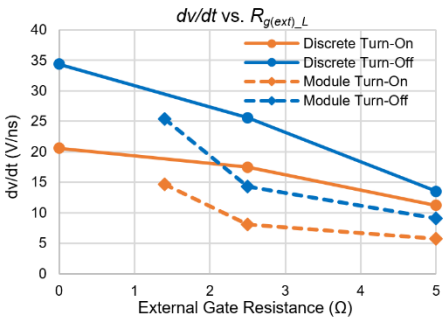


Fig. 9. Comparison of tested *dv/dt* between discrete device and power module.

condition. Clearly, the power module shows higher overvoltage for both the upper and lower MOSFETs. As the external gate resistance decreases, the overvoltage of the power module increases more rapidly, which is due to its lower internal gate resistance.

Fig. 8 and Fig. 9 illustrate *di*/*dt* and *dv*/*dt* versus the applied external gate resistance of the discrete device and the power module at full load condition. The power module exhibits a much higher *di*/*dt* that contributes to the higher overvoltage. The *dv*/*dt* of the discrete device and power module are similar, which matches with the previous analysis.

III. Analysis of Gate Drive Requirements for Discrete Devices and Power Modules

A. Discrete Devices

From the above testing results, there is still much room to increase the switching speed of the discrete device. However, since the external resistance cannot be further decreased and the supply voltage of the gate drive is difficult to increase due to the limited gate voltage rating of SiC MOSFETs, it is not likely to improve the switching speed with a conventional VSG. To develop a more effective gate drive method, it is desired to understand the inherent bottleneck of the VSG during the switching transient.

In Fig. 5, it is observed that the turn-on switching time is 34.6 ns while the turn-off switching time is 15.2 ns at full load condition. Thus, the turn-on transient is worth analyzing in detail. From Fig. 2, the overall turn-on switching time consists of current rise time and voltage fall time. After v_{gs_L} reaches V_{th}, which is the threshold voltage of the MOSFET, the lower MOSFET starts to turn on and the load current begins to commutate from the body diode of the upper MOSFET to the channel of the lower MOSFET. v_{ds_L} does not drop because the body diode of the upper MOSFET still conducts and v_{ds_L} is clamped at the bus voltage. During this process, the lower MOSFET operates in the saturation region, and the drain current can be expressed as

$$i_{d\_L} = g_m\left(v_{gs\_L}(t) - V_{th}\right) \tag{1}$$

where g_m is the transconductance of the MOSFET.

When the drain current reaches the load current I_o, the drain-source voltage of the lower MOSFET starts to drop and the Miller plateau begins. The Miller voltage is given by

$$V_{mil} = V_{th} + \frac{I_o}{g_m} \tag{2}$$

The current rise time can be calculated as

$$t_{cr} = \left(R_{g(int)\_L} + R_{g(ext)\_L}\right)C_{gs\_L}\ln\left(\frac{V_{dr} - V_{th}}{V_{dr} - V_{th} - \frac{I_o}{g_m}}\right) \tag{3}$$

During the Miller plateau, the gate current is mainly used to charge the transfer capacitance. The gate voltage does not change so the gate-source voltage keeps constant, which equals to V_{mil}. During the process, the drain-source voltage of the lower MOSFET v_{ds_L} is

$$v_{ds\_L} = V_{DC} - \frac{V_{dr} - V_{mil}}{\left(R_{g(int)\_L} + R_{g(ext)\_L}\right)C_{gd\_L}}t \tag{4}$$

The gate current during Miller plateau is expressed as

$$I_{g\_L} = \frac{V_{dr} - V_{th} - \frac{I_o}{g_m}}{R_{g(int)\_L} + R_{g(ext)\_L}} \tag{5}$$

The voltage fall time can be calculated as

$$t_{vf} = \frac{C_{gd\_L}V_{DC}}{I_{g\_L}} = \frac{\left(R_{g(int)\_L} + R_{g(ext)\_L}\right)C_{gd\_L}V_{DC}}{V_{dr} - V_{th} - \frac{I_o}{g_m}} \tag{6}$$

From the testing results demonstrated in Fig. 6(a), the voltage fall time is dominant and accounts for 3/4 of the total turn-on time. According to (6), the voltage fall time is impacted by the gate current during the Miller plateau. In (5), it is observed that the gate current is related to V_{th}, g_m and $R_{g(int)\_L}$.

Fig. 10 gives the tested transfer characteristics of a 900 V, 36 A SiC MOSFET using the state-of-the-art die technology as well as the transfer characteristics of a Si CoolMOS listed in Table II. Notably, the SiC MOSFET has much lower transconductance. It contributes to higher Miller voltage at the same load current, which is 9 V for the SiC MOSFET and 5 V for the Si CoolMOS at 30 A in Fig. 10. In addition, as mentioned above, the internal gate resistance of discrete SiC devices is usually large. Based on (5), low g_m and high $R_{g(int)\_L}$

Table II. Parameters of Si and SiC power MOSFETs.

Device	Type	Manufacturer	Packaging	Voltage	Current	$R_{g(int)}$	C_{gs}	C_{gd}
IPW90R120C3	Si	Infineon	TO-247	900 V	36 A	0.9 Ω	6.8 nF	7 pF
C3M0065090D	SiC	Wolfspeed	TO-247	900 V	36 A	4.7 Ω	1.02 nF	20 pF

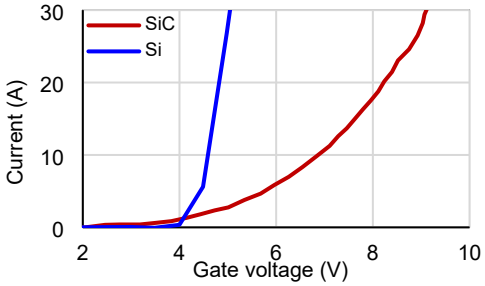


Fig. 10. Tested transfer characteristics of SiC and Si MOSFETs when v_{ds}=500 V.

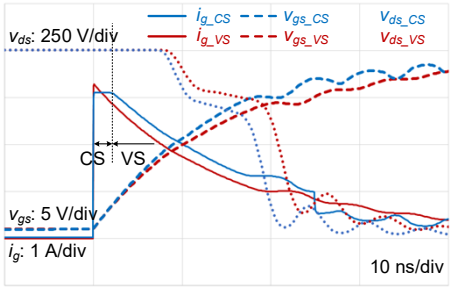


Fig. 11. Simulation waveforms of switching transient with existing CSG and VSG.

contributes to low gate current during the Miller plateau. As a consequence, the voltage across the transfer capacitance decreases slowly with this gate current even without any external gate resistance, and the voltage fall time dominates the turn-on time.

Thus according to (5), it is difficult to increase the gate current during the Miller plateau with conventional VSGs. Therefore, CSG is a better candidate because of its ability to enhance the gate current independently. With the same gate charge, CSGs can provide constant current during the switching transient and hence reduce the switching time, especially the voltage fall time.

B. *Power Modules*

From the testing results, the switching speed of the power module with high current rating is limited by the drain-source overvoltage resulting from the higher *di*/*dt* and the parasitics in the switching loop. Without further improving the layout and achieving lower parasitics, the existing VSG technology is sufficient to maximize the switching speed of power modules with large current rating.

IV. Proposed Current Source Gate Drive for Discrete Devices

A. *Limitation of Existing CSGs*

In the aforementioned analysis, the CSG should be able to provide constant current during the switching transient, especially during the voltage fall time. Nevertheless, existing CSG topologies cannot necessarily provide a constant current for discrete SiC devices with large internal gate resistance. When the gate current flows, large voltage drop occurs across the internal gate resistance. According to (2), the gate-source Miller voltage is only related to threshold voltage V_{th}, transconductance g_m and load current I_o. Thus, the gate-source voltage during the Miller plateau does not change with a CSG and is still relatively high. As a result, to keep the current constant, the external gate voltage $v_{gs(ext)}$ is likely to be higher than the gate drive supply voltage V_{dr}, and existing CSGs will lose current control when $v_{gs(ext)}$ reaches V_{dr}.

For example, a typical CSG topology in [35] is used in Saber simulation for a SiC MOSFET with 10 Ω internal gate resistance, and the result is shown in Fig. 11. The constant current ends when the external gate voltage approaches to V_{dr} and before v_{ds} starts to drop. Then the CSG becomes a classical VSG. With such a CSG, the reduction of switching time is significantly limited, which is only 2.5 ns in Fig. 11. Therefore, it is desired to develop a CSG that can keep constant gate current during the whole switching process regardless of the large internal gate resistance for discrete SiC devices.

B. *Topology and Operation Principle of Proposed CSG*

Fig. 12 shows the proposed CSG for SiC discrete devices. One P-channel MOSFET S_1, one N-channel MOSFET S_4, two bidirectional switches S_2 & S_3, and one inductor L are included in the gate drive. Note that S_1-S_4 are low voltage switches and have small footprints.

During one typical switching period, there are eight modes. The key waveforms are illustrated in Fig. 13, which include the gate signals of switches S_1- S_4, the inductor current i_L, the gate current i_g, the external and real gate-source voltage $v_{gs(ext)}$ and v_{gs}, the drain-source voltage v_{ds}, and drain current i_d. The equivalent circuit in each mode during the turn-on transient is plotted in Fig. 14, and the modes are briefly explained as follows.

1) Mode 1 (t_0-t_1): Pre-charging stage. Before t_0, only S_2 is on, and the SiC MOSFET is in the off state. At t_0, the P-channel MOSFET S_1 is turned-on so the inductor is charged by V_{dr}, and the inductor current i_L increases linearly. This mode aims to build the current required for charging the gate, and the current at t_1 is

$$I_L(t_1) = \frac{V_{dr}}{L}(t_1 - t_0) \tag{7}$$

Therefore, the initial gate current can be tuned by changing t_1 and selecting the proper inductance for L.

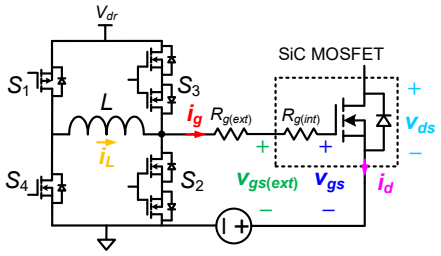


Fig. 12. Circuit of proposed CSG for discrete device.

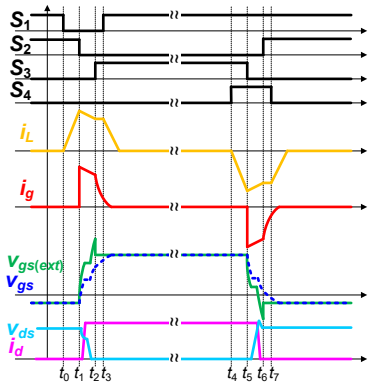


Fig. 13. Operation waveforms of proposed CSG.

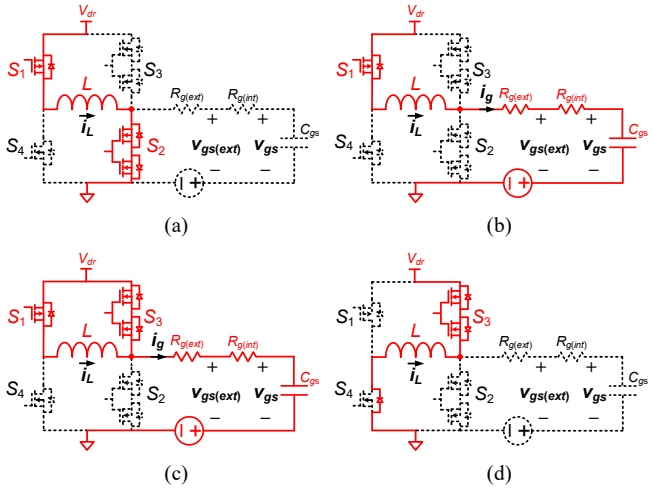


Fig. 14. Equivalent circuits in different operation modes of proposed CSG. (a) Mode 1. (b) Mode 2. (c) Mode 3. (4) Mode 4.

2) Mode 2 (t_1-t_2): Gate charging stage. At t_1, the bi-directional switch S_2 is turned off so the inductor current flows through the gate resistance and charges the gate capacitance C_{gs} of the SiC MOSFET. L, $R_{g(ext)}$, $R_{g(int)}$ and C_{gs} form an LCR resonant network. During the short time interval of this mode, the inductor current i_L does not change much so the gate can be regarded as charged by a current source. The switching transient of the SiC MOSFET completes within this mode, so the switching time, especially the voltage fall time, is reduced compared to a conventional VSG. Note that due to the internal gate resistance, the external gate voltage $v_{gs(ext)}$ is always higher than the real gate voltage v_{gs}. In order to keep the current source during this mode, the bi-directional switch S_3 should be in off state so that $v_{gs(ext)}$ can be higher than V_{dr}. If a simple N-channel MOSFET is adopted for S_3, the body diode of S_3 conducts when $v_{gs(ext)}$ approaches to V_{dr} and $v_{gs(ext)}$ is clamped. In such case, the gate drive automatically changes to be a VSG, and the gate current decreases rapidly like Fig. 11. Therefore, a bi-directional switch is necessary for keeping the current source. The relationship between external and real gate voltage is

$$v_{gs} = v_{gs(ext)} - i_g\left(R_{g(ext)} + R_{g(int)}\right) \tag{8}$$

3) Mode 3 (t_2-t_3): Free-wheeling stage. At t_2, the bi-directional switch S_3 is turned-on, and $v_{gs(ext)}$ is pulled down to be V_{dr}. Then, the gate drive turns to be a conventional voltage source, and i_g reduces until the real gate voltage reaches V_{dr}. Note that the time to turn on S_3 is critical. If t_2 is too early, the transient has not finished and the switching loss increases as i_g drops. Otherwise, if t_2 is too late, the constant current keeps charging and the gate voltage would be higher than the maximum rating, which damages the device. Therefore, the timing of turning on S_3 should be carefully selected, which is one of the challenges to implement this CSG. In this mode, i_L free-wheels through S_1 and S_3 and keeps constant. Since i_L in this mode contributes to nothing but loss, the time interval should be controlled to be as short as possible.

4) Mode 4 (t_3-t_4): Discharging stage. At t_3, the P-channel MOSFET S_1 is turned off, and i_L flows through S_3 and the body diode of S_4. The inductor is discharged by V_{dr} and i_L decreases linearly to zero, which means that the stored energy in L returns to the power supply of the gate drive without being wasted.

From t_4, the turn-off transition starts, and the operation principle is similar to the turn-on transition.

C. Parameter Design and Selection

The key components in the proposed CSG circuit are the inductor L and the external gate resistor $R_{g(ext)}$. In terms of the control, the critical parameters are the inductor charging time t_{ic} (from t_0 to t_1 in Fig. 13) and the gate charging time t_{gc} (from t_1 to t_2 in Fig. 13).

The gate charging time t_{gc} consists of two periods. From the start of the gate charging at t_1 in Fig. 13 to the end of the SiC MOSFET drain current rise, the equivalent circuit for this period is a typical RLC series tank formed by $R_{g(ext)}$, $R_{g(int)}$, L and C_{gs}. The gate current during this period can be derived as

$$\begin{aligned} i_g(t) &= I_{g0}e^{-\alpha t}\cos\left(\omega_d t\right) \\ &+\frac{1}{\omega_d L}\left(V_{dr} - \frac{R_{g(ext)}+R_{g(int)}}{2}I_{g0}\right)e^{-\alpha t}\sin\left(\omega_d t\right) \end{aligned} \tag{9}$$

where I_{g0} is the initial gate current, $\alpha = \dfrac{R_{g(ext)}+R_{g(int)}}{2L}$, $\omega_d = \omega_0\sqrt{1-\zeta^2}$, $\omega_0 = \dfrac{1}{\sqrt{LC_{gs}}}$, and $\zeta = \dfrac{R_{g(ext)}+R_{g(int)}}{2}\sqrt{\dfrac{C_{gs}}{L}}$.

When the drain current of the SiC MOSFET reaches the load current, the drain-source voltage begins to decrease. The gate voltage v_{gs} is clamped to Miller voltage V_{mil}. In this period, the circuit becomes a RL first order system, and the gate current response can be derived as

$$i_g(t) = (I_{g1} - \frac{V_{dr} - V_{mil}}{R_{g(ext)} + R_{g(int)}})e^{-2\alpha(t-t_{cr})} + \frac{V_{dr} - V_{mil}}{R_{g(ext)} + R_{g(int)}} \quad (10)$$

where I_{g1} is the gate current when the voltage starts to fall. When the drain-source voltage of the MOSFET drops to zero at t_2, the switching transient ends and the proposed CSG should be changed to VSG.

For the tested SiC MOSFET, the calculated gate currents during the switching transient with different inductance values are illustrated in Fig. 15. Higher inductance leads to lower current drop and is better from the perspective of maintaining constant current.

However, higher inductance not only results in larger size, but also makes it more difficult to build the required initial gate current during t_0 and t_1. Since the MOSFET cannot be turned on before the current reaches the required value, there is a maximum duty cycle limit for the proposed CSG. For the tested MOSFET, a 1 µH inductor LPS4012-102NRB from Coilcraft is selected in the CSG. The dual N-channel MOSFET chip SI9945BDY from Vishay is used for switches S_2 and S_3, while the N and P-channel MOSFET chip SI4559ADY from Vishay is used for switches S_1 and S_4. The implementation of the control signal is plotted in Fig. 16. The signal isolation is realized with ADuM1200 from Analog Devices Inc., while the isolated power supply is MEJ2D1215 from Murata.

D. Loss Analysis

Generally, the current-voltage overlap loss is the dominant loss for SiC MOSFETs during the hard switching transient. During the turn-on process, it can be written as

$$E_{on} = \int_0^{t_{ov}} i_d v_{ds} dt \quad (11)$$

where t_{ov} is the overlap time of drain current and drain-source voltage. During the turn-on transient, it equals to the sum of current rise time t_{cr} and voltage fall time t_{vf} as shown in Fig. 2.

Assuming the current and voltage during the switching transient change linearly, (9) can be expressed as

$$E_{on} = \frac{1}{2} I_o V_{DC} (t_{cr} + t_{vf}) \quad (12)$$

where I_o is the load current and V_{DC} is the DC bus voltage. For the conventional VSG, t_{cr} and t_{vf} can be calculated by (3) and (6) respectively.

Assuming the gate current is constant, the current rise time of the proposed CSG is

$$t_{cr(CSG)} = C_{gs} \frac{I_o}{g_m I_g} \quad (13)$$

The voltage fall time can be expressed as

$$t_{vf(CSG)} = C_{gd} \frac{V_{DC}}{I_g} \quad (14)$$

Based on the above analysis, the turn-on time of a typical 1.2 kV, 30 A SiC MOSFET with 10.5 Ω internal gate resistance is plotted in Fig. 17. With the same initial gate current, it is observed that the voltage fall time with the proposed CSG decreases significantly compared to the conventional VSG. The total overlap time can be reduced by half, leading to significant switching loss reduction.

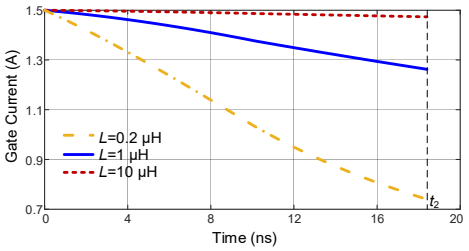


Fig. 15. Calculated gate current with different inductances.

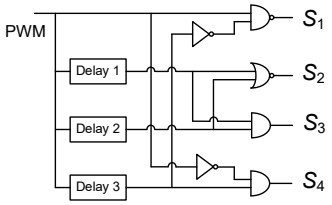


Fig. 16. Control logic implementation for CSG.

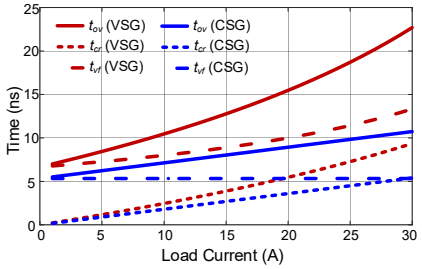


Fig. 17. Turn-on time comparison between VSG and CSG under different load.

For the conventional VSG, the gate drive loss of each switching cycle is

$$E_{g(VSG)} = V_{dr} Q_g \quad (15)$$

where Q_g is the gate charge.

The gate drive loss of the proposed CSG is derived as

$$E_{g(CSG)} = \frac{1}{2} V_{dr} Q_g + (R_{g(ext)} + R_{g(int)}) I_g Q_g + E_c \quad (16)$$

where E_c is the energy loss of the driving circuit, which mainly includes the conduction and switching loss of the switches, and the inductor loss. Based on the switch datasheet, the on-resistance of each switch is around 0.1 Ω, and the switching time is around 10 ns. Assuming the gate current is 1.5 A and the total I-V overlap time of the SiC MOSFET during one switching cycle is 25 ns, the conduction loss and switching loss of the switches is 0.01 µJ and 0.27 µJ, respectively. According to the datasheet of the inductor, the loss during one switching cycle is 0.003 µJ.

With the same SiC MOSFET as in Fig. 17, the relationship between gate drive loss during one switching cycle and external gate resistance $R_{g(ext)}$ is plotted in Fig. 18. Due to the large internal gate resistance, the proposed CSG shows higher gate drive loss than the conventional VSG. However, because of the

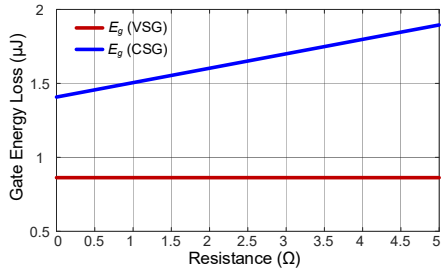


Fig. 18. Gate drive loss comparison between VSG and CSG with different external gate resistance.

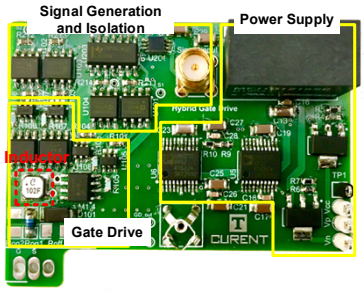


Fig. 19. Prototype of proposed CSG.

superior intrinsic gate charge characteristic of SiC MOSFETs, the gate drive loss is much lower than the switching loss. So the higher gate drive loss of the proposed CSG does not impact the overall loss reduction.

E. Benefits and Challenges of Proposed Gate Drive

Benefits: 1) The current source keeps the gate current at relatively high level during the switching transient. It shortens the long voltage fall/ rise time caused by the small transconductance and high Miller voltage of the SiC MOSFET with conventional VSG. As a result, the switching loss is significantly reduced.

2) The utilization of bi-directional switches enables constant current source during the whole switching transient and is suitable for the discrete SiC MOSFET with large internal gate resistance.

3) The gate current can be tuned by changing the pre-charging time. It provides the potential for more flexible and intelligent control strategies like di/dt and dv/dt control to better utilize and protect the SiC MOSFET.

4) The control of the switches turns the gate drive from current source to voltage source after the switching transient of the SiC MOSFET. The inductor and gate current keep at zero in steady state to eliminate circulating current and extra loss.

5) The stored energy in the inductor can return to the source of the gate drive after the switching transient, which avoids increasing the gate drive loss.

Challenges: 1) The introduction of the bi-directional switches disables the automatic change from CSG to VSG after the switching transient. Thus, the proposed CSG requires accurate time control to turn it to be VSG so that the gate is not overcharged / discharged at different DC bus voltage and load conditions.

2) With the increased dv/dt, the overvoltage and cross-talk of the MOSFET during a switching transient increases. In addition, higher dv/dt can lead to higher noise and deteriorate the EMC performance. Therefore, the trade-off between switching speed, device reliability and noise should be balanced for real applications.

V. Experimental Results and Discussion

The SiC MOSFET C3M0075120K (1.2 kV, 30 A) from Wolfspeed is selected to test the proposed CSG. A conventional VSG is also tested with the same SiC MOSFET for comparison. The internal gate resistance of the MOSFET is 10.5 Ω. To make a fair comparison, the power supply of both gate drives is +15/-4 V. Zero external gate resistance is applied for the conventional VSG, and the gate current of the proposed CSG is set to be 1.4 A so that both gate drives have similar initial gate current.

Fig. 19 demonstrates the picture of the proposed CSG. It can be seen that the inductor is small and does not impact the size of the gate drive. A DPT is implemented to evaluate the switching performance of both gate drives, and a similar platform is adopted as shown in Fig. 3(b).

The tested gate-source voltage of S_1 to S_4 and gate inductor current i_L in the proposed CSG is plotted in Fig. 20. Compared with Fig. 13, it can match well with the theoretical analysis. Fig. 21 and Fig. 22 illustrate the tested switching waveforms of the instantaneous power, drain current and drain-source voltage with both gate drives at 500 V bus voltage and 30 A load current condition. Clearly, the switching time decreases with the proposed CSG during turn-on transient, and voltage fall time reduces significantly. From the shaded area of the instantaneous power, the turn-on loss has great improvement. The penalty is that because of the higher dv/dt, the overvoltage of the upper MOSFET increases from 106 V to 375 V. The turn-off loss and time also decreases with the proposed CSG but the overvoltage of the lower MOSFET does not increase. This is mainly because the displacement current during turn-off cannot exceed the load current. Thus, the voltage rise time is limited by the load current rather than the gate drive capability, which prevents the drain-source voltage from increasing.

The gate voltage and current waveform at 500 V bus voltage and 30 A load current condition with the proposed CSG is shown in Fig. 23. Due to the large internal gate resistance, the real gate voltage cannot be directly monitored. With the measured external gate voltage $v_{gs(ext)}$ and the gate current i_g, the real gate voltage can be back calculated by (8) and is drawn as a blue dashed line. The inductor current i_L is also plotted for reference. Although the external gate voltage exceeds the maximum gate voltage of the MOSFET (+19/-8 V), the real gate voltage is beneath the limitation. However, the margin of gate voltage is very small due to the parasitic ringing. How to avoid the gate overvoltage, accurately control the gate drive to turn to voltage source, and protect the MOSFET can be an issue and requires more attention for the CSG.

Fig. 24 shows the tested switching performance with the conventional VSG and the proposed CSG at different load conditions. From Fig. 24(a), the voltage fall time at full load with the proposed CSG is 6.8 ns while that with the conventional VSG is 25.6 ns. The total turn-on switching time

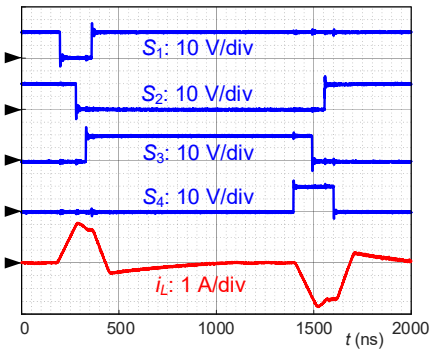


Fig. 20. Tested control signals of CSG.

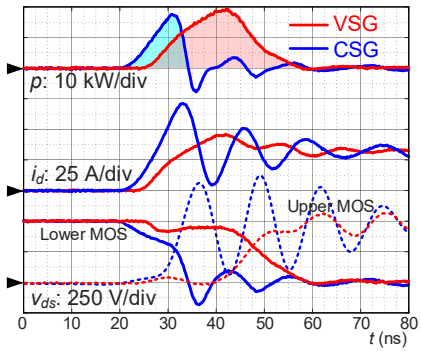


Fig. 21. Tested turn-on waveforms of v_{ds} and i_d at 500 V, 30 A.

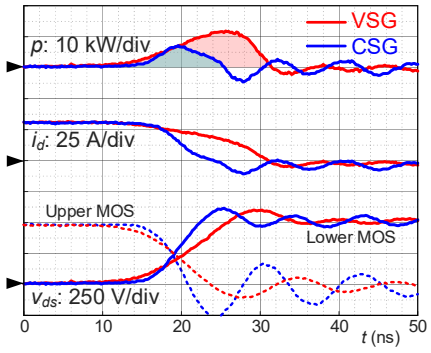


Fig. 22. Tested turn-off waveforms of v_{ds} and i_d at 500 V, 30 A.

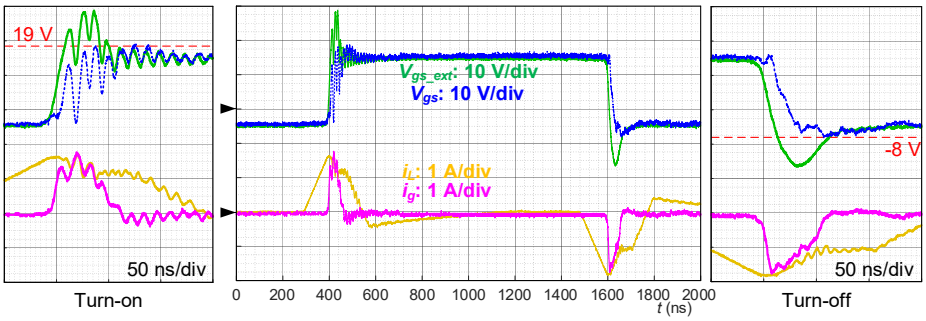
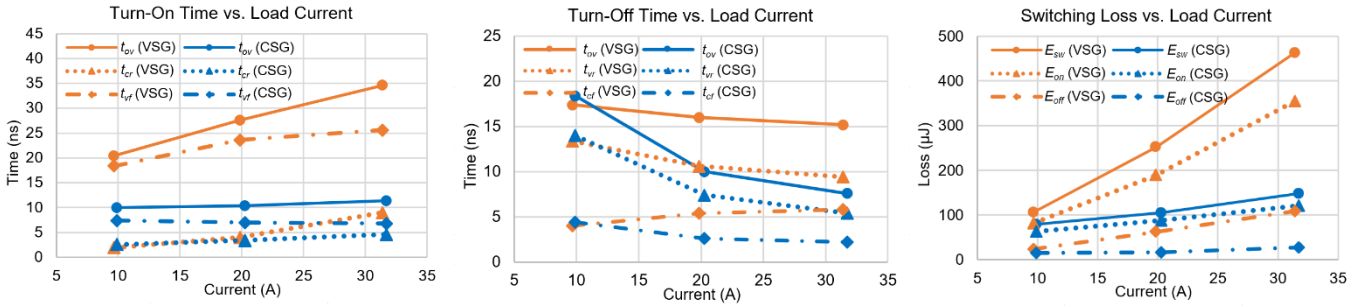


Fig. 23. Waveform of gate voltage and current with proposed CSG at 500 V, 30 A.



(a) (b) (c)

Fig. 24. Comparison of tested switching performance at different load conditions. (a) Turn-on time. (b) Turn-off time. (c) Switching loss.

decreases from 34.6 ns to 11.4 ns with the proposed CSG. In addition, Fig. 24(a) can match with the trend in Fig. 17, which verifies the theoretical analysis.

In Fig. 24(b), the turn-off switching time decreases from 15.2 ns to 7.6 ns at full load with the proposed CSG. Comparing the turn-on and turn-off time, the improvement in turn-on time is better due to two main reasons. First, a negative voltage (e.g. -4 V) is supplied to the gate of the device during turn-off. Since the Miller voltage is relatively high as previously discussed, the gate current during the turn-off transient is higher than during the turn-on with the conventional VSG, which makes the turn-off process faster than the turn-on process. Second, the voltage rise time during the turn-off transient is influenced by not only the gate current charging the transfer capacitance, but also the load current charging the output capacitance. At light load condition, the voltage rise time is dominated by the load current instead of the gate current, so both drive technologies show similar voltage rise time in Fig. 24(b). As the load current increases, the voltage rise time with the conventional VSG is determined by the gate drive current. However, for the proposed CSG with much higher gate current, the voltage rise time is still dominated by the load current. On the contrary, the voltage fall time during turn-on is independent of the load current with the proposed CSG, which is verified in Fig. 24(a) and can help to achieve larger turn-on time reduction. As a result, increasing gate current has more significant improvement for turn-on time than turn-off time.

Fig. 24(c) plots the switching loss at different load conditions. The switching loss with the proposed CSG at full load is 148 μJ, which is less than one third of the loss with the conventional VSG. The trend can match with the switching time curve in Fig. 24(a) and (b). Note that the switching loss with the proposed CSG can be further reduced by increasing the gate current as long as the overvoltage is acceptable.

Fig. 25 presents the overall performance comparison between the conventional VSG and the proposed CSG. The

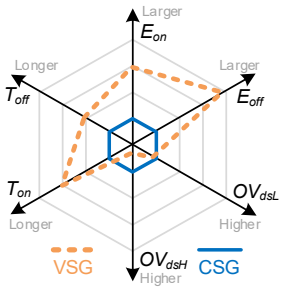


Fig. 25. Performance comparison between conventional VSG and proposed CSG.

smaller area means better overall performance. The proposed CSG can provide significantly shorter switching time and lower switching loss. The only drawback is the higher overvoltage, especially on the upper MOSFET, which is a common trade-off to pursue higher switching speed in hard switching applications.

VI. Conclusions

The switching transient of a 30 A SiC discrete MOSFET and a 800 A power module in a phase-leg based on the traditional VSG is analyzed and evaluated with the help of double pulse tests. The results show that the constraints limiting the switching speed for the discrete device and the power module are different. There is still plenty of room to improve the switching speed for the discrete device even when the external gate resistance is reduced to zero, which means the conventional VSG cannot maximize the switching speed. On the other hand, the power module suffers from high overvoltage caused by the loop parasitics due to higher *di*/*dt*, and the existing gate drive is sufficient to push the switching speed to the upper limit.

To further increase the switching speed of the discrete device, its intrinsic characteristics that impact the performance of the gate drive are analyzed in detail. Due to the high Miller voltage and internal gate resistance of the discrete device, the gate current with the conventional VSG and existing CSG is limited, and the voltage fall time during the turn-on transient is dominant. A CSG is proposed that can achieve constant gate current during the whole switching transient regardless of the influence by the large gate resistance. The CSG can be controlled to turn to VSG after the switching transient ends to avoid the increase of gate drive loss. A comparison is made between the conventional VSG and proposed CSG with double pulse tests. The results show that the turn-on and turn-off time is shortened by 67% and 50% respectively with the proposed CSG at full load condition. A switching loss reduction of 68% is achieved by the proposed CSG in comparison with the conventional VSG.

References

[1] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.,* vol. 58, no. 7, pp. 2872-2882, 2011.

[2] R. Bonyadi, O. Alatise, S. Jahdi, J. Hu, J. A. O. Gonzalez, L. Ran, and P. A. Mawby, "Compact electrothermal reliability modeling and experimental characterization of bipolar latchup in SiC and CoolMOS power MOSFETs," *IEEE Trans. Power Electron.,* vol. 30, no. 12, pp. 6978-6992, 2015.

[3] J. Hu, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, P. Alexakis, L. Ran, and P. Mawby, "Robustness and balancing of parallel-connected power devices: SiC versus CoolMOS," *IEEE Trans. Ind. Electron.,* vol. 63, no. 4, pp. 2092-2102, 2016.

[4] Y. Shi, L. Wang, R. Xie, Y. Shi, and H. Li, "A 60-kW 3-kW/kg five-level T-type SiC PV inverter with 99.2% peak efficiency," *IEEE Trans. Ind. Electron.,* vol. 64, no. 11, pp. 9144-9154, 2017.

[5] E. Gurpinar and A. Castellazzi, "Single-phase T-type inverter performance benchmark using Si IGBTs, SiC MOSFETs, and GaN HEMTs," *IEEE Trans. Power Electron.,* vol. 31, no. 10, pp. 7148-7160, 2016.

[6] Z. Huang, Z. Liu, F. C. Lee, and Q. Li, "Critical-mode-based soft-switching modulation for high-frequency three-phase bi-directional AC/DC converters," *IEEE Trans. Power Electron.,* 2018.

[7] H. Gui, Z. Zhang, R. Ren, R. Chen, J. Niu, L. M. Tolbert, F. Wang, B. J. Blalock, D. J. Costinett, and B. B. Choi, "SiC MOSFET versus Si super junction MOSFET - switching loss comparison in different switching cell configurations," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 6146-6151.

[8] M. Liang, T. Q. Zheng, and Y. Li, "Performance evaluation of SiC MOSFET, Si CoolMOS and IGBT," in *Proc. Int. Power Electron. Appl. Conf. Expo.*, 2014, pp. 1369-1373.

[9] Z. Chen, D. Boroyevich, and J. Li, "Behavioral comparison of Si and SiC power MOSFETs for high-frequency applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2013, pp. 2453-2460.

[10] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. Costinett, "Understanding the limitations and impact factors of wide bandgap devices' high switching-speed capability in a voltage source converter," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, 2014, pp. 7-12.

[11] Z. Zhang, W. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Analysis of the switching speed limitation of wide band-gap devices in a phase-leg configuration," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 3950-3955.

[12] J. Strydom, M. De Rooij, and J. Van Wyk, "A comparison of fundamental gate-driver topologies for high frequency applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, vol. 2, pp. 1045-1052.

[13] N. Sakib, M. Manjrekar, and A. Ebong, "An overview of advances in high reliability gate driving mechanisms for SiC MOSFETs," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, 2017, pp. 291-294.

[14] M. M. Swamy, T. Kume, and N. Takada, "An efficient resonant gate-drive scheme for high-frequency applications," *IEEE Trans. Ind. Appl.,* vol. 48, no. 4, pp. 1418-1431, 2012.

[15] J. Yu, Q. Qian, P. Liu, W. Sun, S. Lu, and Y. Yi, "A high frequency isolated resonant gate driver for SiC power MOSFET with asymmetrical ON/OFF voltage," in *Proc. IEEE Appl. Power Electron. Conf.*, 2017, pp. 3247-3251.

[16] J. V. P. S. Chennu, R. Maheshwari, and H. Li, "New resonant gate driver circuit for high-frequency application of silicon carbide MOSFETs," *IEEE Trans. Ind. Electron.,* vol. 64, no. 10, pp. 8277-8287, 2017.

[17] B. Callanan, "Application considerations for silicon carbide MOSFETs," Cree. 2011. [Online]. Available: http://www.cree.com.

[18] Rohm. SiC power devices and modules, 2013 [Online]. Available: http://www.rohm.com.

[19] Z. Miao, Y. Mao, C.-M. Wang, and K. D. Ngo, "Detection of cross-turn-on and selection of off drive voltage for an SiC power module," *IEEE Trans. Ind. Electron.,* vol. 64, no. 11, pp. 9064-9071, 2017.

[20] Q. Zhou, F. Gao, and T. Jiang, "A gate driver of SiC MOSFET with passive triggered auxiliary transistor in a phase-leg configuration," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 7023-7030.

[21] Z. Zhang, J. Dix, F. Wang, B. Blalock, D. Costinett, and L. Tolbert, "Intelligent gate drive for fast switching and cross-talk suppression of SiC devices," *IEEE Trans. Power Electron.,* vol. 32, no. 12, pp. 9319-9332, 2017.

[22] B. Zhang, S. Xie, J. Xu, Q. Qian, Z. Zhang, and K. Xu, "A magnetic coupling based gate driver for crosstalk suppression of SiC MOSFETs," *IEEE Trans. Ind. Electron.,* vol. 64, no. 11, pp. 9052-9063, 2017.

[23] P. Nayak and K. Hatua, "Active gate driving technique for a 1200 V SiC MOSFET to minimize detrimental effects of parasitic inductance in the

converter layout," *IEEE Trans. Ind. Appl.,* vol. 54, no. 2, pp. 1622-1633, 2018.
[24] Y. Ren, X. Yang, F. Zhang, K. Wang, W. Chen, L. Wang, and Y. Pei, "A compact gate control and voltage-balancing circuit for series-connected SiC MOSFETs and its application in a DC breaker," *IEEE Trans. Ind. Electron.,* vol. 64, no. 10, pp. 8299-8309, 2017.
[25] Z. Zhang, H. Gui, J. Niu, R. Chen, F. Wang, L. M. Tolbert, D. J. Costinett, and B. J. Blalock, "High precision gate signal timing control based active voltage balancing scheme for series-connected fast switching field-effect transistors," in *Proc. IEEE Appl. Power Electron. Conf.*, 2018, pp. 925-930.
[26] J. Ewanchuk, J. Brandelero, and S. Mollov, "Lifetime extension of a multi-die SiC power module using selective gate driving with temperature feedforward compensation," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 2520-2526.
[27] S. Hazra, K. Vechalapu, S. Madhusoodhanan, S. Bhattacharya, and K. Hatua, "Gate driver design considerations for silicon carbide MOSFETs including series connected devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1402-1409.
[28] H. Obara, K. Wada, K. Miyazaki, M. Takamiya, and T. Sakurai, "Active gate control in half-bridge inverter using programmable gate driver ICs to improve both surge voltage and converter efficiency," *IEEE Trans. Ind. Appl.,* vol. 54, no. 5, pp. 4603-4611, 2018.
[29] J. Dyer, Z. Zhang, F. Wang, D. Costinett, L. M. Tolbert, and B. J. Blalock, "Online condition monitoring based dead-time compensation for high frequency SiC voltage source inverter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2018, pp. 1854-1860.
[30] H. C. Dymond, D. Liu, J. Wang, J. J. Dalton, and B. H. Stark, "Multi-level active gate driver for SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 5107-5112.
[31] H. Riazmontazer and S. K. Mazumder, "Dynamic optical turn-off control of a high-voltage SiC MOSFET," in *Proc. IEEE Appl. Power Electron. Conf.*, 2013, pp. 1274-1278.
[32] H. Riazmontazer, A. Rahnamaee, A. Mojab, S. Mehrnami, S. K. Mazumder, and M. Zefran, "Closed-loop control of switching transition of SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf.*, 2015, pp. 782-788.
[33] E. Shelton, X. Zhang, T. Zhang, N. Hari, and P. Palmer, "Low inductance switching for SiC MOSFET based power circuit," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 5093-5100.
[34] "1EDU20I12SV," Infineon. 2017. [Online]. Available: https://www.infineon.com.
[35] W. Eberle, Z. Zhang, Y.-F. Liu, and P. C. Sen, "A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz," *IEEE Trans. Power Electron.,* vol. 23, no. 2, pp. 678-691, 2008.
[36] J. Fu, Z. Zhang, Y.-F. Liu, P. C. Sen, and L. Ge, "A new high efficiency current source driver with bipolar gate voltage," *IEEE Trans. Power Electron.,* vol. 27, no. 2, pp. 985-997, 2012.
[37] I. A. Mashhadi and B. Soleymani, "A dual-switch discontinuous current-source gate driver for narrow on-time buck converter," *IEEE Trans. Power Electron.,* vol. 33, no. 5, pp. 4215-4223, 2017.
[38] Z. Zhang, J. Fu, Y.-F. Liu, and P. C. Sen, "Discontinuous-current-source drivers for high-frequency power MOSFETs," *IEEE Trans. Power Electron.,* vol. 25, no. 7, pp. 1863-1876, 2010.
[39] Z. Zhang, J. Fu, Y.-F. Liu, and P. C. Sen, "Adaptive current source drivers for efficiency optimization of high-frequency synchronous buck converters," *IEEE Trans. Power Electron.,* vol. 27, no. 5, pp. 2462-2470, 2012.
[40] L. Shu, J. Zhang, F. Peng, and Z. Chen, "Active current source IGBT gate drive with closed-loop di/dt and dv/dt control," *IEEE Trans. Power Electron.,* vol. 32, no. 5, pp. 3787-3796, 2017.
[41] Z. Wang, X. Shi, L. M. Tolbert, F. F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Trans. Power Electron.,* vol. 29, no. 7, pp. 3720-3732, 2014.
[42] F. Zhang, X. Yang, Y. Ren, L. Feng, W. Chen, and Y. Pei, "Advanced active gate drive for switching performance improvement and overvoltage protection of high-power IGBTs," *IEEE Trans. Power Electron.,* vol. 33, no. 5, pp. 3802-3815, 2018.
[43] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "Switching-behavior improvement of insulated gate-controlled devices," *IEEE Trans. Power Electron.,* vol. 12, no. 4, pp. 645-653, 1997.
[44] L. Dang, H. Kuhn, and A. Mertens, "Digital adaptive driving strategies for high-voltage IGBTs," *IEEE Trans. Ind. Appl.,* vol. 49, no. 4, pp. 1628-1636, 2013.
[45] Z. Zhang, "Characterization and realization of high switching-speed capability of SiC power devices in voltage source converter," Ph.D. Dissertation, The University of Tennessee, Knoxville, 2015.
[46] J. Wang, H. S.-h. Chung, and R. T.-h. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.,* vol. 28, no. 1, pp. 573-590, 2013.
[47] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Trans. Power Electron.,* vol. 32, no. 12, pp. 9307-9318, 2017.
[48] H. Gui, Z. Zhang, R. Chen, J. Niu, L. M. Tolbert, F. Wang, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Current source gate drive to reduce switching loss for SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf.*, 2019, pp. 972-978.